SM16106

Outline

SM16106 It is designed for led Display driver chip design, within build CMOS Shift register and latch functions may be serial input Data into parallel output data format.

SM16106 Operating voltage 3.3V - 5.0V ,provide 16 Electrical Current source may be provided at each output port 1mA-32mA Constant electricity Flow; single and IC Chip output current difference is less than ± 2.5% ; More stars IC Output current is less than the difference between ± 3.5% ; Output current with the input channel The terminal voltage (V_{DS}) Varies changes; and the current by the voltage and Effect of temperature change is less than 1% ; Output current of each channel by External resistor is adjusted.

SM16106 Output port pressure up 17V , You can be in every A plurality of output terminals connected in series led Lights; Further, SM16106 Up 25MHz It needs to meet the system clock frequency to transfer large amounts of data begging.

Feature

- 16 Channel current source output
- Constant current:

  L- 32mA @ the VDD = 5.0V

  @ Chip error <± 2.5% , Inter-chip error <± 3.5%

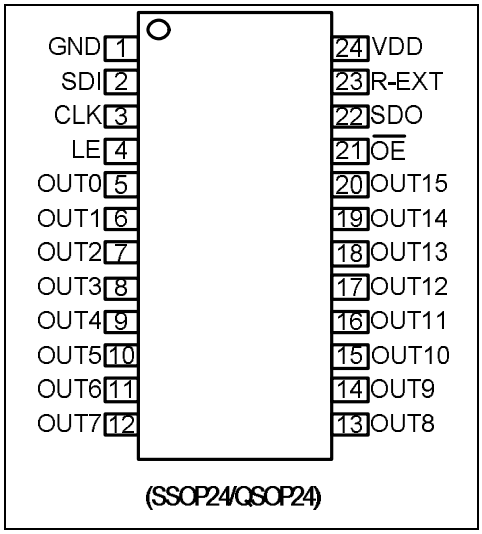
  L- 22mA @ the VDD = 3.3V

  @ Chip error <± 2.5% , Inter-chip error <± 3.5%
- Output current support external Rext Adjustable resistor
- Fast response of output current, $\overline{OE}$ (Minimum): 35ns
- Up 25MHz Clock frequency
- Operating Voltage: 3.3V ~ 5.0V
- Package: SSOP24 , QSOP24 , QFN24 (4 * 4)

Package Information

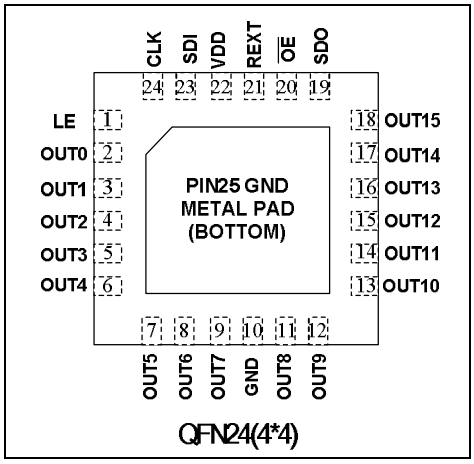
product name	Size plastic package (mm)	Foot spacing (mm)
SM16106D	SSOP24	13.0 * 6.0 * 1.8	1.0
SM16106SC	QSOP24	8.65 * 3.9 * 1.4	0.635
SM16106CN-2	QFN24 (4 * 4)	4 * 4 * 0.85	0.5

Pin definitions

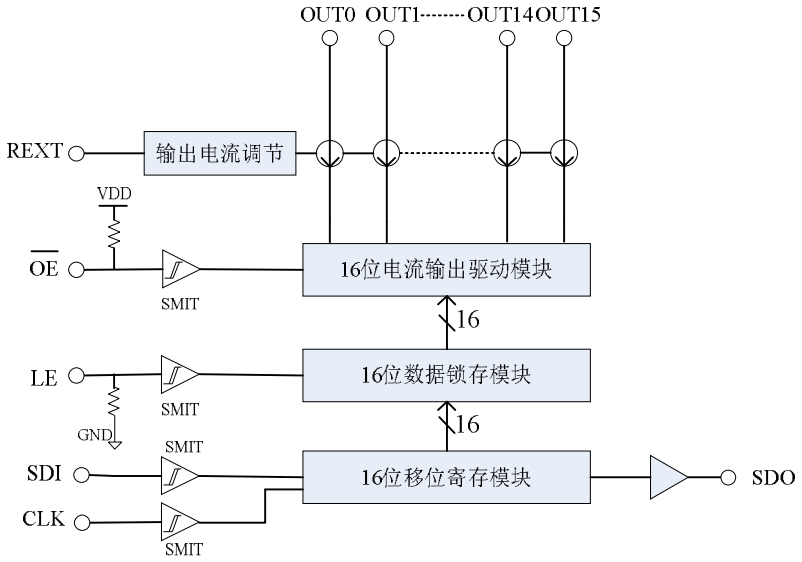


Applications

- Advertising screen
- led illumination



Simplified block diagram of the internal functions



Pin Description

name	Function Description
GND	Chip ground
SDI	Serial data input port
CLK	Input port clock signal; data shift clock rising edge
LE	Data latch control port. when LE Is high, the serial data will be passed to the output latch; when LE It is low, capital Material is latched
OUT0 ~ OUT15	Current source output port
$\overline{OE}$	Output enable control port. when $\overline{OE}$ It is low, triggers OUT0 ~ OUT15 Output; when $\overline{OE}$ It is high, OUT0 ~ OUT15 Output will be shut down
SDO	Serial data output port; can be connected to the next chip, SDI port

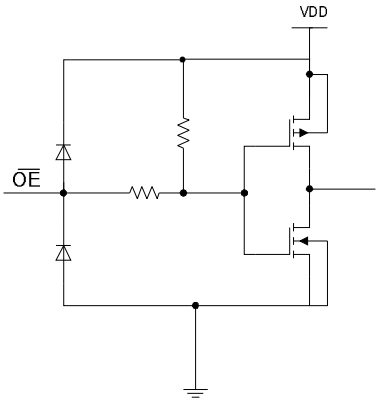
R-EXT	External resistor connected to the input port; furthermore resistor sets the output current of all output channels
VDD	Chip power

Ordering Information

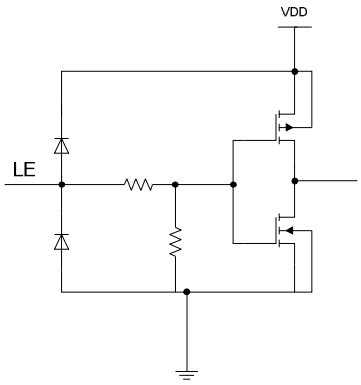
Order Type	Package	Packing		Reel size
		Tube	Taping	
SM16106D	SSOP24	36,000 Pieces / box	2000 Particles / plate	13 Inch
SM16106SC	QSOP24	100 000 Pieces / box	4000 Particles / plate	13 Inch
SM16106CN-2	QFN24 (4 * 4)	/	5000 Particles / plate	13 Inch

Input and output equivalent circuit

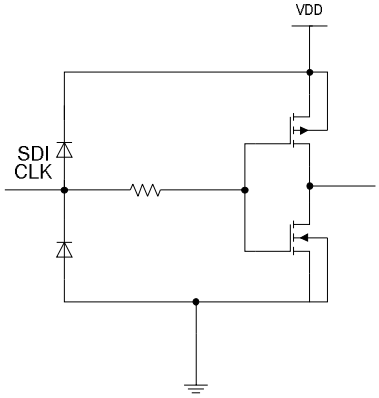
- $\overline{OE}$ Input



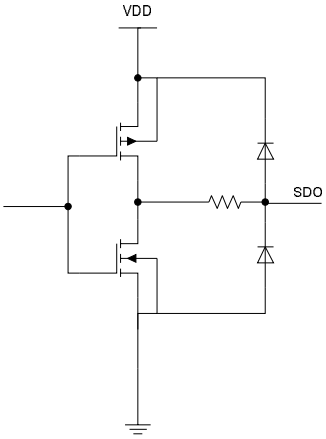
- LE Input



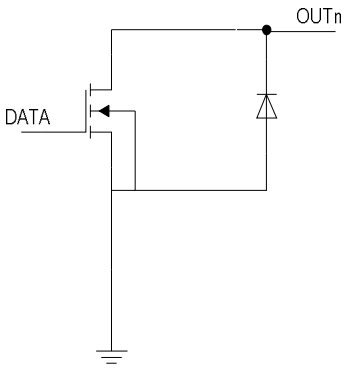
- CLK, SDI Input



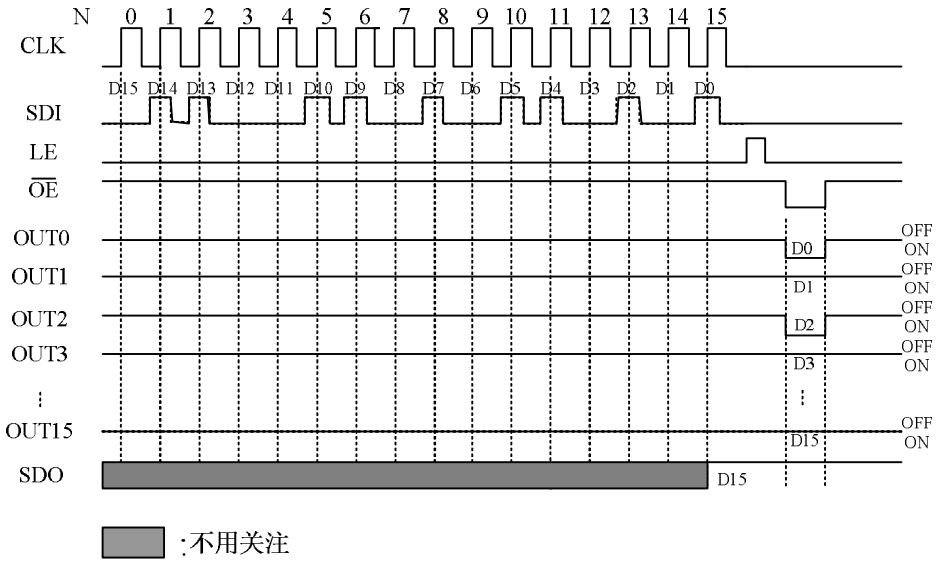
- SDO Output terminal



- OUT0 ~ OUT15 Output terminal



Timing diagram



Truth table

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}\cdots\overline{OUT7}\cdots\overline{OUT15}$	SDO
↑	H	L	Dn	$\overline{Dn}...\overline{Dn-7}...\overline{Dn-15}$	Dn-15
↑	L	L	Dn+1	No Change	Dn-14
↑	H	L	Dn+2	$\overline{Dn+2}...\overline{Dn-5}...\overline{Dn-13}$	Dn-13
↓	×	L	Dn+3	Dn+2...Dn-5...Dn-13	Dn-13
↓	×	H	Dn+3	off	Dn-13

Maximum Stress Ratings

characteristic	Representing the symbol	Defining the maximum range	unit
voltage	VDD	0 ~ 7.0	V
Input Voltage	V_{SDA}, V_{CLK}, V_{LE}, V_{OE}	-0.4 ~ VDD + 0.4V	V
Current Output Current	I_{OUT}	+ 45	mA
Withstand voltage output terminal	V_{DS}	-0.5 ~ + 17.0	V
Clock frequency	f_{CLK}	30	MHz
IC Ambient temperature at work	T_{opr}	- 40 ~ + 85	℃
IC The ambient temperature during storage	T_{stg}	- 55 ~ + 150	℃
HBM Human Body Model	V_{ESD}	> 4	KV

Note: The peak value of the soldering paste product temperature should not exceed 260 ℃, according to the temperature profile J-STD-020 Standard, and with reference to the actual factory's recommendations paste factory settings.

DC Characteristics

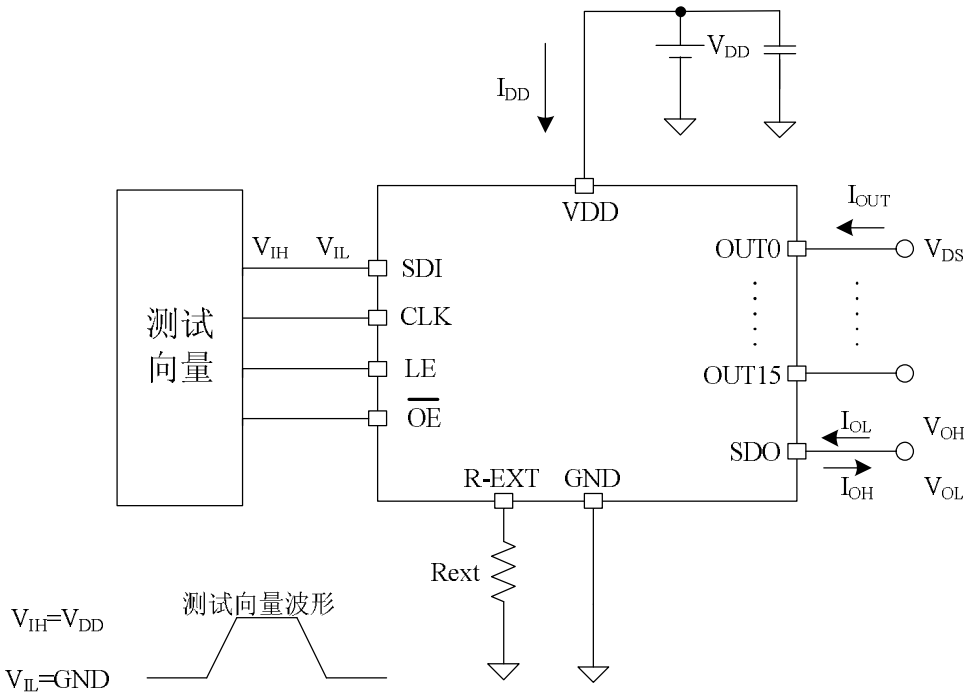
(VDD = 5.0V, Ta = 27 ℃)

characteristic	Representing the symbol	Measurement conditions		Min Typ Max			unit
Quiescent Current	IDD	VDD = 5.0V , R-EXT Vacant, I_{OUT} shut down		-	1.5	-	mA
OUT Pressure port	$V_{DS(MAX)}$	OUT0 ~ OUT15		-	-	17	V
OUT Output Current	I_{OUT}	VDD = 5.0V		1	-	32	mA
SDO Drive current	I_{OH}	VDD = 5.0V		-	-twenty one	-	mA
	I_{OL}			-	twenty one	-	mA
Flip-level input port	V_{IH}			0.7 * VDD	-	VDD	V
	V_{IL}			GND	-	0.3 * VDD	V
OUT Leakage current output terminal	I_{OH}	V_{DS} = 17V		-	-	0.5	uA
SDO Output voltage	V_{OL}	I_{OL} = + 1mA		-	-	0.4	V
	V_{OH}	I_{OH} = - 1mA		4.6	-	-	V
OUT Port Output Current 1	I_{OUT1}	V_{DS} = 1.0V	rext = 1800Ω	-	8.8	-	mA
Output current error	D_{IOUT}	I_{OUT} = 8.8mA V_{DS} = 1.0V rext = 1800Ω	Chip	-	-	± 2.5%	
			Inter-chip	-	-	± 3.5%	
OUT Port Output Current 2	I_{OUT2}	V_{DS} = 1.0V	rext = 920Ω	-	17.5	- mA	
Output current error	D_{IOUT}	I_{OUT} = 17.5mA V_{DS} = 1.0V rext = 920Ω	Chip	-	-	± 2.5%	
			Inter-chip	-	-	± 3.5%	
Output current error / V_{DS} % Change in / ΔV_{DS}		V_{DS} = 1.0V ~ 3.0V		-	± 0.5%	-	% / V
Output current error / V_{DD} % Change in / ΔV_{DD}		V_{DD} = 4.5V ~ 5.5V		-	± 0.5%	-	% / V
Pull-up resistance	$R_{OE(up)}$	$\overline{OE}$		-	250	-	K •
Pull-down resistance	$R_{LE(down)}$	LE		-	250	-	K •
IC Quiescent Current	$I_{DD(off)1}$	R-EXT Vacant, OUT0 ~ OUT15 = OFF		-	1.5	-	mA
	$I_{DD(off)2}$	rext = 1800 • , OUT0 ~ OUT15 = OFF		-	2.6	-	
	$I_{DD(off)3}$	rext = 920 • , OUT0 ~ OUT15 = OFF		-	3.8	-	

(VDD = 3.3V, Ta = 27 ℃)

characteristic	Representing the symbol	Measurement conditions		Min Typ Max			unit
Quiescent Current	IDD	VDD = 3.3V , R-EXT Vacant, I_{OUT} shut down		-	1.2	-	mA
OUT Pressure port	$V_{DS(MAX)}$	OUT0 ~ OUT15		-	-	17	V
OUT Output Current	I_{OUT}	VDD = 3.3V		1	-	twenty two	mA
SDO Drive current	I_{OH}	VDD = 3.3V		-	-10.5	-	mA
	I_{OL}			-	13.3	-	mA
Flip-level input port	V_{IH}			0.7 * VDD	-	VDD	V
	V_{IL}			GND	-	0.3 * VDD	V
OUT Leakage current output terminal	I_{OH}	V_{DS} = 17V		-	-	0.5	uA
SDO Output voltage	V_{OL}	I_{OL} = + 1mA		-	-	0.3	V
	V_{OH}	I_{OH} = - 1mA		3.0	-	-	V
OUT Port Output Current 1	I_{OUT1}	V_{DS} = 1.0V	rext = 1800Ω	-	8.8	-	mA
Output current error	D_{IOUT}	I_{OUT} = 8.8mA V_{DS} = 1.0V rext = 1800Ω	Chip	-	-	± 2.5%	
			Inter-chip	-	-	± 3.5%	
OUT Port Output Current 2	I_{OUT2}	V_{DS} = 1.0V	rext = 920Ω	-	17.5	- mA	
Output current error	D_{IOUT}	I_{OUT} = 17.5mA V_{DS} = 1.0V rext = 920Ω	Chip	-	-	± 2.5%	
			Inter-chip	-	-	± 4.5%	
Output current error / V_{DS} % Change in / ΔV_{DS}		V_{DS} = 1.0V ~ 3.0V		-	± 0.5%	-	% / V
Output current error / V_{DD} % Change in / ΔV_{DD}		V_{DD} = 3.3V ~ 3.8V		-	± 1%	-	% / V
Pull-up resistance	$R_{OE(up)}$	$\overline{OE}$		-	250	-	K •
Pull-down resistance	$R_{LE(down)}$	LE		-	250	-	K •
IC Quiescent Current	$I_{DD(off)1}$	R-EXT Vacant, OUT0 ~ OUT15 = OFF		-	1.2	-	mA
	$I_{DD(off)2}$	rext = 1800 • , OUT0 ~ OUT15 = OFF		-	3.6	-	
	$I_{DD(off)3}$	rext = 920 • , OUT0 ~ OUT15 = OFF		-	2.5	-	

Test circuit DC characteristics



Dynamic characteristic

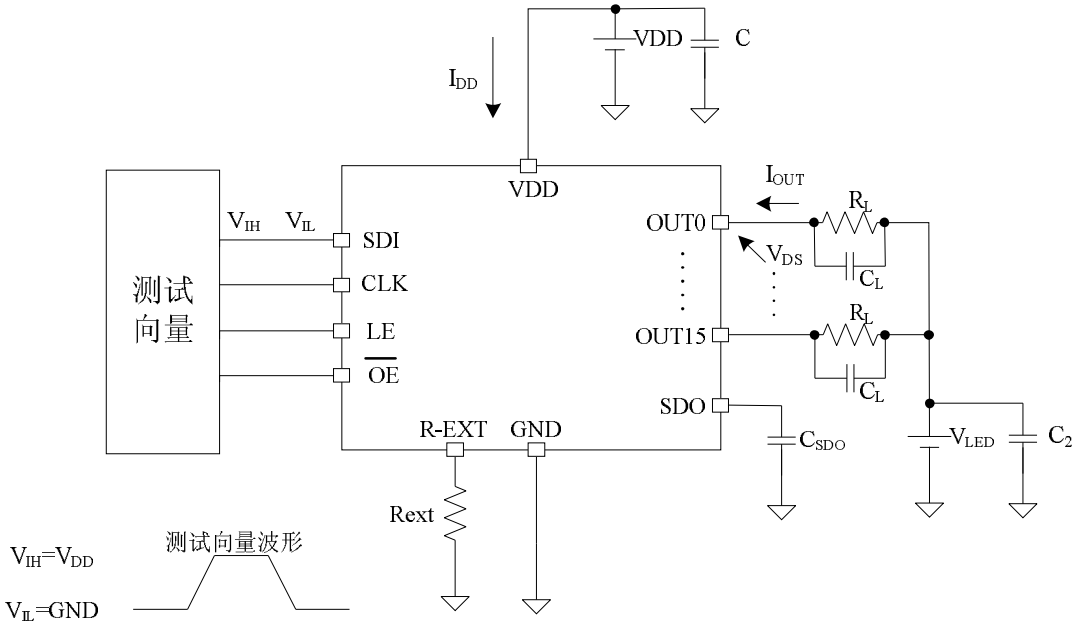
(VDD = 5.0V)

characteristic		On behalf of operators	Measurement conditions	Min.	Max.		unit
delay (Low to high)	CLK - OUT	t_{pLH1}	V_{IH} = VDD V_{IL} = GND Rext = 1800Ω VDD = 5.0V R_L = 400Ω C_L = 10pF	--	30	--	ns
	LE - OUT	t_{pLH2}		--	26	--	ns
	OE - OUT	t_{pLH3}		--	30	--	ns
	CLK - SDO	t_{pLH}		--	28	--	ns
delay (High to low)	CLK - OUT	t_{pHL1}		--	35	--	ns
	LE - OUT	t_{pHL2}		--	33	--	ns
	OE - OUT	t_{pHL3}		--	35	--	ns
	CLK - SDO	t_{pHL}		--	27	--	ns
Current output rise time		$t_{OUT-RISE}$		--	30	--	ns
Current output fall time		$t_{OUT-FALL}$		--	35	--	ns

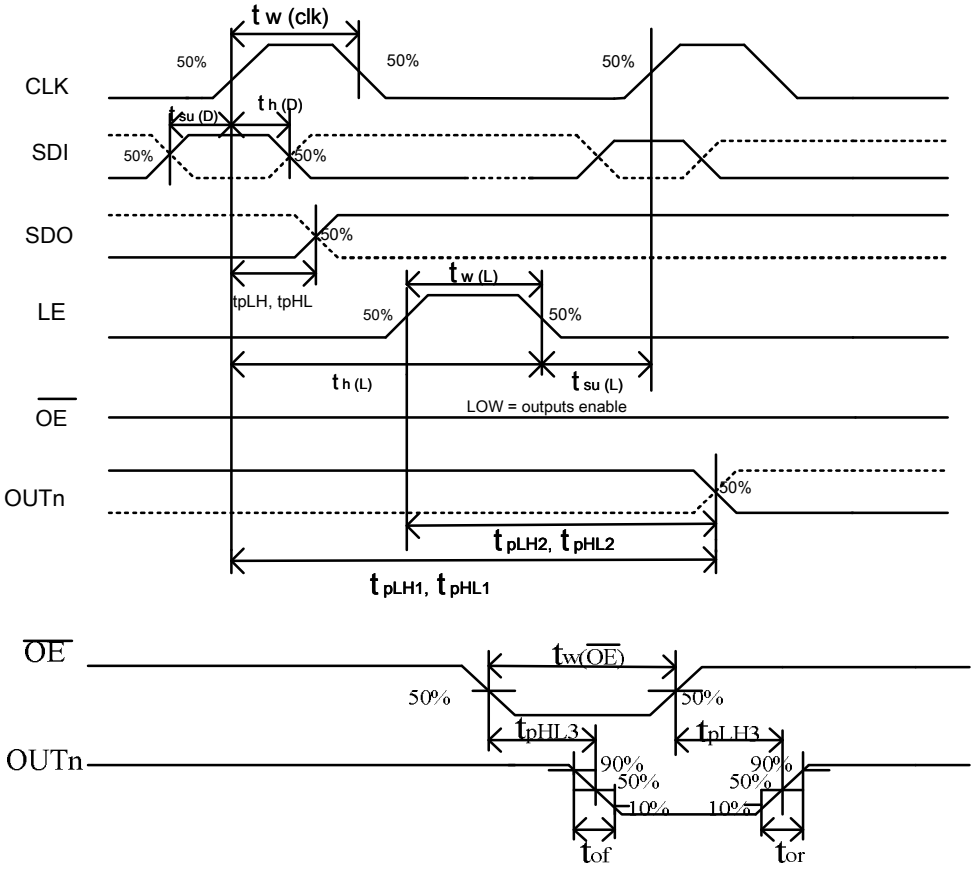
(VDD = 3.3V)

characteristic		On behalf of operators	Measurement conditions	Min.	Max.		unit
delay (Low to high)	CLK - OUT	t_{pLH1}	V_{IH} = VDD V_{IL} = GND Rext = 1800Ω VDD = 3.3V R_L = 200Ω C_L = 10pF	--	42	--	ns
	LE - OUT	t_{pLH2}		--	36	--	ns
	OE - OUT	t_{pLH3}		--	45	--	ns
	CLK - SDO	t_{pLH}		--	30	--	ns
delay (High to low)	CLK - OUT	t_{pHL1}		--	38	--	ns
	LE - OUT	t_{pHL2}		--	33	--	ns
	OE - OUT	t_{pHL3}		--	40	--	ns
	CLK - SDO	t_{pHL}		--	29	--	ns
Current output rise time		$t_{OUT-RISE}$		--	26	--	ns
Current output fall time		$t_{OUT-FALL}$		--	18	--	ns

Dynamic Characteristics Test Circuit



A timing waveform chart

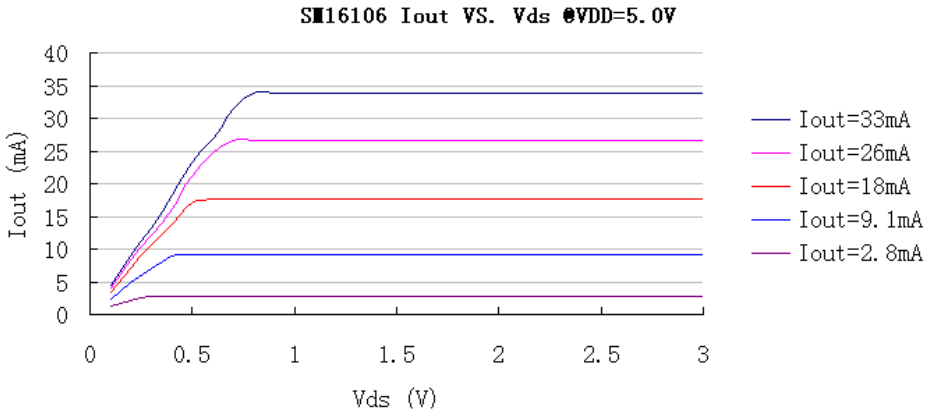


Applications

will SM16106 Applied led Display design, even the inter-channel current between chips, little difference. This comes from SM16106 Excellent Heng

Stream output characteristics:

- Maximum current error between the channels is less than the inner sheet ± 2.5% , The maximum current is less than the error between a chip ± 3.5% .
- When the load voltage (V_{DS}) When changes affected the stability of the output current, as shown in FIG.



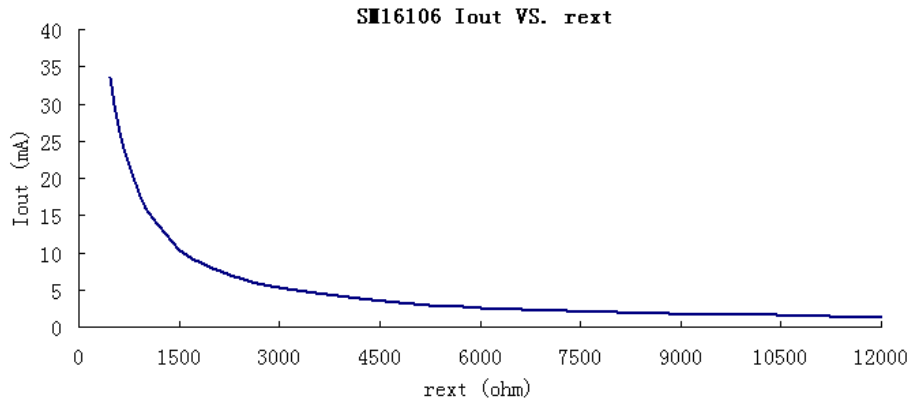
VDD = 5V Time, I_{OUT} versus V_{DS} The relationship between the curve

Adjusting the output current

As shown below, the external one rext Output current resistance adjustment I_{OUT} , Apply the following formula to calculate the output current value:

$$I_{OUT} = (16 / rext) * 1000 \text{ mA} ,$$

Formula rext Refers to R-EXT The resistance value of the port to ground, current units mA . For example, when rext = 750Ω , The formula can be obtained by Output current value 21.4mA ;when rext = 6000Ω , The output current value 2.7mA .



I_{OUT} versus rext Resistance curve

Package thermal power (PD)

The maximum power dissipation is encapsulated by the formula:

$$P_{D(max)} = \frac{(T_T - T)\ P}{R\ \text{To decide}_{th(ja)}}$$

when 16 When the channel is fully open, the actual power consumption:

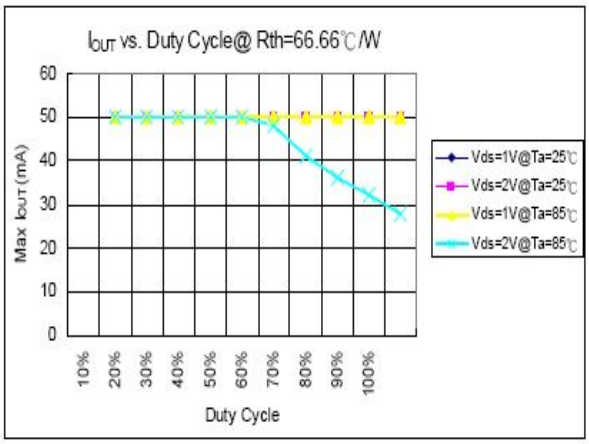
$$P_{D(act)} = IDD * VDD + I_{OUT} \cdot Duty * V_{DS} \cdot 16$$

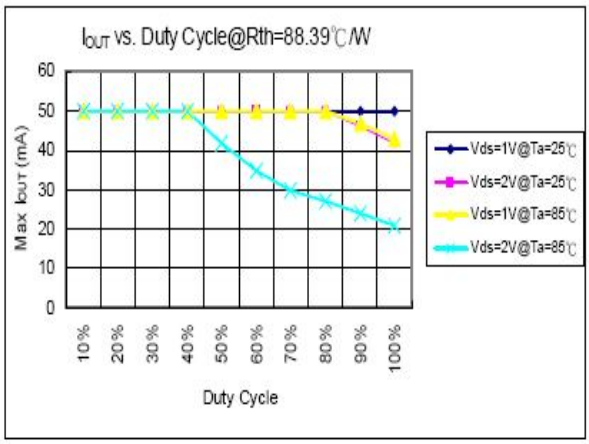
Actual power consumption must be less than the maximum power consumption, that is, $P_{D(act)} < P_{D(max)}$, to maintain $P_{D(act)} < P_{D(max)}$, The relationship between the maximum output current and duty cycle are

$$I_{out} \cdot \frac{\cdot\ TT_{aj} \cdot IDD\ R^{*}\ VDD}{V_{DS} * Duty * 16}$$

among them Tj for IC Operating temperature, Ta Ambient temperature, V_{DS} For the steady flow port output voltage, Duty The duty cycle, $R_{th(ja)}$ Thermal resistance of the package. The following figure

The relationship of the maximum output current and duty cycle:





If you need higher output current I_{OUT} , The need to add some fins, which is calculated as:

$$\text{by}\ \frac{1}{R_{th(ja)}} + = \frac{1}{RT_{e} - T\ \text{Too:}_{a}} \frac{P_{D\,act} \cdot}{}$$

$$R_{fe} = P \frac{R^{*}_{th(ja)} T - T \cdot_{j\ a} \cdot}{D\,act \cdot * R_{th(ja)} + T_{j\ a}}$$

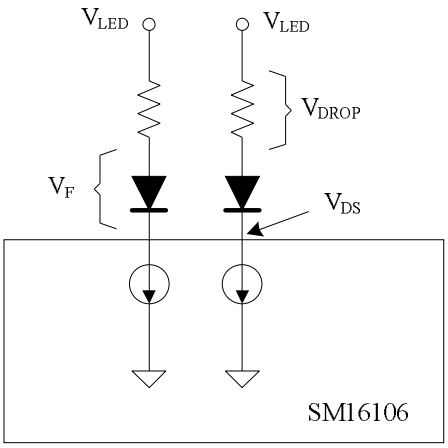
among them $P_{D(act)} = IDD * VDD + I_{OUT} \cdot Duty * V_{DS} \cdot 16$

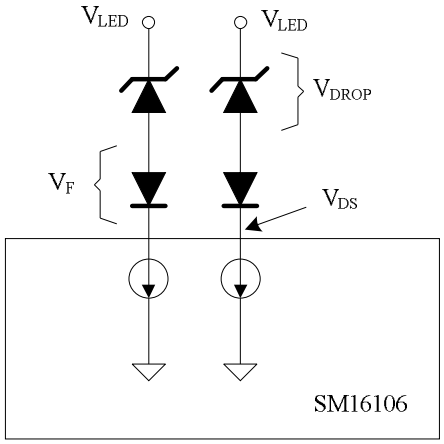
So if you want to output more current I_{OUT} , It can be calculated from the above formula to be IC Resistance heating is R_{fe} Fins.

Load voltage (VLED)

To enable the package to optimize heat dissipation capacity, the output voltage is recommended (V_{DS}) The optimum working range 1.0V About (based on I_{OUT} = 1mA ~ 32mA) . in case V_{DS} = V_{LED}- V_F And V_{LED} = 5.0V When, at this time the high voltage output terminal (V_{DS}) May cause P_D(act)> P_D(max) . In this state Conditions, it is recommended to use a low as possible V_{led} Voltage supply, it can also be used Resistors or as a regulator V_{Drop} This may lead to V_{DS} =(V_{LED}- V_F)- V_{DROP} ,

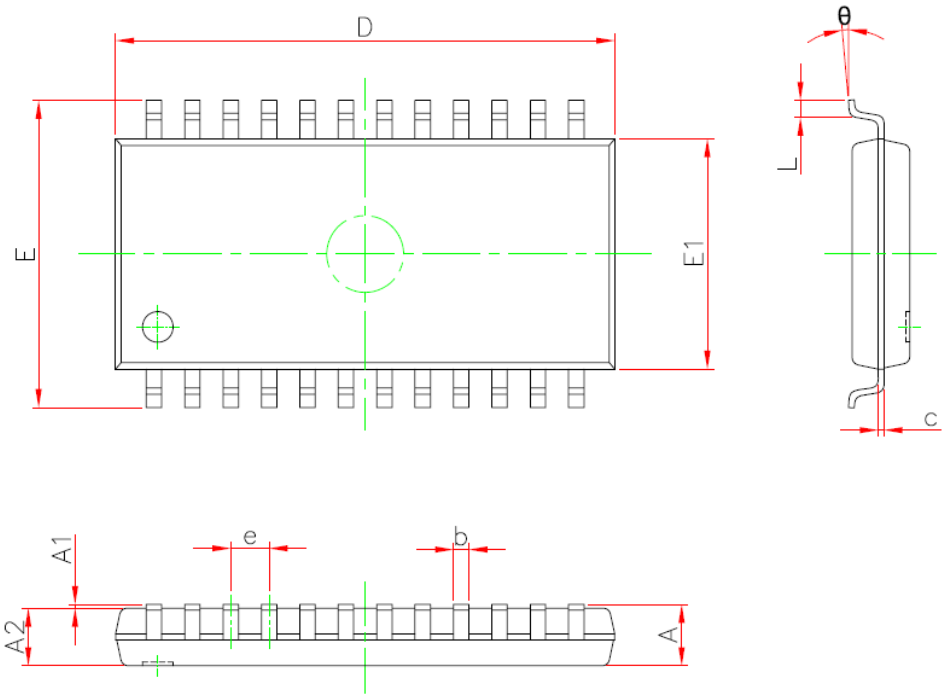
To reduce the output voltage (V_{DS}) Effect.





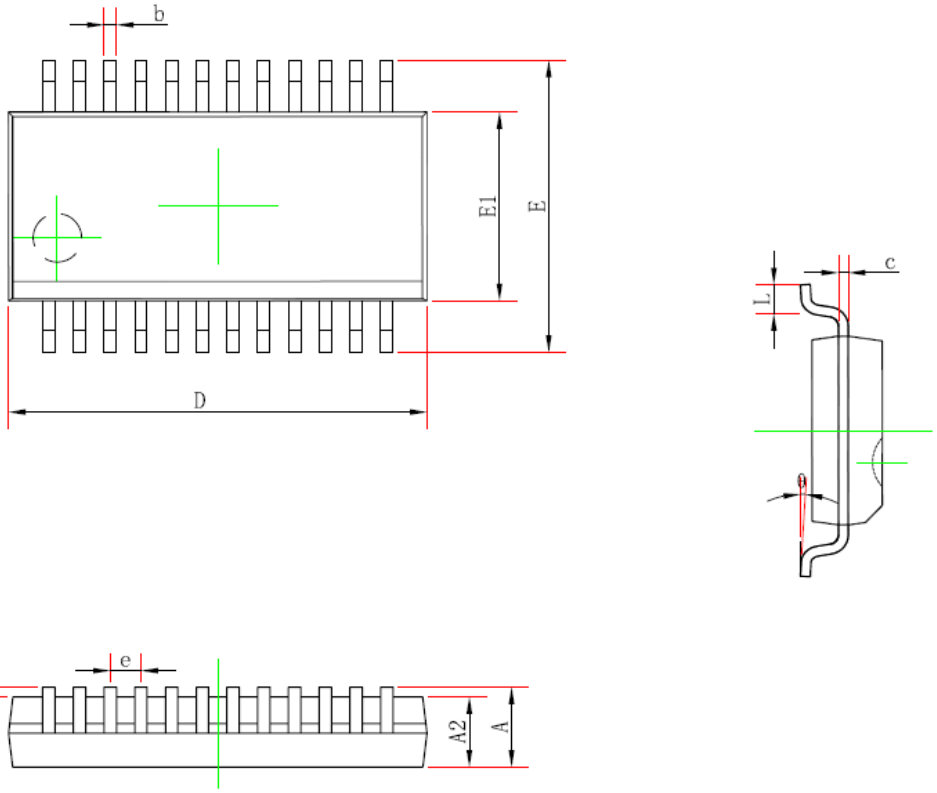
Package

SSOP24



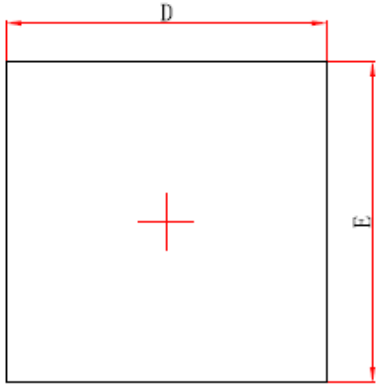
Symbol	Min (mm)	Max (mm)
A	-	2.15
A1	0.05	0.35
A2	1.2	1.9
b	0.15	0.75
c	0.05	0.45
D	12.6	13.5
E	7.6	8.5
E1	5.6	6.5
e	1.0TYP	
L	0.2	1.0
θ	0 °	10 °

QSOP24

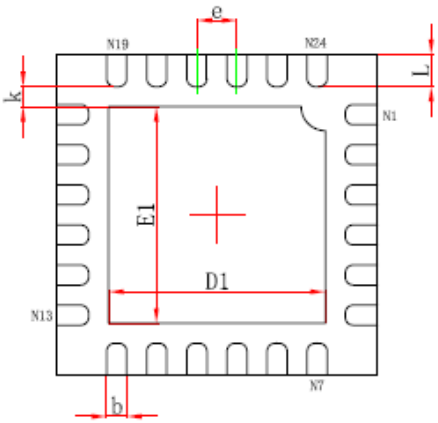


Symbol	Min (mm)	Max (mm)
A	-	1.95
A1	0.05	0.35
A2	1.05	-
b	0.1	0.4
c	0.05	0.254
D	8.2	9.2
E1	3.6	4.2
E	5.6	6.5
e	0.635TYP	
L	0.3	1.5
θ	0 °	10 °

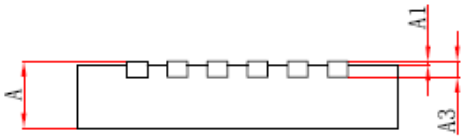
QFN24 (4 * 4)



Top View



Bottom View



Side View

Symbol	Min (mm)	Max (mm)
A	0.6	1.0
A1	-	0.1
A3	0.203REF	
D	3.8	4.3
E	3.8	4.3
D1	2.4	3.0
E1	2.4	3.0
K	0.2min	
e	0.5TYP	
b	0.1	0.4
L	0.2	0.7