AND9183/D

Using Interline CCD Image Sensors in High Intensity Lighting Conditions

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APPLICATION NOTE

Introduction

ON Semiconductor image sensors are successfully deployed in a wide range of harsh outdoor applications. They are well suited for both bright and low light conditions and operate fully as expected. However, in the rare case that extreme bright light reaches the sensor, there are some design considerations necessary to avoid sensor damage. A camera design enhancement is recommended by ON Semiconductor to improve system robustness, as detailed in this document. The scope of this application note is limited to visible imaging applications using ON Semiconductor Interline Transfer CCDs. Issues related to short wavelength radiation [1] and physical damage due to excessive heating are not addressed here.

High Intensity Visible Lighting Conditions

What conditions constitute “high intensity visible lighting”? A helpful rule of thumb is if the scene would be considered painful or harmful when viewed by the human eye, then it might be damaging to the image sensor. Conditions such as imaging a direct reflection of the sun from a shiny surface or imaging the sun directly through a wide aperture are examples of potentially damaging illumination levels. For outdoor applications, designers should consider whether the camera may be inadvertently pointed at the sun or a specular reflection of the sun. In trials conducted by ON Semiconductor, these kinds of scenes, especially when viewed through wider apertures, generated light levels that could damage CCDs. It was also found that these conditions make useful imaging difficult because of lens flare, internal reflections and other secondary effects.

Interline CCD Device Structure and Operation

When an image is captured with optimal exposure [2], light enters the pixel and is converted into electron−hole pairs (ehp) in the silicon. The photodiode collects the electrons which are subsequently transferred to the output through the CCD shift registers. The GND (or PWell) pin electrically balances the region by removing the excess supply of holes. At exposures above the photodiode charge capacity, a portion of the electron current begins to flow from the photodiode through the PWell region to the SUB pin [3] – otherwise known as the vertical overflow drain (VOD) for blooming control. All electron charge collected in the photodiode can be optionally removed during imaging by pulsing the SUB pin with a sufficiently high voltage. This function is commonly used for electronic shuttering and, in this case, all electron current flows to the SUB pin.

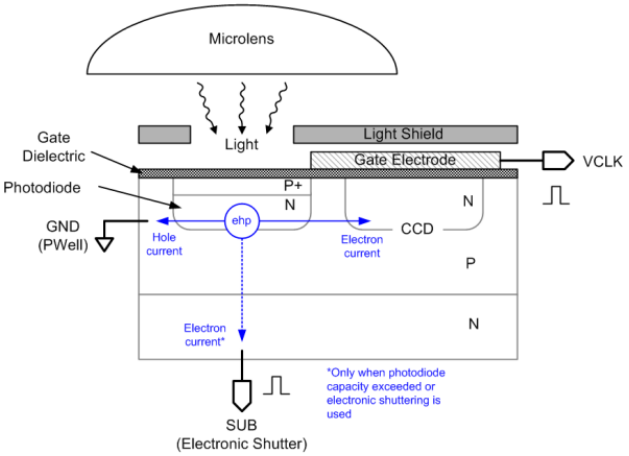

Figure 1. Interline CCD Structure and Operation

Device Effects under High Intensity Lighting Conditions

The interline CCD pixel structure contains a parasitic NPN transistor (Qp) comprising the SUB and GND pins and the internal CCD buried channel regions as shown in Figure 2 [4, 5]. The GND pin effectively consists of a ring surrounding the array of pixels. Pixels physically close to the edge of the array, therefore, have relatively low values of PWell resistance (Rp) whereas pixels in the center have the highest Rp values.

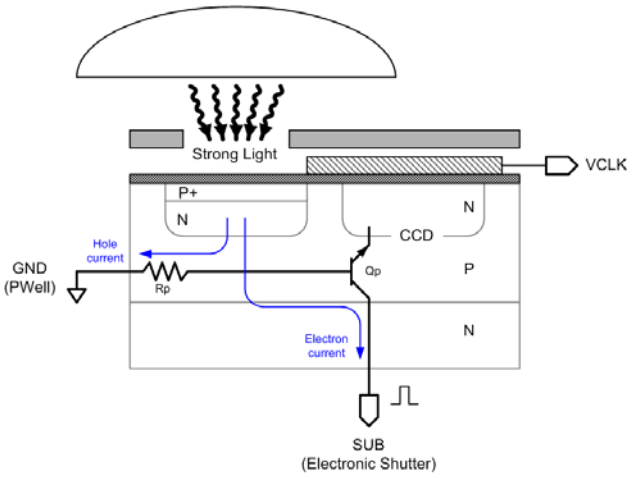

Figure 2. Interline CCD Structure Illustrating Parasitic NPN Transistor

As the array size increases, and pixels are placed farther from the GND ring, Rp values will grow higher. The effective Rp resistance will also depend on other factors such as pixel design and pixel array aspect ratio. The ON Semiconductor 9 μm, 7.4 μm and 5.5 μm interline pixel sizes all use different pixel designs meaning Rp values are different even in cases where the physical array sizes are the same. Likewise, a square format sensor will generally have higher Rp values at the center than a sensor with a 16:9 aspect ratio of the same resolution.

When light levels are sufficiently high, it is possible to create a sensor plane irradiance as high as 1000 W/cm^2. This irradiance has been observed to create electron currents to the SUB pin in the milliamp range. Under these conditions, the corresponding hole current in combination with Rp cause the PWell potential to rise locally – possibly to the point where Qp turns on. When this situation occurs, the voltage being applied to the SUB pin is effectively connected to the CCD.

Operational Limits: Mechanism and Observations

While Qp is on, the gate dielectric (see Figure 1) will experience an electric field (E) related to the SUB and VCLK voltages and the gate dielectric thickness (tOX) as shown in Equation 1.

$$E = \left(\frac{V_{SUB} - V_{VCLK}}{t_{OX}}\right) V/cm \qquad \text{(eq. 1)}$$

If the electric field approaches or exceeds the material breakdown properties of the gate dielectric, damage to the interface can result at the bright spot location affecting dark current and charge transfer efficiency – both from the photodiode to the CCD (lag) and within the CCD register itself (CTE). In practice, SUB voltages less than 20 V do not cause damage under any illumination condition. However, the electronic shutter voltage requirements range anywhere from 30 V to 50 V and therefore damage is possible whenever this voltage level is applied in conjunction with high intensity lighting conditions.

Figure 3 demonstrates these points using the KAI−16000 Image Sensor, a 35 mm format device, as a test vehicle. In this case, the device was exposed to several instances of a high intensity light spot at different locations within the array while an electronic shutter pulse of 50 V was repeatedly applied. The image shown is a flat field exposure that is subsequently contrast enhanced to better observe the artifacts.

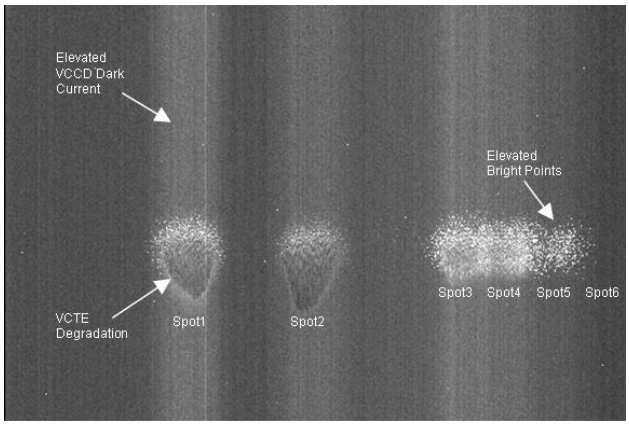

Figure 3. Examples of Damage to a KAI−16000 Image Sensor due to Bright Spot Exposures

Spot1 and Spot2 are exposure events near the center of the array where Rp is highest. It shows the elevated photodiode and readout dark current and worst CTE degradation. Spot3 through Spot6 are moved towards the edge of the array and show progressively less damage for the same exposure condition. In general, repeated exposure events at the high SUB voltage continually degrade the observed performance of the sensor.

Recommended Operating Guidelines

ON Semiconductor has developed operating guidelines that can be followed to help reduce the probability for damage under these conditions:

1. Use the minimum shutter voltage specified.
2. Do not operate the electronic shutter while the camera is in idle mode.
3. If operating the electronic shutter in idle mode is necessary, increase the lens f/# (that is close the camera iris to a minimum) instead.
4. If operating the electronic shutter in idle mode is necessary, hold VCLKS to their specified high level instead.
5. If operating an auto exposure routine that controls the lens iris (or lighting levels in some other way), if possible, initialize the iris to the smallest aperture and adjust it wider until the desired lighting levels are reached rather than starting at the widest aperture.

In many cases, these practices may provide very minimal protection. Because images taken under these extreme bright light conditions yield extremely limited information,camera designers might also consider the addition of a circuit which preemptively disables the operation of the electronic shutter when the SUB current exceeds a pre−determined level. An example is shown in Figure 4 but other similar approaches may be more appropriate depending on camera architecture. In this case, a SUB current of ~0.5 mA through resistor R1 will logically disable the high voltage electronic shutter pulse from being applied to the device, preventing damage under any condition. VLogic represents the logic power (5 V, 3.3 V, etc.) used for camera digital circuits. The additional circuit components to implement this functionality are highlighted in blue. The disable signal could also be used as part of an auto−exposure system.

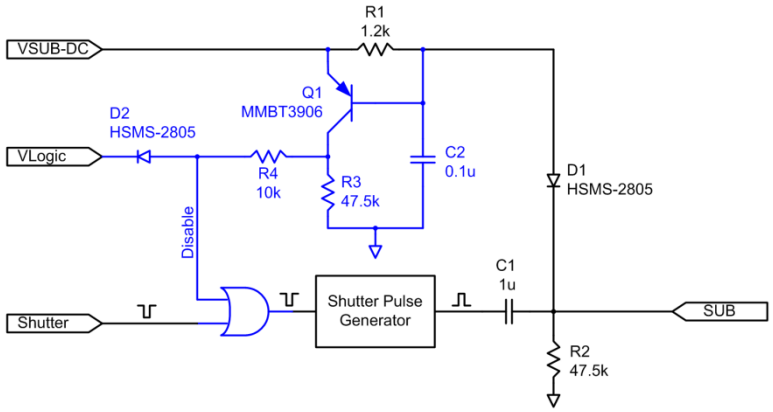

Figure 4. Example Electronic Shutter Disable Circuit

The maximum current at which to trigger the disabling circuit is dependent on many factors as described earlier. Sensor sizes ranging from ½" to 35 mm optical formats at varying pixel sizes have been characterized. The resulting threshold for damage ranges from ~4 mA to ~2.5 mA respectively. Therefore, setting a threshold at 0.5 mA gives sufficient margin for protection for all ON Semiconductor devices within this format range. Testing of devices in high intensity lighting conditions showing SUB currents of 0.5 mA did not produce any useable regions of the image regardless of spot size. The camera designer, however, should always evaluate the proper threshold for the particular application involved.

References

1. J. Killiany, "Radiation effects on silicon charge coupled devices," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. CHMT−1, No. 4 (1978).
2. Such as found in general home or office controlled lighting conditions.
3. Longer (eg NIR, IR) wavelength light also contributes to SUB electron current even if the photodiode capacity has not been exceeded.
4. There is a similar parasitic NPN formed to the photodiode but, because there is no overlying gate electrode, it becomes a secondary effect in this situation.
5. There is also a resistance for electron current from the photodiode to the SUB pin but it remains constant for all pixel locations and is generally lower than Rp and therefore is not as relevant to this discussion.

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