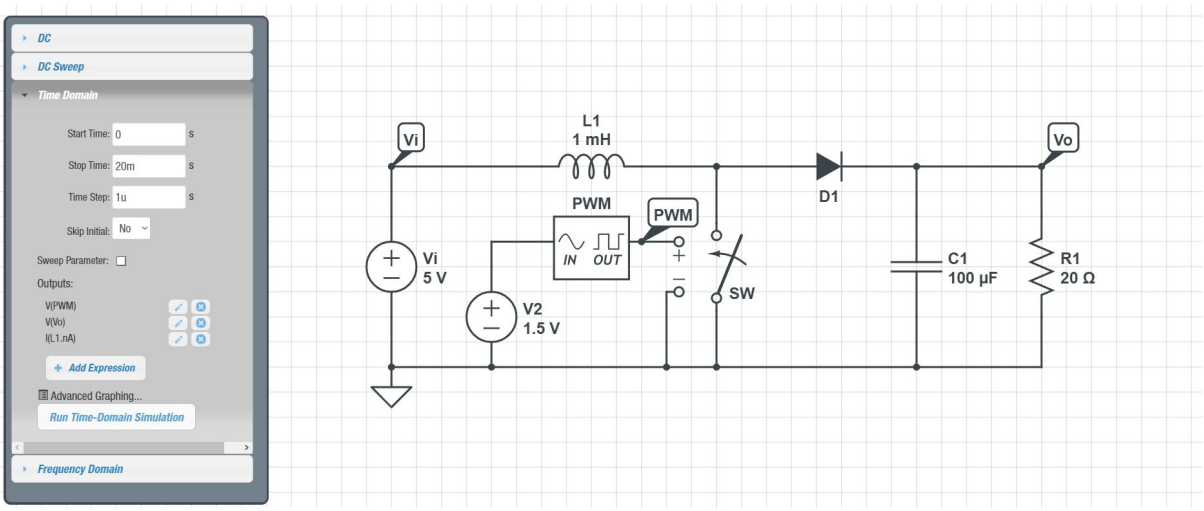
EEP1 ELogBook – Week 9

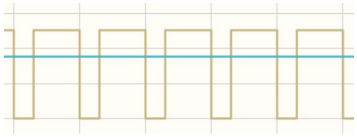
AXXXXXXX - Brians Tjipto Meidianto

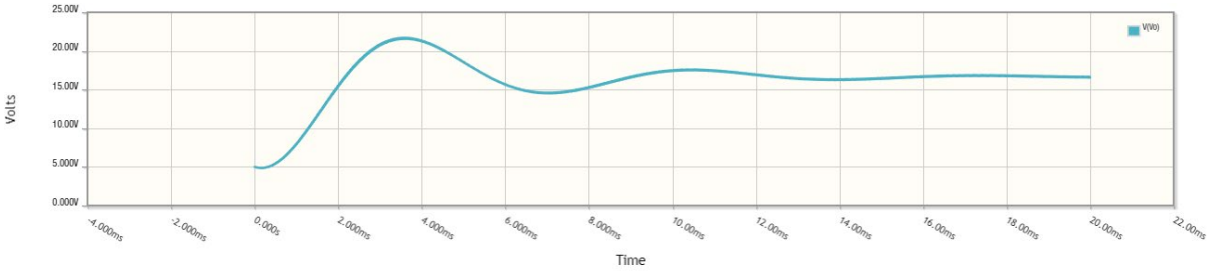
Studio

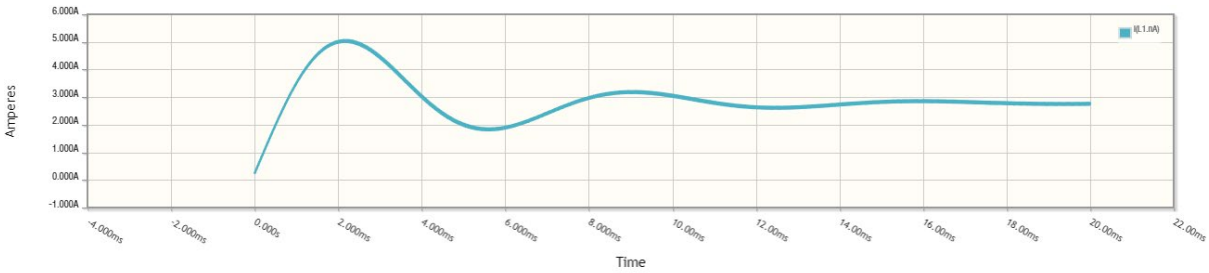
Activity 1



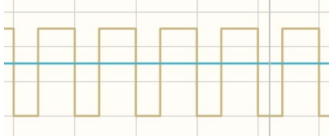
70% Duty Cycle (control 3.5V)

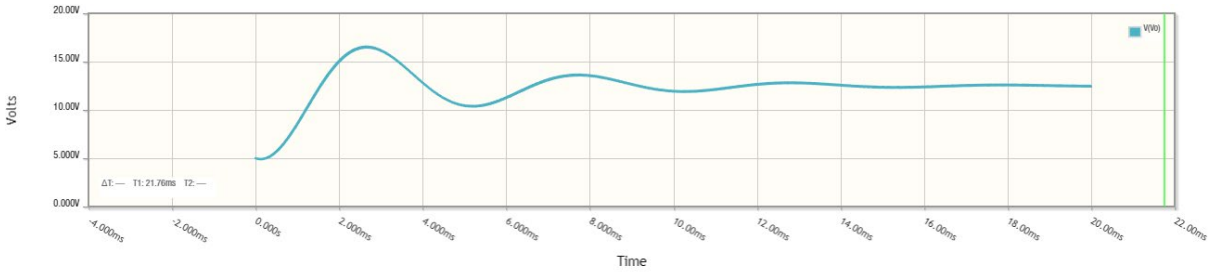


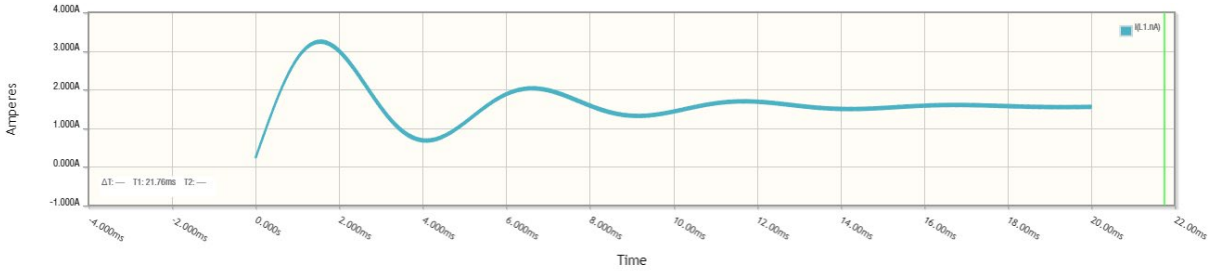




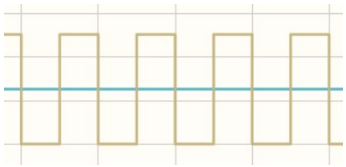
60% Duty Cycle (control 3V)

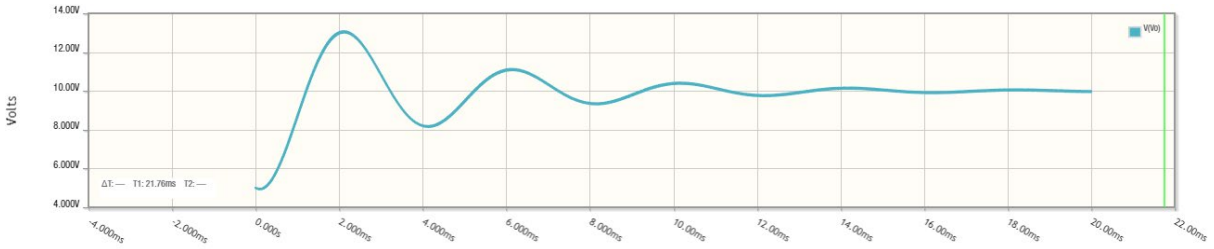


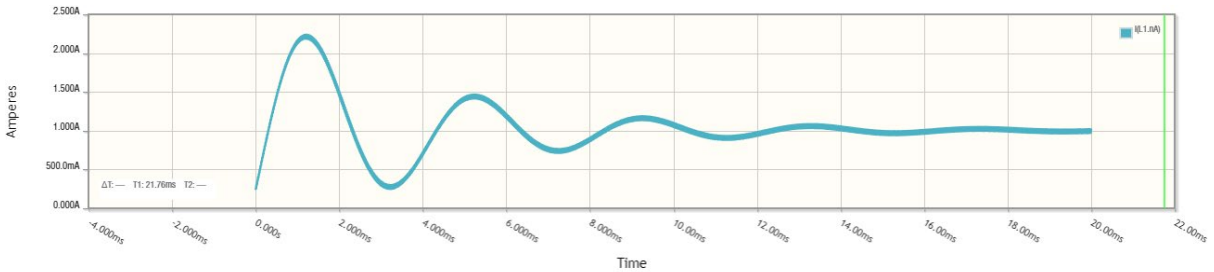




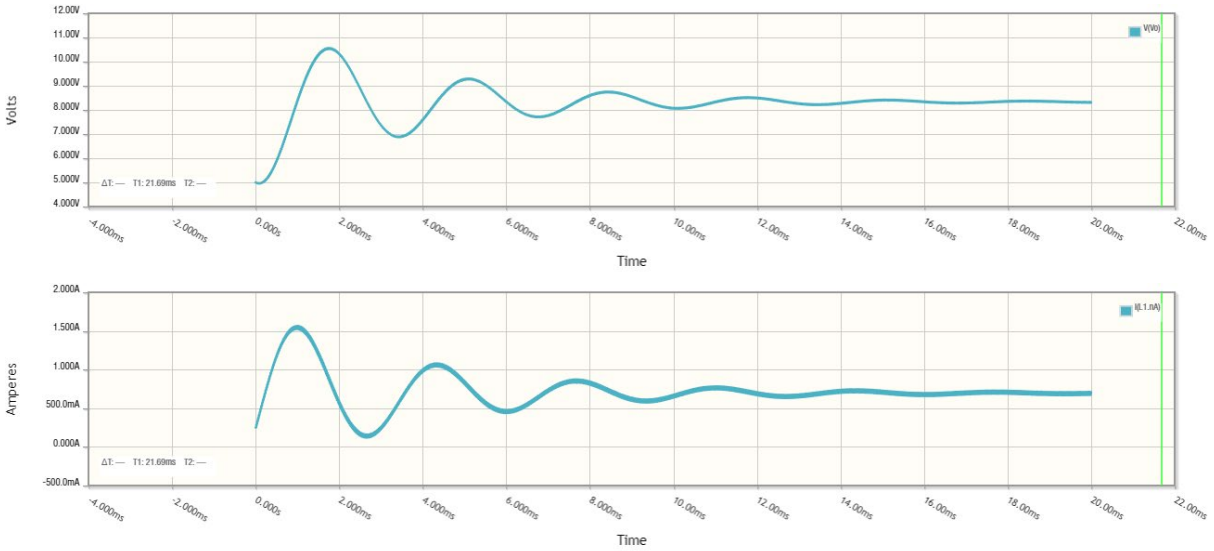
50% Duty Cycle (control 2.5V)



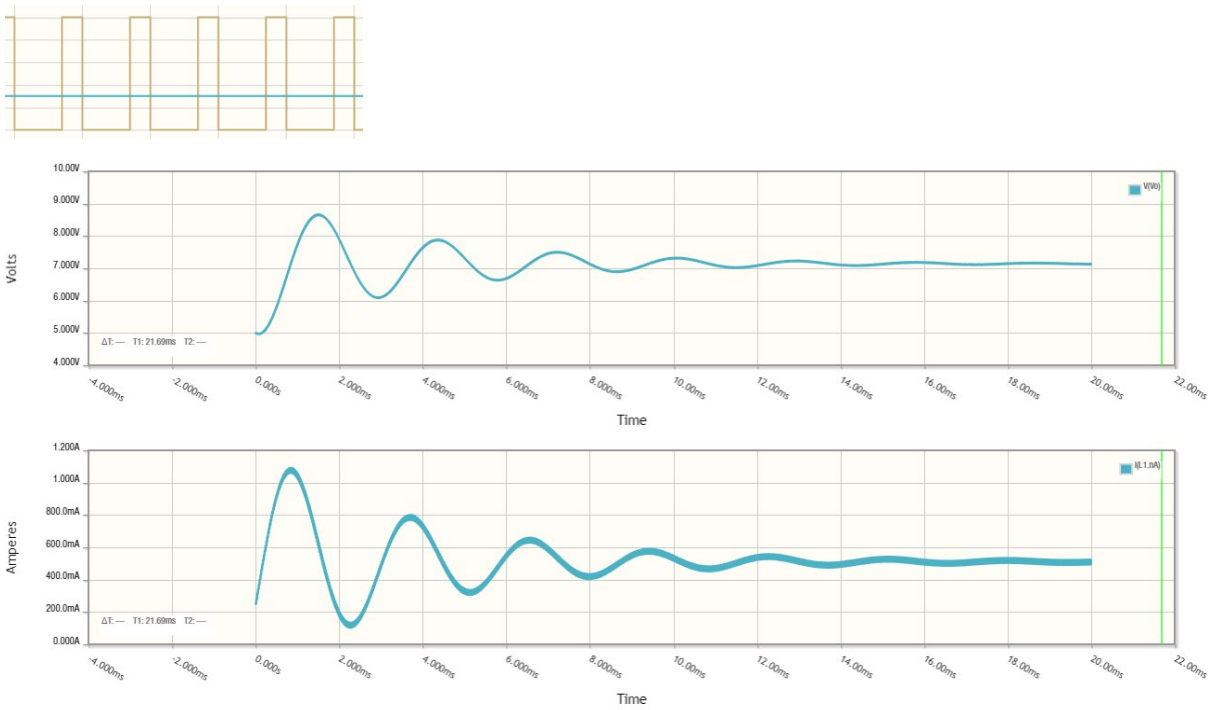




40% Duty Cycle (control 2V)



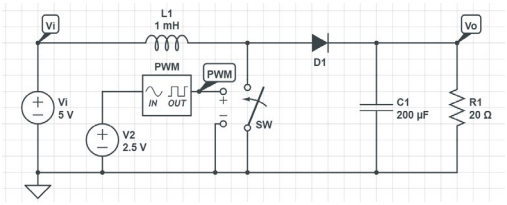
30% Duty Cycle (control 1.5V)

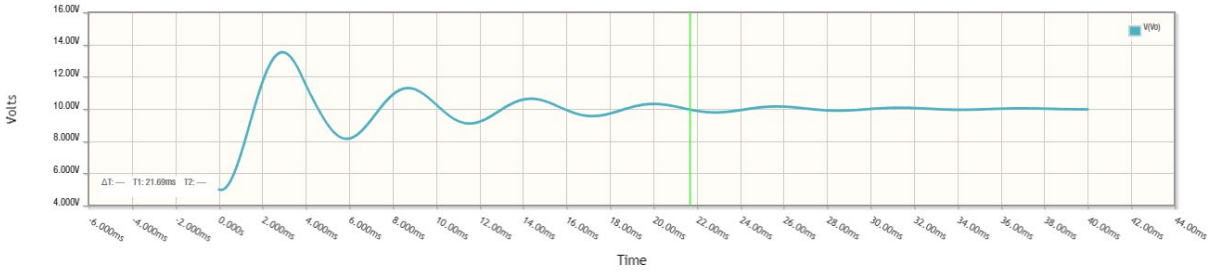


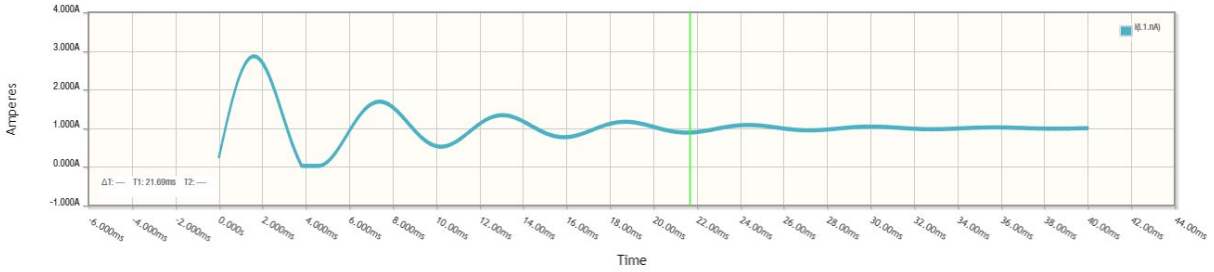
Duty Cycle, D	Control Voltage	Theoretical Vo	Vo from simulation
70%	3.5V	16.67V	16.56V
60%	3V	12.5V	12.42V
50%	2.5V	10V	9.948V
40%	2V	8.33V	8.299V
30%	1.5V	7.14V	7.121V

As the Duty cycle decreases, the Voltage also decreases, the ripple will slowly go to a steady state, the lower the steady state, the less amount of time it will take to reach the steady state.

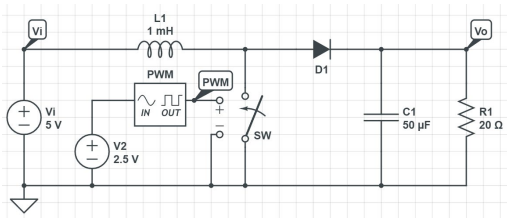
200uF – 0 to 40ms

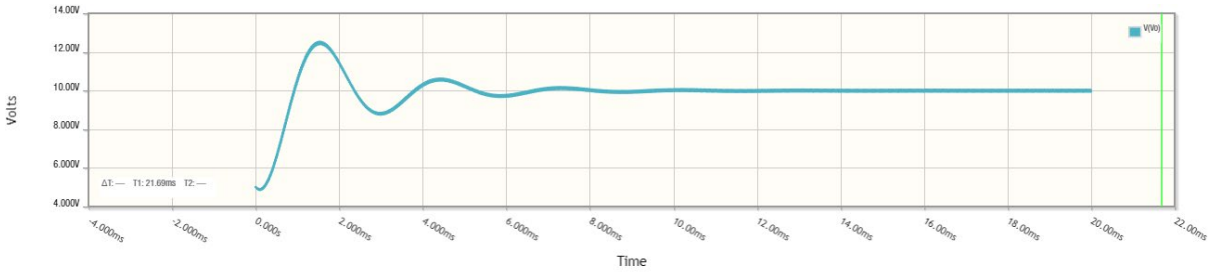


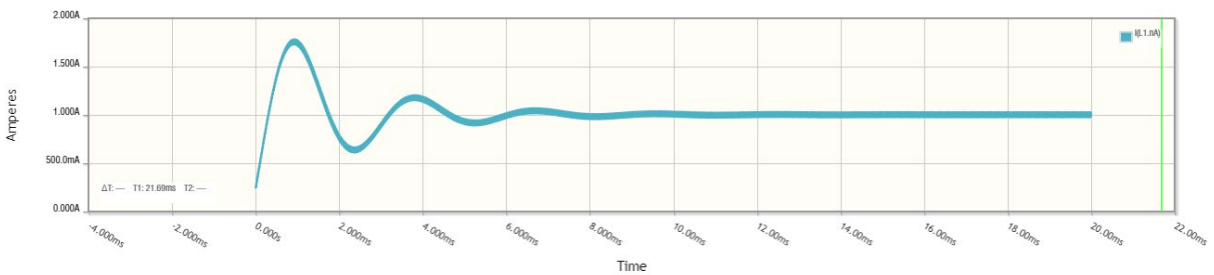




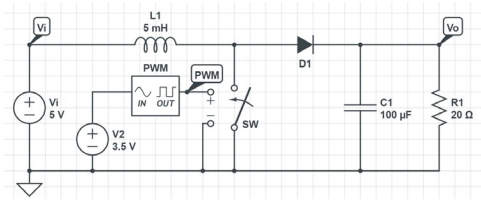
50uF

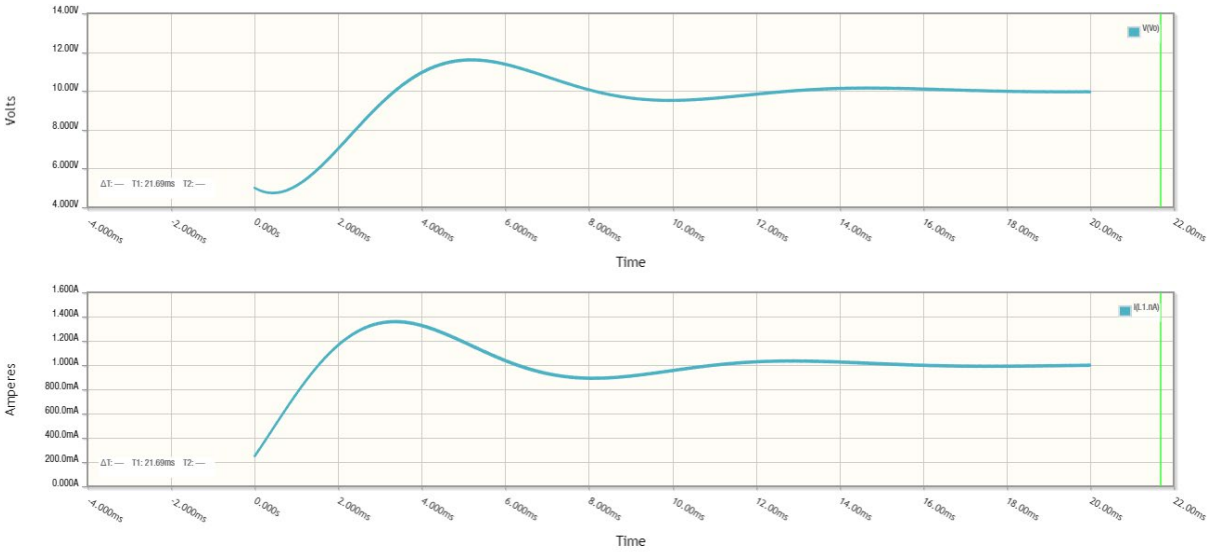




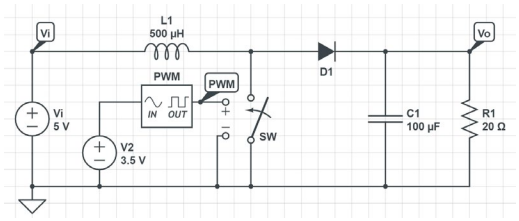


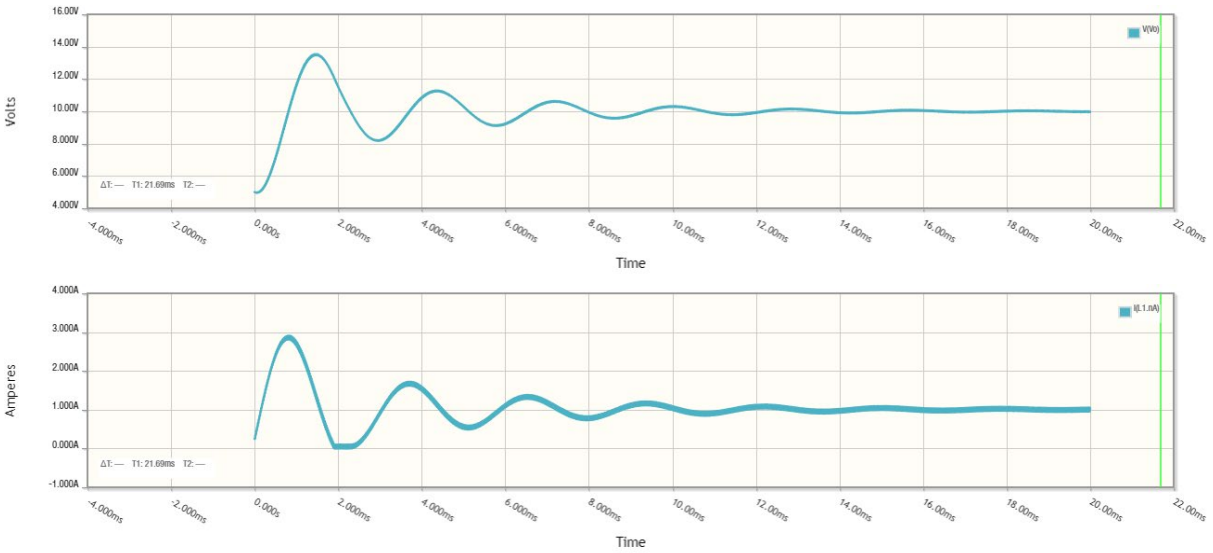
5mH





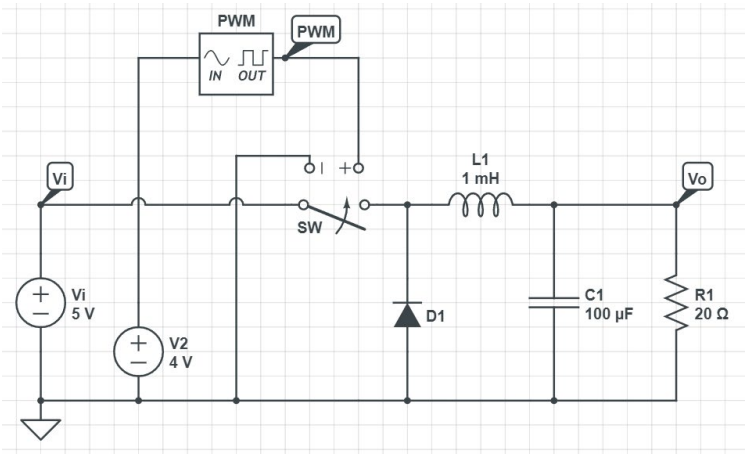
500uH

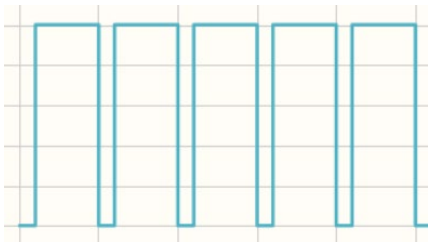




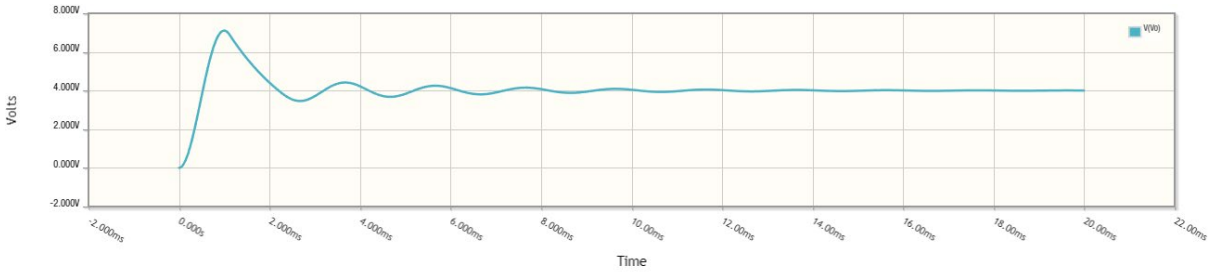
The higher the Capacitor, the more ripple will form, while the lower the Inductor, the more ripple will form.

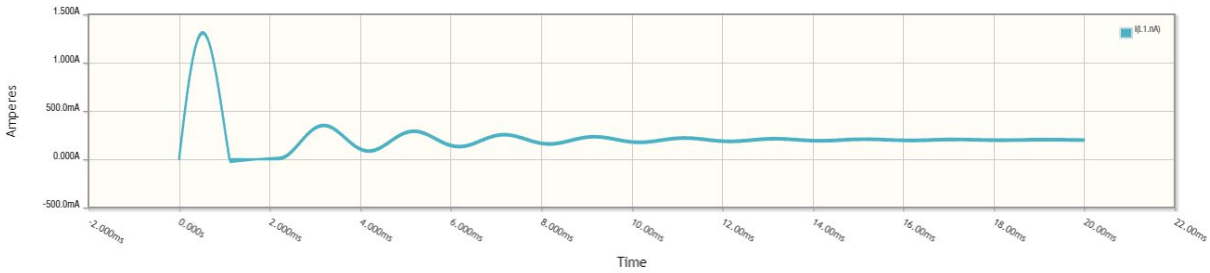
Activity 2



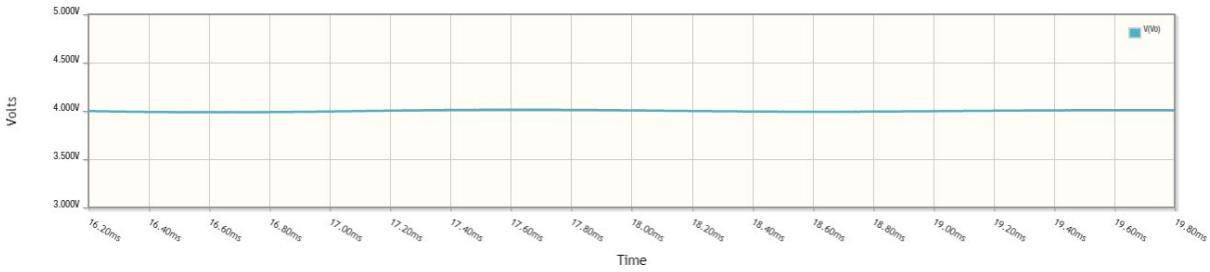


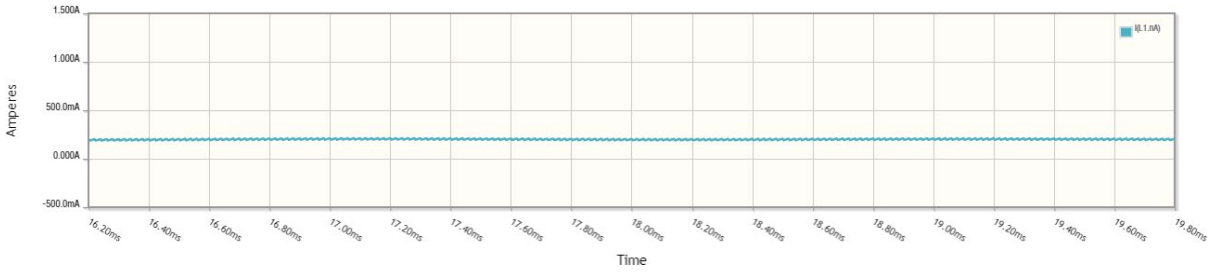
80% Duty cycle – steady state voltage: 4.003V





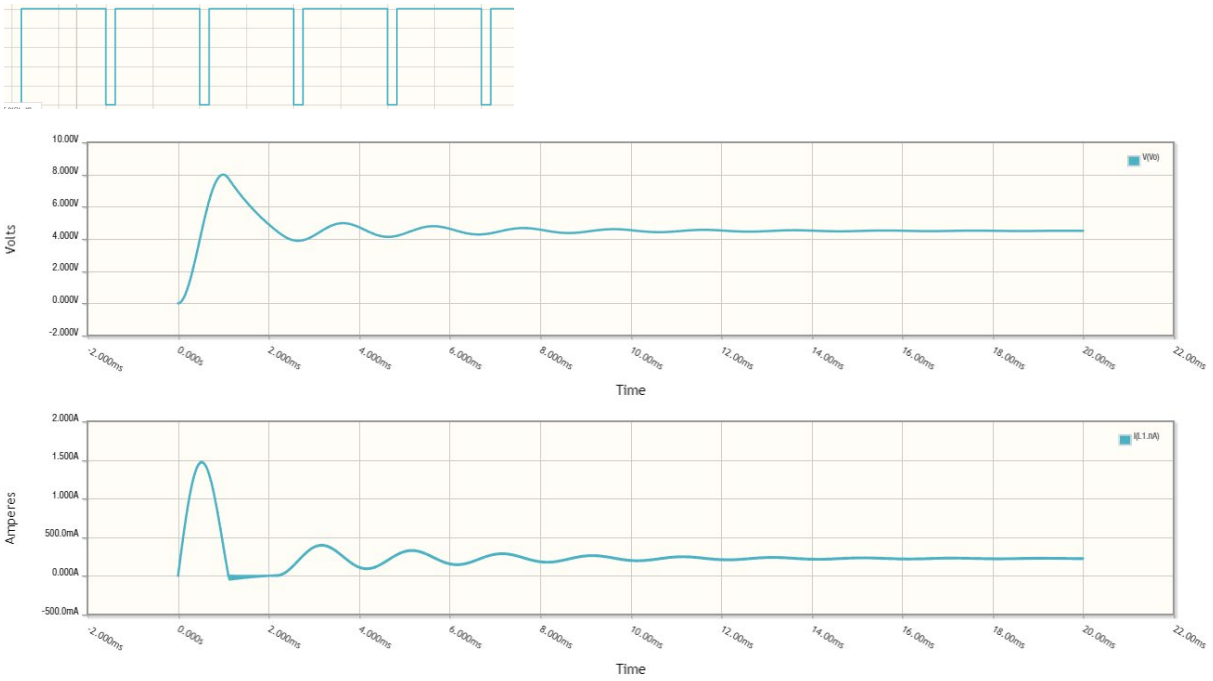
When steady state





70% Duty cycle – steady state voltage: 3.503V

90% Duty cycle – steady state voltage: 4.503V

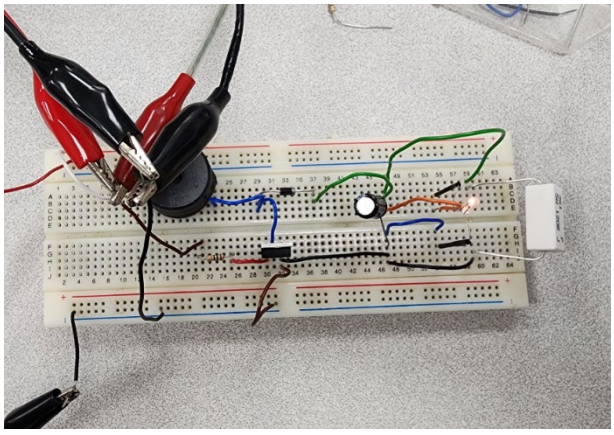


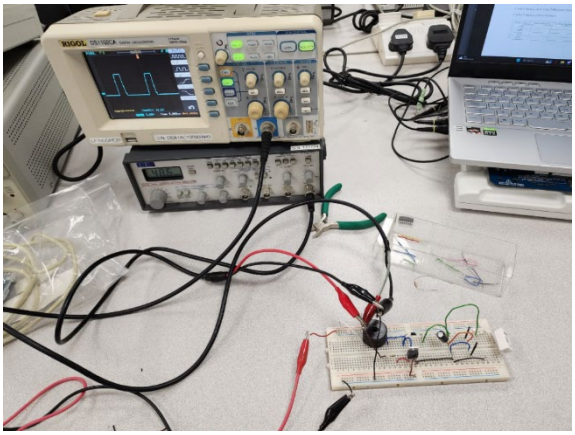
As the Duty cycle increases, the steady state voltage also increases, and he higher the Duty cycle is the more ripples will form.

Lab

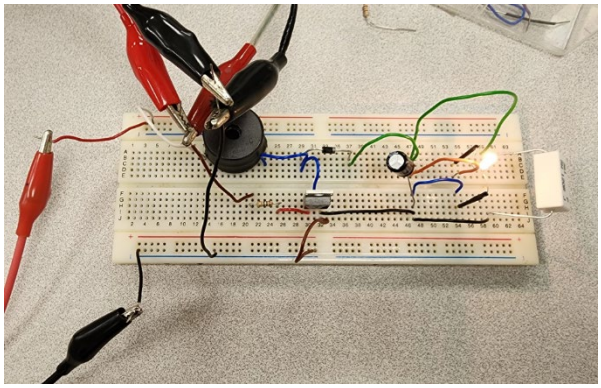
Duty Cycle, D	Theoretical Vo	Vo from simulation
60%	12.5V	12.002V
50%	10V	9.693V
40%	8.33V	8.192V
30%	7.14V	6.916V

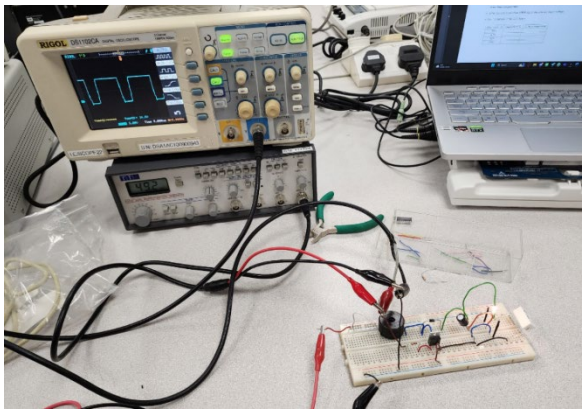
Dim (Lower Duty Cycle)



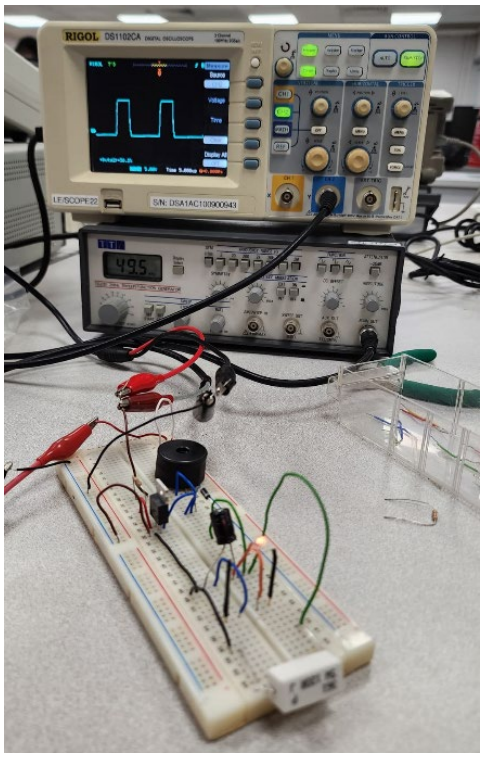


Bright (Higher Duty Cycle)

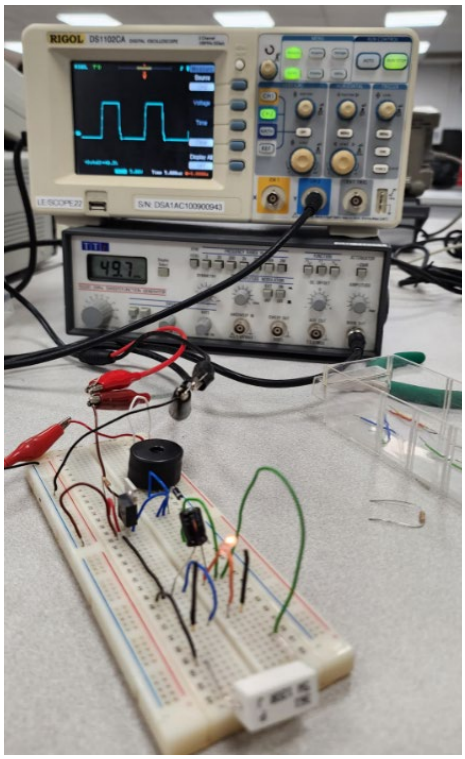




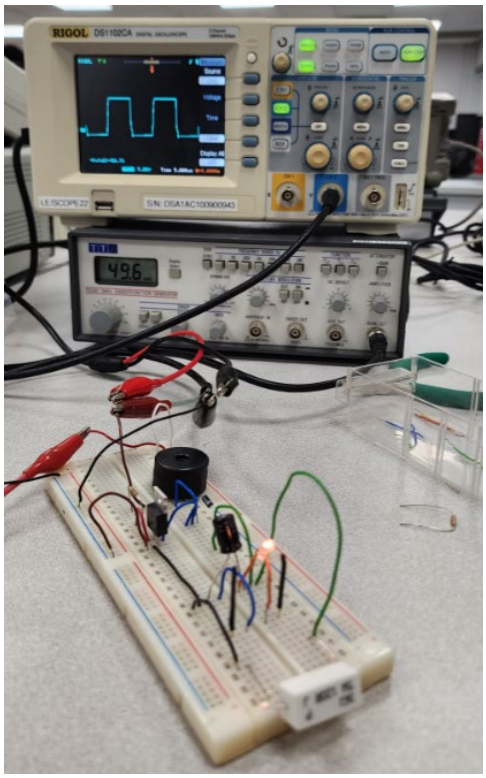
30%


RIGOL DS1102CA
49.5

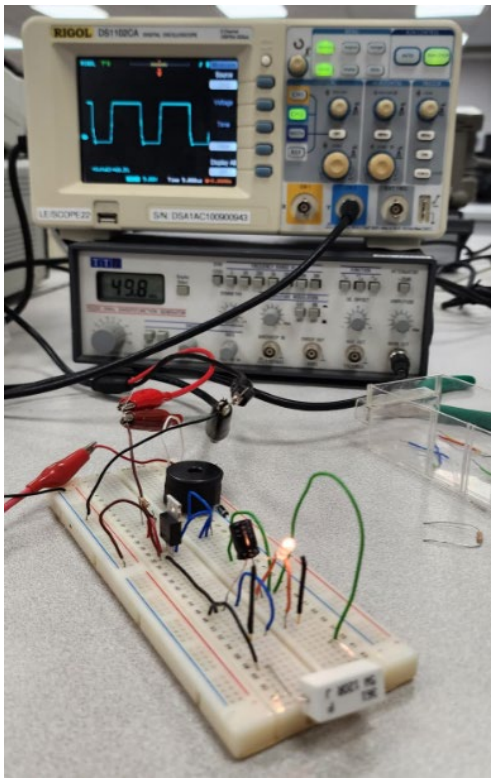
40%


RIGOL DS1102CA
49.7

50%


RIGOL DS1102CA
49.6

60%


RIGOL DS1102CA
49.8

The differences between the simulation with the ideal device and the actual implementation is that the values vary by a bit due to the internal resistance in the wire, but generally it is still accepted under the range experimental accuracy. Another reason may be that the values of the capacitor inductor and the resistor may not be the exact same as the stated values.