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Conference Paper · July 2012

DOI: 10.1109/CICSyN.2012.84

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Performance Analysis of First Order Digital Sigma Delta ADC

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***Abstract*— Ever-growing era of mobile and personal wireless networks, motivated research in several fields of engineering resulted in low power and low cost consumer products. The voice band processing required in mobile applications demand for architectures, which can easily be integrated in single chip SoC applications. The conventional approach is to have a dedicated IC outside the digital ICs to perform analog to digital conversion. The motivation of single chip radios demand for integration of such ADC modules on digital cellular related ICs. Mixed signal design is very challenging and hence usually it is preferred to have separate ADC chip before the ASIC/FPGA. In this paper we present a digital sigma delta ADC architecture, which can perfectly be integrated in any digital IC with a targeted sampling rate of 20 kS/s with more than 80 dB dynamic range**.

Keywords—Analog to digital converter, Digital Sigma Delta ADC, LVDS, Decimator, Inter Modulation.

I. INTRODUCTION

CMOS technology scaling has motivated the replacement of analog components in signal-processing systems with their digital counterparts for improved reliability, flexibility, and process portability Analog to Digital Converters (ADCs) are the most critical modules in modern voice band, audio, communication and high-resolution precision industrial measurement applications. The efficient realization of ADC, with low power, smaller board size and low cost allows benefits in all most all electronic products. The present day scenario of separate ADC chip followed by ASIC or FPGA approach for doing DSP has the following limitations.

(a) In spite of tremendous growth in EDA for VLSI, the analog VLSI synthesis is not automated. Hence the ADC kind of mixed signal design circuit remains as challenge and heavily depends on experience VLSI designers.
(b) The ADC chip occupies additional space on the board.
(c) Most of the ADC chips require a considerable number of passive components outside resulting in increase of BOM, board real estate and cost.
(d) With more number of components, the reliability is less.
(e) The interface between ADC and ASIC/FPGA requires special attention in terms of protocol and timing.

Sigma Delta (ΣΔ)ADCs stand different in comparison with other ADC architectures due to their basic principle of operation and approaches to improvise the performance. An extensive research work was carried out by VLSI engineers studying the various aspects. Most of the research work related to architecture exploration of ΣΔ ADC, can be classified in to two categories. Firstly, Studying various analog block variants for performance improvisation and second, Analog versus digital implementation variants for several blocks of ΣΔ ADC. ΣΔ ADC architecture as in fig. 1 allows the realization of reasonably good performance ADC with single bit ADC, single bit DAC, noise shaping and oversampling principles [1]. Recently the research oriented for realizing the implementation of ΣΔ ADC with full digital techniques is motivated by the fact that the digital ICs are capable of running the core at GHz clock rates and I/Os more than 500 MHz clock rates[2].

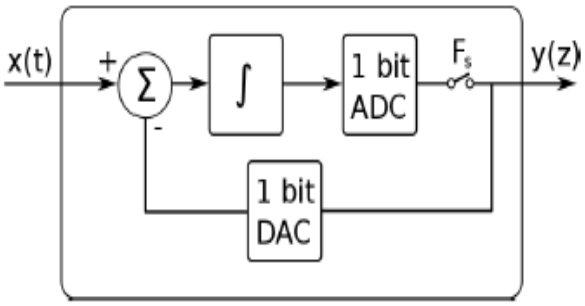

Fig.1 Basic Sigma Delta ADC Architecture.

Section II of this paper presents the proposed Digital ΣΔ ADC Architecture and LVDS characteristics. Transient analysis of the analog section are carried out in section III followed by the performance analysis and two-tone test for linearity in section IV. Section V concludes the paper.

II. PROPOSED SIGMA-DELTA ADC ARCHITECTURE

A very little research has gone in the direction of realizing the ΣΔ ADC with full digital techniques and further optimization towards achieving better performance. As the present day digital ASICs and FPGAs are available with higher clock rates for both logic and I/O operations, it is possible to realize novel architectures achieving required performance level. The proposed Digital ΣΔ ADC architecture with LVDS digital comparator and first order RC integrator is as shown in fig. 2.

978-0-7695-4821-0/12 $26.00 © 2012 IEEE
DOI 10.1109/CICSyN.2012.84

The LVDS differential input pin is proposed to be used as comparator which is fed with analog input signal and Integrated Digital Representative of Analog signal (referred as IDRA signal from now onwards). The input signal is compared with the IDRA signal and results in output 1 when input analog signal is higher than IDRA and 0 otherwise. The rate at which the LVDS comparator output can be read becomes a crucial parameter (assuming the analog counter parts are made to work at those speeds) for deciding the highest possible oversampling for a targeted ADC sampling rate.

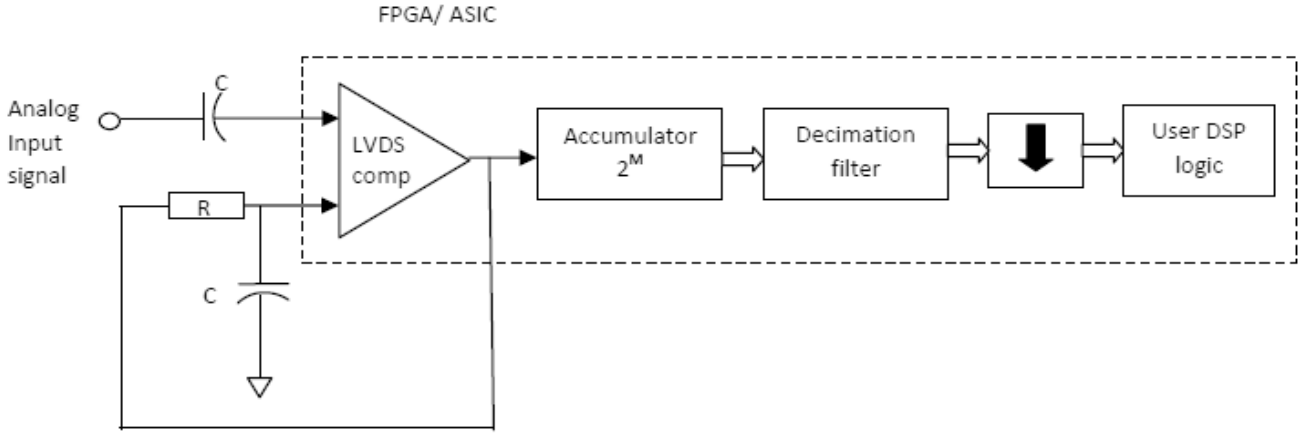

Fig. 2. High Level design of proposed first order Digital Sigma Delta ADC.

This rate depends on technology factors with which the ASIC/FPGA is realized. The rate at which the LVDS comparator output is designated as LVDS_CLK and the maximum possible value will be referred as MAX_LVDS_CLK for analysis. The full scale input value depends on the LVDS characteristics of acceptable input voltage range over which the comparator performance is suitable to the sigma-delta requirement.

The comparator output signal being "1" indicates that a positive excursion has occurred since the last sample, and a "0" indicates that a negative excursion has occurred since the last sample. If the input signal is near positive full-scale, it is clear that there will be more "1"s than "0"s in the bit stream. Likewise, for signals near negative full-scale, there will be more "0"s than "1"s in the bit stream. For signals near midscale, there will be approximately an equal number of "1"s and "0"s.

Accumulator accumulates the LVDS comparator output bits for 2^M clock cycles producing M bit word. The decimation low pass filter decimates by factor D resulting in a sampling rate given with below expression.

$$f_s = F_{LVDS\_CLK} / D. 2^M$$

Simulation of the proposed architecture is done considering the Xilinx Spartan 6 FPGA's LVDS characteristics. Even though, the aim is to evolve architecture for both ASIC and FPGA, the Spartan-6 is considered for simulation so that it becomes possible to develop the hardware proto type easily. Simulation is carried out in MATLAB and SNR analysis for single tone input signal is performed considering the non idealities of components for simulation. The noise shaping achieved by first order integrator and SNR gain achieved with oversampling is studied and their effect on gain in ENOB is presented.

A. LVDS characteristics of Xilinx

The differential I/O standards supported by Xilinx Spartan-6 FPGA are presented in table. I. The selection of I/O standard has effect on the DC bias assumed at the input and also the peak signal swing supported by realized ADC [4].

TABLE I
LVDS CHARACTERISTICS OF XILINX

Description	V_L	V_H
LVDS (Low Voltage Differential Signaling) 2.5V & 3.3V	1.25-0.125	1.25 +0.125
LVPECL (Low Voltage Positive Emitter coupled Logic) 2.5 V & 3.3 V	1.2 - 0.3	1.2 + 0.3
Mini- LVDS 2.5V & 3.3V	1.2 - 0.125	1.2 + 0.125
BLVDS(Bus LVDS) 2.5V & 3.3V	1.3 - 0.125	1.3 + 0.125

Low voltage positive emitter coupled logic (LVPECL) with V_L=0.9 v and V_H = 1.5 V is considered. This allows the input signal to be with DC bias 1.2 V and with 0.6 V full scale signal swing. Table II shows the simulation parameters considered for the analysis of the digital sigma delta ADC.

III. TRANSIENT CIRCUIT ANALYSIS OF ANALOG SECTION

The architecture proposed as in fig. 2 consists of first order RC. The comparator output which is coming from the single ended LVDS pin of digital logic can be viewed as sequence of positive pulses. If the period at which this pin changes value is T_{clk_LVDS} then the pulse corresponding to one LVDS period duration starting at time T_o can be represented as below.

$$P_o = V [u (t-T_o) – u (t - T_o - T_{CLK\_LVDS})]$$

Where V is equal to V_H, when the digital value is logic '1' and V_L when the digital value is logic '0'.

TABLE II
SIMULATION PARAMETERS FOR THE PROPOSED ADC ARCHITECTURE.

Module	Parameter	Value
Analog Section	Input signal peak-to-peak	0.6 V
	Input signal DC bias	1.2
	R	100 ohms
	C	10 nF
Digital I/O	$F_{LVDS\ CLK}$	400 MHz
	V_L	0.9 V
	V_H	1.5 V
Accumulator	Number of bits to accumulate	4096
	Effective ADC resolution	13 bits (1 sign bit 12 mag bits)
	Output sample rate	97.65 KHz
Decimation low pass filter	Filter order	203
	Filter BW	90% of output sample rate
	Decimation factor	4
	Sampling rate after decimation	24.41 KHz

The V_H and V_L depends on the technology and type of logic used. The 1st order RC network continuously gets the pulses from digital logic. The integrator action of RC network produces the integrated signal level at the V^- input of the comparator [9,12]. The input voltage to the 1st order RC network can be written as below.

$$V_i(n) = \sum_{n=0}^{n} P_i$$

The v_i(n) is effective signal present at the input from 0 sec to i^{th} time period of T_{CLK_LVDS}. To analyze the response of it, the transient analysis must be done.

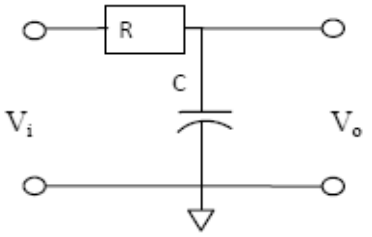

Fig. 3. RC circuit used as integrator

The RC circuit has following exponential response for step input with V volts.

$$V_o = V(1-e^{-t/RC})$$

As the input to the RC circuit is sequence of pulses with V_L and V_H values, the voltage at the output of the RC integrator can be expressed as below.

$$V_o(n) = V_o (n – 1) + (V_i (n) – V_o (n – 1)) e^{-T_{CLK\_LVDS}/\tau}$$

As the voltage output at the single ended pin directly decided step final value, noises in power supply lines of the FPGA/ASIC can effect the performance of the ADC. Fig. 4 illustrate the charge and discharge of integrator's capacitor tracking the input signal.

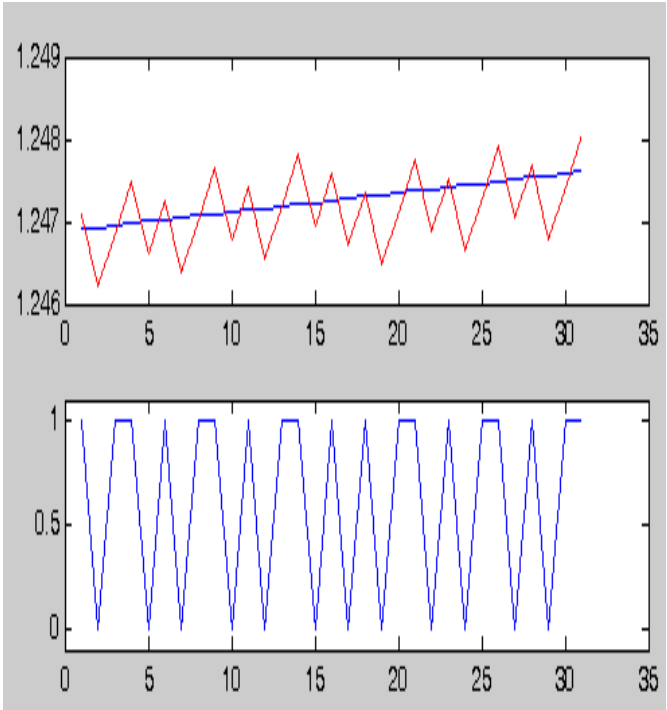

Fig. 4. Integrator output voltage tracking the input signal and the corresponding LVDS comparator output (at the DC level crossing)

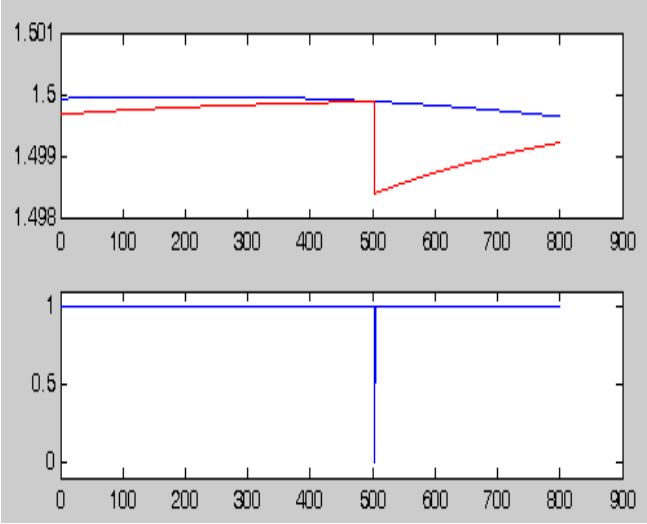

Fig. 5. Integrator output voltage tracking the input signal and corresponding LVDS output (at the positive peak of input sin wave)

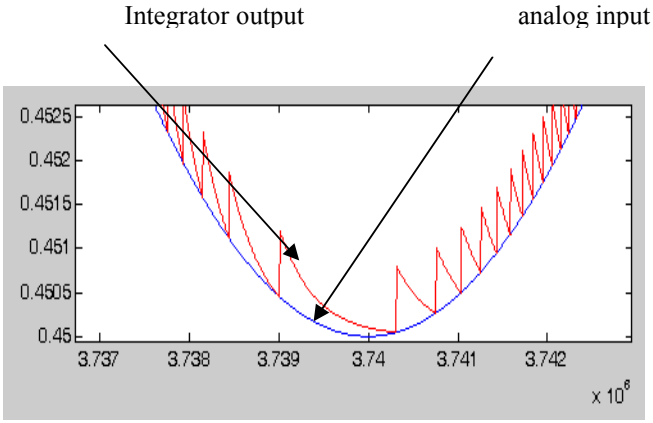

Fig. 6. Integrator output voltage tracking the input signal (at the negative peak of input sin wave)

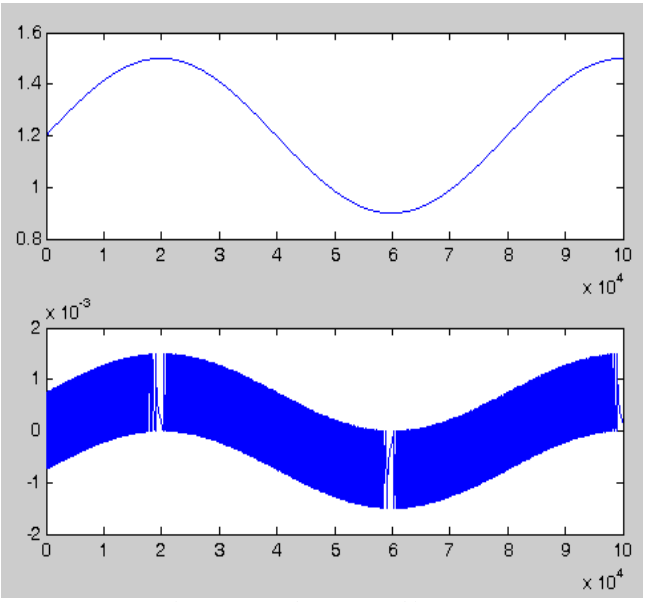

Fig. 7. Input voltage Vs tracking error

The figures 5 and 6 show that the integrator charges/discharges slowly at the peaks, which results in more error between the input signal and integrated signal at the peaks. The figure 7 illustrates the same. The rate at which the capacitor charges proportional to the voltage difference between final value towards which capacitor is charging and the present voltage on capacitor: V(f) – V(i). When the input signal is close to the full scale positive or negative voltages, then this difference is small. Hence the RC integrator slowly tracks the input voltage signal.

IV. Digital Processing and Performance Analysis

A. *Decimation filter*

Decimation filter is the anti aliasing filter required to band limit the signal by $f_s/2D$, such that even after decimation the aliased zone will not disturb the band of interest. The Low pass filter with cutoff frequency $f_s/2D$ is designed using MATLAB FDATOOL, with the following filter specifications.

Filter order = 203
Filter cutoff frequency = $f_s/2D$
Attenuation is stop band = -80 dB
Ripple in pass band = 1 dB
The magnitude response of the low pass filter for decimation factor 4, is shown in figure 8.

B. *Sensitivity (Dynamic Range and SNR)*

The dynamic range of a system is defined as the ratio of the system's maximum input signal power to the system's minimum detectable input signal power or receiver sensitivity over a specified bandwidth [5,7]. The required dynamic range for a receiver can then be specified as the ratio of the largest in-band or out-of-band signal power to the minimum receiver sensitivity. The Blackman-Harris window function is used to avoid the spectral leakage while computing the power spectrum of the ADC captured data. The 1024 point FFT on the windowed samples is computed and power spectrum is estimated. The figure 9 shows the estimated power spectrum in dB scale before the decimation filter stage. The single tone dynamic range observed at this stage is 76.75 dB. The figure 10 shows the power spectrum after the decimation filter stage reporting 82.96 dB dynamic range.

C. *Linearity*

Linearity is very essential property for ADCs. The linearity ensures that no inter modulation (IMD) products are introduced when multiple single tone signals are applied. In practical usage of ADC the input signal can be viewed as multiple single tone signals. In ADCs, linearity is typically specified as SFDR. The SFDR can be defined as the signal-to-noise ratio when the powers of the third-order intermodulation products equal the Noise power [6].

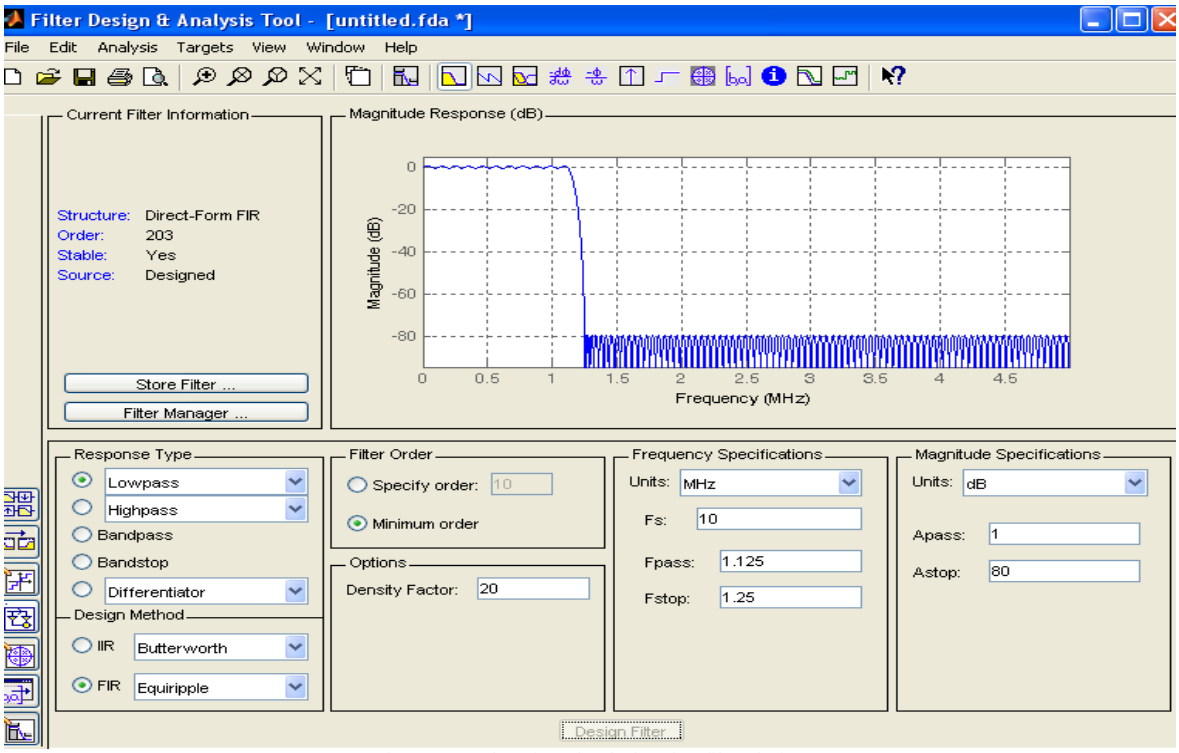

Figure 8. Tool settings for decimation filter design

IMD is generally caused by modulation, and it can occur when an ADC samples a signal composed of two (or multiple) sine-wave signals [4,11]. IMD spectral components can occur at both the sum (f_{IMF_SUM}) and the difference (f_{IMF_DIFF}) frequencies for all possible integer multiples of the fundamental (input frequency tone) or signal-group frequencies.

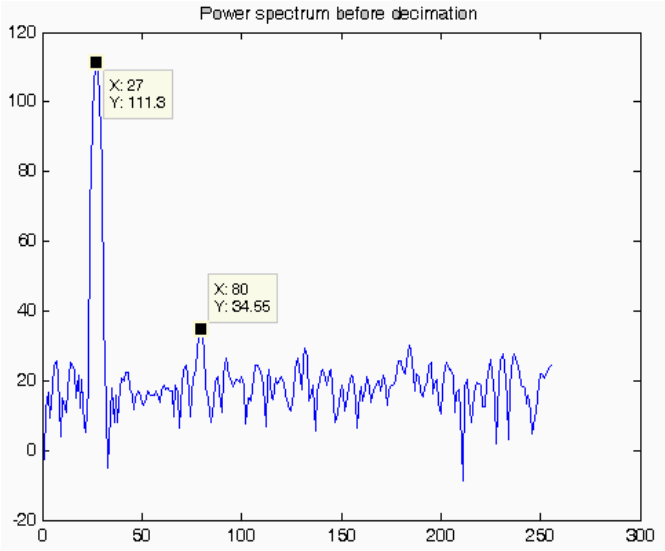

Fig. 9. Power spectrum computed with 512 point FFT

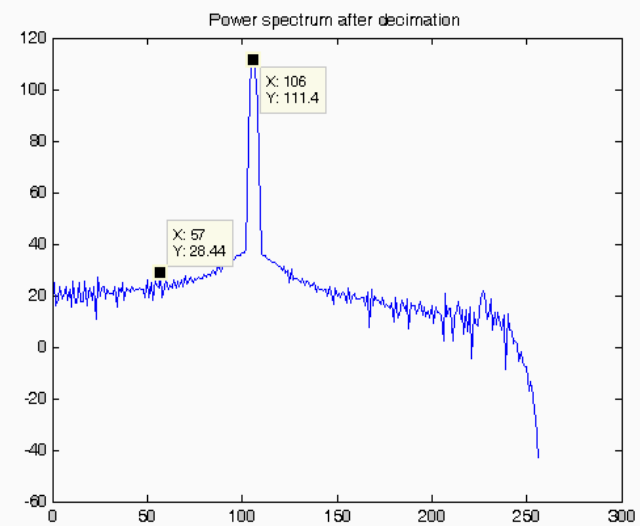

Fig. 10. Sigma delta ADC power spectrum after decimation

For the two-tone IMD test, the input test frequencies f_{IN1} and f_{IN2} are set to 5 KHz and 8 KHz values. The IMD amplitudes for a two-tone input signal are found at the specified sum and difference frequencies:

$f_{IMF\_SUM} = |m \times f_{IN1} + n \times f_{IN2}|$ and $|m \times f_{IN1} - n \times f_{IN2}|$, where m and n are positive integers. The condition that m and n are greater than zero creates the 2nd order ($f_{IN1} + f_{IN2}$ and $f_{IN1} - f_{IN2}$) and 3rd order ($2f_{IN1} + f_{IN2}$, $2f_{IN1} - f_{IN2}$, $f_{IN1} +$

$2f_{IN2}$, and f_{IN1} - $2f_{IN2}$, $3f_{IN1}$ and $3f_{IN2}$) intermodulation products. Simulation results as in fig. 11 shows that no intermodulation products are observed and the ADC presents linear characteristics. However as the peak input signal swing for both the input signals is set to half of the full scale value the two tone SFDR is 6 dB less than single tone SFDR.

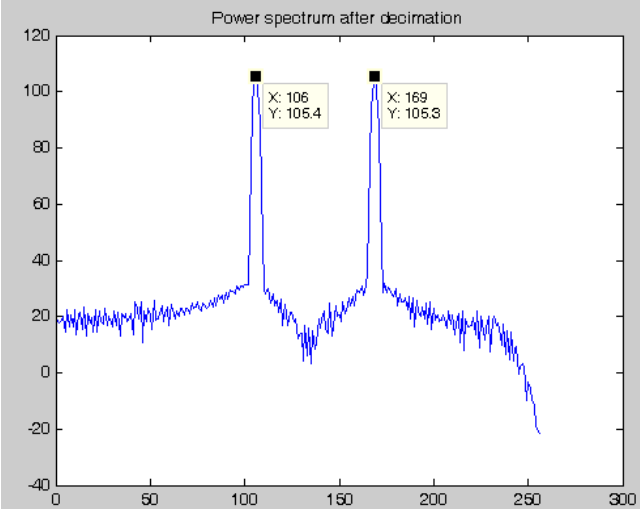

Fig. 11. ADC response for two tone input signal

V. CONCLUSION

Digital ΣΔ ADC architecture is realized with discrete analog components and high speed FPGA/ASICs. The architecture is aimed at evolving custom ADC design framework without separate VLSI design flow. A single pole RC integrator is used to track the input analog signal. The differential I/O based on low voltage positive emitter coupled logic (LVPECL) of spartan 3E is used for comparator and integrator input pulse generation. The accumulator with 4096 bits accumulation is used to form 13 bit 2s complement samples. A decimation filter with order 203 and decimation factor by 4 is used to produce the final ADC samples with 24.41 kS/s sampling rate.

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