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Design and Implementation of Decimation Filter for 15-bit Sigma-Delta ADC Based on FBGA

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Abstract*—A 15 bit Sigma-Delta ADC for a signal band of 40K Hz is designed in MATLAB Simulink and then implemented using Xilinx system generator tool. The second order Sigma-Delta modulator is designed to work at a signal band of 40 KHz at an Oversampling ratio (OSR) of 128 with a sampling frequency of 10.24 MHz. The proposed decimation filter design is consists of a third order Cascaded Integrator Comb filter (CIC) followed by two finite impulse response filters. This architecture reduces the need for multiplication which is need very large area. This architecture implements a decimation ratio of 128 and allows a maximum resolution of 15 bits in the output of the filter. The decimation filter was designed and tested in Xilinx system generator tool which reduces the design cycle by directly generating efficient VHDL code. The results obtained show that the overall Sigma-Delta ADC is able to achieve an ENOB (Effective Number of Bit) of 14.73bits and SNR of 90.4dB.

***Index Terms*—Sigma-Delta modulation, decimation filter, A/D conversion, oversampling, FPGA, VHDL.**

I. INTRODUCTION

Modern electronic systems use front-end ADC's and rear-end DAC's so that the performance of the system can benefit from the use of digital signal processing techniques. As the progress in signal processing continues, the demand for high-speed and high-resolution ADC's and DAC's is growing in applications such as medical imaging, high-resolution video and graphics, high performance controller and actuators, and modem data communication systems including wireless cell site or base station receivers. These new applications demand a large spurious-free dynamic range, wide input bandwidth, and high integral linearity [1]. In the digital form the data can be easily and accurately processed to extract the information desired. [2]. There are different types of analog to digital conversion techniques available today, each having its own advantages and disadvantages. Analog-to-digital converters are categorized into two types namely Nyquist rate converters and oversampling converters depending on the sampling rate. Sigma-delta ADCs come in oversampling converters group [3, 4]. Over sampling converters reduce the requirements of analog circuitry at expense of faster and more complex digital circuitry [5,6]. Sigma-Delta analog-to-digital converters need relatively imprecise analog circuits and digital decimation filtering [5].The sigma-delta ADC works on the principle of sigma-delta modulation. The sigma-delta modulation is a process for encoding high-resolution signals into lower resolution signals using pulse-density modulation. it samples the input signal at a rate much higher than the Nyquist rate. A sigma-delta ADC consists of an analog block of modulator and a digital block of decimator. The modulator samples the input signal at an oversampling rate, generating a one bit output stream and decimator is a digital filter or down sampler where the actual digital signal processing is done [6].

II. SIGMA-DELTA A/D CONVERTER

Fig.1 shows the block diagram of a Sigma-Delta A/D converter. It consists of a sigma-delta modulator and a decimation filter. The modulator can be realized using analog technique to produce a single bit stream and a digital Decimation filter to achieve a multi bit digital output thus completing the process of analog to digital conversion [4,6].

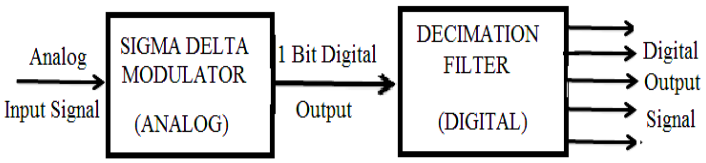

Fig1. Block Diagram of Sigma delta A/D converter [4].

The second order Sigma-Delta modulator consists of an analog difference node, a two integrator, a 1- bit quantizer (A/D converter) and a 1-bit D/A converter in a feed- back structure. The modulator output has only 1-bit (two levels) of information, i.e., 1 or -1. Fig.2 shows second order Sigma-Delta modulator [7].

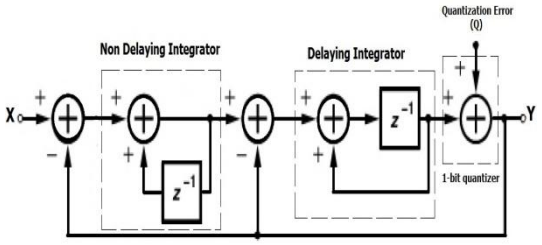

Fig 2. Second Order Sigma-Delta Modulator [7].

The relation between the input and output in the discrete time is shown as:

$$Y(z) = X(z) + (1- z^{-1})^2 Q(z) \quad (1)$$

The error introduced from the quantizer is pushed to the high frequency terms due to the term $(1- z^{-1})$ [8]. The key equations can be given by [9]:

$$\frac{Y(z)}{Q(z)} = (1- z^{-1})^2 \quad (2)$$

Where $z = e^{j2\pi fT}$, then

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$$\frac{Y(}{Q(} = (1 - e^{-j2\pi fT})^2 \quad (3)$$

Hence the noise shaping function is written as:

$$(f) = S_q(f)|2\sin(\pi fT_{ck}) \quad (4)$$

Where:

T: is the clock frequency of Sigma-Delta modulator

fs = $\frac{}{T}$ (sampling frequency of Sigma-Delta modulator)

Where S_q (is relatively flat for the low frequencies.

Fig. 3 shows the spectrum of a second order Sigma-Delta noise shaping.

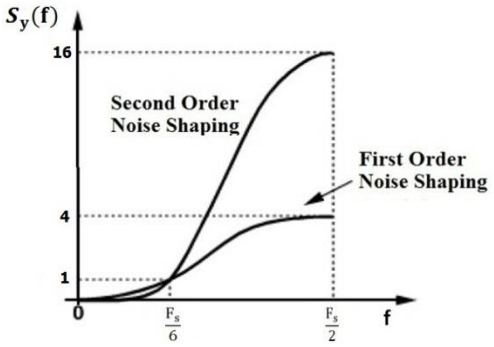

Fig 3. Noise shaping of the Second Order Modulator [9].

The sigma-delta modulator suffers from high quantization noise at high frequencies. To achieve high resolution, this quantization noise must be removed, and decimate or reduce the sample rate of the Sigma-Delta modulator output to the Nyquist rate which minimizes the amount of information for subsequent transmission, storage or digital signal processing [10]. The basic aim of the digital filter is to remove the quantization Noise at high frequencies due to using of sigma-delta modulator, reduce the sample rate of the Sigma-Delta modulator output to the Nyquist rate and increase the 1-bit or several-bit data word to high-resolution sample word. Practically it is impossible to implement a single filter that would meet the characteristic of decimation filter, because the order of such filters would be very high [11]. So it is necessary to divide the architecture of decimation filter into two parts: Cascaded integrator-comb (CIC) and FIR filters. The CIC filter is a combination of digital integrator and digital differentiator stages which execute the operation of digital low pass filtering and decimation. The CIC filter is a multiplier free filter that can accepts large rate changes. The CIC filter first performs the averaging process then follows it with the decimation. A simple block diagram of a first order CIC filter is shown in Fig.4 [12].

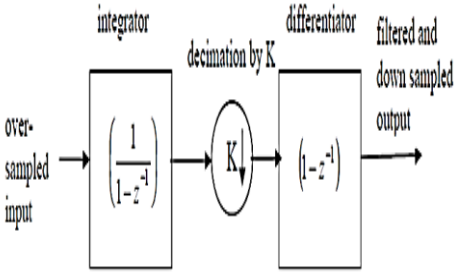

Fig 4. Block Diagram of CIC filter [12].

The integrator works at the sampling clock frequency, (fs) while the differentiator works at down sampled clock frequency of (fs/K). By operating the differentiator at lower frequencies, a saving in the power consumption is achieved. Eq.(5) gives the magnitude response of a CIC filter at frequency,(f) where (N) is the order of the filter[13].

$$H(z) = \left(\frac{1}{k}\frac{1-z^{-k}}{1-z^{-1}}\right) \quad (5)$$

Fig. 5 shows the frequency response of the CIC filter found using Eq. (7). The aliasing bands 2fc centered around multiples of the low sampling rate. As the number of stages in a CIC filter is increased, the frequency response has a smaller flat pass band. To overcome the magnitude droop, an FIR filter can be applied to achieve frequency response correction. Such filters are called “compensation filters" [13].

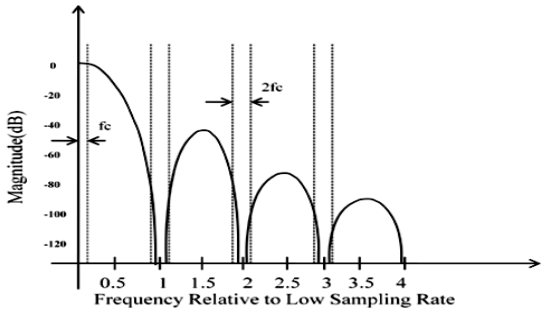

Fig 5. Frequency responses of a CIC filter [13].

III. DESIGN AND SIMULATION METHODS

The proposed Sigma-Delta ADC used in this paper is shown in Fig.6 which consists of a sigma delta modulator followed by a Decimation Filter which is designed in MATLAB Simulink.

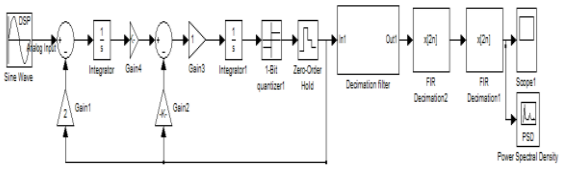

Fig 6. MATLAB model of the Sigma-Delta ADC.

The characteristics of the proposed Sigma-Delta ADC are shown in Table 1. A 15 bit Sigma-Delta ADC for a signal band of 40K Hz is designed in MATLAB Simulink and then the decimation filter has been designed using Xilinx system generator tool , which reduces the design cycle by directly

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generating efficient VHDL code .The VHDL code has been implemented on a Spartan 3E FPGA using ISE 14.1 tool.

Table 1. The characteristics of Sigma-Delta ADC

Parameters	*Symbol*	*Value*
Signal bandwidth:	BW	40 KHz
Sampling Frequency:	F_S	10.24 MHz
Over Sampling Ratio:	K	128
Modulator order:	M	2
Number of bits in modulator bit stream:	B_{Mod}	1
Number of bits in output of filter:	B	15

The Simulink Model of second order Sigma Delta Modulator is shown in Fig.7. It consists of two difference operator, two integrator, 1-bit quantizer, and a negative feedback.

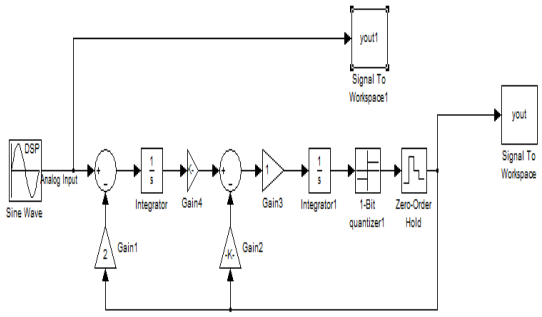

Fig 7. MATLAB model of Second Order Sigma-Delta Modulator

The modulator achieves a SNR of 69.0 dB for a signal bandwidth of 40 KHz. The modulator operates with an oversampling ratio (OSR) of 128 and a sampling frequency of 10.24MHz. In order to remove the high quantization noise at high frequencies, the sample rate of the output of the Sigma-Delta modulator must be reduced to the Nyquist rate and to achieve high resolution the decimation filter should have the characteristics shown in table 2.

Table 2.decimation filter characteristics

Filter parameters	*Value*
Sampling frequency:	F_s = 10.24 MHz
Down Sampling Ratio:	DSR = 128
Pass band frequency:	F_{pass} = 40 KHz
Stop band frequency:	F_{stop} = 41.6 KHz

The decimation filter accepts the single bit stream from the modulator and converts it into a 15 bit digital output. Practically it is not possible to implement a single filter that would meet the characteristics of Table 2. The order of such filter would be close to 5000. It is difficult to implement such a hardware filter. Therefore, it is needed to use a multi-stage approach, whereby the decimation is performed in several stages. The proposed decimation filter architecture is consist of three stages Second-order Cascaded Integrator Comb filter followed by two (FIR) filters, as shown in Fig.8.

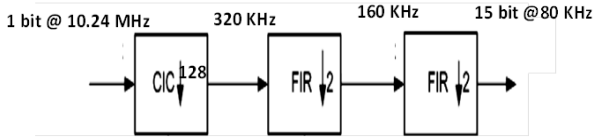

Fig 8. Decimation filters architecture

The multistage architecture allows most of the filter hardware to operate at a lower clock frequency, and have lower hardware complexity when compared to a single state decimator. The frequency response of a Third order Cascaded Integrator Comb filter is shown in Fig.9.

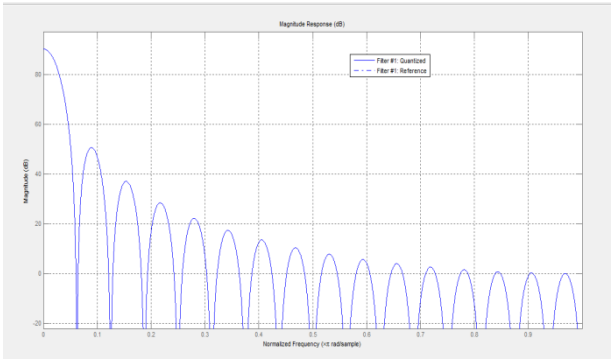

Fig 9. Frequency response of a Third order CIC filter.

The input to the Cascaded Integrator Comb (CIC) filter is a 1-bit pulse density modulated signal from a first order sigma-delta modulator. Internal word width (W) for this design of CIC filter need to ensure that there is no run time overflow given by Eq.6 [4]. W = (1Sign bit) + (Number of input bits) + (Number of stages, N) log2 (Decimator factor) (6)

In this paper, W = 1 + 1 + 2 log2 (128) i.e. W=16

The output from the Cascaded Integrator Comb (CIC) filter is a (1 sign bit +15 resolution bits) digital output. To overcome the magnitude droop in Cascaded Integrator Comb (CIC) filter, two FIR filters has been used to achieve frequency response correction. The order of the designed FIR filters is 18 and 150 respectively. Fig.10 shows the frequency response of the designed FIR filters.

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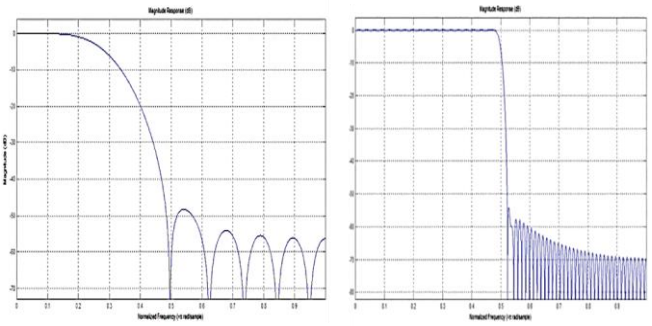

Fig10. Frequency response of first and second FIR filter.

For the first-order over sampled sigma-delta modulator and the second-order CIC filter used in the design, the desired output resolution is given by Eq. (7)[7].

$$N_{final} = N_{i/p} + \frac{50 \log k - 1}{6.02} \quad (7)$$

Where :

N_{final} is the final output resolution,

$N_{i/p}$ is the input resolution of the decimator.

So, for K=128, the output resolution achieved is 15 bits.

The proposed decimation filter has been designed using MATLAB Xilinx system generator tool, which reduces the design cycle by directly generating efficient VHDL code. Figure 11 shows the decimation filter designed in system generator . The VHDL code has been implemented on a Spartan FPGA using ISE 14.1 tool.

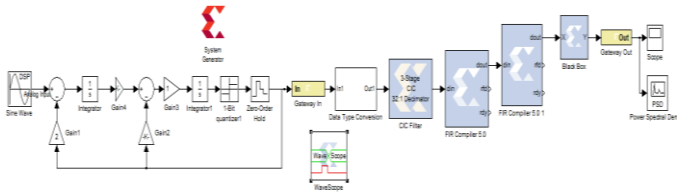

Fig 11. Decimation filter designed in system generator

IV. RESULTS AND DISCUSSION

The output of second order Sigma-Delta modulator with a sampling frequency of 10.24 M Hz for a sine wave input of 1 Vpp and 20 KHz is shown in Fig.12.

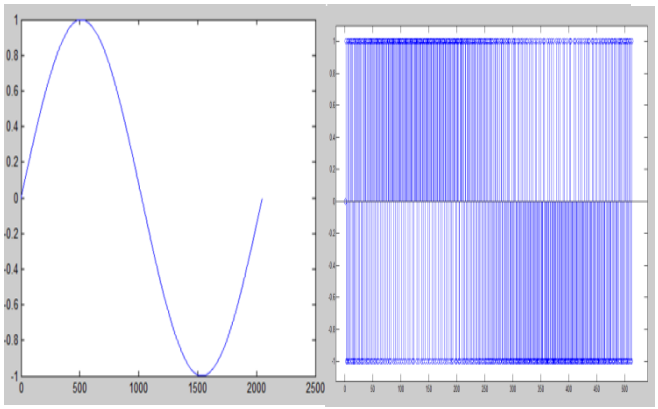

Fig 12. Transient response of second order Sigma-Delta modulator for a sine wave input of 20 KHz.

It is clearly evident that the output (single bit) is a pulse width modulated in accordance with input sine wave. The number of 1's increases at the positive peak of the input sine wave and the number of -1's are more at the negative peak. There are equal number of 1's and -1's when the input signal is at zero amplitude, which is the expected response of a Sigma Delta Modulator. Fig.13 shows the simulated power spectral density (PSD) of the proposed Delta Sigma modulator for a 20 KHz input sine wave.

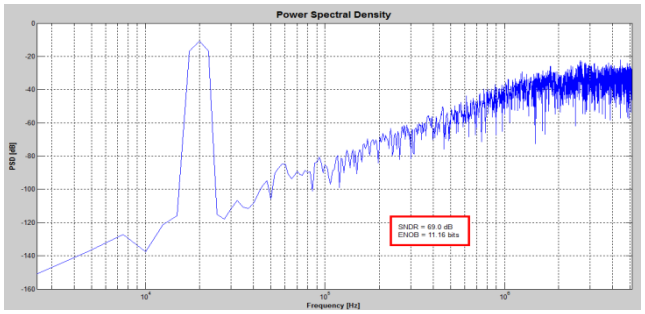

Fig13. Power Spectral Density (PSD) of output of Sigma-Delta modulator.

As shown in Fig.13 the quantization noise shifted towards high frequency band. The modulator signal to noise ratio (SNR) and ENOB were designed to be 69.0 dB and 11.16 bits for second-order output with an OSR of 128.

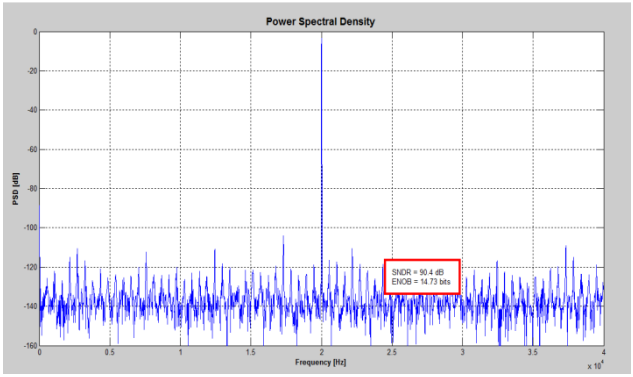

Fig14. Power Spectral Density (PSD) of Output of decimation filter

Fig.14 shows the output spectrum of the decimation filter, it is clear that the decimation filter is able to remove the out-of-band noise effectively and increases the SNR. The complete ADC is able to achieve a resolution of 14.73 bits and SNR of 90.4dB.

The output Power Spectral Density (PSD) of the decimation filter using Xilinx system generator tool was exactly the same as the result in MATLAB Simulink as shown in Fig.14. Fig.15 shows the digital output from decimation filter for 20 KHz analog signal.

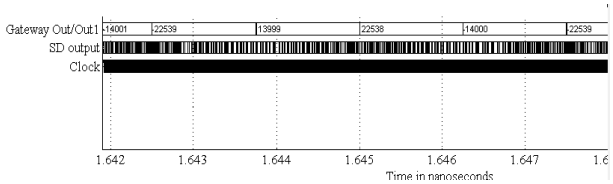

Fig15. Digital output for analog signal 20 KHz

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To implement the decimation filter in Spartan 3E the efficient VHDL code was directly generated from the design of the decimation filter in Xilinx system generator. Using Xilinx ISE to simulate the VHDL code which generated from system generator, the result of digital output from decimation filter for 20 KHz analog signal in Xilinx ISE simulation is shown in Fig.16.

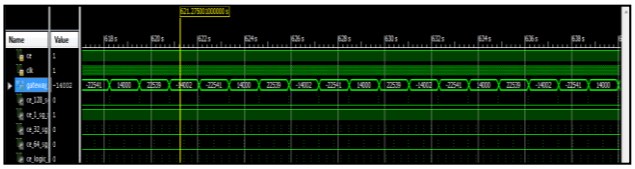

Fig16. Digital output for analog signal 20 KHz in Xilinx ISE.

The result of Xilinx ISE simulation exactly the same as the result from MATLAB Simulink. Table 2 show a summary of the resources utilized in the implementation of the decimation filter in Spartan 3E.

Type Resources (or Frequency)	Utilized Resources	Total Resources	Ratio
Number of Slices Flip flops	800	9312	8%
Number of 4 input LUTs	591	9312	6%
Number of occupied Slices	499	4656	10%
Number of Bounded IOBs	19	232	8%
Number of Block RAMS	3	20	15 %
Number of MULT 18*18 SIOs	3	20	15%
Maximum Operating Frequency		144.655 MHz	

Table 2. Resource Utilization for Spartan 3E

The decimation filter performance has been ascertained using the hardware co-simulation that uses Chipscope Pro Analyzer in ISE. The digital output results from implementing the decimation filter in Spartan 3E by using the chip scope for 20 KHz analog signalis shown in figure 17.

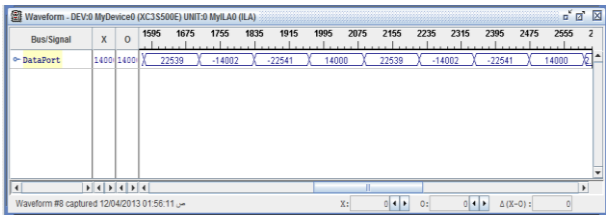

Fig 17. Result of implementation the decimation filter in Spartan 3E

By comparing digital signal obtained using chip scope with the digital signal obtained using MATLAB Simulink, it can be seen that the two digital signals are very similar and this mean that generation and implementation of the VHDL code in Spartan 3E is performed without any error. Because of similarity in time domain between two digital signals of simulation and implementation that shown in Fig(15),(17), it can be assumed that the output spectrum of implementing the decimation filter is the same as the simulated output spectrum.

V. CONCLUSION

A complete sigma delta ADC is designed using a second order Sigma-Delta modulator and a Digital decimation filter with an OSR of 128. The multistage architecture reduces the need for multiplication which is need very large area to implement in hardware and allows most of the filter hardware to operate at a lower clock frequency which have lower hardware complexity when compared to a single state decimation filter. Digital decimation filter for Sigma Delta ADC is successfully implemented into Xilinx Spartan series FPGA. This ADC gives overall 15 bits resolution and SNR of 90.4dB.

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