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A sigma–delta fluxgate magnetometer for space applications

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Abstract

This paper describes the concept and development of an innovative combination of conventional fluxgate magnetometer readout electronics with the control loop of a sigma–delta modulator in order to achieve a new magnetometer design that provides direct digital output without the use of a separate analogue-to-digital converter chip. The new concept is especially aimed at the measurement of extraterrestrial magnetic fields within a dynamic range of approximately ±2000 nT aboard scientific space missions which are affected by high radiation doses.

A digital domain model of the new magnetometer electronics is presented, which is essential for a successful hardware implementation, and the test results of a single-axis prototype are discussed.

The test results show that the fluxgate and sigma–delta modulator control loops can be merged for dynamic ranges up to ±2000 nT without significant deterioration of the overall performance of the magnetometer. The remaining quantization noise in the signal bandwidth (10 Hz) was minimized to below the sensor's noise level (7 pT $Hz^{-1/2}$ at 1 Hz) due to the noise-shaping effect of the sigma–delta principle. An offset stability of 0.25 nT over four days was achieved and the linearity error is less than $\pm 3.3 \times 10^{-5}$ even though the fluxgate sensor is not kept at near-zero field as for traditional fluxgate magnetometers.

A technological model of this new fluxgate magnetometer concept will be built for a test flight aboard the NASA discovery mission DAWN.

Keywords: digital magnetometer, fluxgate, sigma–delta modulation, high resolution data conversion

1. Introduction

A state-of-the-art space-borne fluxgate magnetometer (triaxial sensor plus sensor electronics including analogue-to-digital conversion) is characterized by a magnetic field resolution of about 10 pT as well as low power consumption (500–700 mW), low weight (250 g including a triaxial sensor) and a suitable temperature stability of offset, scale factor and sensor misalignment. These specifications are already very good but probably not sufficient enough for highly integrated multi-constellation missions (50 or more nanosatellites) planned for the near future (Spence *et al* 2001). Furthermore, a radiation-hard electronics, which is tolerant to 100 krad of total ionizing dose (TID) without additional

spot shielding, is of interest for space missions either orbiting in the midst of the planets' radiation belts (especially for the Earth and Jupiter) or flying towards the Sun (e.g. a mission to Mercury).

Both, the traditional analogue as well as the more recently developed digital readout electronics for fluxgate magnetometers use high-resolution analogue-to-digital converter (ADC) and digital-to-analogue converter (DAC) chips for signal quantization. The disadvantages of such converter components are the power consumption, mass and price of successive approximation-based converters on the one hand and the availability of radiation-hard chips of sigma–delta modulation-based converters on the other hand. The recently tested sigma–delta ADC AD7714, for example, became non-functional between 10 and 20 krad (O'Bryan *et al* 2002) and the sigma–delta ADC CS5508 tested for the Rosetta mission was found to be tolerant for 27 krad (Omerbegović 1999).

Compared to the availability of suitable converter chips it is not trivial but easier to acquire proper operational amplifiers (e.g. OP 471, LM108), analogue switches (e.g. HS1-302, HS1-303) and voltage references (e.g. RH1021, REF05) which are tolerant to 100 krad of TID.

Driven by these considerations, we examined the possibility of combining the control loops of a conventional fluxgate magnetometer with the control loop of a sigma–delta modulator in order to get a magnetometer with direct digital output which does not contain a separate ADC chip. In order to achieve a field resolution in the 10 pT range, which is required for the scientific objectives, a ring-core-based sensor is still used for this new sigma–delta fluxgate (SDF) magnetometer.

A similar technique has also been worked out for micro-fluxgate sensors (Kawahito *et al* 1999, 2002). The micro-fluxgate magnetometer is based on the same working principle as the traditional fluxgate magnetometer, but sensor and readout electronics are fully implemented in silicon microtechnology. This implementation is optimized for small and low-cost applications such as digital magnetic compasses. Due to the current system parameters—the linearity error is of the order of $\pm 4 \times 10^{-3}$ and the noise density at 1 Hz is about 150 nT $\mathrm{Hz}^{-1/2}$—it is not appropriate for typical space and ground-based scientific applications.

In this paper the feasibility of a second-order SDF magnetometer for space is examined. Sections 2 and 3 give a brief overview of the fluxgate principle and the sigma–delta modulation theory. In section 4 the new magnetometer readout concept is analytically described and the design criteria are applied to a single-axis prototype. Furthermore, first test results are given and discussed in this section. The paper finishes with an outlook on future development steps.

2. Analogue and digital readout electronics

Commonly, a single-axis fluxgate sensor for space applications is made of a soft magnetic ring-core placed in the centre of a solenoid pick-up coil. The ring-core is toroidally wrapped with an homogeneous single layer of drive windings (also an excitation coil). With the excitation coil the soft magnetic material is periodically saturated at a fundamental frequency of several kilohertz (F_0) by feeding an ac current through the drive windings. The output signal of the pick-up coil (voltage and current detection are in use) contains odd and even harmonics of the fundamental drive frequency. The even harmonics are proportional to the external magnetic field along the magnetic axis of the sensor. The odd harmonics constitute the feed-through signal coupled from the drive coil and the soft magnetic core to the pick-up coil. The readout electronics has to perform the extraction of the magnetic field information by synchronously converting the even harmonics (or just the second harmonic) into a dc or slowly changing ac output voltage according to the bandwidth of the magnetometer. A very comprehensive overview of the fluxgate magnetometer in particular and different magnetometer types in general is given in Ripka (2000).

Until now the field extraction has successfully been done using analogue circuits (Acuña 1974, Primdahl 1988, and many others). The second-harmonic method for example (see upper block diagram of figure 1) uses a band-pass filter after the pre-amplifier to suppress the feed-through signal. The filter stage is followed by a symmetric synchronous demodulator. With the demodulator and integrator (the integrator can be replaced by a low-pass filter whereas the integrator causes a nearly infinite dc gain in the control loop) the field-proportional second harmonic is rectified and converted to a dc and low-frequency output voltage respectively. It is digitized by an ADC and fed back via a resistor into the pick-up or a separate feedback coil in order to compensate the measured external field within the sensor which increases the linearity of the magnetometer.

More recently, so-called digital magnetometers (see lower block diagram of figure 1) have been developed (Primdahl *et al* 1994, Auster *et al* 1995, Pedersen *et al* 1999, Magnes and Auster 2001). This sensor electronics concept reduces the number of analogue parts by digitizing the output signal of the pick-up coil directly after the input amplifier at four times the drive frequency ($4F_0$) and higher. The former analogue signal processing is replaced by mathematical algorithms implemented in either a field-programmable gate array (FPGA) or in a digital signal processor. The feedback signal is generated by a DAC controlled and updated by the digital processing unit. The reduced number of analogue parts increases the robustness against environmental influences (temperature change and electromagnetic disturbances) and the flexibility of the instrument operation (dynamic range and output data rate).

However, as already mentioned in the introduction, both sensor electronics types are based on conventional ADC and DAC chips for getting digital output which limits the miniaturization and radiation hardness capability.

3. Sigma–delta modulation technique

When comparing the resolution versus bandwidth characteristics of various ADC principles the sigma–delta technique is the one with the highest resolution and the smallest bandwidth. Flash converters show high output data rates with comparably low resolution, and the successive approximation converters lie somewhere in between.

The sigma–delta modulation technique, which is also a very cost effective and robust (except for radiation hardness) type of analogue-to-digital conversion, features the exchange

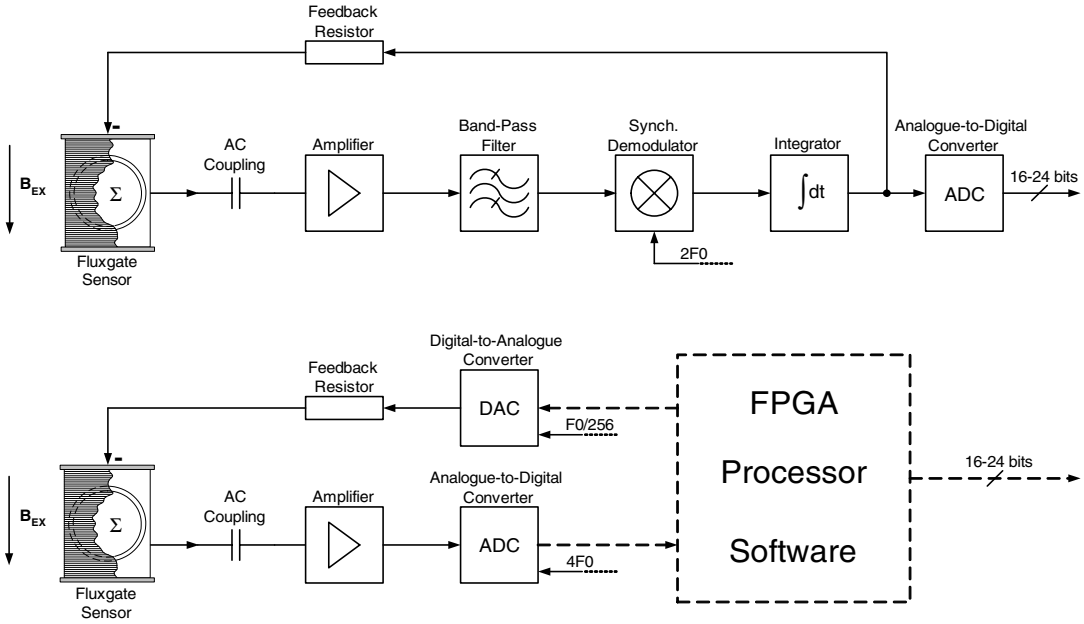

Figure 1. Block diagram of the analogue (upper) and digital (lower) fluxgate readout electronics.

of resolution in time for that in amplitude. It digitizes the signal with low resolution (between one and four bits) but with a very high sampling rate (F_s). A digital decimation filter reduces the sampling rate and increases the resolution of the coarsely digitized input signal according to the chosen oversampling rate.

The simplest sigma–delta (Σ–Δ) modulator is a first-order loop with single-bit quantization (Candy 1985). It consists of an integrator and a comparator (two-level or single-bit quantizer respectively) in the forward path and a single-bit DAC in the negative feedback (see figure 2). The feedback forces the average value of the quantized signal to track the average value of the input signal. Any difference between them accumulates in the integrator and eventually corrects itself.

Grossly oversampling the input signal causes the quantization noise, which is large due to the single-bit quantization, to spread over a wide bandwidth and the noise in the bandwidth of interest (signal band) is significantly decreased. Furthermore, the sigma–delta loop pushes the quantization noise into higher-frequency regions (noise-shaping effect) and leaves the input signal unchanged. Since the signal is sampled at a frequency much greater than the chosen final output Nyquist rate, the high-frequency quantization noise can be removed without affecting the signal band by means of a digital decimation (low-pass) filter operating at the output of the sigma–delta modulator.

However, the quantization noise from first-order modulators is highly correlated (Candy and Benjamin 1981). The 1 bit output stream of the modulator includes repetitive patterns which causes frequency spectral peaks of noise in the filtered output signal when the dc input value is adjacent to integer divisions of the quantization level (Candy and Temes 1992). Due to this drawback of first-order modulators, which is called pattern noise or in-band tone, the oversampling ratio necessary to achieve resolution greater than 12 bits is large. The in-band tone can be minimized by using higher-order sigma–delta modulators (the order is equal to the number of integrators and feedback loops in the modulator circuit), a multibit quantizer or a combination of both. This not only reduces the quantization noise in the signal band and thus increases the dynamic range but also decorrelates the quantization noise spectrum from the input signal more efficiently.

Taking into account potential instabilities, gain-matching constraints of different modulator building blocks, the need for accurate circuit parameters, signal band resolution, quantization noise as well as the robustness of various Σ–Δ modulators, the second-order sigma–delta modulator with single-bit quantization is particularly attractive for high-resolution analogue-to-digital conversion (Boser and Wooley 1988).

When the quantization noise is ideally modelled by an additive white-noise source (no correlation between quantization error and input signal), the signal-to-noise ratio (SNR) of a second-order sigma–delta modulator can be written in the form

$$\mathrm{SNR2} = \frac{\sqrt{60}}{\pi^2} M^{5/2} \tag{1}$$

where M is the oversampling ratio (F_s/f_s). Compared with first-order modulators the resolution grows faster with M and for $M = 128$ a practical output resolution of 16 bits (theoretically 17.15 bits) can already be achieved (Candy and Temes 1992).

Figure 3 shows the digital domain block diagram of a second-order sigma–delta modulator. The z-transformed digital output signal can be written in the form

$$Y(z) = Hx(z)X(z) + Hq(z)Q(z). \tag{2}$$

With the z-transformed integrator

$$I(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{3}$$

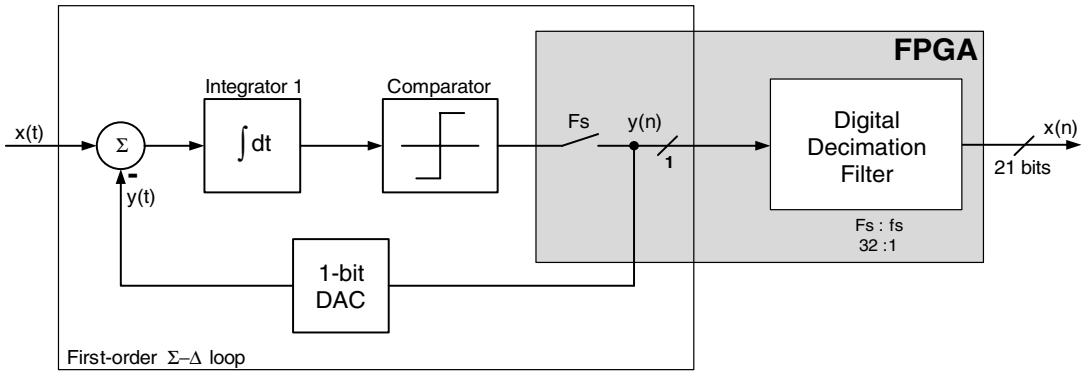

Figure 2. Block diagram of a first-order sigma–delta converter.

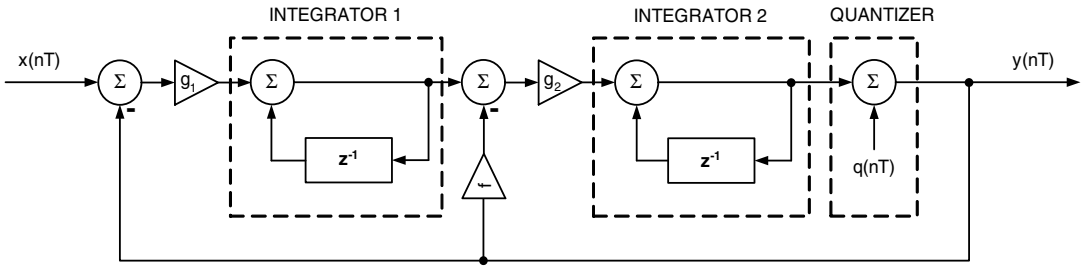

Figure 3. Digital domain block diagram of a second-order sigma–delta modulator.

the transfer function for the input signal becomes

$$Hx(z) = \frac{g_1 g_2 z^{-2}}{1 + (fg_2 - 2)z^{-1} + (1 - fg_2 + g_1 g_2)z^{-2}} \quad (4)$$

and the transfer function for the modelled quantization noise is

$$Hq(z) = \frac{(1 - z^{-1})^2}{1 + (fg_2 - 2)z^{-1} + (1 - fg_2 + g_1 g_2)z^{-2}}. \quad (5)$$

For two different sets of amplification parameters ($g_1 = g_2 = 1$, $f = 2$ and $g_1 = 0.5$, $g_2 = 2$, $f = 1$) equations (4) and (5) become

$$Hx(z) = z^{-2} \quad (6)$$

and

$$Hq(z) = (1 - z^{-1})^2. \quad (7)$$

Apart from a delay of two sampling periods ($1/F_s$) the input signal is kept completely unchanged and the quantization noise is ideally noise shaped with second-order characteristics according to the noise-shaping model explained in Candy and Temes (1992). For the SDF magnetometer the second set of parameters simplifies the implementation of the modulator with straightforward analogue circuits. The attenuation of 0.5 preceding the first integrator reduces the signal ranges at the output of this integrator and since the second integrator is followed immediately by a single-threshold quantizer, its gain can be adjusted arbitrarily without impairing the performance of the modulator (Boser and Wooley 1988).

4. The second-order SDF magnetometer

4.1. Practical implementation and parameter settings

Based on the considerations presented in the previous section, the second-order principle with single-bit quantization was found to be the most attractive circuit in terms of robustness, stability, resolution and simplicity for the realization of an SDF magnetometer. Figure 4 shows how this merging process took place and the final block diagram of the second-order SDF magnetometer is depicted in figure 5. All functional blocks from figure 4 are included except the band-pass filter and the ADC. In comparison to the block diagram of the second-order sigma–delta modulator, where the first summation node in reality is formed by an analogue amplifier circuit, the fluxgate sensor itself is the first summation node (magnetic field summation). The difference of the external magnetic field along the measurement axis and the current feedback field causes an induction of field proportional even-harmonics in the pick-up coil as already explained in section 2. The modulated magnetic field is intensified by a pre-amplifier and rectified by the following synchronous demodulator. The first integrator acts as a conjunction point between the fluxgate and sigma–delta control loops. This is essential for proper fluxgate operation and builds the first integration stage of the second-order sigma–delta converter. The second summation node and the second integrator are realized with only one analogue amplifier circuit and its output is connected to a zero-referenced comparator. In order to get a time-discrete single-bit data stream, the comparator output is sampled at the positive edge of the $F_0/2$ signal (4630 Hz, which is half of the fundamental drive frequency) in the FPGA. This modulator output signal is connected to the decimation filter as well as directly to the feedback circuit. The feedback circuit contains

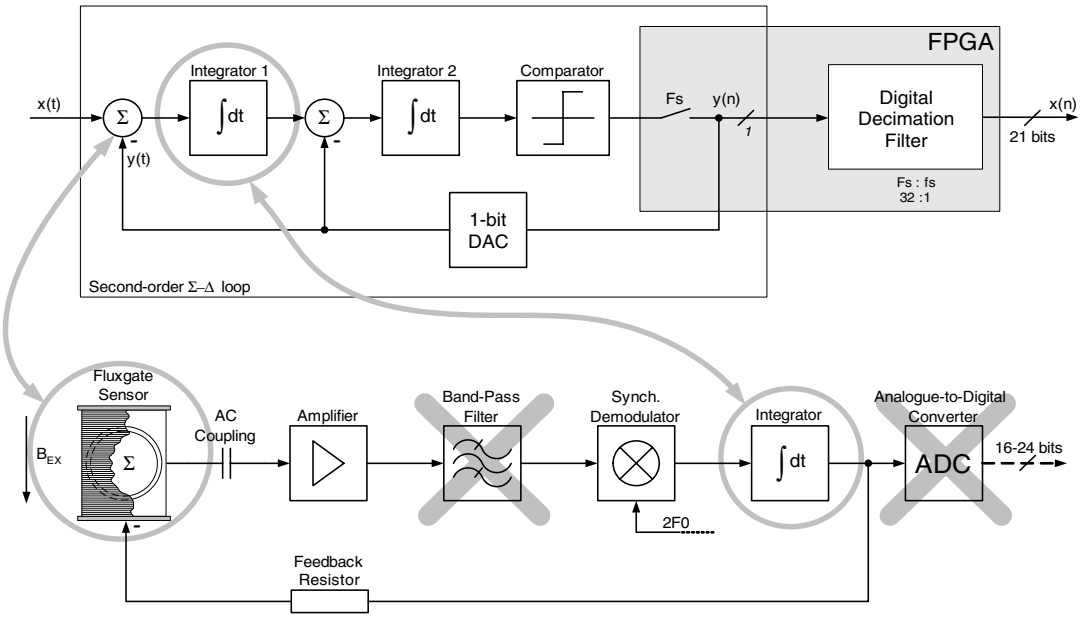

Figure 4. Merging of second-order sigma–delta and fluxgate control loops.

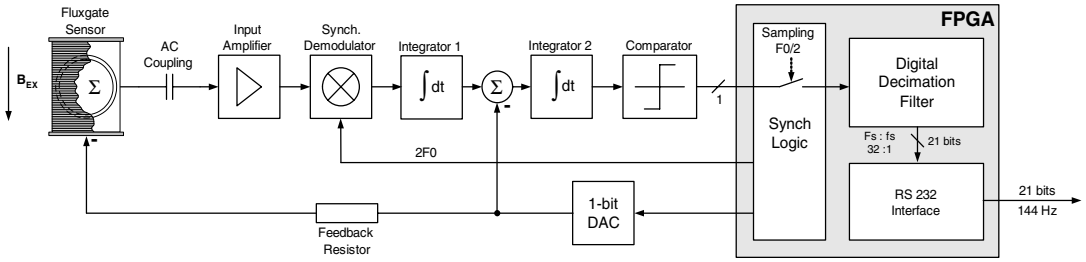

Figure 5. Block diagram of the second-order SDF magnetometer.

a 1 bit DAC realized with a highly stable voltage reference (5 V, LT1021) and a CMOS-based analogue switch. The stability and low noise parameter of the voltage reference are very important because the voltage reference directly influences the quality of the entire analogue-to-digital conversion. The output of the DAC is connected to the second summation node (integrator 2 circuit) and via a feedback resistor to the field summation node in the fluxgate sensor. The chosen feedback resistor sets the current through the feedback coil and therefore the single-bit (digital) feedback field to ± 2635 nT, which is theoretically also the maximum measurement range. In reality, the measurement range of the presented SDF magnetometer is limited to about ± 2000 nT. Firstly, it is caused by a typical performance breakdown of sigma–delta modulation for near full-amplitude input signals due to an increasing periodicity in the single-bit modulator output signal (many ones and only a few zeros for positive and vice versa for negative near full-amplitude signals) and secondly, by an increased non-linearity of the fluxgate sensor towards higher input fields due to the digital feedback which differs from the classic feedback in fluxgate magnetometers. The sigma–delta caused limitation of the measurement range, which is also a kind of pattern noise, is outlined in more detail in appendix A of Ledzius and Irwin (1993).

Figure 6 presents a representative snapshot of the F_0 square wave (Ch 01, 9260 Hz), which is the control signal

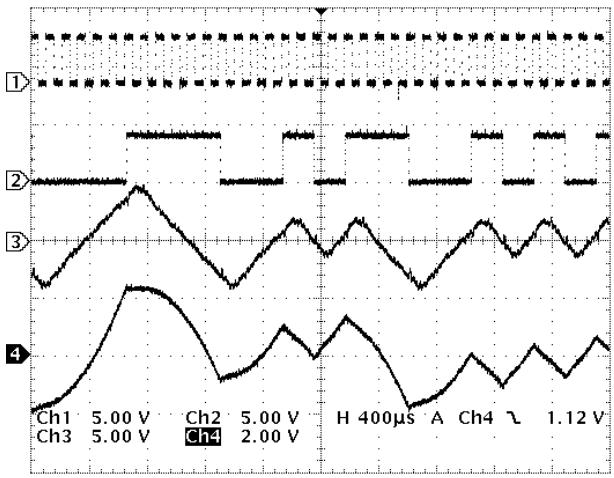

Figure 6. Oscillogram of the comparator (Ch 2) and integrator (Ch 3, Ch 4) output signals.

for the excitation of the soft-magnetic ringcore in the fluxgate sensor, the output of the two integrators (Ch 3 and 4) and the latched output signal of the comparator (Ch 2). The output of integrator 1 is linear within the sampling period due to the constant input from the sensor whereas the output of integrator 2 shows a mostly quadratic shape caused by

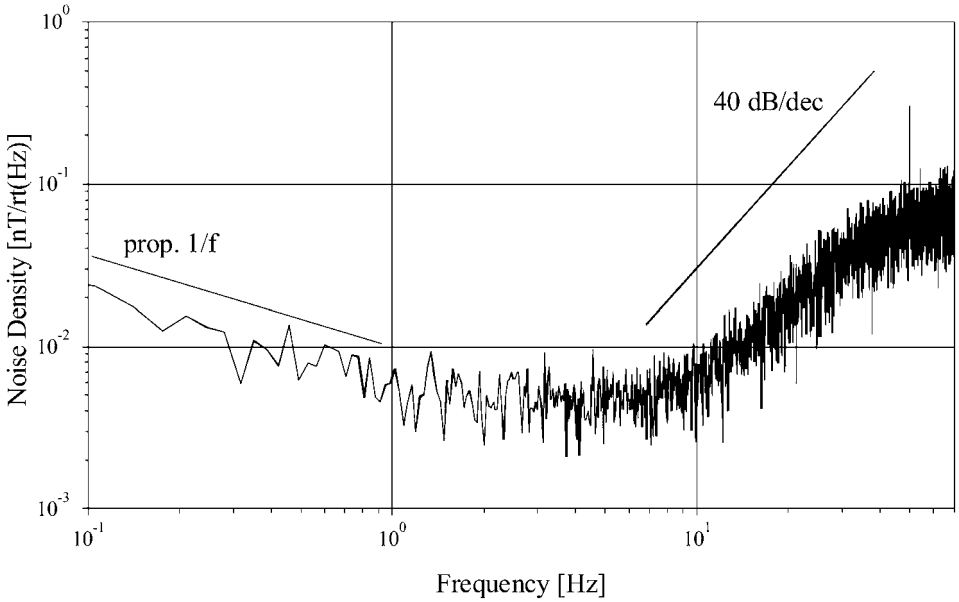

Figure 7. Noise density plot of the 144 Hz output data of the decimation filter.

the integration of the sum of the integrator 1 output and the feedback signal.

The integrator circuits are realized using standard operational amplifiers with resistors (R) at the input and capacitors (C) in the feedback. If the $R \cdot C$ product of one of the integrator circuits was equal to the reciprocal of the sampling frequency

$$R \cdot C = \frac{1}{F_S} = \frac{2}{F_0} \cong 216\ \mu s \tag{8}$$

the analogue integrator would exactly match the digital integrator in figure 3 (the dc gain of the amplifiers is thought to be sufficiently great). By tuning the resistors and capacitors of both integrator circuits one can perfectly match the gain factors g_1 and g_2 as well as the feedback factor f. In the SDF circuit, g_1 is the product of the sensor's sensitivity, the gain of the pre-amplifier, the rectification factor of the synchronous demodulator and the ratio between the $R \cdot C$ product of the first integrator and the value in equation (8). For all test measurements presented in the following section, $g_1 \cong 0.5$ (see Ch 2 in figure 6) and the ratio $g_1/f \cong 0.5$ (set with the input resistors of integrator 2) in order to meet the considerations of equations (6) and (7). During the tests it turned out that a deviation of 10% and more is not critical as far as the stability of the instrument is concerned. In which way the noise shaping and the input signal are influenced by deviations from the ideal set of parameters will certainly be part of future investigations.

Besides the latching of the comparator, the FPGA in figure 5 also includes a single-stage decimation filter as well as the control and the communication logic. For the prototype SDF magnetometer the decimation filter stage (decimation factor of 32) was realized by four cascaded comb-filters of length 32.

The closed form of a single comb-filter transfer function (also of length 32) can be separated into an integration and a differentiation part

$$H_C(z) = I(z)D(z) = \frac{1}{1 - z^{-1}}(1 - z^{-32}). \tag{9}$$

Since the comb-filter will be followed by a 32:1 decimation, the differentiation can already be calculated at the decimated data rate. Cascaded comb-filters can be made up in the same way, which results in a hardware-optimized realization in the FPGA. This filter design, which was introduced by Hogenauer (1981), is called a cascade integrator comb (CIC) filter and Hogenauer filter, respectively.

In this application, the CIC decimation filter consists of four successive integrators, a decimation stage (32:1) and four successive differentiators. It produces a final output data rate of 144 Hz with a word length of 21 bits, which is mandatory due to the optimized CIC design in the FPGA. The comb filter is used because its performance is good enough for a proper attenuation of the quantization noise and furthermore it can be implemented to an FPGA in a very efficient way. A second mostly recursive filter stage is normally used in order to remove out-of-band components of the input signal (Candy and Temes 1992). However, the second stage has not been realized in the FPGA for this test application. The 144 Hz and 21 bit broad (but not accurate) output data are transmitted to a data acquisition PC via an RS 232 interface which enables an accurate investigation as well as a proper and flexible filtering of the high-resolution output data.

4.2. Test results

The offset of the SDF magnetometer is less than 1 nT, which is a typical value for fluxgate magnetometers and is mainly caused by non-homogeneities in the soft-magnetic ringcore. The proposed measurement principle, therefore, does not increase the offset value.

The spectral density of the 144 Hz output data is depicted in figure 7. For this test measurement the sensor was placed

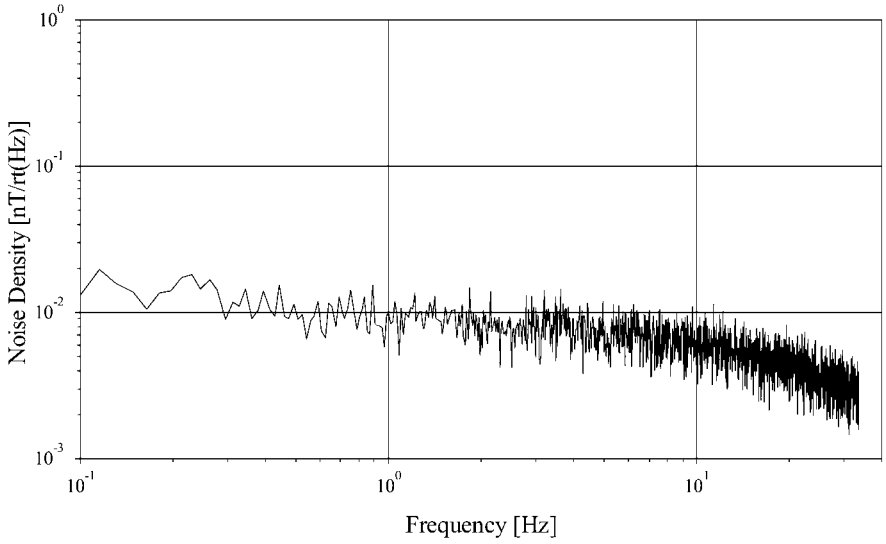

Figure 8. Noise density plot of the DSP FGM sensor.

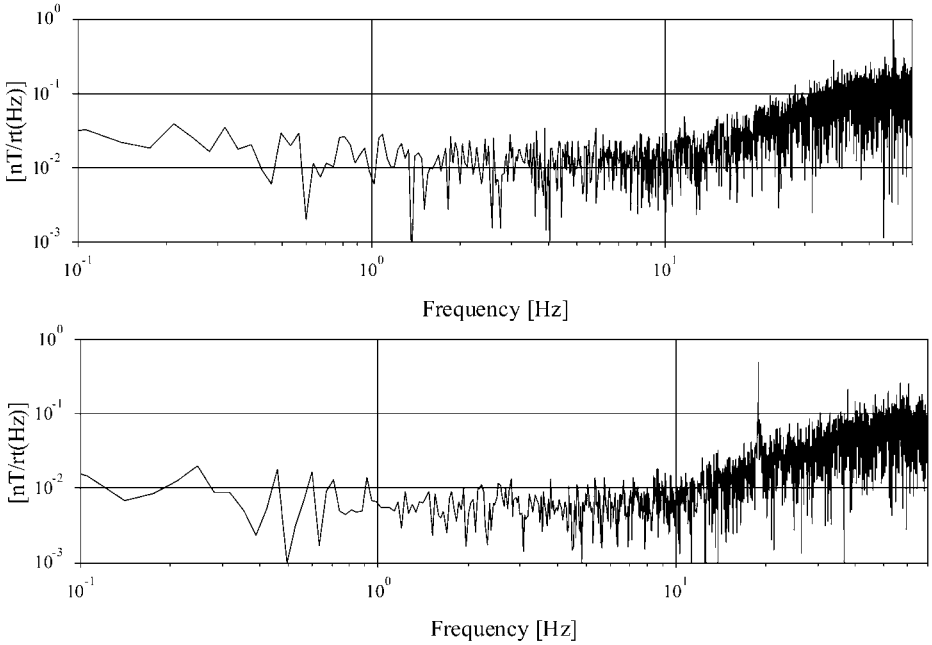

Figure 9. Spectral density with pattern noise: upper plot with dither and lower plot without dither.

in a three-layer magnetic shield can made from Mu-metal (Magnes *et al* 1998). The plotted spectrum is the average of six spectra without data overlapping. The expected noise-shaping effect with second-order behaviour (40 dB/decade) is clearly visible. Due to the decimation filter stage, the 40 dB/decade increase is attenuated at higher frequencies and becomes nearly flat at about 70 Hz. The artificial noise of the single-bit quantization is pushed to higher frequencies as explained by theory, and in the bandwidth of interest, which is below 10 Hz in this application (with an intended final output data rate of 20 Hz and an oversampling factor M of approximately 256), only the sensor noise itself is dominant. A 24 mm ringcore with a soft magnetic material made from moly-permalloy (Rustenbach *et al* 1998) was used. It features excellent low-noise behaviour. The noise density of the output data is well below 10 pT $Hz^{-1/2}$ above 0.5 Hz and the derived band noise between 0.1 and 10 Hz is about 21 pT rms which is theoretically equivalent to the quantization noise of a 15.8 bit ADC for a measurement range of ± 2000 nT (17.6 bits in the band 0.1–1 Hz). The increase of the noise proportional to the reciprocal of the frequency at lower frequencies is typical for all fluxgate sensors and thus there is no degradation of the noise behaviour below 10 Hz due to the new measurement principle. For comparison, the noise density plot of a 12 mm ringcore, currently assembled for a Chinese–European space mission called double star (DSP), with traditional analogue readout electronics similar to the upper block diagram of figure 1, is presented in figure 8. The higher noise is caused by the smaller ring-core which was chosen for DSP because of its better offset stability.

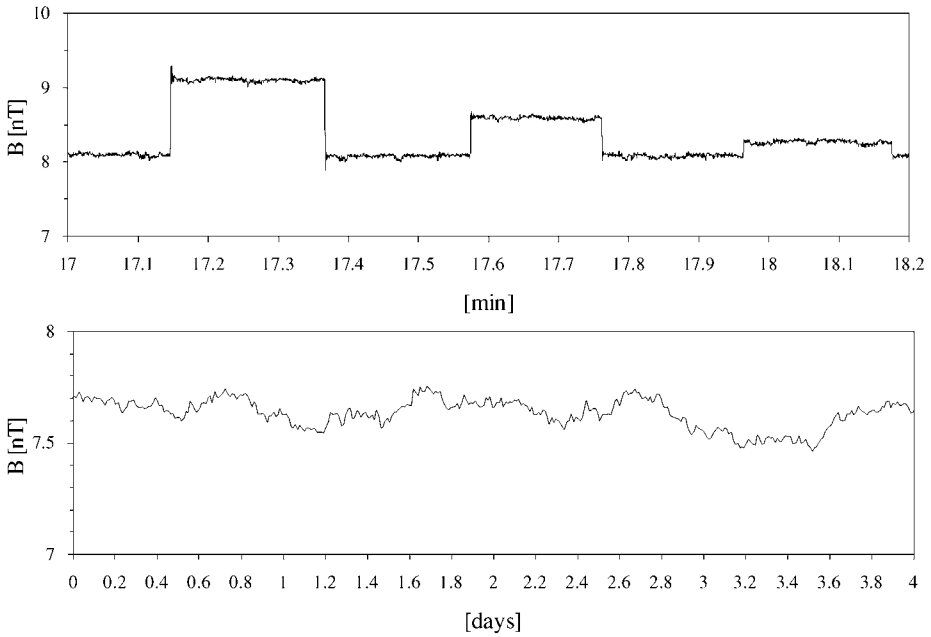

Figure 10. Resolution and stability performance.

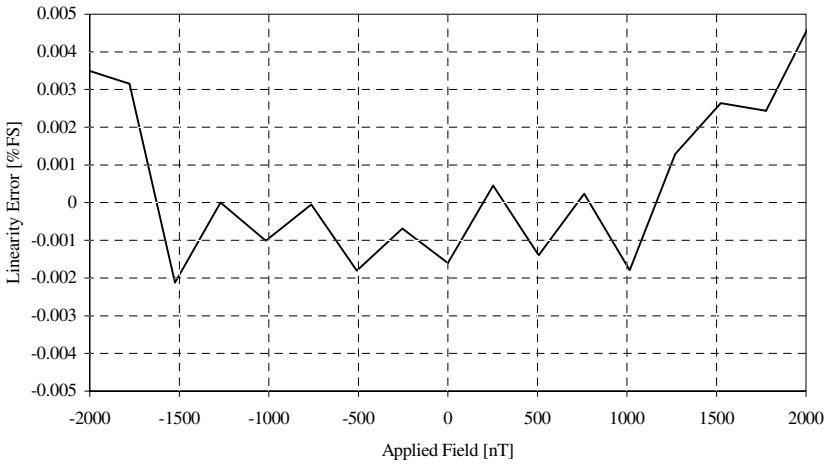

Figure 11. Linearity error.

In section 3 it was noted that the second-order sigma–delta configuration is still affected by pattern noise (in-band tone) in the output spectra even though the influence is much smaller than in first-order modulators. The tone travels from dc to half the sampling frequency for a dc input from zero to $\pm 1/2$ of the measurement range (Ledzius and Irwin 1993). In the proposed application it is not visible for dc input fields above ± 41.2 nT due to the decimation filter stage (as in figure 7). In the lower spectral density plot of figure 9 a spectral line at 18.9 Hz was observed caused by a dc input of approximately 10.8 nT. When considering a signal bandwidth of 10 Hz the tone interferes with dc inputs within ± 5.7 nT. The problem can be overcome by adding a dither noise signal to the circuit which sufficiently decorrelates the input signal from the pattern noise. In the upper spectral plot of figure 9 a pseudo random noise signal (generated in the FPGA) was coupled to the input of integrator 2 with the effect that the tone vanishes and the overall signal-to-noise ratio slightly decreases. This results in a loss of about 1.3 bits of resolution in the 0.1–10 Hz bandwidth compared to the noise plot in figure 7.

The field resolution capability of the SDF magnetometer is once more demonstrated in the upper measurement of figure 10. Three different field pulses (1, 0.5 and 0.15 nT) were applied to the sensor in the magnetic shielding can. The 144 Hz output data were averaged offline by a low-pass filter with a corner frequency of 10 Hz. The used filter (tenth-order Butterworth) caused the overshoot noticeable in figure 10.

The stability of the SDF magnetometer over four days is depicted in the lower plot of figure 10. Again the measurement was done with the sensor placed in the magnetic shielding. The high-resolution output data were averaged to 15 min means. During the four days the SDF output stays within a maximum drift of ± 0.125 nT. The measured dc value of about 7.7 nT is the residual field within the shielding can.

Finally, the linearity error of $\pm 3.3 \times 10^{-5}$ is presented in figure 11. It was measured within a field range of ± 2000 nT

(2000 nT is also the referred full scale value). Taking into account that the sensor sees a rapidly (with F_s) changing field due to the single-bit (digital) feedback of ±2635 nT instead of an almost zero field like in the traditional feedback configuration of fluxgate sensors, the achieved linearity is better than expected. For comparison, in classic fluxgate magnetometers the linearity is in the order of 10 ppm (Acuña *et al* 1978) and better.

5. Future developments and conclusion

A new readout electronics concept for a space-borne fluxgate magnetometer with a dynamic range of ±2000 nT has been described. The idea for the SDF magnetometer arose from considering a new technique for future space missions which would enable a realistic chance for further miniaturization and higher reliability in terms of radiation hardness. With the prototype version presented in this paper it was intended to prove the functionality of the concept rather than the exact factor of miniaturization and the final degree of radiation hardness.

The test results have successfully shown that the new concept works without degradation of the important instrument parameters of offset, noise (apart from the noise-shaped quantization noise) and stability. The decreased linearity due to the digital feedback in the magnetic field domain must be calibrated and needs further investigation, especially when considering the new concept for dynamic ranges which are larger than the presented ±2000 nT range.

The usable bandwidth is limited by the shaped quantization noise. In order to increase it from the currently 10 Hz to at least 20 Hz or even more, the sampling frequency can be doubled from $F_0/2$ to F_0 and the fundamental excitation frequency (F_0) can be set to a value well above 20 kHz in future applications especially when using sensors with smaller ringcores. A trade-off between increased noise at lower frequencies caused by the smaller sensor and a greater signal bandwidth due to a shift of the quantization noise to higher frequencies will be unavoidable.

As far as pattern noise is concerned, further investigations will be necessary for an optimized use of dither noise, in order to avoid in-band tone for low and stable dc input values, as well as for the limited measurement range due to the breakdown of the sigma–delta principles for full-range input signals.

Since the described instrument characteristics were obtained with a rather simple prototype version (flying wires, poor grounding concept, non-optimized layout, low-quality passive components etc) we conclude that the second-order SDF modulation, apart from the 1 bit digital-to-analogue conversion in the feedback, is not very critical in the selection of passive and active components.

As a next step, a technological model of this new fluxgate magnetometer concept will be jointly developed by the Institut für Weltraumforschung, Graz, and the Institute of Geophysics and Planetary Physics, UCLA, for a test flight aboard the NASA discovery mission DAWN in order to qualify the concept for scientific space applications. A standard radiation-hard FPGA, one quadruple operational amplifier (pre-amplifier, integrator 1 and 2, comparator) as well as a dual single-pole/double-throw (SPDT) analogue switch per axis, a precise voltage reference for the 1 bit DAC and several non-critical passive components will be used for this triaxial space-borne magnetometer. The design goals in terms of the main instrument characteristics are 30–40 pT rms (0.1–10 Hz) band noise, 250–300 mW power consumption, 100–150 g mass and a radiation hardness of 100 krad of the complete electronics without additional spot shielding.

Since sigma–delta modulators have been fully integrated on silicon chips for various applications for years and radiation tolerant mixed-signal application specific integrated circuits (ASICs) have already been developed for other space-borne instruments, the new concept gives a realistic hope that the readout electronics for a space-borne triaxial fluxgate magnetometer can be implemented in a single silicon chip in the future as well.

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