Design and FPGA Implementation of a 2nd Order Adaptive Delta Sigma Modulator with One Bit Quantization

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DESIGN AND FPGA IMPLEMENTATION OF A 2ND ORDER ADAPTIVE DELTA SIGMA MODULATOR WITH ONE BIT QUANTIZATION

Authors:

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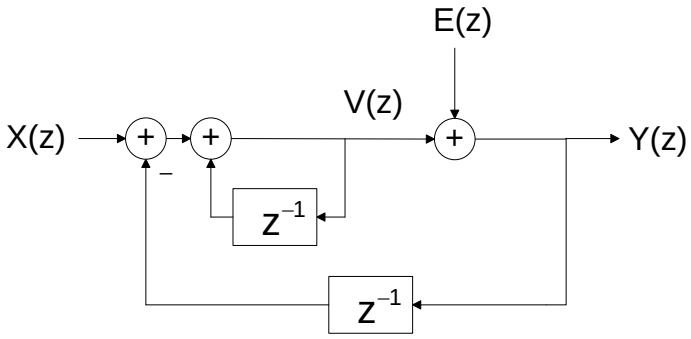
Introduction

- Delta Sigma ($\Delta\sum$) modulators are used in the design of:
  - ✓ Analog to Digital Converters (ADC)
  - ✓ Digital to Analog Converters (DAC)
  - ✓ Frequency Synthesizers
  - ✓ Digital Radios
  - ✓ High Accuracy Oscillators
- $\Delta\sum$ modulators use the techniques of:
  - ✓ Oversampling
  - ✓ Noise Shaping

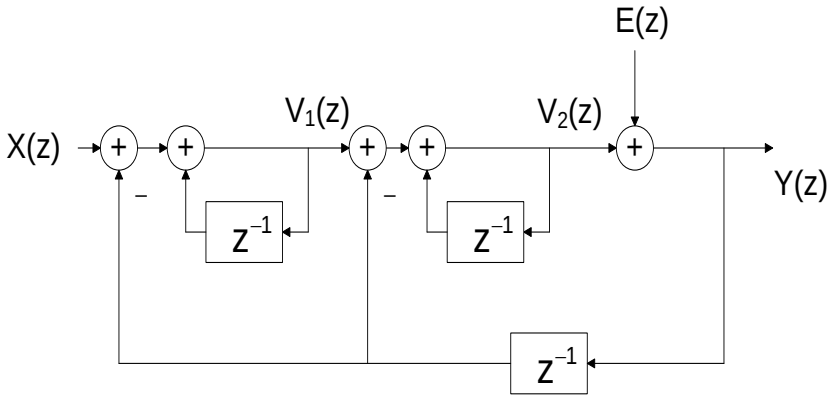
Delta Sigma Modulators (Non-Adaptive)

- Digital $\Delta\sum$ modulators consist of a subtractor, an accumulator and, in most cases, a one bit quantizer.
- The order of the accumulator transfer function determines the order of the modulator.
- Operate on the difference of the input and its predicted value.
- The 2nd order $\Delta\sum$ modulator performs better noise shaping due to the characteristics of the accumulator transfer function.
- Demodulation requires only an appropriate low pass filter.

1st order $\Delta\sum$ modulator with one bit quantization



2nd order $\Delta\sum$ modulator with one bit quantization

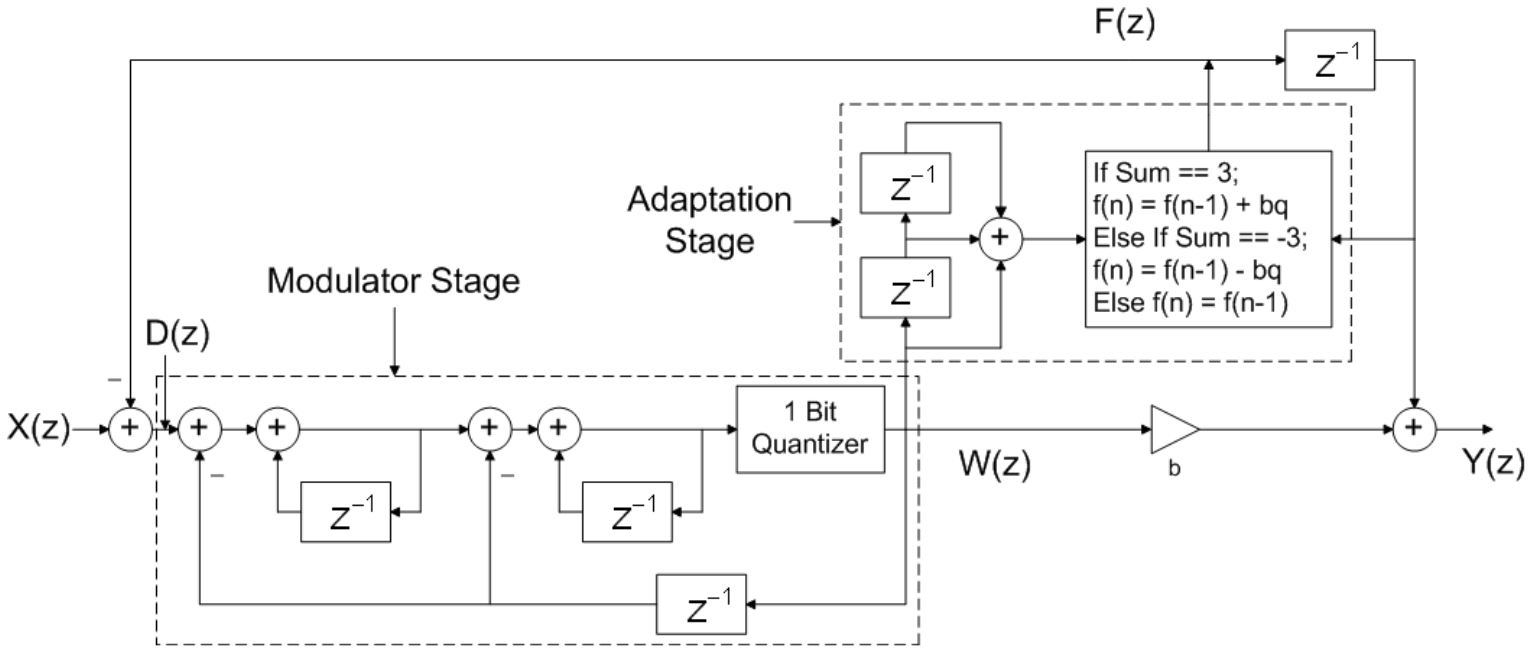


Adaptive ΔΣ Modulator

- The purpose of adaptive ΔΣ techniques is to enhance the stability and the dynamic range of the ΔΣ modulators.
- The design of a 1st order adaptive ΔΣ modulator with one bit quantization (ADSM1) has been discussed in [7]. The main features of this modulator are:
  - ✓ An adaptive feedback signal is generated which tracks the input signal.
  - ✓ The adaptive feedback signal is subtracted from the input signal resulting in a difference signal which is in a reduced range.
  - ✓ A 1st order ΔΣ modulator resides within the adaptive ΔΣ modulator.
  - ✓ The difference signal is given to the internal 1st order ΔΣ modulator.
  - ✓ This results in less quantization noise which translates into a better Signal to Quantization Noise Ratio (SQNR) and an enhanced dynamic range.

Architecture of the 2nd Order Adaptive ΔΣ Modulator with One Bit Quantization (ADSM2)

- ADSM2 was designed by replacing the internal 1st order ΔΣ modulator with a 2nd order one.
- ADSM2 consists of two stages:
  - ✓ The *Modulator Stage*
  - ✓ The *Adaptation Stage*



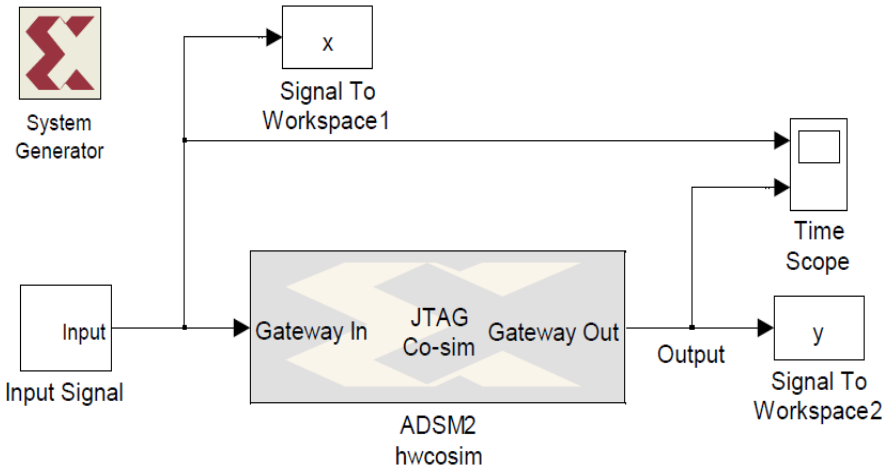
Architecture of the 2nd Order Adaptive ΔΣ Modulator with One Bit Quantization (ADSM2)

- The Adaptation algorithm works on the basis of the output values of the internal 2nd order ΔΣ modulator and has the following characteristics (as reported in [7]):
  - ✓ It is an *instantaneous adaptation algorithm*.
  - ✓ It uses *backward estimation.*
- Changes are made in the adaptive feedback signal based on the changes detected in the input signal power so that it can continue tracking the input signal.
  - ✓ If the internal 2nd order ΔΣ modulator cannot track the signal at its input, then a continuous string of either +1's or -1's appear at its output.
  - ✓ If local density of +1's or -1's exceeds a particular threshold, then the adaptive feedback signal can be changed accordingly.

Sample values			Adaptive Feedback Signal f(n)
w(n)	w(n-1)	w(n-2)	
+1	+1	+1	f(n) = f(n-1) + bq
-1	-1	-1	f(n) = f(n-1) – bq
All other combinations			f(n) = f(n-1)

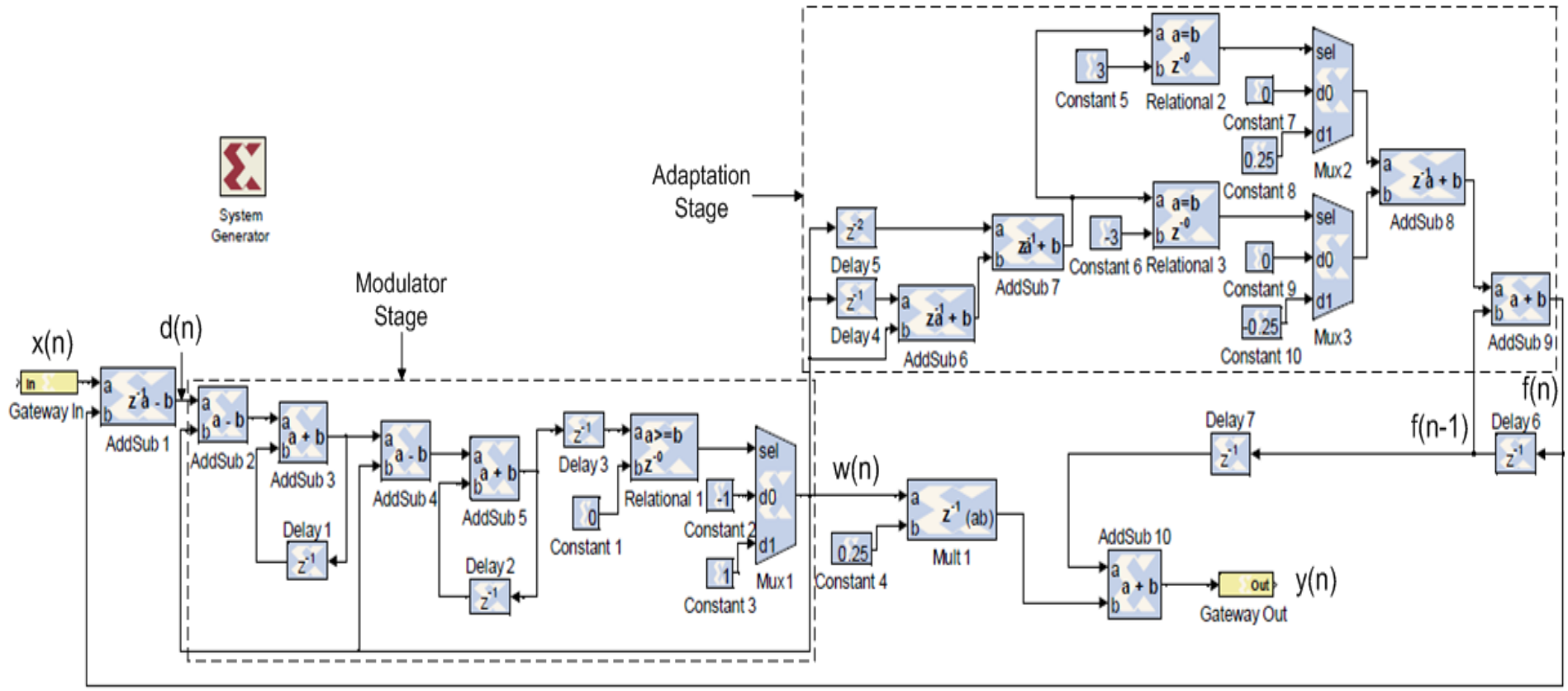
Hardware Implementation of ADSM2

- The Xilinx System Generator for DSP was used to model and implement the design on to the FPGA.
- It is a system level modeling tool that facilitates FPGA design.
- It has the ability to work at a higher level of abstraction.
- It integrates itself with Simulink in the form of Xilinx Block sets.
- It allows Hardware Emulation and generates the HDL Code of the hardware model.
- The *Hardware Co-Simulation Mode* of the System Generator was used which allowed extensive testing on the FPGA.



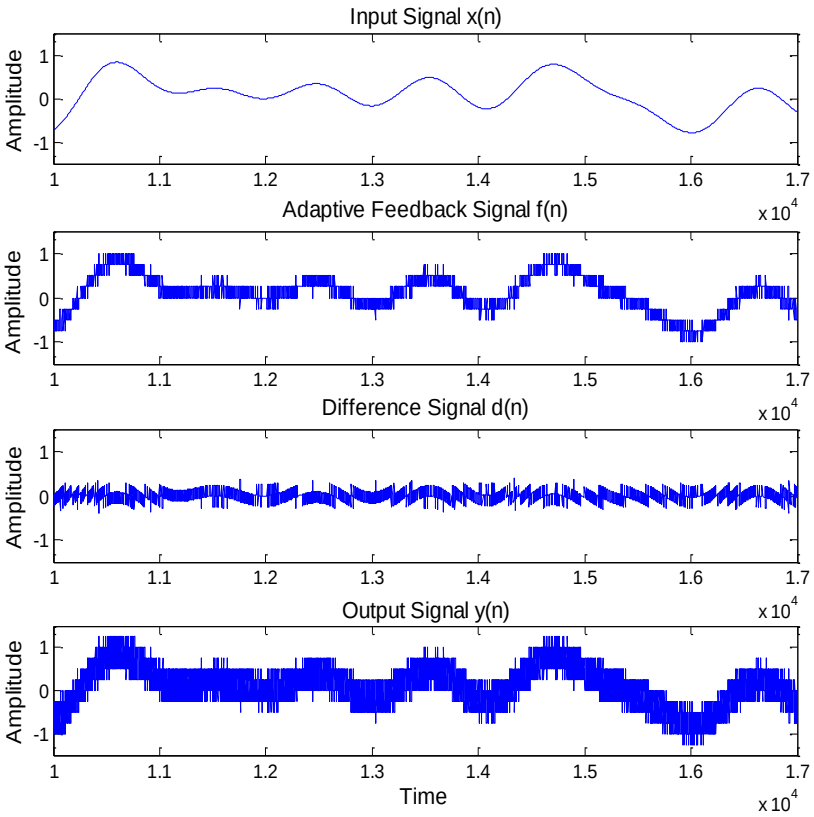
Hardware Implementation of ADSM2

- The implementation model of the ADSM2 as constructed in the Xilinx System Generator for DSP is shown here.



Signals at various stages of ADSM2

- The input signal x(n) has a bandwidth of 20 KHz and is composed of five sinusoidal components.
- It is evident that the adaptive feedback signal f(n) tracks the input signal x(n) and the difference signal d(n) is in a reduced range.
- The output signal y(n) is a multilevel signal despite the fact that the quantizer used is one bit.
- The output signal y(n) is a better digital representation of the input signal as compared to the traditional $\Delta\sum$ modulator output.

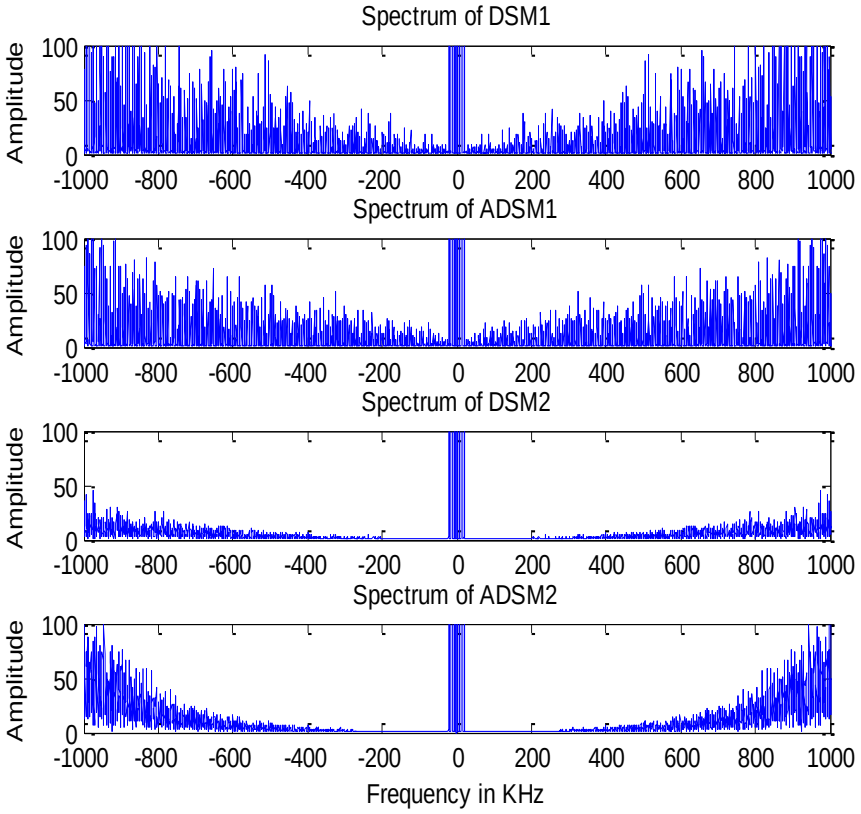


FPGA Performance Analysis of ADSM2

- The Digilent Inc., Spartan-3E Started Kit was used to implement this work.
- This board has the Xilinx Spartan-3E XC3S500E FPGA device with an on-board clock of 50 MHz.
- Three other $\Delta\sum$ modulators were implemented on the FPGA for comparison purposes. These are:
  - ✓ 1st order (non-adaptive) $\Delta\sum$ Modulator (DSM1)
  - ✓ 1st order adaptive $\Delta\sum$ Modulator (ADSM1)
  - ✓ 2nd order (non-adaptive) $\Delta\sum$ Modulator (DSM2)
- The performance of the four modulators was compared and analyzed in the following ways:
  - ✓ Spectral Analysis of all four modulators
  - ✓ Input Power versus Signal to Quantization Noise Ratio (SQNR) analysis of all four modulators at fixed values of Oversampling Ratio (OSR)
  - ✓ Input Power versus SQNR analysis of ADSM2 at four different OSR values

Spectral Analysis of ADSM2 in comparison with other modulators (DSM1, ADSM1 and DSM2)

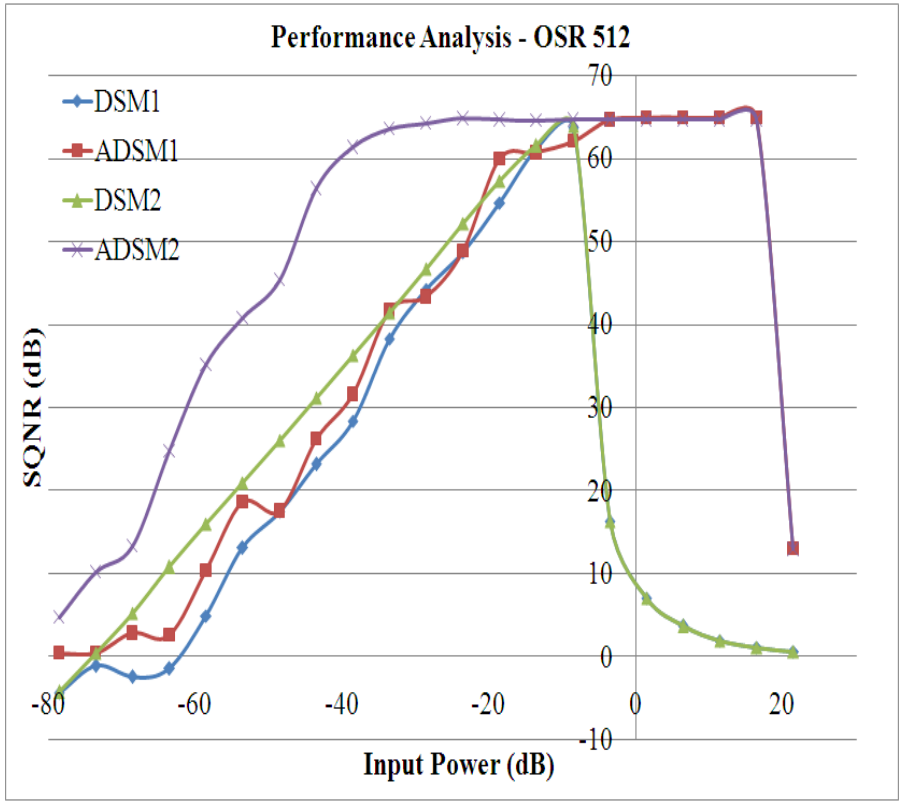
- Noise shaping is evident in all four cases.
- Noise shaping is better in case of 2^{nd} order modulators when compared to 1^{st} order modulators.
- For DSM2 the band without significant quantization noise components is 0 to 200 KHz.
- For ADSM2 the band without significant quantization noise components is 0 to 300 KHz making it the better of the four modulators under consideration.



Input Power VS SQNR Analysis

Analysis of all four modulators at an OSR of 512

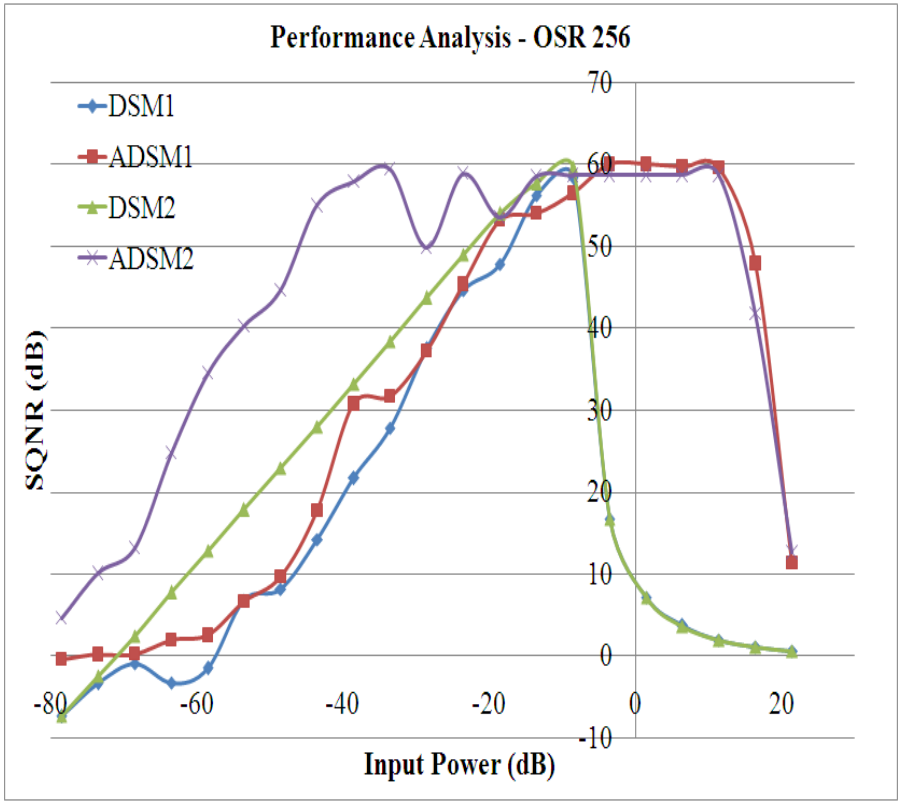
- Analysis done in the input signal power range of -80 to 20 dBs.
- ADSM2 gives the best results.
- ADSM1 matches ADSM2 only in the input power range of -3.5 to 20 dBs and not elsewhere.
- The adaptive modulators have a larger dynamic range as compared to the non-adaptive modulators.



Input Power VS SQNR Analysis

Analysis of all four modulators at an OSR of 256

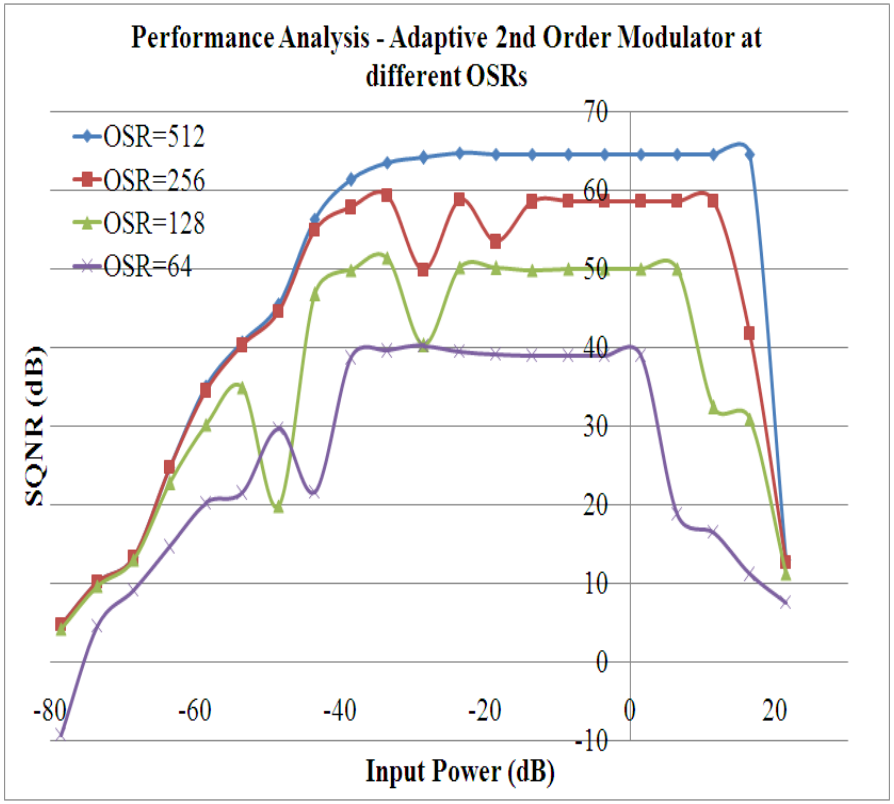
- Trends similar to those seen for the OSR of 512 are seen here as well.
- ADSM2 again gives better results.
- Two dips are seen in the SQNR curve of ADSM2 at the input powers of -28 dB and -18 dB.
- The performance of ADSM2 remains better than or equal to that of other modulators even at these points.



Input Power VS SQNR Analysis

Analysis of ADSM2 at four different OSR values of 64, 128, 256 & 512

- Like any other modulator, the performance of ADSM2 gets better with higher values of OSR.
- Certain dips are visible in the SQNR curves at lower values of OSR.
- These dips occur in regions where a small portion of the input signal requires change in the adaptive feedback signal.
- Removal of these dips may be regarded as future work.



Summary of Results

- The 2nd order Adaptive ΔΣ Modulator presented in our work displays the following improvements:
  - ✓ It exhibits better spectral noise shaping as compared to the other modulators.
  - ✓ As compared to the 2nd order (non-adaptive) ΔΣ modulator (DSM2), in an input power range of -80 to 20 dB, ADSM2 exhibits an average SQNR improvement of:
    - 24.66 dB at an OSR of 512.
    - 22.11 dB at an OSR of 256.
    - 16.59 dB at an OSR of 128.
    - 8.24 dB at an OSR of 64.
  - ✓ ADSM2 exhibits an increased dynamic range of 24 dB when compared to the DSM2.

Conclusion

- The design and FPGA implementation of a 2^{nd} order all-digital Adaptive $\Delta\sum$ Modulator with one bit quantization was presented.
- DSM1, ADSM1 and DSM2 were also implemented on the FPGA to carry out detailed performance analysis.
- It has been found that ADSM2 performs better noise shaping, exhibits and increased dynamic range and gives better SQNR performance when compared to the other modulators.
- Implementation was carried out on a Xilinx Spartan-3E FPGA.
- The high level design tool Xilinx System Generator for DSP was used to emulate and implement ADSM2.
- The Hardware Co-Simulation mode of the System Generator enabled the extensive testing of the ADSM2.

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Thank you

Q & A