CS 242-01 Homework 1 (Due day: 02/8/2016)

1. <§1.2> The eight great ideas in computer architecture are similar to ideas from other fields. Match the eight ideas from computer architecture, “Design for Moore’s Law”, “Use Abstraction to Simplify Design”, “Make the Common Case Fast”, “Performance via Parallelism”, “Performance via Pipelining”, “Performance via Prediction”, “Hierarchy of Memories”, and “Dependability via Redundancy” to the following ideas from other fields:

**a.** Assembly lines in automobile manufacturing

**b.** Suspension bridge cables

**c.** Aircraft and marine navigation systems that incorporate wind information

**d.** Express elevators in buildings

**e.** Library reserve desk

**f.** Increasing the gate area on a CMOS transistor to decrease its switching time

**g.** Adding electromagnetic aircraft catapults (which are electrically-powered as opposed to current steam-powered models), allowed by the increased power generation offered by the new reactor technology

**h.** Building self-driving cars whose control systems partially rely on existing sensor systems already installed into the base vehicle, such as lane departure systems and smart cruise control systems

2. <§1.4> Assume a color display using 8 bits for each of the primary colors (red, green, blue) per pixel and a frame size of 1280 × 1024.

**a.** What is the minimum size in bytes of the frame buffer to store a frame?

**b.** How long would it take, at a minimum, for the frame to be sent over a 100 Mbit/s network?

3. <§1.6> Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

**a.** Which processor has the highest performance expressed in instructions per second?

**b.** If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

**c.** We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

4. <§1.6> Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). **P1** with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and **P2** with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.

Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

**a.** What is the global CPI for each implementation?

**b.** Find the clock cycles required in both cases.

5. <§1.10> Assume a program requires the execution of 50 × 10^6 FP instructions, 110 × 10^6 INT instructions, 80 × 10^6 L/S instructions, and 16 × 10^6 branch instructions. The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate.

**a.** By how much must we improve the CPI of FP instructions if we want the program to run two times faster?

**b.** By how much must we improve the CPI of L/S instructions if we want the program to run two times faster?

**c.** By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 40% and the CPI of L/S and Branch is reduced by 30%?