

## **ADC10**

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The ADC10 module is a high-performance 10-bit analog-to-digital converter. This chapter describes the operation of the ADC10 module of the 2xx family in general. There are device with less than eight external input channels.

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## 22.1 ADC10 Introduction

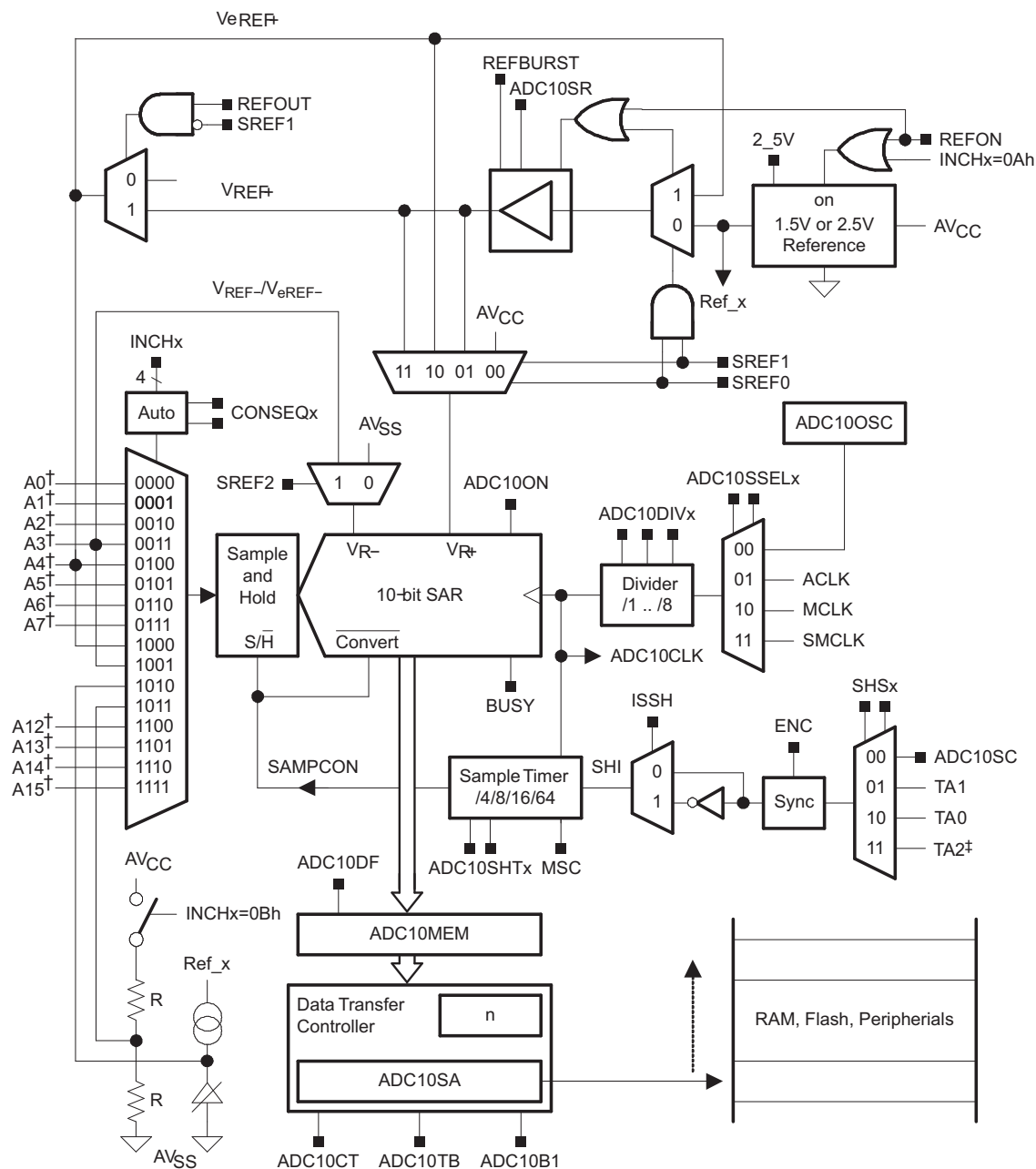
The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and data transfer controller (DTC).

The DTC allows ADC10 samples to be converted and stored anywhere in memory without CPU intervention. The module can be configured with user software to support a variety of applications.

ADC10 features include:

- Greater than 200-ksps maximum conversion rate
- Monotonic 10-bit converter with no missing codes
- Sample-and-hold with programmable sample periods
- Conversion initiation by software or Timer\_A
- Software selectable on-chip reference voltage generation (1.5 V or 2.5 V)
- Software selectable internal or external reference
- Up to eight external input channels (twelve on MSP430F22xx devices)
- Conversion channels for internal temperature sensor,  $V_{CC}$ , and external references
- Selectable conversion clock source
- Single-channel, repeated single-channel, sequence, and repeated sequence conversion modes
- ADC core and reference voltage can be powered down separately
- Data transfer controller for automatic storage of conversion results

The block diagram of ADC10 is shown in [Figure 22-1](#).



†Channels A12-A15 are available in MSP430F22xx devices only. Channels A12-A15 tied to channel A11 in other devices. Not all channels are available in all devices.

‡TA1 on MSP430F20x2, MSP430G2x31, and MSP430G2x30 devices

**Figure 22-1. ADC10 Block Diagram**

## 22.2 ADC10 Operation

The ADC10 module is configured with user software. The setup and operation of the ADC10 is discussed in the following sections.

### 22.2.1 10-Bit ADC Core

The ADC core converts an analog input to its 10-bit digital representation and stores the result in the ADC10MEM register. The core uses two programmable/selectable voltage levels ( $V_{R+}$  and  $V_{R-}$ ) to define the upper and lower limits of the conversion. The digital output ( $N_{ADC}$ ) is full scale (03FFh) when the input signal is equal to or higher than  $V_{R+}$ , and zero when the input signal is equal to or lower than  $V_{R-}$ . The input channel and the reference voltage levels ( $V_{R+}$  and  $V_{R-}$ ) are defined in the conversion-control memory. Conversion results may be in straight binary format or 2s-complement format. The conversion formula for the ADC result when using straight binary format is:

$$N_{ADC} = 1023 \times \frac{V_{IN} - V_{R-}}{V_{R+} - V_{R-}}$$

The ADC10 core is configured by two control registers, ADC10CTL0 and ADC10CTL1. The core is enabled with the ADC10ON bit. With few exceptions the ADC10 control bits can only be modified when ENC = 0. ENC must be set to 1 before any conversion can take place.

#### 22.2.1.1 Conversion Clock Selection

The ADC10CLK is used both as the conversion clock and to generate the sampling period. The ADC10 source clock is selected using the ADC10SSELx bits and can be divided from 1 to 8 using the ADC10DIVx bits. Possible ADC10CLK sources are SMCLK, MCLK, ACLK, and internal oscillator ADC10OSC.

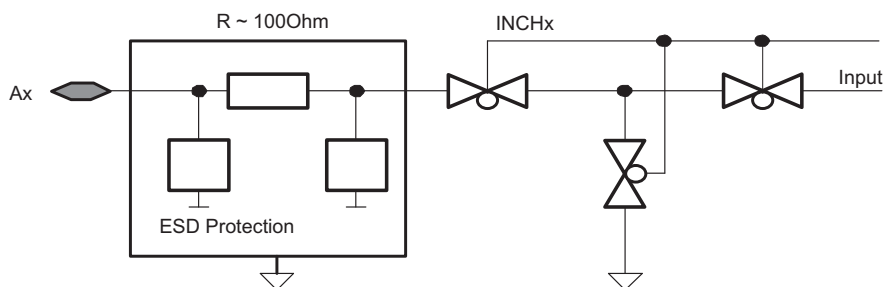
The ADC10OSC, generated internally, is in the 5-MHz range, but varies with individual devices, supply voltage, and temperature. See the device-specific data sheet for the ADC10OSC specification.

The user must ensure that the clock chosen for ADC10CLK remains active until the end of a conversion. If the clock is removed during a conversion, the operation does not complete, and any result is invalid.

### 22.2.2 ADC10 Inputs and Multiplexer

The eight external and four internal analog signals are selected as the channel for conversion by the analog input multiplexer. The input multiplexer is a break-before-make type to reduce input-to-input noise injection that can result from channel switching (see Figure 22-2). The input multiplexer is also a T-switch to minimize the coupling between channels. Channels that are not selected are isolated from the A/D, and the intermediate node is connected to analog ground ( $V_{SS}$ ) so that the stray capacitance is grounded to help eliminate crosstalk.

The ADC10 uses the charge redistribution method. When the inputs are internally switched, the switching action may cause transients on the input signal. These transients decay and settle before causing errant conversion.



**Figure 22-2. Analog Multiplexer**

### 22.2.2.1 Analog Port Selection

The ADC10 external inputs  $A_x$ ,  $V_{REF+}$ , and  $V_{REF-}$  share terminals with general purpose I/O ports, which are digital CMOS gates (see the device-specific data sheet). When analog signals are applied to digital CMOS gates, parasitic current can flow from VCC to GND. This parasitic current occurs if the input voltage is near the transition level of the gate. Disabling the port pin buffer eliminates the parasitic current flow and therefore reduces overall current consumption. The ADC10AEx bits provide the ability to disable the port pin input and output buffers.

```
; P2.3 on MSP430F22xx device configured for analog input
BIS.B    #08h,&ADC10AE0    ; P2.3 ADC10 function and enable
```

Devices which don't have all the ADC10 external inputs channels  $A_x$  or  $V_{REF+}$ / $V_{REF-}$  and  $V_{REF-}$ / $V_{REF-}$  available at device pins must not alter the default register bit configuration of the not available pins. See device specific data sheet.

### 22.2.3 Voltage Reference Generator

The ADC10 module contains a built-in voltage reference with two selectable voltage levels. Setting  $REFON = 1$  enables the internal reference. When  $REF2\_5V = 1$ , the internal reference is 2.5 V. When  $REF2\_5V = 0$ , the reference is 1.5 V. The internal reference voltage may be used internally ( $REFOUT = 0$ ) and, when  $REFOUT = 1$ , externally on pin  $V_{REF+}$ .  $REFOUT = 1$  should only be used if the pins  $V_{REF+}$  and  $V_{REF-}$  are available as device pins.

External references may be supplied for  $V_{R+}$  and  $V_{R-}$  through pins A4 and A3 respectively. When external references are used, or when  $V_{CC}$  is used as the reference, the internal reference may be turned off to save power.

An external positive reference  $V_{REF+}$  can be buffered by setting  $SREF0 = 1$  and  $SREF1 = 1$  (only devices with  $V_{REF+}$  pin). This allows using an external reference with a large internal resistance at the cost of the buffer current. When  $REFBURST = 1$  the increased current consumption is limited to the sample and conversion period.

External storage capacitance is not required for the ADC10 reference source as on the ADC12.

#### 22.2.3.1 Internal Reference Low-Power Features

The ADC10 internal reference generator is designed for low power applications. The reference generator includes a band-gap voltage source and a separate buffer. The current consumption of each is specified separately in the device-specific data sheet. When  $REFON = 1$ , both are enabled and when  $REFON = 0$  both are disabled. The total settling time when  $REFON$  becomes set is approximately 30  $\mu$ s.

When  $REFON = 1$ , but no conversion is active, the buffer is automatically disabled and automatically re-enabled when needed. When the buffer is disabled, it consumes no current. In this case, the bandgap voltage source remains enabled.

When  $REFOUT = 1$ , the  $REFBURST$  bit controls the operation of the internal reference buffer. When  $REFBURST = 0$ , the buffer is on continuously, allowing the reference voltage to be present outside the device continuously. When  $REFBURST = 1$ , the buffer is automatically disabled when the ADC10 is not actively converting and is automatically re-enabled when needed.

The internal reference buffer also has selectable speed versus power settings. When the maximum conversion rate is below 50 ksp/s, setting  $ADC10SR = 1$  reduces the current consumption of the buffer approximately 50%.

### 22.2.4 Auto Power-Down

The ADC10 is designed for low power applications. When the ADC10 is not actively converting, the core is automatically disabled and is automatically re-enabled when needed. The  $ADC10OSC$  is also automatically enabled when needed and disabled when not needed. When the core or oscillator is disabled, it consumes no current.

### 22.2.5 Sample and Conversion Timing

An analog-to-digital conversion is initiated with a rising edge of sample input signal SHI. The source for SHI is selected with the SHSx bits and includes the following:

- The ADC10SC bit
- The Timer\_A Output Unit 1
- The Timer\_A Output Unit 0
- The Timer\_A Output Unit 2

The polarity of the SHI signal source can be inverted with the ISSH bit. The SHTx bits select the sample period  $t_{\text{sample}}$  to be 4, 8, 16, or 64 ADC10CLK cycles. The sampling timer sets SAMPCON high for the selected sample period after synchronization with ADC10CLK. Total sampling time is  $t_{\text{sample}}$  plus  $t_{\text{sync}}$ . The high-to-low SAMPCON transition starts the analog-to-digital conversion, which requires 13 ADC10CLK cycles as shown in Figure 22-3.

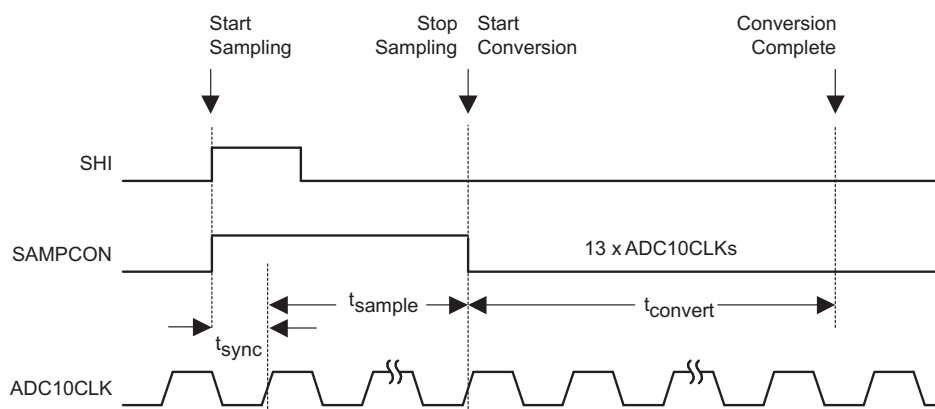


Figure 22-3. Sample Timing

#### 22.2.5.1 Sample Timing Considerations

When SAMPCON = 0 all Ax inputs are high impedance. When SAMPCON = 1, the selected Ax input can be modeled as an RC low-pass filter during the sampling time  $t_{\text{sample}}$ , as shown in Figure 22-4. An internal MUX-on input resistance  $R_I$  (2 k $\Omega$  maximum) in series with capacitor  $C_I$  (27 pF maximum) is seen by the source. The capacitor  $C_I$  voltage  $V_C$  must be charged to within  $\frac{1}{2}$  LSB of the source voltage  $V_S$  for an accurate 10-bit conversion.

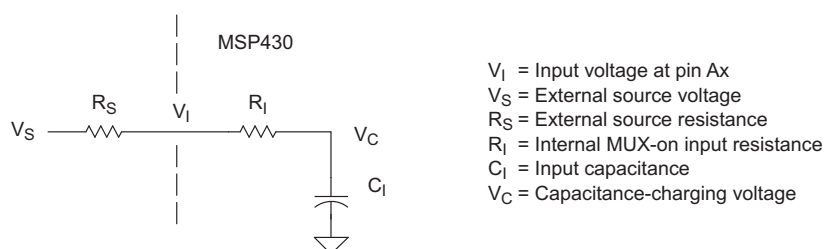


Figure 22-4. Analog Input Equivalent Circuit

The resistance of the source  $R_S$  and  $R_I$  affect  $t_{\text{sample}}$ . The following equations can be used to calculate the minimum sampling time for a 10-bit conversion.

$$t_{\text{sample}} > (R_S + R_I) \times \ln(2^{11}) \times C_I$$

Substituting the values for  $R_I$  and  $C_I$  given above, the equation becomes:

$$t_{\text{sample}} > (R_S + 2 \text{ k}\Omega) \times 7.625 \times 27 \text{ pF}$$

For example, if  $R_S$  is 10 k $\Omega$ ,  $t_{\text{sample}}$  must be greater than 2.47  $\mu\text{s}$ .

When the reference buffer is used in burst mode, the sampling time must be greater than the sampling time calculated and the settling time of the buffer,  $t_{\text{REFBURST}}$ :

$$t_{\text{sample}} > \begin{cases} (R_S + R_I) \times \ln(2^{11}) \times C_I \\ t_{\text{REFBURST}} \end{cases}$$

For example, if  $V_{\text{Ref}}$  is 1.5 V and  $R_S$  is 10 k $\Omega$ ,  $t_{\text{sample}}$  must be greater than 2.47  $\mu\text{s}$  when ADC10SR = 0, or 2.5  $\mu\text{s}$  when ADC10SR = 1. See the device-specific data sheet for parameters.

To calculate the buffer settling time when using an external reference, the formula is:

$$t_{\text{REFBURST}} = S_R \times V_{\text{Ref}} - 0.5 \mu\text{s}$$

Where:

$S_R$  = Buffer slew rate ( $\sim 1 \mu\text{s/V}$  when ADC10SR = 0 and  $\sim 2 \mu\text{s/V}$  when ADC10SR = 1)

$V_{\text{Ref}}$  = External reference voltage

### 22.2.6 Conversion Modes

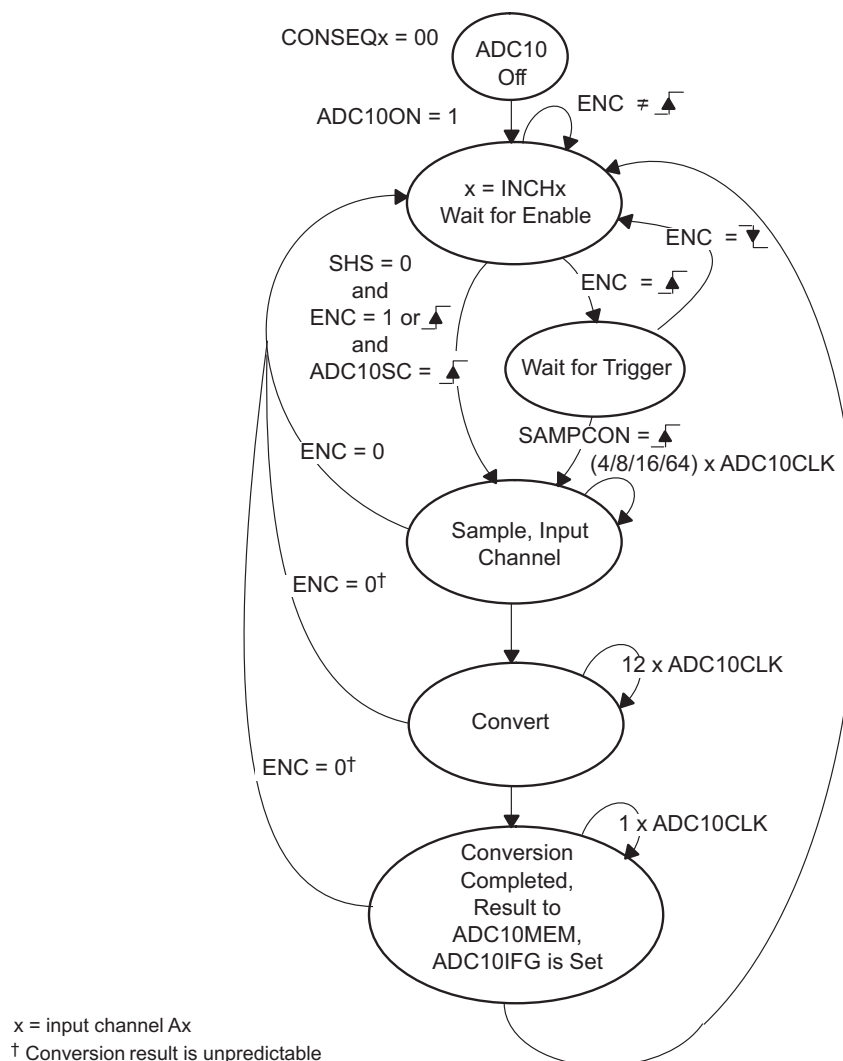
The ADC10 has four operating modes selected by the CONSEQx bits as discussed in [Table 22-1](#).

**Table 22-1. Conversion Mode Summary**

CONSEQx	Mode	Operation
00	Single channel single-conversion	A single channel is converted once.
01	Sequence-of-channels	A sequence of channels is converted once.
10	Repeat single channel	A single channel is converted repeatedly.
11	Repeat sequence-of-channels	A sequence of channels is converted repeatedly.

### 22.2.6.1 Single-Channel Single-Conversion Mode

A single channel selected by INCHx is sampled and converted once. The ADC result is written to ADC10MEM. Figure 22-5 shows the flow of the single-channel, single-conversion mode. When ADC10SC triggers a conversion, successive conversions can be triggered by the ADC10SC bit. When any other trigger source is used, ENC must be toggled between each conversion.



**Figure 22-5. Single-Channel Single-Conversion Mode**



### 22.2.6.2 Sequence-of-Channels Mode

A sequence of channels is sampled and converted once. The sequence begins with the channel selected by INCHx and decrements to channel A0. Each ADC result is written to ADC10MEM. The sequence stops after conversion of channel A0. Figure 22-6 shows the sequence-of-channels mode. When ADC10SC triggers a sequence, successive sequences can be triggered by the ADC10SC bit. When any other trigger source is used, ENC must be toggled between each sequence.

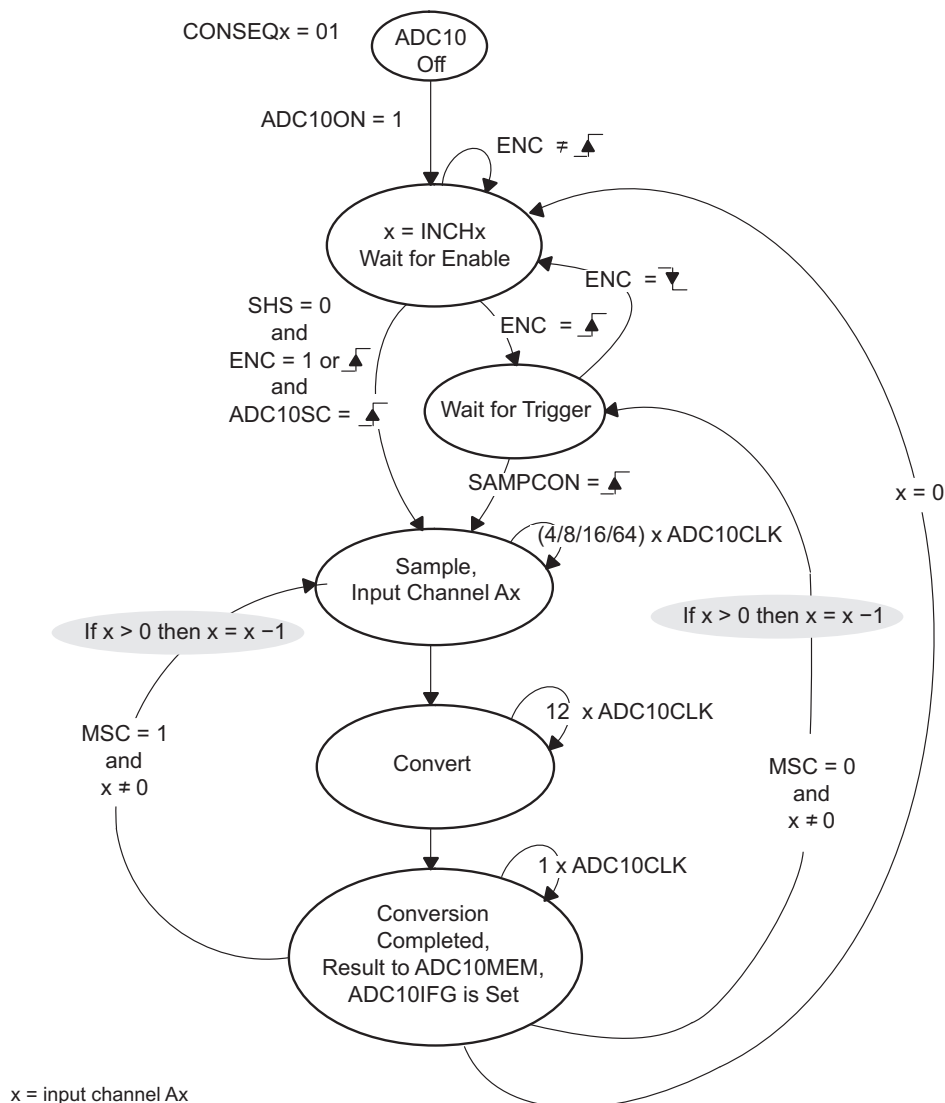
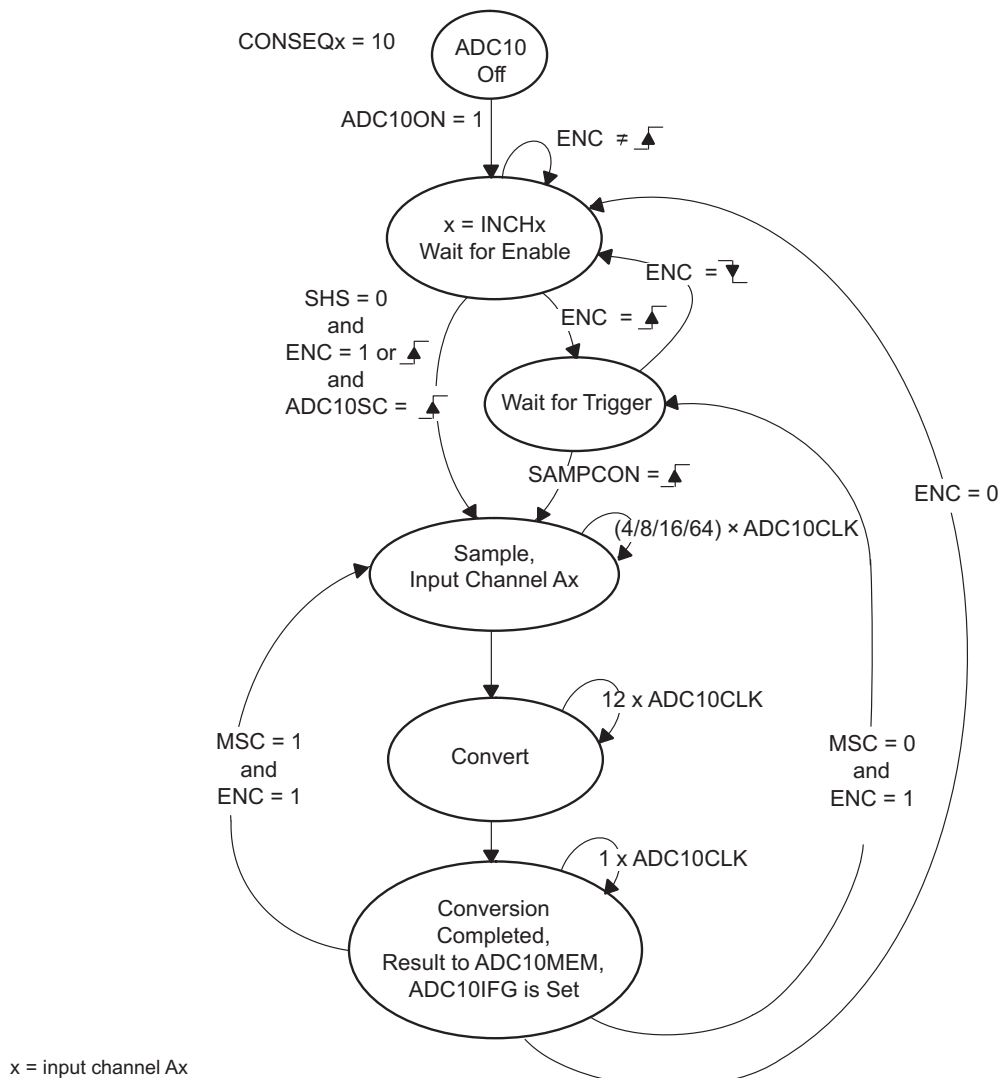


Figure 22-6. Sequence-of-Channels Mode

### 22.2.6.3 Repeat-Single-Channel Mode

A single channel selected by INCHx is sampled and converted continuously. Each ADC result is written to ADC10MEM. [Figure 22-7](#) shows the repeat-single-channel mode.



**Figure 22-7. Repeat-Single-Channel Mode**

#### 22.2.6.4 Repeat-Sequence-of-Channels Mode

A sequence of channels is sampled and converted repeatedly. The sequence begins with the channel selected by INCHx and decrements to channel A0. Each ADC result is written to ADC10MEM. The sequence ends after conversion of channel A0, and the next trigger signal re-starts the sequence.

Figure 22-8 shows the repeat-sequence-of-channels mode.

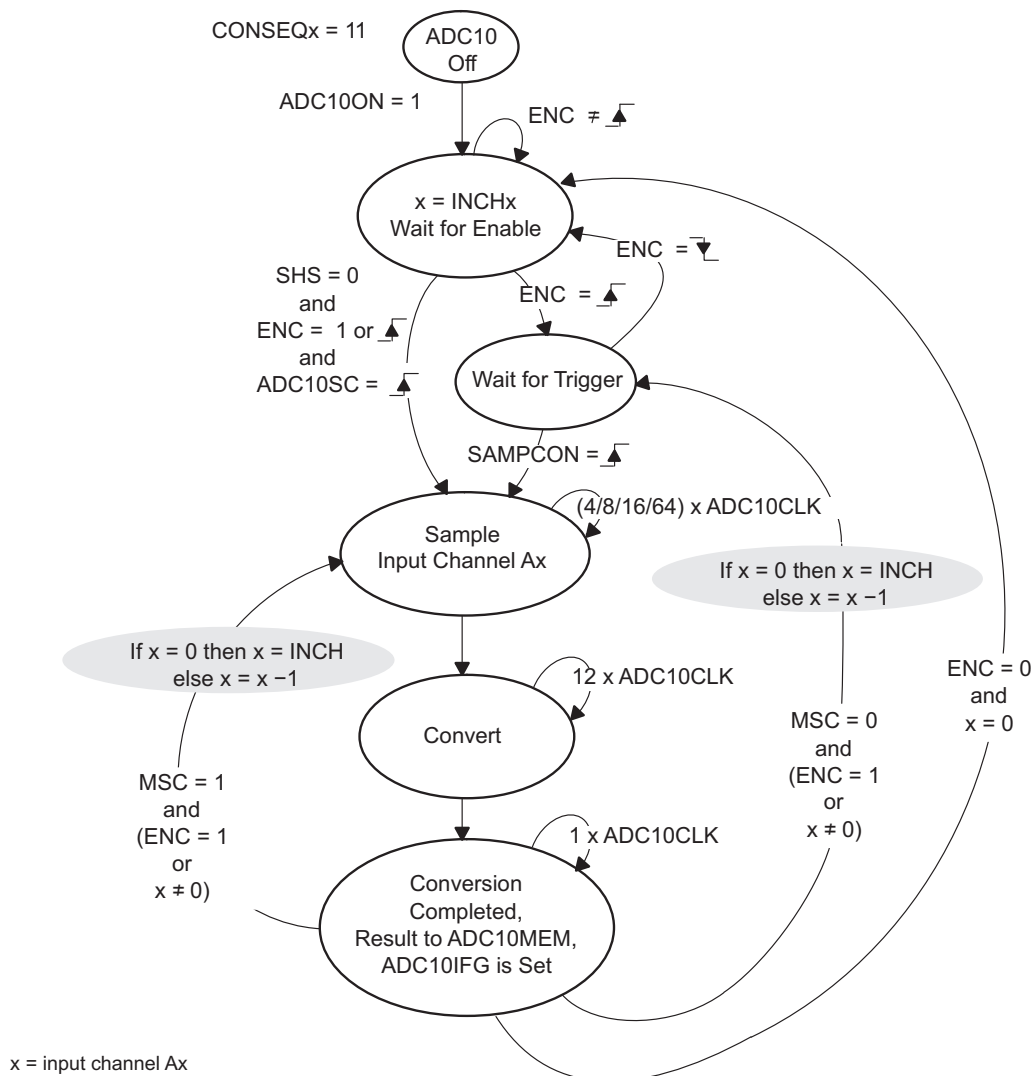


Figure 22-8. Repeat-Sequence-of-Channels Mode

### 22.2.6.5 Using the MSC Bit

To configure the converter to perform successive conversions automatically and as quickly as possible, a multiple sample and convert function is available. When MSC = 1 and CONSEQx > 0, the first rising edge of the SHI signal triggers the first conversion. Successive conversions are triggered automatically as soon as the prior conversion is completed. Additional rising edges on SHI are ignored until the sequence is completed in the single-sequence mode or until the ENC bit is toggled in repeat-single-channel, or repeated-sequence modes. The function of the ENC bit is unchanged when using the MSC bit.

### 22.2.6.6 Stopping Conversions

Stopping ADC10 activity depends on the mode of operation. The recommended ways to stop an active conversion or conversion sequence are:

- Resetting ENC in single-channel single-conversion mode stops a conversion immediately and the results are unpredictable. For correct results, poll the ADC10BUSY bit until reset before clearing ENC.
- Resetting ENC during repeat-single-channel operation stops the converter at the end of the current conversion.
- Resetting ENC during a sequence or repeat sequence mode stops the converter at the end of the sequence.
- Any conversion mode may be stopped immediately by setting the CONSEQx = 0 and resetting the ENC bit. Conversion data is unreliable.

### 22.2.7 ADC10 Data Transfer Controller

The ADC10 includes a data transfer controller (DTC) to automatically transfer conversion results from ADC10MEM to other on-chip memory locations. The DTC is enabled by setting the ADC10DTC1 register to a nonzero value.

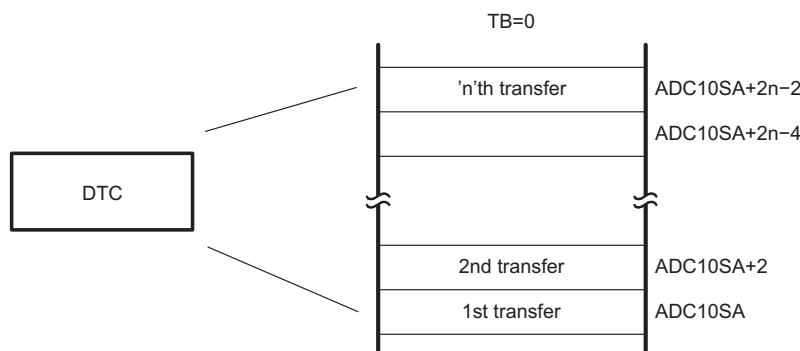
When the DTC is enabled, each time the ADC10 completes a conversion and loads the result to ADC10MEM, a data transfer is triggered. No software intervention is required to manage the ADC10 until the predefined amount of conversion data has been transferred. Each DTC transfer requires one CPU MCLK. To avoid any bus contention during the DTC transfer, the CPU is halted, if active, for the one MCLK required for the transfer.

A DTC transfer must not be initiated while the ADC10 is busy. Software must ensure that no active conversion or sequence is in progress when the DTC is configured:

```
; ADC10 activity test
      BIC.W    #ENC,&ADC10CTL0    ;
busy_test  BIT.W    #BUSY,&ADC10CTL1 ;
      JNZ     busy_test          ;
      MOV.W    #xxx,&ADC10SA      ; Safe
      MOV.B    #xx,&ADC10DTC1     ;
; continue setup
```

### 22.2.7.1 One-Block Transfer Mode

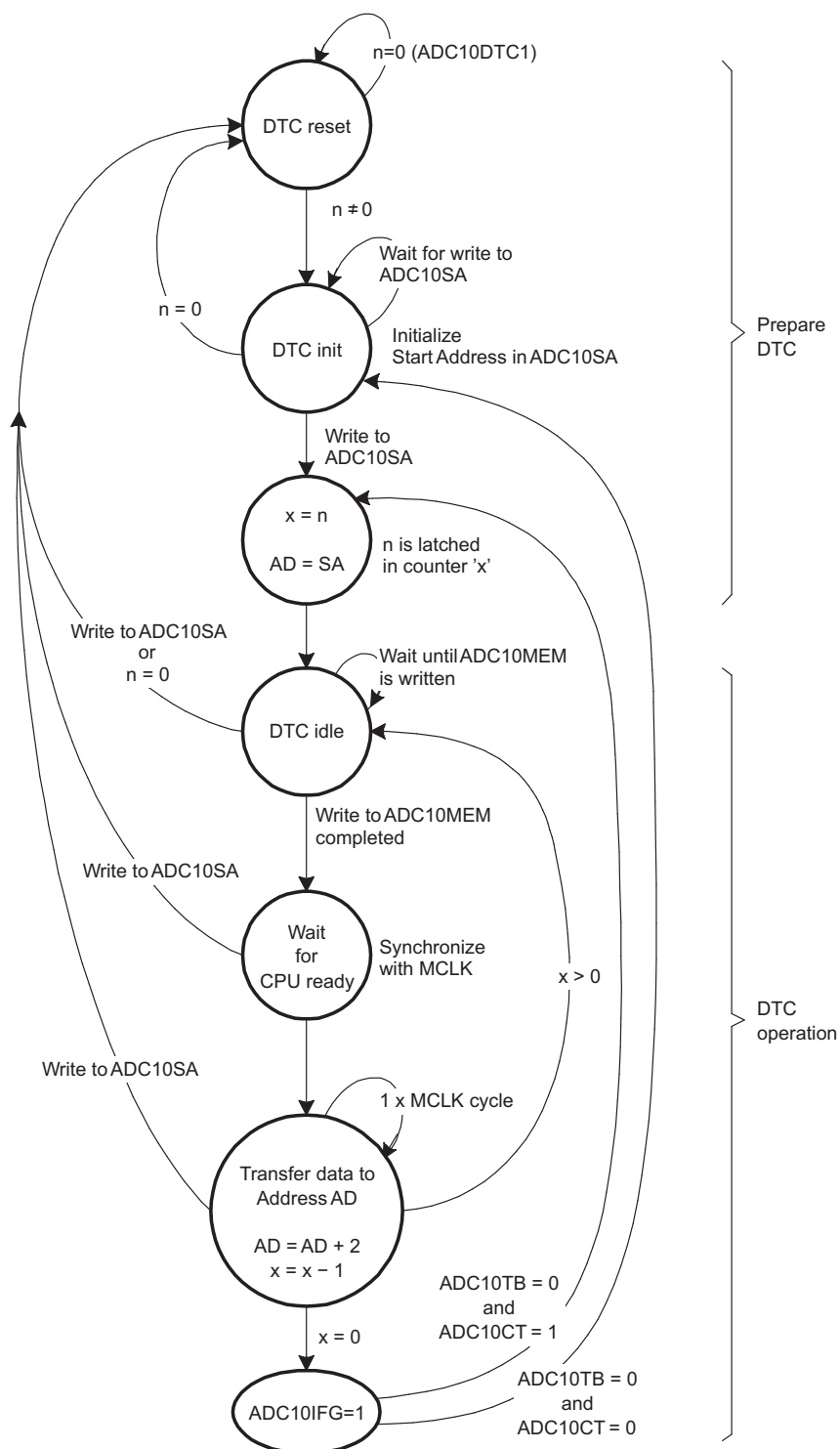
The one-block mode is selected if the ADC10TB is reset. The value  $n$  in ADC10DTC1 defines the total number of transfers for a block. The block start address is defined anywhere in the MSP430 address range using the 16-bit register ADC10SA. The block ends at  $\text{ADC10SA} + 2n - 2$ . The one-block transfer mode is shown in Figure 22-9.



**Figure 22-9. One-Block Transfer**

The internal address pointer is initially equal to ADC10SA and the internal transfer counter is initially equal to  $n$ . The internal pointer and counter are not visible to software. The DTC transfers the word-value of ADC10MEM to the address pointer ADC10SA. After each DTC transfer, the internal address pointer is incremented by two and the internal transfer counter is decremented by one.

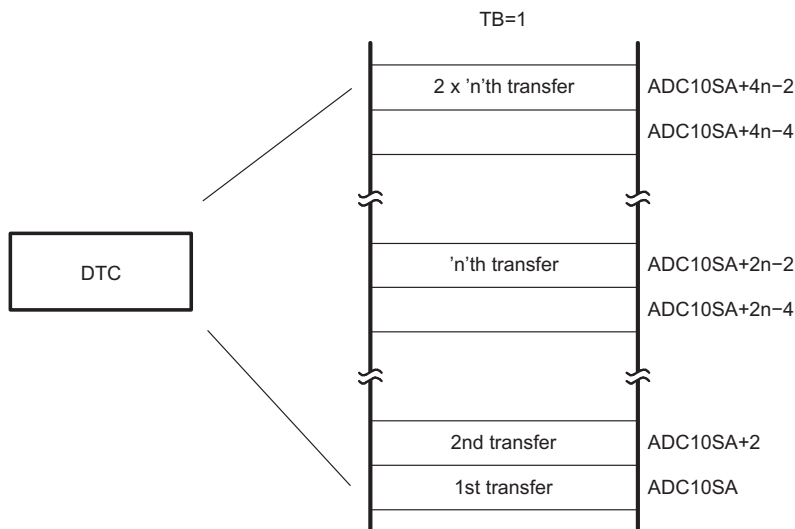
The DTC transfers continue with each loading of ADC10MEM, until the internal transfer counter becomes equal to zero. No additional DTC transfers occur until a write to ADC10SA. When using the DTC in the one-block mode, the ADC10IFG flag is set only after a complete block has been transferred. Figure 22-10 shows a state diagram of the one-block mode.



**Figure 22-10. State Diagram for Data Transfer Control in One-Block Transfer Mode**

### 22.2.7.2 Two-Block Transfer Mode

The two-block mode is selected if the ADC10TB bit is set. The value  $n$  in ADC10DTC1 defines the number of transfers for one block. The address range of the first block is defined anywhere in the MSP430 address range with the 16-bit register ADC10SA. The first block ends at  $\text{ADC10SA} + 2n - 2$ . The address range for the second block is defined as  $\text{SA} + 2n$  to  $\text{SA} + 4n - 2$ . The two-block transfer mode is shown in Figure 22-11.



**Figure 22-11. Two-Block Transfer**

The internal address pointer is initially equal to ADC10SA and the internal transfer counter is initially equal to 'n'. The internal pointer and counter are not visible to software. The DTC transfers the word-value of ADC10MEM to the address pointer ADC10SA. After each DTC transfer the internal address pointer is incremented by two and the internal transfer counter is decremented by one.

The DTC transfers continue, with each loading of ADC10MEM, until the internal transfer counter becomes equal to zero. At this point, block one is full and both the ADC10IFG flag the ADC10B1 bit are set. The user can test the ADC10B1 bit to determine that block one is full.

The DTC continues with block two. The internal transfer counter is automatically reloaded with 'n'. At the next load of the ADC10MEM, the DTC begins transferring conversion results to block two. After  $n$  transfers have completed, block two is full. The ADC10IFG flag is set and the ADC10B1 bit is cleared. User software can test the cleared ADC10B1 bit to determine that block two is full. Figure 22-12 shows a state diagram of the two-block mode.

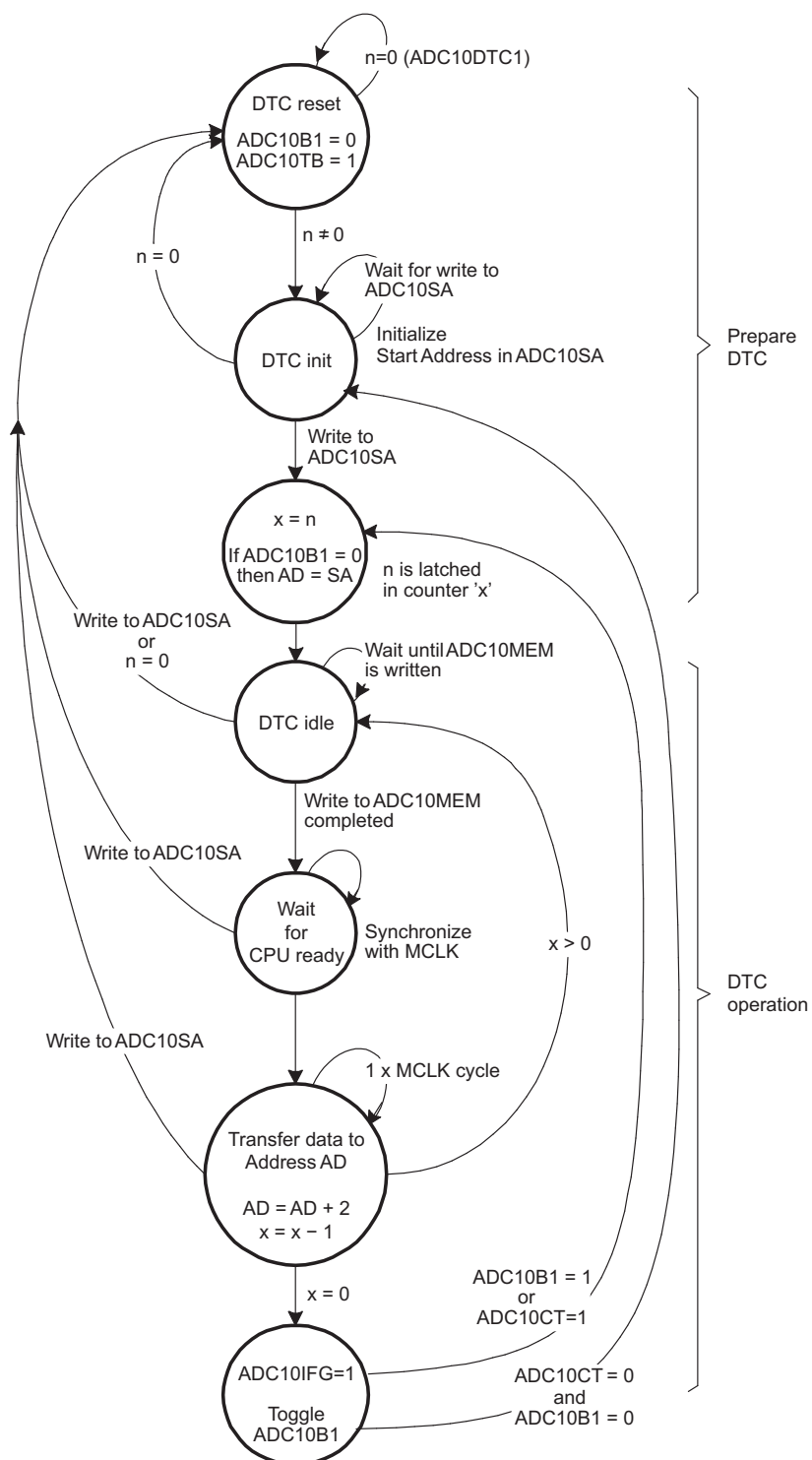


Figure 22-12. State Diagram for Data Transfer Control in Two-Block Transfer Mode



### 22.2.7.3 Continuous Transfer

A continuous transfer is selected if ADC10CT bit is set. The DTC does not stop after block one (in one-block mode) or block two (in two-block mode) has been transferred. The internal address pointer and transfer counter are set equal to ADC10SA and n respectively. Transfers continue starting in block one. If the ADC10CT bit is reset, DTC transfers cease after the current completion of transfers into block one (in one-block mode) or block two (in two-block mode) have been transferred.

### 22.2.7.4 DTC Transfer Cycle Time

For each ADC10MEM transfer, the DTC requires one or two MCLK clock cycles to synchronize, one for the actual transfer (while the CPU is halted), and one cycle of wait time. Because the DTC uses MCLK, the DTC cycle time is dependent on the MSP430 operating mode and clock system setup.

If the MCLK source is active but the CPU is off, the DTC uses the MCLK source for each transfer, without re-enabling the CPU. If the MCLK source is off, the DTC temporarily restarts MCLK, sourced with DCOCLK, only during a transfer. The CPU remains off, and MCLK is again turned off after the DTC transfer. The maximum DTC cycle time for all operating modes is show in [Table 22-2](#).

**Table 22-2. Maximum DTC Cycle Time**

CPU Operating Mode	Clock Source	Maximum DTC Cycle Time
Active mode	MCLK = DCOCLK	3 MCLK cycles
Active mode	MCLK = LFXT1CLK	3 MCLK cycles
Low-power mode LPM0/1	MCLK = DCOCLK	4 MCLK cycles
Low-power mode LPM3/4	MCLK = DCOCLK	4 MCLK cycles + 2 $\mu$ s <sup>(1)</sup>
Low-power mode LPM0/1	MCLK = LFXT1CLK	4 MCLK cycles
Low-power mode LPM3	MCLK = LFXT1CLK	4 MCLK cycles
Low-power mode LPM4	MCLK = LFXT1CLK	4 MCLK cycles + 2 $\mu$ s <sup>(1)</sup>

<sup>(1)</sup> The additional 2  $\mu$ s are needed to start the DCOCLK. See the device-specific data sheet for parameters.

### 22.2.8 Using the Integrated Temperature Sensor

To use the on-chip temperature sensor, select the analog input channel INCHx = 1010. Any other configuration is done as if an external channel was selected, including reference selection, conversion-memory selection, etc.

The typical temperature sensor transfer function is shown in [Figure 22-13](#). When using the temperature sensor, the sample period must be greater than 30  $\mu$ s. The temperature sensor offset error is large. Deriving absolute temperature values in the application requires calibration. See the device-specific data sheet for the parameters. See [Section 24.2.2.1](#) for the calibration equations.

Selecting the temperature sensor automatically turns on the on-chip reference generator as a voltage source for the temperature sensor. However, it does not enable the V<sub>REF+</sub> output or affect the reference selections for the conversion. The reference choices for converting the temperature sensor are the same as with any other channel.

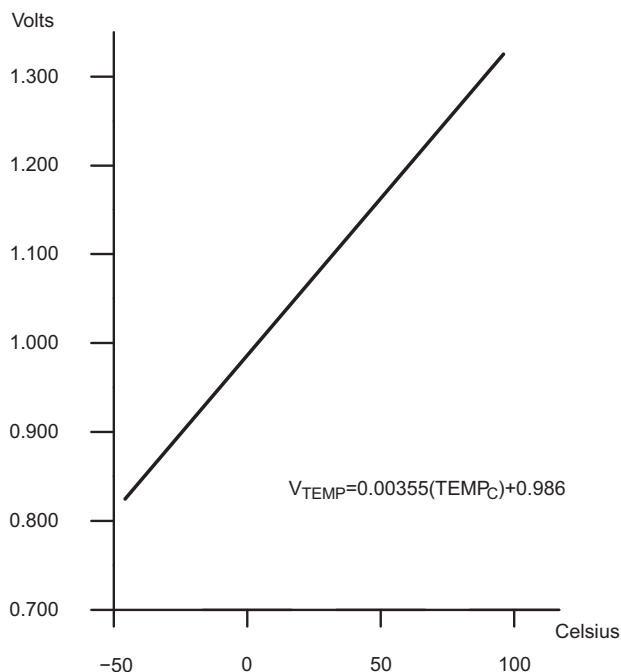


Figure 22-13. Typical Temperature Sensor Transfer Function

### 22.2.9 ADC10 Grounding and Noise Considerations

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the A/D flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small, unwanted offset voltages that can add to or subtract from the reference or input voltages of the A/D converter. The connections shown in [Figure 22-14](#) and [Figure 22-15](#) help avoid this.

In addition to grounding, ripple and noise spikes on the power supply lines due to digital switching or switching power supplies can corrupt the conversion result. A noise-free design is important to achieve high accuracy.

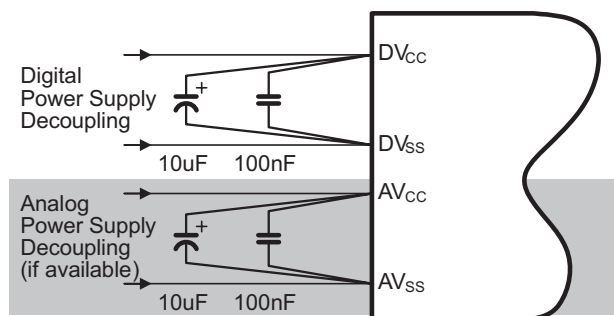
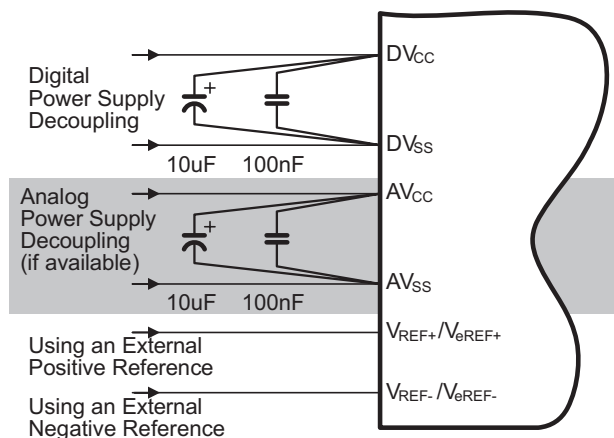


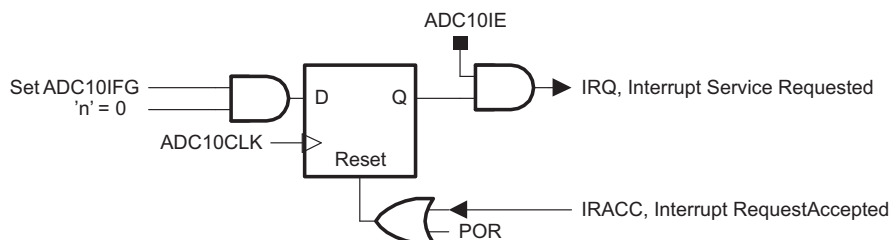
Figure 22-14. ADC10 Grounding and Noise Considerations (Internal  $V_{REF}$ )



**Figure 22-15. ADC10 Grounding and Noise Considerations (External  $V_{REF}$ )**

### 22.2.10 ADC10 Interrupts

One interrupt and one interrupt vector are associated with the ADC10 as shown in Figure 22-16. When the DTC is not used ( $ADC10DTC1 = 0$ ),  $ADC10IFG$  is set when conversion results are loaded into  $ADC10MEM$ . When DTC is used ( $ADC10DTC1 > 0$ ),  $ADC10IFG$  is set when a block transfer completes and the internal transfer counter  $n = 0$ . If both the  $ADC10IE$  and the  $GIE$  bits are set, then the  $ADC10IFG$  flag generates an interrupt request. The  $ADC10IFG$  flag is automatically reset when the interrupt request is serviced, or it may be reset by software.



**Figure 22-16. ADC10 Interrupt System**

## 22.3 ADC10 Registers

The ADC10 registers are listed in [Table 22-3](#).

**Table 22-3. ADC10 Registers**

Register	Short Form	Register Type	Address	Initial State
ADC10 input enable register 0	ADC10AE0	Read/write	04Ah	Reset with POR
ADC10 input enable register 1	ADC10AE1	Read/write	04Bh	Reset with POR
ADC10 control register 0	ADC10CTL0	Read/write	01B0h	Reset with POR
ADC10 control register 1	ADC10CTL1	Read/write	01B2h	Reset with POR
ADC10 memory	ADC10MEM	Read	01B4h	Unchanged
ADC10 data transfer control register 0	ADC10DTC0	Read/write	048h	Reset with POR
ADC10 data transfer control register 1	ADC10DTC1	Read/write	049h	Reset with POR
ADC10 data transfer start address	ADC10SA	Read/write	01BCh	0200h with POR

### 22.3.1 ADC10CTL0, ADC10 Control Register 0

15	14	13	12	11	10	9	8
<b>SREFx</b>			<b>ADC10SHTx</b>		<b>ADC10SR</b>	<b>REFOUT</b>	<b>REFBURST</b>
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
<b>MSC</b>	<b>REF2_5V</b>	<b>REFON</b>	<b>ADC10ON</b>	<b>ADC10IE</b>	<b>ADC10IFG</b>	<b>ENC</b>	<b>ADC10SC</b>
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Can be modified only when ENC = 0

SREFx	Bits 15-13	Select reference.	
		000	$V_{R+} = V_{CC}$ and $V_{R-} = V_{SS}$
		001	$V_{R+} = V_{REF+}$ and $V_{R-} = V_{SS}$
		010	$V_{R+} = V_{eREF+}$ and $V_{R-} = V_{SS}$ . Devices with $V_{eREF+}$ only.
		011	$V_{R+} = \text{Buffered } V_{eREF+}$ and $V_{R-} = V_{SS}$ . Devices with $V_{eREF+}$ pin only.
		100	$V_{R+} = V_{CC}$ and $V_{R-} = V_{REF-} / V_{eREF-}$ . Devices with $V_{eREF-}$ pin only.
		101	$V_{R+} = V_{REF+}$ and $V_{R-} = V_{REF-} / V_{eREF-}$ . Devices with $V_{eREF+/-}$ pins only.
		110	$V_{R+} = V_{eREF+}$ and $V_{R-} = V_{REF-} / V_{eREF-}$ . Devices with $V_{eREF+/-}$ pins only.
111	$V_{R+} = \text{Buffered } V_{eREF+}$ and $V_{R-} = V_{REF-} / V_{eREF-}$ . Devices with $V_{eREF+/-}$ pins only.		
ADC10SHTx	Bits 12-11	ADC10 sample-and-hold time	
		00	4 × ADC10CLKs
		01	8 × ADC10CLKs
		10	16 × ADC10CLKs
		11	64 × ADC10CLKs
ADC10SR	Bit 10	ADC10 sampling rate. This bit selects the reference buffer drive capability for the maximum sampling rate. Setting ADC10SR reduces the current consumption of the reference buffer.	
		0	Reference buffer supports up to ~200 ksps
		1	Reference buffer supports up to ~50 ksps
REFOUT	Bit 9	Reference output	
		0	Reference output off
REFBURST	Bit 8	Reference output on. Devices with $V_{eREF+} / V_{REF+}$ pin only.	
		Reference burst.	
		0	Reference buffer on continuously
MSC	Bit 7	Reference buffer on only during sample-and-conversion	
		Multiple sample and conversion. Valid only for sequence or repeated modes.	
		0	The sampling requires a rising edge of the SHI signal to trigger each sample-and-conversion.
REF2_5V	Bit 6	The first rising edge of the SHI signal triggers the sampling timer, but further sample-and-conversions are performed automatically as soon as the prior conversion is completed	
		Reference-generator voltage. REFON must also be set.	
		0	1.5 V
REFON	Bit 5	2.5 V	
		Reference generator on	
		0	Reference off
ADC10ON	Bit 4	Reference on	
		ADC10 on	
		0	ADC10 off
ADC10IE	Bit 3	ADC10 on	
		ADC10 interrupt enable	
		0	Interrupt disabled
		1	Interrupt enabled

<b>ADC10IFG</b>	Bit 2	ADC10 interrupt flag. This bit is set if ADC10MEM is loaded with a conversion result. It is automatically reset when the interrupt request is accepted, or it may be reset by software. When using the DTC this flag is set when a block of transfers is completed.
		0 No interrupt pending 1 Interrupt pending
<b>ENC</b>	Bit 1	Enable conversion
		0 ADC10 disabled 1 ADC10 enabled
<b>ADC10SC</b>	Bit 0	Start conversion. Software-controlled sample-and-conversion start. ADC10SC and ENC may be set together with one instruction. ADC10SC is reset automatically.
		0 No sample-and-conversion start 1 Start sample-and-conversion

## 22.3.2 ADC10CTL1, ADC10 Control Register 1

15	14	13	12	11	10	9	8
<b>INCHx</b>				<b>SHSx</b>		<b>ADC10DF</b>	<b>ISSH</b>
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
<b>ADC10DIVx</b>			<b>ADC10SSELx</b>		<b>CONSEQx</b>		<b>ADC10BUSY</b>
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-0

Can be modified only when ENC = 0

INCHx	Bits 15-12	Input channel select. These bits select the channel for a single-conversion or the highest channel for a sequence of conversions. Only available ADC channels should be selected. See device specific data sheet.	
		0000	A0
		0001	A1
		0010	A2
		0011	A3
		0100	A4
		0101	A5
		0110	A6
		0111	A7
		1000	V <sub>eREF+</sub>
		1001	V <sub>REF-</sub> /V <sub>eREF-</sub>
		1010	Temperature sensor
		1011	(V <sub>CC</sub> - V <sub>SS</sub> ) / 2
		1100	(V <sub>CC</sub> - V <sub>SS</sub> ) / 2, A12 on MSP430F22xx devices
		1101	(V <sub>CC</sub> - V <sub>SS</sub> ) / 2, A13 on MSP430F22xx devices
		1110	(V <sub>CC</sub> - V <sub>SS</sub> ) / 2, A14 on MSP430F22xx devices
		1111	(V <sub>CC</sub> - V <sub>SS</sub> ) / 2, A15 on MSP430F22xx devices
SHSx	Bits 11-10	Sample-and-hold source select.	
		00	ADC10SC bit
		01	Timer_A.OUT1 <sup>(1)</sup>
		10	Timer_A.OUT0 <sup>(1)</sup>
		11	Timer_A.OUT2 (Timer_A.OUT1 on MSP430F20x0, MSP430G2x31, and MSP430G2x30 devices) <sup>(1)</sup>
ADC10DF	Bit 9	ADC10 data format	
		0	Straight binary
		1	2s complement
ISSH	Bit 8	Invert signal sample-and-hold	
		0	The sample-input signal is not inverted.
		1	The sample-input signal is inverted.
ADC10DIVx	Bits 7-5	ADC10 clock divider	
		000	/1
		001	/2
		010	/3
		011	/4
		100	/5
		101	/6
		110	/7
		111	/8
ADC10SSELx	Bits 4-3	ADC10 clock source select	
		00	ADC10OSC
		01	ACLK
		10	MCLK
		11	SMCLK

<sup>(1)</sup> Timer triggers are from Timer0\_Ax if more than one timer module exists on the device.

<b>CONSEQx</b>	Bits 2-1	Conversion sequence mode select
		00 Single-channel-single-conversion
		01 Sequence-of-channels
		10 Repeat-single-channel
		11 Repeat-sequence-of-channels
<b>ADC10BUSY</b>	Bit 0	ADC10 busy. This bit indicates an active sample or conversion operation
		0 No operation is active.
		1 A sequence, sample, or conversion is active.

### 22.3.3 ADC10AE0, Analog (Input) Enable Control Register 0

	7	6	5	4	3	2	1	0
	<b>ADC10AE0x</b>							
	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
<b>ADC10AE0x</b>	Bits 7-0	ADC10 analog enable. These bits enable the corresponding pin for analog input. BIT0 corresponds to A0, BIT1 corresponds to A1, etc. The analog enable bit of not implemented channels should not be programmed to 1.						
		0 Analog input disabled						
		1 Analog input enabled						

### 22.3.4 ADC10AE1, Analog (Input) Enable Control Register 1 (MSP430F22xx only)

	7	6	5	4	3	2	1	0
	<b>ADC10AE1x</b>				<b>Reserved</b>			
	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
<b>ADC10AE1x</b>	Bits 7-4	ADC10 analog enable. These bits enable the corresponding pin for analog input. BIT4 corresponds to A12, BIT5 corresponds to A13, BIT6 corresponds to A14, and BIT7 corresponds to A15. The analog enable bit of not implemented channels should not be programmed to 1.						
		0 Analog input disabled						
		1 Analog input enabled						
<b>Reserved</b>	Bits 3-0	Reserved						

### 22.3.5 ADC10MEM, Conversion-Memory Register, Binary Format

	15	14	13	12	11	10	9	8
	0	0	0	0	0	0	<b>Conversion Results</b>	
	r0	r0	r0	r0	r0	r0	r	r
	7	6	5	4	3	2	1	0
	<b>Conversion Results</b>							
	r	r	r	r	r	r	r	r
<b>Conversion Results</b>	Bits 15-0	The 10-bit conversion results are right justified, straight-binary format. Bit 9 is the MSB. Bits 15-10 are always 0.						



### 22.3.6 ADC10MEM, Conversion-Memory Register, 2s Complement Format

15	14	13	12	11	10	9	8
<b>Conversion Results</b>							
r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
<b>Conversion Results</b>	0	0	0	0	0	0	0
r	r	r0	r0	r0	r0	r0	r0

**Conversion Results** Bits 15-0 The 10-bit conversion results are left-justified, 2s complement format. Bit 15 is the MSB. Bits 5-0 are always 0.

### 22.3.7 ADC10DTC0, Data Transfer Control Register 0

7	6	5	4	3	2	1	0
<b>Reserved</b>				<b>ADC10TB</b>	<b>ADC10CT</b>	<b>ADC10B1</b>	<b>ADC10FETCH</b>
r0	r0	r0	r0	rw-(0)	rw-(0)	r-(0)	rw-(0)

**Reserved** Bits 7-4 Reserved. Always read as 0.

**ADC10TB** Bit 3 ADC10 two-block mode  
0 One-block transfer mode  
1 Two-block transfer mode

**ADC10CT** Bit 2 ADC10 continuous transfer  
0 Data transfer stops when one block (one-block mode) or two blocks (two-block mode) have completed.  
1 Data is transferred continuously. DTC operation is stopped only if ADC10CT cleared, or ADC10SA is written to.

**ADC10B1** Bit 1 ADC10 block one. This bit indicates for two-block mode which block is filled with ADC10 conversion results. ADC10B1 is valid only after ADC10IFG has been set the first time during DTC operation. ADC10TB must also be set.  
0 Block 2 is filled  
1 Block 1 is filled

**ADC10FETCH** Bit 0 This bit should normally be reset.

### 22.3.8 ADC10DTC1, Data Transfer Control Register 1

7	6	5	4	3	2	1	0
<b>DTC Transfers</b>							
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

**DTC Transfers** Bits 7-0 DTC transfers. These bits define the number of transfers in each block.  
0 DTC is disabled  
01h-0FFh Number of transfers per block

### 22.3.9 ADC10SA, Start Address Register for Data Transfer

15	14	13	12	11	10	9	8
<b>ADC10SAx</b>							
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
<b>ADC10SAx</b>							<b>0</b>
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r0
<b>ADC10SAx</b>	Bits 15-1	ADC10 start address. These bits are the start address for the DTC. A write to register ADC10SA is required to initiate DTC transfers.					
<b>Unused</b>	Bit 0	Unused, Read only. Always read as 0.					