

## Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed), the CPU goes into LPM4 immediately after power-up.

**Table 5. Interrupt Sources, Flags, and Vectors**

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range <sup>(1)</sup>	PORIFG RSTIFG WDTIFG KEYV <sup>(2)</sup>	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG <sup>(2)(3)</sup>	(non)-maskable (non)-maskable (non)-maskable	0FFFCCh	30
Timer1_A3	TA1CCR0 CCIFG <sup>(4)</sup>	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG <sup>(2)(4)</sup>	maskable	0FFF8h	28
Comparator_A+	CAIFG <sup>(4)</sup>	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG <sup>(4)</sup>	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG <sup>(5)(4)</sup>	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG <sup>(2)(5)</sup>	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG <sup>(2)(6)</sup>	maskable	0FFECCh	22
ADC10 (MSP430G2x53 only)	ADC10IFG <sup>(4)</sup>	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7 <sup>(2)(4)</sup>	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7 <sup>(2)(4)</sup>	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See <sup>(7)</sup>			0FFDEh	15
See <sup>(8)</sup>			0FFDEh to 0FFC0h	14 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.

(2) Multiple source flags

(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.

(4) Interrupt flags are located in the module.

(5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.

(6) In UART or SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.

(7) This location is used as bootstrap loader security key (BSLSKEY). A 0xAA55 at this location disables the BSL completely. A zero (0h) disables the erasure of the flash if an invalid password is supplied.

(8) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.