UNIVERSITY OF HARTFORD

COLLEGE OF ENGINEERING, TECHNOLOGY, AND ARCHITECTURE

Design, Simulation, and Implementation of 1 Byte of D-Latch Memory

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Abstract

Memory is a necessary component of any computer system. Random Access memory allows for a processor to randomly read and write data to memory at any given point. This specific design focuses on using data latches in order to perform the function of memory. The design of the memory for this project was done within OrCAD PSpice. The simulation was done using the Allegro AMS Simulator and the PCB design was done using Allegro PCB Designer. After all the design and simulation was completed. The PCB was printed in order for the circuit to be implemented and tested in a real world environment. The finished PCB would be used as a tool to learn how memory works within the confines of a board. There are switches that allow for the eases of use to manipulate the binary value stored in memory. Each switch corresponds to a bit and LEDs show the contents of memory to the user. This project does into depth with the variety of current memory systems, and how they are designed, as well as all the design and thought that went into building the memory for this project.

Introduction

Memory is a crucial part of any computer based system. It is what allows the ability to reference any value and have it used for the processor. Memory in a computer system is sometimes called random access memory. In RAM the memory is able to hold on to a value as it is necessary but once power is reset the value would be cleared. There are ways to avoid this by using more permanent storage solutions, however they are much slower and not meant to be used with the processor. Memory can be made in a variety of ways but the one focused on for this report is the use of D-type latches to create one byte of memory.

D-Latches

In electronics there is a component known as a Gated D-Latch. This component takes an input, usually an enable, and data and with that information will output a Q accordingly. This can be seen in the figure below.

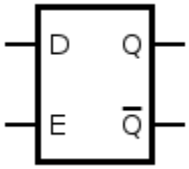

Figure 1. Gated D-Latch [1]

The Q Not is used to define the Boolean not of whatever Q is equal to. Each latch can have a bit of information stored at a time and in order to have one byte it would be necessary to have 8 of these gated latches together to form one byte of memory. In order to make one of these gated latches it is

possible to combine 4 NAND Gates together that would operate the same logically as the D-Latch. This can be seen in the figure below and also that all the necessary inputs and outputs are still present.

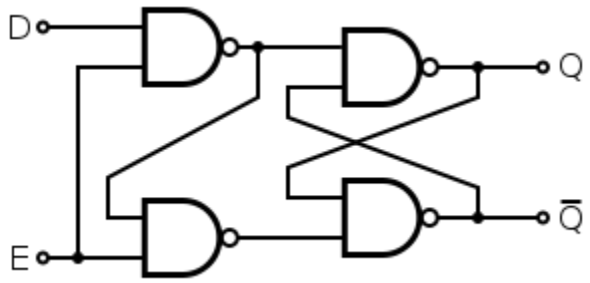

Figure 2. D-Latch from NAND Gates [1]

In order to figure out how this circuit works it is important that the truth table for a NAND gate is known as well as some basic Boolean algebra. First is the truth table for a NAND Gate with only two inputs.

X	Y	*Z*
0	0	***1***
0	1	***1***
1	0	***1***
1	1	***0***

Table 1. NAND Gate Truth Table

This presents that the only time in which a NAND gate will reach logic low is if both of its inputs are high. Using this data as well as looking at the D-Latch circuit, it is possible to see what is happening inside when a signal is applied. For the latch, if the enable pin (E) is high, then whatever is in the data pin (D) will be passed through to the Q and the opposite of it will be placed in Q not. If the enable pin is low, then nothing will be able to change what is in the outputs Q and Q not. This is why the gated D-Latch is able to act as memory, because depending on an enable input and data it is able to remember the value that was put in to it. It is also possible to see now why the D-latch is only able to hold 1 bit of information because the output is only one or zero.

Statement of the Problem

The problem being addressed in this project was the practicality of building a simple memory system that could be interacted with to show the relations of memory in real time. There are many ways to go about solving this problem because of the variety of the types of memory used in today's modern computers. One that stood out was the use of SRAM which is built with intention for being fast, reliable, and easy to access when reading and writing.

Purpose of the Study

The main purpose of this study was to get acquainted with the fundamentals of a memory system that is used in the development of a microprocessor system. There are different types of memory that serve different purposes in the computer based system and the structure that these create form the memory hierarchy on which all computer platforms are built.

Research Questions

One question asked again and again during this study was, what is an efficient way to show memory to the end user? In addition to that, how can the memory be produced without a proper manufacturing plant and a limited time frame? The questions persisted throughout the entire study because the answer is always a variable. There are many ways to design memory and there are many ways in which someone in their own home can build memory as well. The real question is how to put these together than end with a result that is informative and instructive to the end user.

Limitations of the Study

The main limitation when building digital circuits from their respective digital components is the size of the PCB area. Digital logic components typically come in a dual in-line package which takes up a fair amount of room considering how many transistors are on a single chip. This limitation would prove to be the most difficult when designing memory, because memory is supposed to be of a significant amount so that it can store many values. In addition the more memory width available allows for larger binary numbers to be stored and used. Many computers have addresses that can be 32 or 64 bits long which allows for more complex numbers such as floating point values to be read and written.

The other limitation involved in this study is the cost of production. For example, building a circuit that is only 5cm by 5cm is significantly cheaper than one that is 15cm by 15cm. This cost prohibits a lot of the design, because building in more memory directly relates to the cost of the end product. The cost is further increased if the amount of layers on the PCB is increased. In some cases this might actually be worth it, if the resulting product is significantly reduced in size. However, by going this route it may be necessary to use surface mount components as opposed to DIP. Surface components make the production of the product even more challenging to construct when there is no simple way to solder these components to the board. Because this study was not done with any other help, the better solution was to use DIP for all the logic components and build it on a bigger board.

The last significant limitation to the study was time. The time span given was about one full school year, which equates to about 4 months. This proves to be a lot more challenging than originally thought because there are many other factors involved that affect the time to complete such as the manufacturing of the PCB. In addition the time for construction and testing also had to be taken into consideration. Therefore the only way to overcome the time barrier was to start as early as possible in the school year.

Definitions and Terms

DIP: Dual In-Line Package or Dual In-Line Pin Package (DIPP), this is a package type that digital components typically come in. The most common application for these chips is bread boarding because of their ability to slot right in but they can also be used as a through-hole component on a PCB.

Surface Mount: Surface mount components refer to the way in which the component, whether it be digital or analog, connects to the board. In surface mount the pads are expected to be on the top physical layer of the board so that they can be soldered and used.

PCB: Printed Circuit Board, a PCB is the way in which analog and digital devices can be connected. PCBs usually have two layers or more allowing for complex routing between different components. They are used in all the stages of development of a circuit and in addition are significantly cleaner because the "wires" or traces are located on or inside the board. This allows a much simpler layout of components

RAM: Random Access Memory, this term usually refers to the memory that is available to a computer system. RAM allows for data to be read or written to in a random fashion without any sequence. One thing to note about all RAM is that it is volatile, meaning that when it is not powered none of the data is stored within the RAM. Some memory located on the processor itself behaves in the same way that random access memory does but these are typically given other names because of their different purposes such as cache.

SRAM: Static Random Access Memory, static RAM refers to the way that data is accessed on the chip. In SRAM there are cells made up of flip-flops that store a bit of information in each cell. The cells/flip-flops are made up of transistors and this makes them very fast for accessing data.

DRAM: Dynamic Random Access Memory, in this type of memory, bits are stored within a charged or discharged capacitor which refers to a logic high or low. This type of memory took off as the primary way to store large amounts of memory that needed to be randomly accessed because of its cheaper manufacturing and its density of bits. In addition DRAM needs to be refreshed because capacitors will generally leak out some of their charge regardless. This increases the amount of power necessary for DRAM to operate.

Memory Hierarchy: memory hierarchy refers to the way that computer architects look at the memory system of a computer. At the lowest levels are registers and cache that are located on the processor which provides very fast accessing times and at the higher levels is the main memory, where something such as DRAM would be, and the storage memory, such as a hard drive, which isn't used for random access with the processor but rather a place to store data.

Cache: Cache is a type of memory used on the processor chip that allows the data that needs to be immediately accessed, a relative small distance to travel to the processor. It is made up of SRAM because of the speed but the more data that is needed to be accessed means there will need to be more physical chip space dedicated to it. In addition, cache is typically made with levels that way the fastest and most important data is closest to the processor and the other values that are not being needed as much can be located outside of the direct processor area, but still close enough to ensure quick speeds.

PSpice: PSpice refers to the OrCAD suite of applications that make electronic automated design possible. SPICE itself refers to the simulation program with integrated circuit emphasis and it is used to simulate and design the circuit.

Review of the Literature

The biggest thing in memory is that there is a hierarchy of memory that allows a computer to efficiently go through the data at a fast rate. Many early computer architects predicted that the need for high amount of memory available to programmers and users would need to increases significantly over the decades following. Therefore research was done in a hierarchy to provide a better end result. The hierarchy is as follows. At the lowest level is registers on a CPU, these are typically extremely fast memory made from SRAM cells and it allows for very quick access to a value in memory [2]. In addition there are levels of cache, also made from extremely fast memory that is made from SRAM cells, and then there is memory on board the computer system which is made up of DRAM cells to provide the user with fast, yet large enough memory for most applications [2]. Finally is the disk memory which is much slower but used for holding data even when the power is turned off to the system. These memory systems used together make up a fast and reliable hierarchy for which data can travel without affecting the performance of the processor or the performance of the system [2].

Latches have been used in a number of scenarios in the design of computer memory and specifically for storing values of varying size. Static RAM can be made by combining many latches together with a decoder to specify where the byte of memory is supposed to be stored. Static RAM or SRAM is typically used in scenarios where much faster memory is necessary than the density of the amount of data bytes available. This is why it is typically used in the registers of processors. Dynamic RAM or DRAM is slower than the static type and so it is typically reserved for the system wide memory [3]. This project focuses on the design of SRAM by designing and implementing a circuit of D-Latches that would be accessible for the user to interact with to see the change within the circuit.

There are many different ways to store bits of memory in electronic design. Some of the more common ways include using D-Flip-flops as well as SR-Latches [4]. With the design using D-Flip-Flops it is

important to take the timing into consideration. This is because with Flip-Flops instead of using a write enable a clock signal is used to synchronize the reading and writing of memory. One thing to note however that is a flip flop can be made by the same process in which latches are made. This makes them functionally very similar and it is one of the reasons that creating memory is also possible with flip flops just as it is possible with latches. The downside to using a memory module that is synchronized with a clock cycle is the potential of a slower read and write do to the wait time involved [5].

After the consideration of all that was possible, latch memory seemed like the way to go when the only desired outcome for the circuit was to represent what was possible with latch memory. Intel even used latch memory in conjunction with its microprocessors [6].

Early History

Memory in computers was originally taken care of by using relays or even mechanical drums. In these mechanical drums there was a magnetic layer on the outside of the drum and inside were read and write heads that produced a small electronic pulse causing the bits to be recorded in the magnetic layer [7]. These were slow however and only truly used for the storage of the results.

The next method that was introduced in 1947 was the Williams-Kilburn tube. This tube could store data as electrically charged spots on the face of a cathode ray tube [8]. This proved to be very effective at reading and writing because the tube was able to read and write to the spots in any order. Now there was an effective way of storing and accessing data in a random pattern, thus random access memory.

For many years after, the main form of random access memory came in the form of magnetic core memory. Magnetic core memory used lines intersecting each other with magnets on those intersections that at any given time could be written to and accessed [9]. This was a much cheaper and reliable

solution for memory that had to be randomly accesses, especially because of its speed. The fundamentals from this memory system would shape the memory soon to come in solid-state memory systems. Memory core memory started to fade out as integrated circuit based memory surfaced because of manufacturing limits and the cost would soon be too great compared to its alternatives.

Recent Research

The two primary technologies that took over in recent years are static RAM and dynamic RAM. They both have their own purpose in the computing world. Static RAM is the technology that is focused on the most throughout this study because of the architecture of latches being very close to that of the flip-flops that make up static RAM. Static RAM is made up of cells of memory that are made of flip-flops that can each store 1 bit of information and they are still currently some of the fastest available memory today. Dynamic RAM on the other hand uses a transistor in conjunction with a capacitor to store 1 bit. By creating the DRAM in this fashion it is able to have a significant increase in memory density with the tradeoff being the speed.

The main research that is being done in recent years has to do with the improvements in speed and memory density of dynamic RAM. The two primary technologies that differentiate dynamic ram are synchronous and asynchronous. In synchronous memory the data can only be written or read on a system clock cycle where as in asynchronous memory the data can be accessed at any point during the clock cycle [10]. Some of the first DRAM that saw wide application and use was single data rate RAM. This ram was able to transfer 16 bits of data per clock cycle and it was used in a variety of computer systems within the 1990s [10].

The next progress was made with the double data rate SDRAM which would allow the 16 bits of data to transfer on the positive as well as the negative edge of the clock cycle. These double data rate memory modules would soon become even more popular as the standard improved with DDR2 and DDR3 memory. Both of these standards looked for ways to reduce energy consumption and increased speeds while decreasing latency. The obvious benefit is that as time goes on the size of the transistor manufacturing made it much easier to improve the memory density. DDR4 was released in recent years and its primary benefit over those before it was the size available of each module and a higher data transfer speed. However, not all computers and platforms have the ability to run the newer RAM due to incompatibility with older hardware.

Method

The design of this circuit started as an idea to build fully functional RAM that able to be interacted with. After much research, the best way and most efficient way to have a similar feel for the RAM was using the D-latch as the memory storage and switches to interact with each of the data pins on the chips. In addition, LEDs would be used to display the state of each of the bits which would make for a much better interactive experience rather than probing each of the pins with an oscilloscope or multimeter. With the idea of the design the first step was to create the circuit in PSpice. Once it was completed then the circuit could be thoroughly tested to ensure that's its operation was as expected and correct. After this was verified, the PCB design could be started as well as the purchase of components. Finally all the components would be assembled and soldered to the PCB to test the circuit to ensure its operation matched those in the simulation process.

Materials and Procedures Examinations

The materials necessary to complete the implementation of the circuit were as follows. 8 74HC00 DIP14 chips, these would be used to construct each of the data latches for each bit. 8 LEDs, which would be used to display the memory contents to the user. A custom PCB, which would allow the circuit to be fully implemented and connect to power. Then are the switches which are DIP switches, these would be used for manipulation of writing to the bits as well as powering the system and the write enable.

The circuit was first constructed in OrCAD PSpice so that it could be simulated with the other tools available in the OrCAD suite of applications. Once the circuit was constructed an analog and digital simulation were both performed to ensure the correct operation.

After the circuit was tested it would be designed in Allegro PCB Designer which cooperates nicely with OrCAD PSpice to allow a 2 layer PCB to be designed. In the PCB designer there were many challenges to overcome, because the design connected many different gates together and digital logic chips come with many gates per package meaning the direct net listing could not be used without modifications.

In PCB designer the footprints needed would be for all of the components that would eventually be soldered onto the printed circuit board. For the Quad 2 input NAND gates on the 74HC00, a footprint of DIP14 was used and for the 3 DIP switches, a footprint of DIP8 was used. Last were the LEDs which each needed their own footprint close enough to the 74HC00 to show to the user each of the bits that were stored on the corresponding logic.

The PCB was two layers with through-hole components. Each component slotted into the board and then needed to be soldered from the back to make the connections final. In addition sockets could have been used for all of the logic components as a way of simplifying the replacement of them because only the socket would need to be soldered on and then the logic could be replaced as necessary.

Once the board was built, it could be tested with a variety of circumstances or even the same ones that were used during simulation to make sure that it operated as expected and that the project was complete.

Results

The schematic that was used for the simulation is shown below. The only difference is that one of schematics was used for analog and the other for digital simulations.

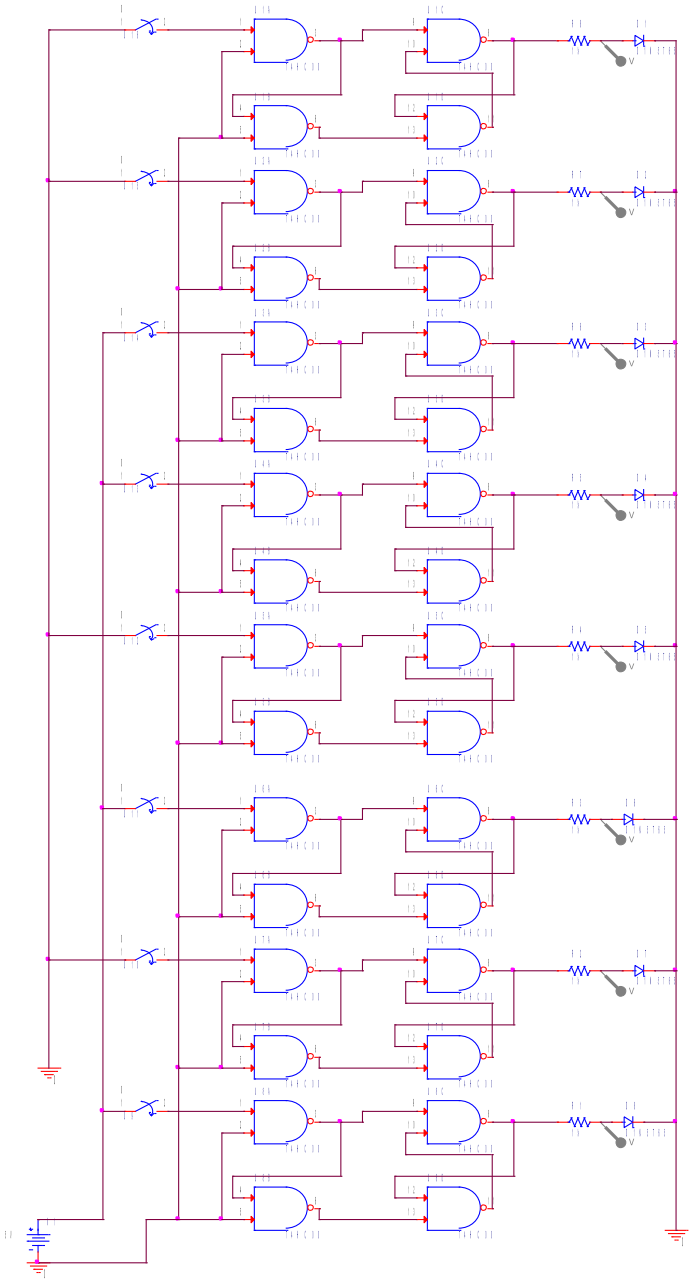

Figure 3. Schematic for Analog Simulations

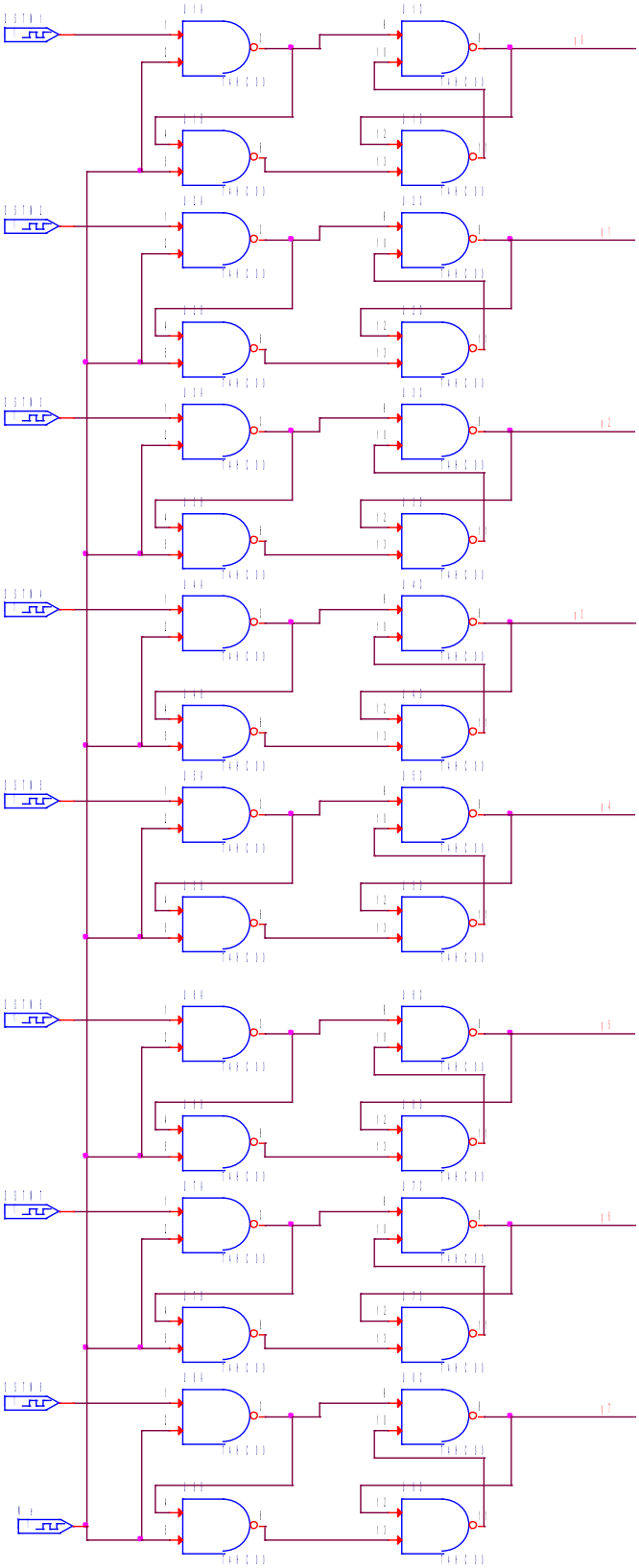

Figure 4. Schematic for Digital Simulations

Part I Simulation

Analog Simulation

For the analog simulations, the gates were tested with 5V, as the input to represent a logic high, and each latch was tested with and without the write enable pin enabled. In addition a combination of switches being set to open and others to close would allow for a binary number to be represented by the logic.

With the write enable bin disabled, all of the results should be a logic 0.

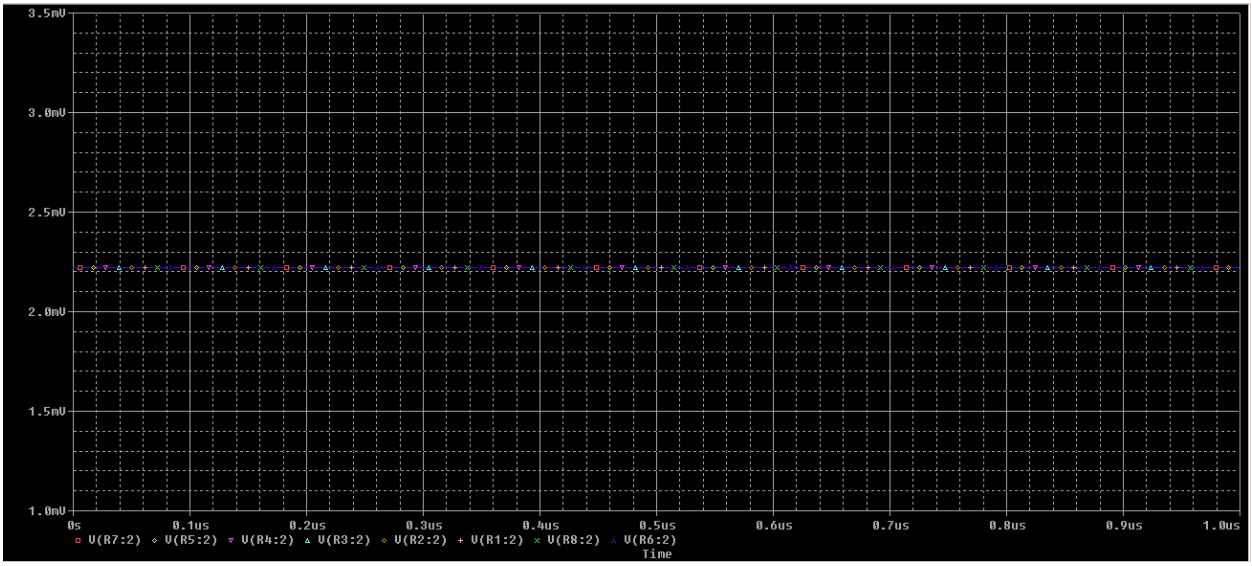

Figure 5. Analog Sim; Write is off; All logic 0

In figure 5 it is easy to see that when the write enable pin is low, all the voltages at the output of the logic is 2.2218mV which is the same as a logic 0.

Next was a simulation with some of the gates set to be high with the write enable and other set to be low.

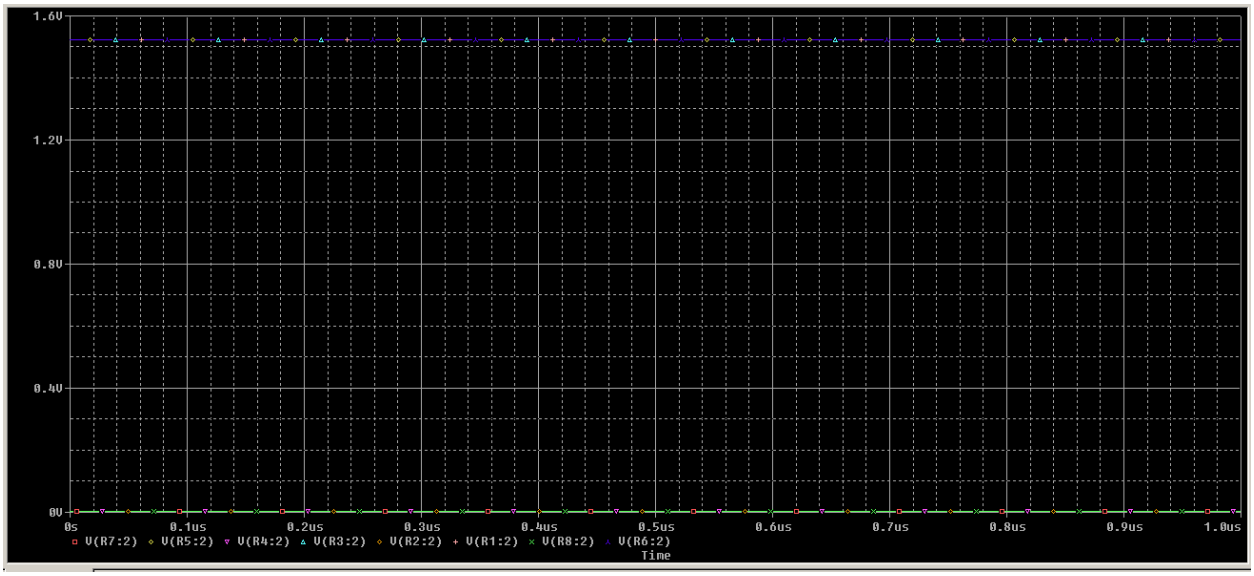

Figure 6. Analog Sim; Some Gates High others Low; With Write enabled

In figure 6, it is possible to see that some of the gates are high and others are low but it is hard to differentiate between them. This is why digital simulation would prove to be much more useful while also allowing a greater variety in results that could be seen and tested.

Digital Simulation

To start with digital simulation the first thing that needed to be done was to remove all of the analog components and replace them. For the switches that controlled the write enable and the data pins, a digital stimulus would be used because they are programmable with commands for a given time segment. This would allow for a much better and thorough simulation. The outputs were all labeled so that they could be easily recognized after the simulations were done. This can be seen in figure 4 above.

The biggest benefit to using a digital simulation is that it would allow for multiple different configurations to be tested in one simulation. This is mostly because time and the write enable are the

main thing that were being tested. Everything else was an output in relation to what the state of the write enable was. Below is the commands that were given to each of the possible inputs.

COMMAND1	0s 0	0s 0	0s 0	0s 0	0s 0	0s 0	0s 0	0s 0	0s 0
COMMAND2	1ms 1	1ms 1	1ms 1	1ms 1	1ms 1	1ms 0	1ms 0	1ms 0	1ms 1
COMMAND3	2ms 1	2ms 0	2ms 1	2ms 0	2ms 0	2ms 1	2ms 1	2ms 0	2ms 0
COMMAND4	3ms 1	3ms 1	3ms 1	3ms 1	3ms 1	3ms 1	3ms 1	3ms 1	3ms 1
COMMAND5	4ms 1	4ms 0	4ms 0	4ms 0	4ms 0	4ms 0	4ms 0	4ms 0	4ms 1
COMMAND6	5ms 1	5ms 1	5ms 1	5ms 1	5ms 0	5ms 1	5ms 0	5ms 1	5ms 0
COMMAND7	6ms 0	6ms 1	6ms 1	6ms 1	6ms 1	6ms 1	6ms 1	6ms 1	6ms 1
COMMAND8	7ms 0	7ms 1	7ms 1	7ms 1	7ms 1	7ms 1	7ms 1	7ms 1	7ms 1
COMMAND9	8ms 1	8ms 1	8ms 0	8ms 1	8ms 0	8ms 1	8ms 0	8ms 1	8ms 1
COMMAND10	9ms 1	9ms 0	9ms 0	9ms 0	9ms 0	9ms 0	9ms 0	9ms 0	9ms 1
COMMAND11	10ms 1	10ms 1	10ms 1	10ms 0	10ms 0	10ms 1	10ms 1	10ms 0	10ms 1
Reference	We	DSTM8	DSTM7	DSTM6	DSTM5	DSTM4	DSTM3	DSTM2	DSTM1

Table 2. Commands for every Digital Stimulus

This command table makes it very easy to see what the logic inputs would be for all of the possible inputs. It would also allow a comparison between the actual results obtained during simulation and the expected results. Therefore, the expected inputs should give the expected outputs as shown below in table 3.

Time	We	p7	p6	p5	p4	p3	p2	p1	p0	{p[7:0]}
0s	**0**	0	0	0	0	0	0	0	0	**XX**
1ms	**1**	1	1	1	1	0	0	0	1	**F1**
2ms	**1**	0	1	0	0	1	1	0	0	**4C**
3ms	**1**	1	1	1	1	1	1	1	1	**FF**
4ms	**1**	0	0	0	0	0	0	0	1	**01**
5ms	**1**	1	1	1	0	1	0	1	0	**EA**
6ms	**0**	1	1	1	0	1	0	1	0	**EA**
7ms	**0**	1	1	1	0	1	0	1	0	**EA**
8ms	**1**	1	0	1	0	1	0	1	1	**AB**
9ms	**1**	0	0	0	0	0	0	0	1	**01**
10ms	**1**	1	1	0	0	1	1	0	1	**CD**

Table 3. Expected Output based on Input Commands

The first thing that was done when the simulation was run, was to make sure that all the inputs were what they were supposed to be. By adding each digital stimulus manually to the simulator it was possible to see all the waveforms, however this still proved to be harder to keep track of so additionally a bus was made out of all the digital stimuli. This can be seen in the figure below.

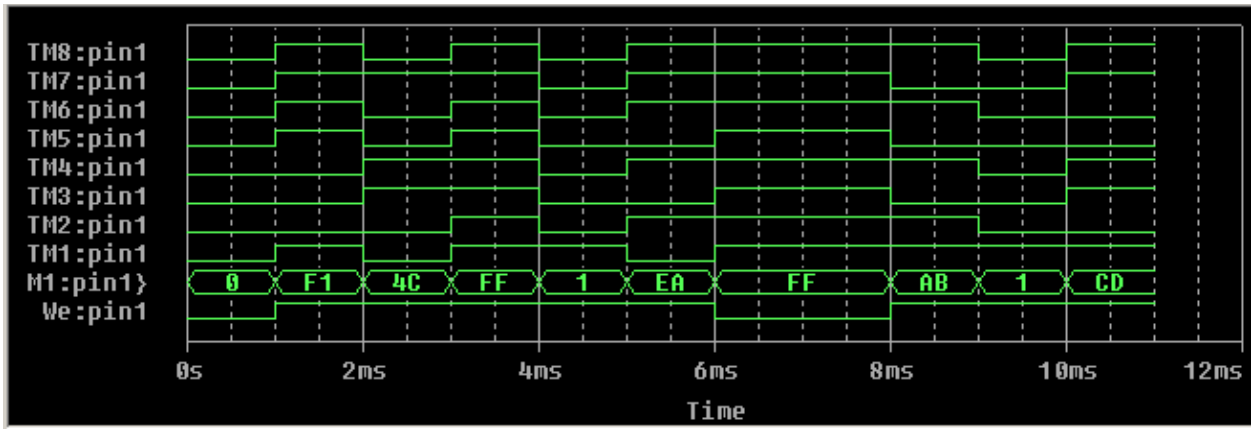

Figure 7. Inputs of all the Digital Stimuli

This was a much nicer simulation and it's easy to see where the write enable is set to low. In the time span from 6ms to 8ms the result is what it was set to at the end of the clock cycle. Once it was known that the inputs all worked correctly than the output could be simulated and compared against the table 3 which were the expected outputs from these given inputs. Below shows the results of the output.

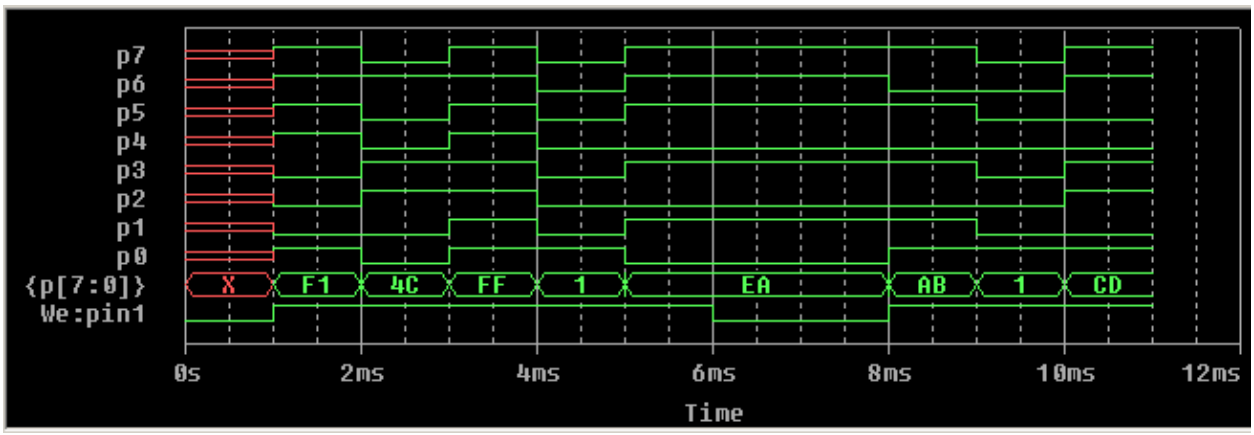

Figure 8. Outputs from given Inputs

The simulation done in figure 8 is configured in the same way that figure 7 was done, as in all the individual outputs are shown first and then there is a bus containing all of the outputs to show the value as hexadecimal and therefore much easier to read. Comparing these results with the expected results, shows that everything is working as expected and all the outputs display what the given input was when the write enable is high. And in addition, the outputs stay at their value when the enable is switched to low.

Part II Testing

To be tested the first thing that would need to be done is the design of the printed circuit board. This was all done in Allegro PCB designer. Figure 9 shows the finalized PCB that was sent off for printing.

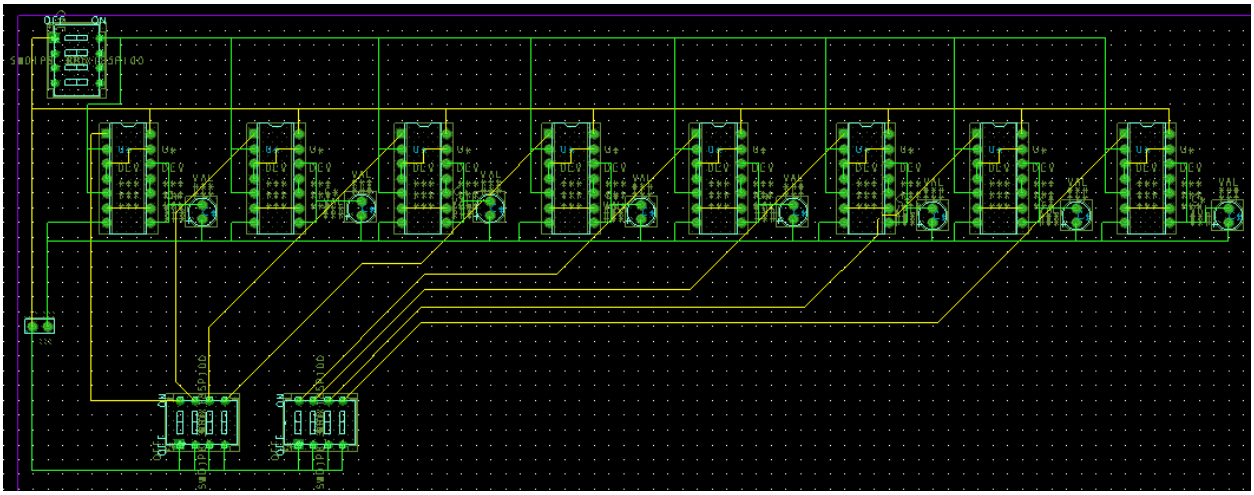

Figure 9. Finalized PCB Design

The files containing all the layers were all sent off to *Advanced Circuits* to be produced. The final dimensions were 3.9x8.9 in. The board showed up in about 2 weeks and is shown in figure 10 below. Three were ordered as that was the minimum but it would also allow a board to be swapped out if necessary.

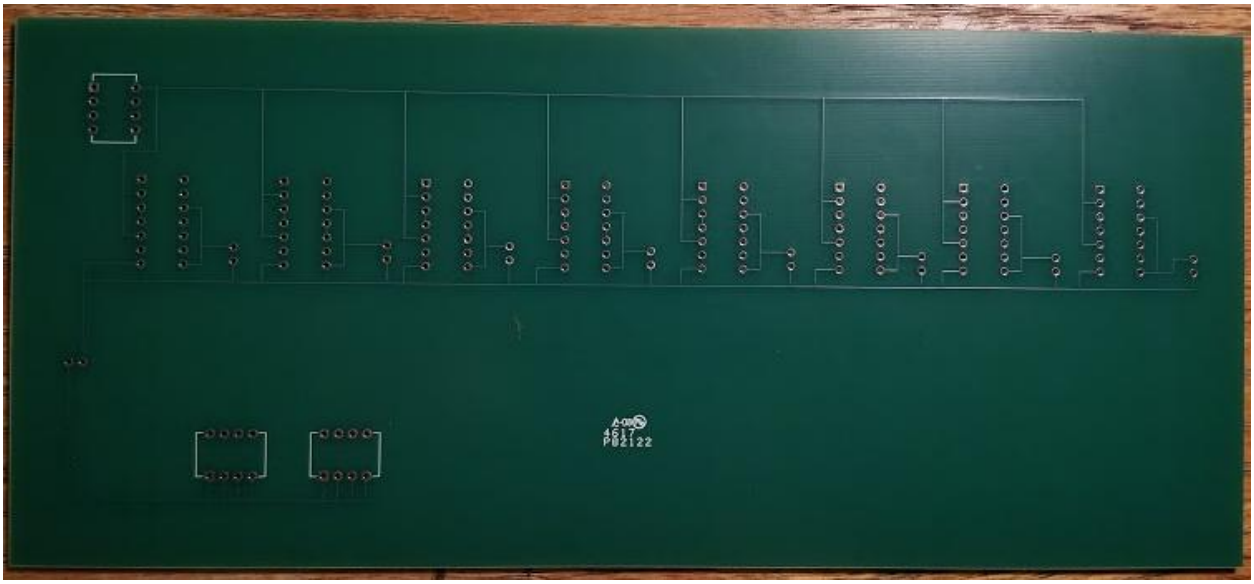

Figure 10. Unpopulated PCB from Advanced Circuits

Now that the PCB was in and the parts, from Digi-Key, were also in. It was time to construct the circuit and test it. The fully assembled board below shows all the components and to connect them each pin was soldered by hand on the back of the board while the components would face outward toward the user.

Figure 11. Fully Constructed PCB

Testing on the board was done by connecting it first to a 5V supply from a variable bench power supply. Then the DIP switch at the top left of the board would be used to control the write enable and the DIP switches at the bottom would be the data in pins. The only picture I have during the testing stage is one where all the first 4 latches are set to 0 and the next 4 are set to 1. Many more combinations were tested and compared against the expected to make sure that the board was operational and that there were no dead components or bad solder joints.

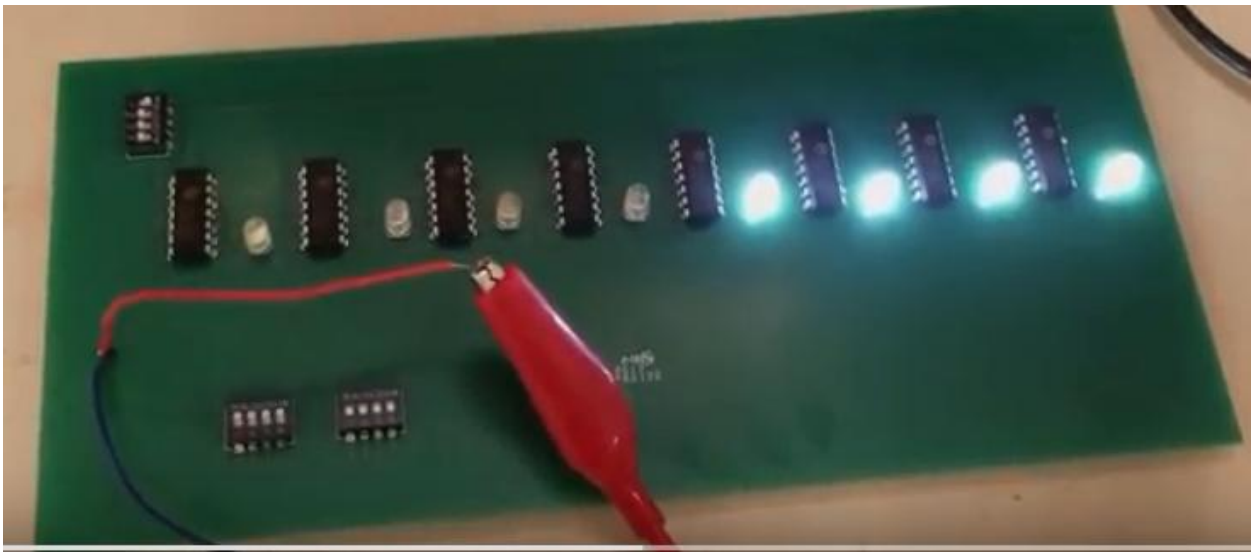

Figure 12. Functioning PCB with 0F shown after write

Part III Comparison

The board was easy to compare to the simulation because of the way that it output results to the user. All that was done during the comparison was checking to make sure that when the write enable was off, that no changes would be made to the memory's state and when write enable was on, that the data was being written as expected. All the outputs would be shown nicely on the LED's making it easy to see what the result was as compared to the inputs.

One thing that was unexpected yet important to mention was the usability of the DIP switches. Although they provided a great way to switch on and off the data as necessary to the board, they also presented a problem if they were not fully switched off or on. This made the testing a bit harder but still the results were the same in the end.

Future Work

This project was very informative and instructive about teaching me all the basis of knowledge of memory systems and how they are designed and constructed. There is a lot in the future that I would do to further improve this work as well as expand the knowledge learned into an even bigger and better project.

To improve this current project the first thing that I would change would be the use of the DIP switches. Although they were convenient and a footprint was available for them off of the Digi-Key website it is clear that they are not meant for constant switching. In addition to this, there was also plenty of room on the board to allow for larger switches and it would make more sense for the switch to be right in front of the bit that it was changing. Also to improve this current design, I would try to make the PCB more compact just to have the cost lowered. This could mean potentially using more layers for the board which would also increase the price but the overall design would end up better because of it. Lastly to improve the current design would just be to add sockets for all of the logic components that way if any one of them died it would be very easy to replace.

For a future project the biggest thing that I would want to accomplish would be to build fully functioning RAM as in much more memory and multiplexers to access the memory. In addition surface mount logic could be used to further increase the memory density as well as offer up the other side of the board for

even more memory. This would be a much more complex design but then it could also be potentially used by microcontrollers or even some microprocessors.

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Appendices

Appendix A: 74HC00 Datasheet

74HC00; 74HCT00

Quad 2-input NAND gate

Rev. 7 — 25 November 2015 **Product data sheet**

1. General description

The 74HC00; 74HCT00 is a quad 2-input NAND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels:
  - For 74HC00: CMOS level
  - For 74HCT00: TTL level
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC00D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT00D				
74HC00DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT00DB				
74HC00PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT00PW				
74HC00BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT00BQ				

4. Functional diagram

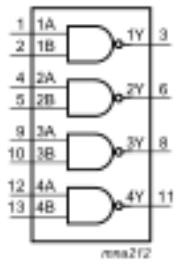


Fig 1. Logic symbol

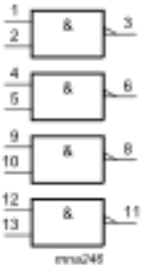


Fig 2. IEC logic symbol

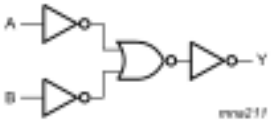


Fig 3. Logic diagram (one gate)

5. Pinning information

5.1 Pinning

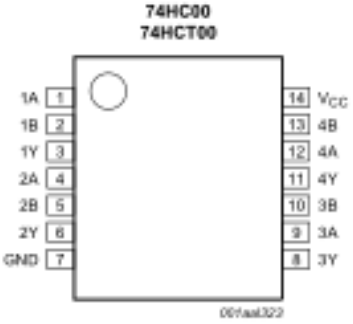
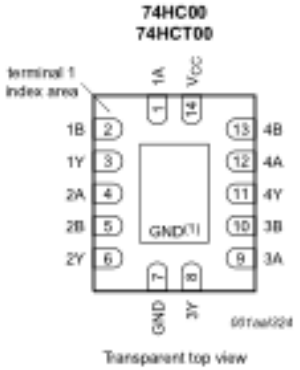


Fig 4. Pin configuration SO14 and (T)SSOP14



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10, 13	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input		Output
nA	nB	nY
L	X	H
X	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V [1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		−50	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	[2]			
	SO14, (T)SSOP14 and DHVQFN14 packages		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC00			74HCT00			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

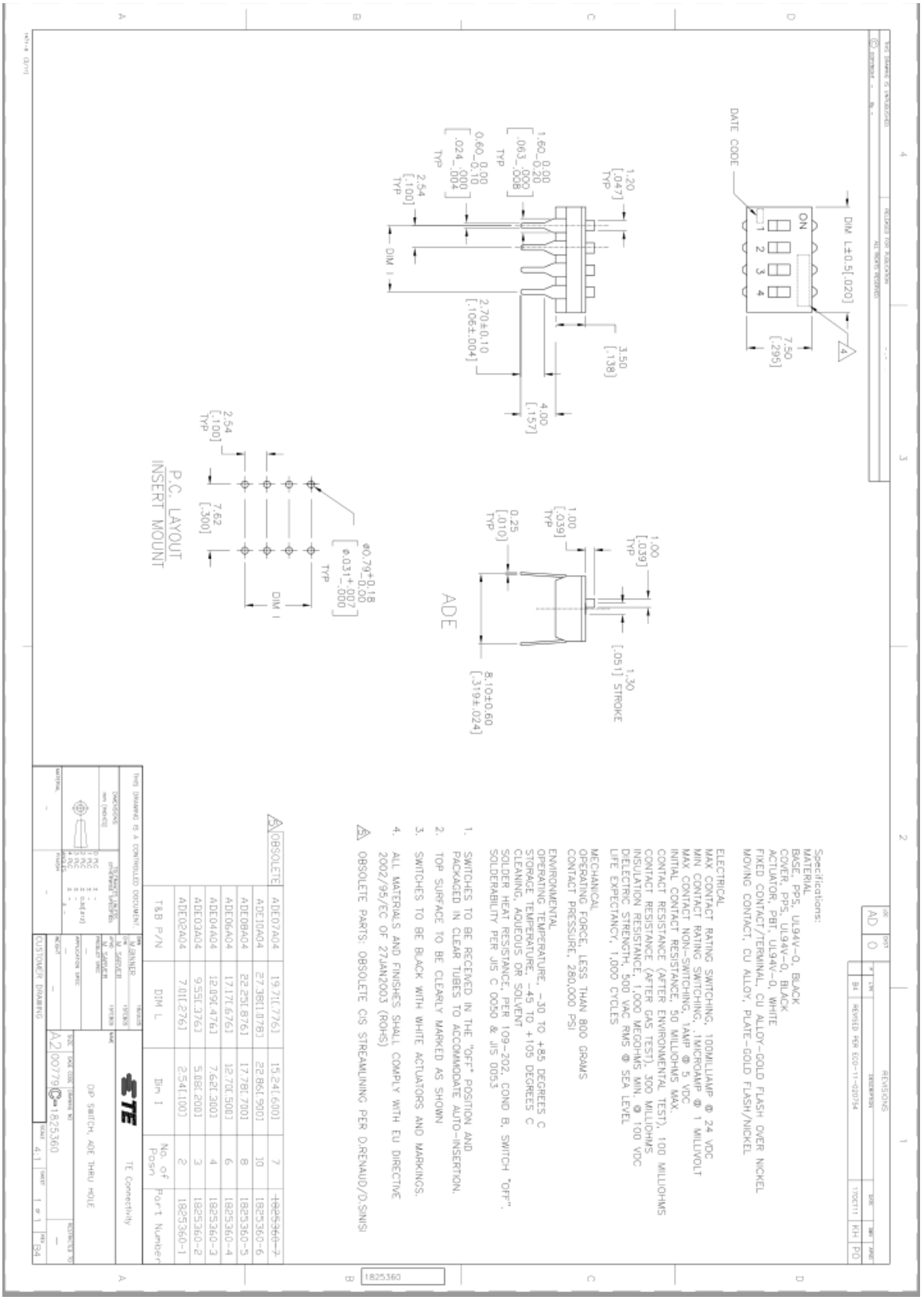
9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC00										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	-	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	-	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	-	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	-	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	-	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	-	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = −20 μA; V_{CC} = 2.0 V	-	2.0	-	1.9	-	1.9	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	-	4.5	-	4.4	-	4.4	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	-	6.0	-	5.9	-	5.9	-	V
		I_O = −4.0 mA; V_{CC} = 4.5 V	-	4.32	-	3.84	-	3.7	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	-	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	-	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	-	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	-	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	-	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	-	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	-	-	±1	-	±1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	-	-	20	-	40	μA

Appendix B: DIP Switch Drawing



Appendix C: LED Datasheet

Data Sheet

Through Hole Lamp
LTW-2S3D8

Through Hole Lamp

LTW-2S3D8

Rev	Description	By	Date
Above data for PD and Customer tracking only			
-	Create new data sheet	Javy H.	02/13/2008
A	Update DS	Leo KC C.	09/21/2012
B	Update VF bins	Makha K.	04/06/2015
C	Paper correction on IV spec	Craig P.	03/30/2016
D	Update Vf bin as PCN	Norah	09/22/2017

Through Hole Lamp
LTW-2S3D8

1. Description

Through-hole white LEDs are offered in a variety of packages such as 3mm, 4mm, 5mm, rectangular and cylinder which are suitable for all applications requiring status indication. Several intensity and viewing angle choices are available in each package for design flexibility.

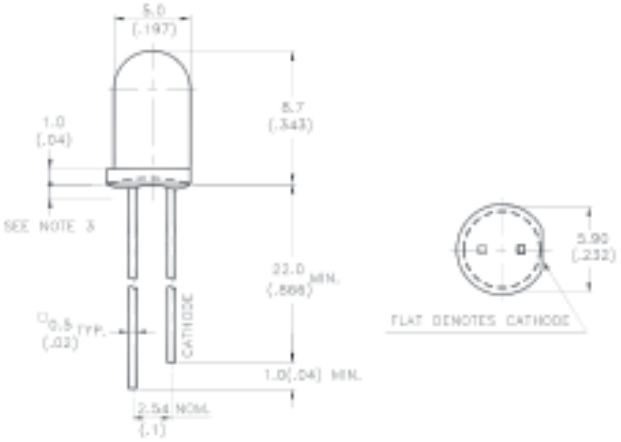
1. 1. Features

- Lead (Pb) free product - RoHS compliant
- Low power consumption & High efficiency.
- High efficiency & reliability.
- Versatile mounting on p.c. board or panel.
- I.C. compatible/low current requirement.
- Popular T-1 3/4 diameter. InGaN White & Water Clear lens

1.2. Applications

- Computer
- Communication
- Consumer
- Home appliance
- Industrial

2. Outline Dimensions



Notes :

1. All dimensions are in millimeters (inches).
2. Tolerance is ±0.25mm (.010") unless otherwise noted.
3. Protruded resin under flange is 1.0mm (.04") max.
4. Lead spacing is measured where the leads emerge from the package.
5. Specifications are subject to change without notice.

3. Absolute Maximum Ratings at TA=25℃

Parameter	Maximum Rating	Unit
Power Dissipation	93	mW
Peak Forward Current (Duty Cycle≤1/10, Pulse Width≤10ms)	100	mA
DC Forward Current	30	mA
Derating Linear From 30℃	0.45	mA/℃
Operating Temperature Range	-40℃ to + 85℃	
Storage Temperature Range	-40℃ to + 100℃	
Lead Soldering Temperature [2.0mm (.079") From Body]	260℃ for 5 Seconds Max.	

4. Electrical / Optical Characteristics at TA=25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Luminous Intensity	Iv	13000	23000	29000	mcd	IF = 20mA Note 1,3,4
Viewing Angle	2θ1/2		15		deg	Note 2 (Fig.6)
Chromaticity Coordinates	x		0.30		nm	IF = 20mA, Note 5 Hue Spec. Table & Chromaticity Diagram
	y		0.30		nm	
Forward Voltage	VF	2.5	2.8	3.1	V	IF = 20mA
Reverse Current	IR			10	μA	VR = 5V

NOTE:

1. Luminous intensity is measured with a light sensor and filter combination that approximates the CIE eye-response curve.
2. θ1/2 is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
3. Iv classification code is marked on each packing bag.
4. The Iv guarantee must be included with ±15% testing tolerance.
5. The chromaticity coordinates (x, y) is derived from the 1931 CIE chromaticity diagram..
6. Reverse voltage (VR) condition is applied for IR test only. The device is not designed for reverse operation.