Mechtron 3TB4: Embedded Systems Design II
Tutorial Lab 1

Introduction to Quartus Prime and DE1-SoC

Reports Due: On Avenue, by 11:59PM of the day of your lab sessions next week (along with the pre-lab report)

Goals

- Introduce the Quartus Prime software
- Learn how to describe simple circuitry in Verilog HDL
  Note: **The following documents may help you with your lab. Please go over them at your convenience, in addition to the class notes.**
- Introduction to the software
  Go to ALTERA's web site at:
  https://www.altera.com/products/design-software/fpga-design/quartus-prime/overview.html
- After you install the software (see"Activities" below) you may find more help topics under the "`Help`" menu.
- You may also wish to consult http://www.asic-world.com/verilog/index.html for lessons and references on Verilog HDL.

Remote Lab Procedure

Note: Ensure you connect to the VPN before starting Quartus Prime, otherwise compilation will not be available.

For this and every lab: Lab/Tutorial periods will be hosted online through Teams. Each lab begins with TAs giving announcements, after which you may work with your partner. Your TAs will periodically check in with you.

As this is the first lab/tutorial, your TA's will be ensuring the technology is working. To 'join' your lab, start Microsoft Teams and select 'Teams' on the left toolbar. Click on the MT 3TB4 team for your lab section. Once your TA starts the meeting, you will be able to join by clicking 'Join meeting' in the chat. You do not need a webcam and you can mute yourself unless you wish to talk. You may send text messages by selecting the message icon at the bottom of the screen.

Once the TA is done giving announcements, leave the channel and click 'Lab Group n' and click 'Meet Now' (The video camera icon below the chat). Check that both you and your partner's 'voice chat' and 'screenshare' features are working. Your TA will check in with each group to verify this and will help you troubleshoot any issues.

Voice Chat help

1. If you can't hear your partner:

a) Turn up your volume

b) Select the correct output device (For Windows 10: https://support.microsoft.com/en-us/office/manage-your-call-settings-in-teams-456cb611-3477-496f-b31a-6ab752a7595f)

c) Unmute your partner through Teams

2. If your partner can't hear you:

i) Select the correct input device (For Windows 10: Win+I\System\Sound\Input\"Choose your input device drop down menu")

ii) Unmute yourself through Teams

iii) Increase your microphone's volume (For Windows 10: Go to Control Panel\Sound\Recording. Select your input device and click 'Properties'. Choose the 'Levels' tab and increase 'Microphone Boost' to the maximum)

Screenshare help

1. To begin screensharing hover your mouse over the Teams app to show the bottom toolbar
2. Select the 'Share' icon (Box with upwards pointing arrow)
3. Choose the screen you want to share - it could be a PDF, Quartus Prime, a browser, etc. Keep in mind that ONLY the screen you selected will be shared, even if you're using another application
4. To share a different screen select the 'Stop Sharing' icon (Box with an X), then repeat the previous steps.

Lab Equipment and Software

In this tutorial you will be introduced to the new development board that we will use for future labs. Altera's DE1-SoC development board is built around an FPGA device that can be programmed to implement arbitrary logic circuits. The FPGA is connected to many on-board peripherals, as shown in Figure **??**.

Peripheral connections

This device contains many peripherals that can be used with the FPGA. The file `DE1-SoC.qsf` provides a pin-map to connect the FPGA's output ports to the surrounding peripherals. For this lab, you will be required to use the DE1-SoC pin assignments to interface with the peripherals of the DE1-SoC development board.

Cyclone V FPGA

The Cyclone V FPGA will be used to implement the hardware logic.

Software Environment

The software environment consists of the Quartus Prime CAD tool.

As a part of your preparation, you will complete a tutorial that will introduce you to the Quartus Prime user interface.

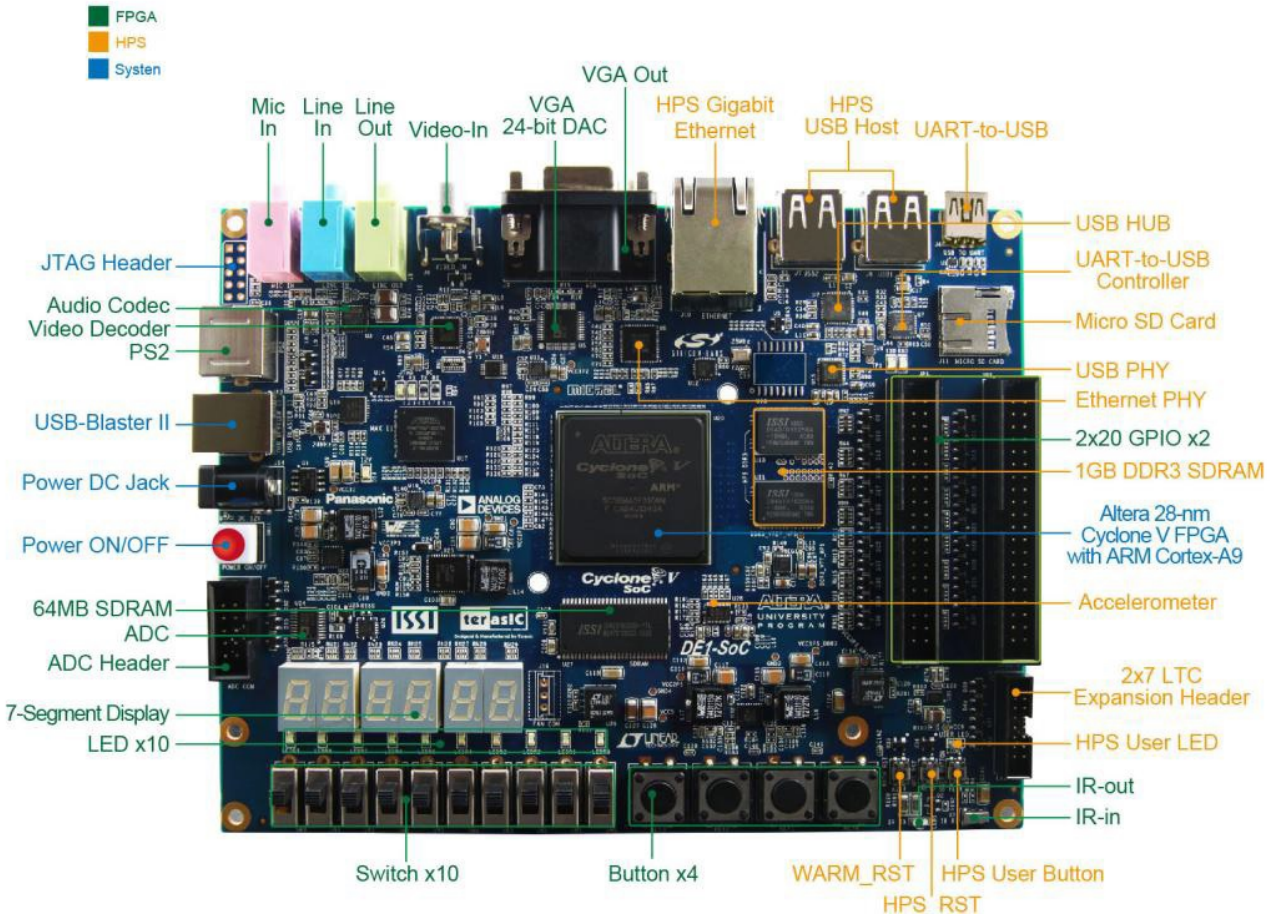

Figure 1: Altera DE1-SoC Board

Activities

Pre-tutorial

The following activities must be completed by each student **independently** before attending this tutorial.

1. Install either the Standard Edition or the Lite Edition of Quartus Prime on your personal computer, available from Altera's website (https://www.altera.com/downloads/download-center.html).

   It is recommended to download and install version 17.1, since this is the version that is installed on our lab computers. Quartus Prime Lite Edition is a free version. If you install the Standard Edition,

you need to set up the license. To do so, click `Tools | License Setup...` from Quartus, input "`27000@alteralm.mcmaster.ca`" (without quotation marks) in the "`License File`" box. You will need a VPN connection to use the license file.

You need to download 1) Quartus Prime (includes Nios II EDS). 2) ModelSim-Intel FPGA Edition (includes Starter Edition). 3) Cyclone V device support.

2. The FAQ for SE2DA4 at http://www.cas.mcmaster.ca/~leduc/FAQ.html contains some useful information about the DE1-SoC board. This FAQ also provides details for setting up the license and some instructions for programming the board and simulating a project. Reading this FAQ should help you with your labs.
3. Complete the tutorial "`Quartus Prime Introduction Using Verilog Designs`" available on the course web page.

In the Lab

In the lab you need to work in groups. Using one of the computers in the lab, create a new Quartus project, as you learned in the "`Quartus Prime Introduction Using Verilog Designs`" tutorial.

1. Connect the DE1-SoC board to its power supply.
2. Follow Section 7 of the tutorial for pin assignment. **Alternatively**, you can import pin assignments from the `DE1-SoC.qsf` file provided on the course web page. To assign pins by importing the file `DE1-SoC.qsf`, you need to use the DE1-SoC peripheral names as in the file `DE1-SoC.qsf`. In the pin assignment file `DE1-SoC.qsf`, the pins are assigned by sentences like: "`set_location_assignment PIN_AB12 -to SW[0]`". In this sentence, the pin is "**PIN_AB12**", the peripheral name is "**SW[0]**", which is the first toggle switch on the DE1-SoC board.
3. **Before compiling, make sure that all unused pins are reserved as "Input tri-stated"**. This option is available under `Assignments | Device` > `Device and Pin Options` > `Unused Pins`.
4. Complete Sections 8 and 10 of the `Quartus Prime Introduction Using Verilog Designs` tutorial.
5. Submit your compiled circuit (the .sof file located in `project_name\output_files`) to the Avenue dropbox and request a demo from your TA. Take a screenshot of the compilation report for inclusion in your report.
6. Use functional simulation to verify the intended function of the circuit.

Note: The steps in this document: `DE1_SoC_Quartus17_Simulation_Notes.pdf` need to be completed before simulating

Note: For Quartus Prime version 17.1, timing simulations are not supported for the Cyclone V FPGA. For a project that is set up for Cyclone V, the result of running a timing simulation will be identical to the functional simulation.

7. Complete the tutorial "Introduction to Simulation of Verilog Designs" available on the course web page.

   Please Note: In some situations, some nodes may be "synthesized away" during the synthesis and analysis process, as a result it is not possible to observe these nodes during simulation or the signal probing process. Verilog HDL provides some synthesis attributes to direct Analysis & Synthesis to keep them intact. These attributes include "/*synthesis keep */", "/*synthesis preserve */" and "/*synthesis noprune */". For more details about these three synthesis attributes, please read the appropriate Quartus help files or other materials available on the web.

   With Quartus version 17.1 and the Modelsim-Altera simulator, the above mentioned synthesis attributes and directives appear to not work well. To correctly simulate some nets or regs in your modules that would be "synthesized away", please temporarily declare them as output ports. In this lab project, there is no node that will be "synthesized away", but it may happen with your later lab projects.

8. Show the result of your simulation through Teams to one of the TAs and take screenshots for your report.

Report

Describe what you did in this tutorial, and include the screen shots taken during various experiments. You are also required to submit the pre-lab report as described in the Lab 1 document. This material must be submitted to Avenue 1 minute prior to the start of Lab 1.