Lab 4 Prelab: ON/OFF Button

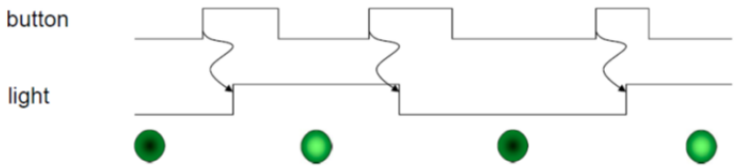
(2 hours)

Goal

To learn how to implement an ON/OFF Button.

Procedure

Implement the ON/OFF Button learnt in class with the following function diagram (see slides of lecture 4).



1) Test whether the following code can have the correct results.

```
module onoff(input button, output reg light);
  always @(posedge button) light <= ~light;
endmodule
```

2) Write the correct Verilog module and implement it in the board.

```
module onoff_sync(input clk, reset, button_in,
                  output reg light);
  // synchronizer
  reg button,btemp;
  always @(posedge clk)
    {button,btemp} <= {btemp,button_in};

  // debounce push button
  wire bpressed;
  debounce db1(.clock(clk),.reset(reset),
               .bouncey(button),.steady(bpressed));

  reg old_bpressed;  // state last clk cycle
  always @ (posedge clk) begin
    if (reset)
      begin light <= 0; old_bpressed <= 0; end
    else if (old_bpressed==0 && bpressed==1)
      // button changed from 0 to 1
      light <= ~light;
    old_bpressed <= bpressed;
  end
endmodule
```

3) There are three processing sub-circuits in the module. Try remove part of them and test wither the results are correct.