

Information Documentaire / Document Information

Titre / Title : BUS ELECTRICAL DESIGN INTERFACES ENVIRONMENT REQUIREM*Auteur / Author :* ALLAUD CHRISTOPHE*Reference :* ABU-JPT-SP-563 Vged=3

Electronic Signature

Page laissée blanche intentionnellement

Page left intentionally blank

DOCUMENT DISTRIBUTION

From: C. ALLAUD

Project Name: ALPHABUS
Title: @BUS ELECTRICAL DESIGN, INTERFACES & ENVIRONMENT REQUIREMENTS

Issue: 03
Reference : ABU-JPT-SP-563
Date: 17/09/04
Pages Number: 214
File: Electrical_GDIE.doc
Classification: **ALPHABUS CONFIDENTIAL RESTRICTIVE USE**
PT Code: 100 000
Contract: 02CNES028800-DSO200
Emitting Entity: JPT
DOORS baseline



**@BUS ELECTRICAL DESIGN, INTERFACES &
ENVIRONMENT REQUIREMENTS**

Written by	Responsibility-Company
C. Allaud	@Bus Electrical Architect
Verified by	
P. Bertheux	Technical Manager Alphasbus
Approved by	
M. Ritoux	System engineer Alphasbus
P. Bertheux	Technical Manager Alphasbus
Release by	
B. MAUREAU	Chef de Projet ALCATEL @BUS
D. PAWLAK	Chef de Projet ASTRIUM @BUS

DOORS baseline

PT Code : 100 000

Emitting entity : JPT
(original holding)

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

CHANGE RECORDS

ISSUE	DATE	§ : CHANGE RECORD	AUTHOR
01	11/12/03	First issue	C. ALLAUD
02	12/12/03	False issue	C. ALLAUD
03	17/09/04	Update to take new industrial agreement into account	C. ALLAUD

REQUIREMENT HISTORY

TABLE OF CONTENTS

1. SCOPE OF THE DOCUMENT.....	5
1.1 INTRODUCTION	5
1.2 GENERAL DEFINITION	5
2. DOCUMENTATION & TERMINOLOGY	6
2.1 INPUT DOCUMENTS	6
2.2 REFERENCE DOCUMENTS	6
2.3 APPLICABLE DOCUMENTS	6
2.4 TERMINOLOGY & ABBREVIATIONS	7
3. GENERAL REQUIREMENTS	8
3.1 ENGINEERING STANDARDS-UNITS	8
3.2 EQUIPMENT INTERFACE CONTROL	8
3.3 DEFINITION	8
3.3.1 Command.....	8
3.3.2 Electrical Ground Reference Plane	9
3.3.3 Bus Users.....	9
4. ELECTRICAL DESIGN AND INTERFACES SPECIFICATIONS.....	10
4.1 COMMANDABILITY AND OBSERVABILITY	10
4.1.1 Commandability	10
4.1.2 Observability.....	11
5. ELECTRICAL DESIGN AND INTERFACES REQUIREMENTS.....	14
5.1 ELECTRICAL DESIGN REQUIREMENTS	14
5.1.1 Electrical Grounding	14
5.1.2 Electrical Connectors.....	25
5.1.3 Magnetic Requirements.....	35
5.1.4 Double Insulation requirements	35
5.2 ELECTRICAL INTERFACE REQUIREMENTS	37
5.2.1 Power interface.....	37
5.2.2 Data Handling Interfaces for payload units.....	45
5.2.3 Data handling interfaces for platform units	76
6. GROUND AND FLIGHT ENVIRONMENTS.....	211

LIST OF FIGURES

FIGURE: MAIN BUS GROUNDING - OPTION A	16
FIGURE: MAIN BUS GROUNDING - OPTION B	17
FIGURE : ELECTRICAL BONDING	21
FIGURE: TRANSIENT DUE TO FUSE CLEARING	40
FIGURE: HIGH-LEVEL COMMAND: SIGNAL WAVEFORM AND TIMING DIAGRAM	48
FIGURE: HIGH-POWER COMMAND: SIGNAL WAVEFORM AND TIMING DIAGRAM	50
FIGURE: ARCHITECTURE OF CK, SAMPLE-CMD, SAMPLE-ACQ AND DATA OUT LINES	55
FIGURE: ARCHITECTURE OF DATA IN LINE	56
FIGURE : BUS VOLTAGE DEFINITION	57
FIGURE: SERIAL COMMAND BIT TIMING	62
FIGURE: SERIAL TELEMETRY ACQUISITION BIT TIMING	63
FIGURE: INTERRUPTION BY THE DWELL - NORMAL AND DWELL REGISTERS	SERREUR! SIGNET NON DÉFINI.

LIST OF TABLES

TABLE 1: INPUT DOCUMENTS	6
TABLE 2: REFERENCE DOCUMENTS	6
TABLE 3: APPLICABLE DOCUMENTS	6
TABLE 4: ABBREVIATION TABLES	7
TABLE: TIMING DEFINITIONS FOR SERIAL TELEMETRY DATA TRANSFER	64
TABLE: COMMAND WORD BIT ALLOCATION	66

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 5 / 213

1. SCOPE OF THE DOCUMENT

1.1 Introduction

This document, called GDIE-E is an applicable document to the equipment specification. Together with the GDIE-M, they establish the general mechanical/thermal/electrical design, interface, environment and verification requirements to be met to ensure their specified performance during assembly, integration, testing, storage, transportation, launch and orbital operations.

Equipment Test requirements will be an extract of the relevant part applicable at unit level from the Satellite Qualification and Acceptance Requirements [AD22].

Each requirement has a unique reference *ABU-SAT-GDIEE-REQ- xxx* to be used as identifier to address the present requirement.

Figures or tables that are called by a requirement are part of the requirement.

1.2 General definition

Satellite is the complete spacecraft assembly, including all those hardware items present after separation of the spacecraft from the launch vehicle.

Sub system is a functioning entity comprising two or more equipment within the system and described by a subsystem specification.

Equipment has to be understood as any electronic box, structural element, module (group of equipment or components eventually delivered with dedicated structures and thermal control hardware) that is assembled before delivery to the Prime.

2. DOCUMENTATION & TERMINOLOGY

2.1 Input Documents

The Input Documents are the input of the present document. If one of these documents is updated, relevant requirements in the present document may change accordingly.

Ref.	Document name	Document Ref.	Issue	Date
ID01				
ID02				

Table 1: Input Documents

2.2 Reference Documents

The Reference Documents are not contractual but they may offer a better understanding of this document.

Ref.	Document name	Document Ref.	Issue	Date
RD01	DIET E3000			
RD02	AD03			
RD03	MIL-STD-1553B + notice2			

Table 2: Reference Documents

2.3 Applicable Documents

The Applicable Documents, applicable to the satellite, contain additional requirements to be used during product design, development, manufacturing, assembly, tests and delivery.

Ref.	Document name	Doc. Ref.	Issue	Date

Table 3: Applicable Documents

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 7 / 213

2.4 Terminology & abbreviations

Specific abbreviations used in the present document are given in the following table.

Abbrev.	Meaning
.../...	.../...

Table 4: Abbreviation Tables

3. GENERAL REQUIREMENTS

All requirements of this section are relevant as far as the electrical design of the equipment is concerned.

REQ

This specification applies to the whole mission life, except for ground activities where the specification is to be met with respect to beginning of life parameters.

3.1 Engineering Standards-Units

Reference **ABU-SAT-GDIEE-REQ-001**

The metric standard (SI - System International) shall be used for design, manufacturing, testing and measurements of all equipment or subassembly. For components, equipment, subassemblies and assemblies, the dimensions shall be given in millimetres and the angles in degrees.

*

3.2 Equipment Interface Control

3.3 Definition

3.3.1 Command

The classification of the commands is performed in three categories. This classification is under Prime Contractor responsibility.

Category 1: Critical commands.

These are commands that, if executed at the wrong time, could cause the loss of, or significant degradation to the mission with irreversible state of the satellite or with a modification of functional performances (such as pyro orders, LAE fire commands).

Category 2: Vital commands

These are commands, which do not belong to category 1, but which are essential to the success of the mission, and if sent at the wrong time could cause a momentary loss of the mission.

Category 3: Configuration - dependant commands

These commands shall only be sent if a particular configuration of sub-system or payload is not established, or that shall be sent under a certain defined condition.

3.3.2 Electrical Ground Reference Plane

3.3.2.1 Payload units

The spacecraft structure is intended to provide an electrical ground plane reference (EGRP).

This EGRP will carry the primary power return currents.

For each equipment, the secondary voltage reference (0V) and the housing will be connected to the EGRP via a bonding stud and a bonding strap with the minimum impedance (resistive and inductive).

3.3.2.2 Platform units

Platform units will use "return by wires" bonding and grounding concept:

- The return of all power bus shall be grounded to the EGRP according to a system plan
- Secondary power line returns shall be referenced to the electrical ground reference (structure) at only one location point.

3.3.3 Bus Users

Bus users are equipment that are connected to the power bus. These equipment shall be considered as standard equipment for grounding, current monitoring, power bus interface and protection philosophy, unless superseded by the equipment specification as for EPS equipment that are upstream the power bus.

4. ELECTRICAL DESIGN AND INTERFACES SPECIFICATIONS

4.1 COMMANDABILITY AND OBSERVABILITY

Requirements for commands and monitoring, including any automatic function and reconfiguration logic are detailed hereafter.

REQ.

The execution of each command, received by the user, shall be verified by a corresponding Telemetry information, indicating the proper execution of the command function, not only the command reception

4.1.1 Commandability

Reference **ABU-SAT-GDIEE-REQ-002**

The ground shall have the possibility to send any command necessary to activate, to put in operational state, or to define the performance of any on-board function or equipment.

*

Reference **ABU-SAT-GDIEE-REQ-003**

There shall not be any function or equipment on which the ground has no direct access (commands directly sent to the function or to the equipment) or indirect access (through a function or equipment of higher level).

*

Reference **ABU-SAT-GDIEE-REQ-004**

All telecommands shall be compliant with the following requirements:

- It shall be possible to acknowledge by telemetry, all telecommands under ground control.
- Telecommands controlling relays, switches or electronic circuits, shall be associated to telemetry of the relay, switch state or the operation status of the electronic equipment.
- Memory load commands controlling equipment(s) configuration shall be associated to telemetry of the corresponding operational effect.
- Critical memory load commands of category 1 (as defined in § 3.3.1 and categorised by the Prime Contractor), shall have a separate execute command to permit verification of load data (TBC)
- ON/OFF commands shall only operate one function. In case of equipment critical configuration (decided at Prime Contractor level), multiple ON/OFF command is authorised; for instance if nominal and redundant equipment or function must not be ON simultaneously, it is recommended that the same ON/OFF command controls the execution.
- All telecommands shall always have the same action during the mission.
- Critical commands of category 1 (as defined in § 3.3.1 and categorised by the Prime Contractor), shall require at least two separate operations and commands for execution: an arm/safe or enable/disable followed by an execute command, operating on different circuits.

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03

Page 11 / 213

- No telecommand shall be dependant on any previous command history. This is neither applicable to memory load + execute commands nor to arm + execute commands. This is mainly applicable to incremental commands (switch rotation, mechanism steps, ...), with no direct TM of the current status.
- Repetition of the same telecommand shall be possible, without any detrimental effect on the equipment.
- Incorrect sending or receiving of a nominal set of telecommands shall be possible (ex: anyone of the set not executed; abortion of the set at any location; start of the set not at the beginning) without causing any stress or loss of functionality when nominal sequence resumes.
- Non-valid/non-defined telecommands shall be rejected or at least shall have no action (including re-initialisation, stop, stop receiving, stop execution modes).
- Each unit using power from the power bus shall be provided with ON and OFF commands. OFF commands shall operate correctly even under failure condition of the corresponding function leading to power consumption excess, so that after OFF command completion, no more power is drawn from the power bus. (TBC)
- It shall be possible, to override/inhibit partially or totally, any on-board autonomous function. This requirement is not applicable to electrical protections that require a reaction time not compatible with ground or on-board software reaction time, but in any case desirable. It shall be possible to replace any on-board autonomous function with ground control, unless not compatible with ground reaction time.
- In case of an on-board automatism, using several criteria, the ground shall have access to each criteria. Particularly, the inhibition of an OR-ing configuration shall be performed independently at each criteria level, without affecting the functioning of the automatism for the remaining criteria. The same restrictions as for point (m) shall apply.
- Each data used in the definition of an on-board automatism (bias, threshold, mask, temporisation, selection,...) shall be configurable by ground TC. Limitations to this requirement shall be identified and proposed to the Prime Contractor.
- For payload computers managing their own time-tag, it shall be possible to terminate immediately an on-going on-board command execution (not yet executed command).
- A reset telecommand, or equivalently a read-reset, shall be associated to any memorisation of transient events. (TBC)
- The definition of data or address shall be always considered MSW first and then LSW.

*

4.1.2 Observability

Reference **ABU-SAT-GDIEE-REQ-005**

The satellite functioning shall be observable in any mode and shall be compliant with the following requirements:

- Monitoring shall be unambiguous and provided by direct measurement rather than secondary effects or combination.
- Monitoring shall not be dependant on previous command knowledge.

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 12 / 213

- Redundant elements shall be monitored through failure independent telemetry channels (the loss or failure of one channel shall not prevent access to telemetry of other channels).
- Monitoring shall be able to detect failures of automatic reconfiguration functions.
- For hot active redundancy functions, telemetry of both functions shall be provided at the same time with unambiguous status determination.
- The status of inhibit functions and of internal switches (relay or electronic switch) shall be monitored and telemetered even if equipment is not powered.
- For all bus users active units which have a primary consumption greater than 3W (TBC), a primary current measurement shall be provided for external ANA SE acquisition. (TBC)
- Content of all registers or memories that determine an operational state shall be monitored (including autonomous on-board functions and internal diagnostic).
- For thermostatically controlled devices: each independently controlled heater shall have a temperature sensor for regulation and a temperature sensor for telemetry, both of them being transmitted to ground via telemetry.
- Bus users power converters shall provide the following telemetry signals in addition to the primary current telemetry (ANA SE):
 - - temperature (TEMA)
 - - secondary voltages (ANA SE) necessary to provide adequate observability of unit proper operation and critical parameters drift trend.
- Concerning bilevel telemetry: the logical level "1" shall correspond as far as possible to the following labels: ON, enabled, authorised, armed, powered, opened, ...; the logical level "0" shall correspond as far as possible to the following labels: OFF, inhibited, disarmed, closed, ...
- The state of protection devices (authorised/inhibited) as well as the action of the protection (triggered, not triggered) shall be monitored.
- All telemetry corresponding to a transient event shall remain in the same logical state and cleared upon reading or dedicated reset TC.
- The telemetry range of an operational parameter shall include margins in order to monitor degraded modes or failures. The telemetry accuracy shall allow to detect unambiguously any abnormal behaviour, without saturation. (TBC)
- For units where a test connector has to be replaced by a flight connector before launch, a status indication verifying the installation of the appropriate flight connector shall be provided.
- Mechanisms: (TBC)
 - Telemetry shall be provided to determine directly or not, but unambiguously, the absolute position of all mechanisms and deployable devices in all phases of the mission.
 - As a minimum, the following TM shall be provided: pointing of steerable antennas; position of all electromechanical devices; positive latch-up indication of all deployment mechanisms; voltage or current of reference supplies used in conjunction with the position indicating devices; solar array position; temperature of electrical motors; commanded current (image of the control torque).

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 13 / 213

-
- Payload: as a goal, the Communications Subsystem shall provide sufficient data to unambiguously determine the configuration and performance of all repeater hardware at any time. To achieve this, the following information shall be provided:
 - Actual position of all RF switches which provide a static connection (for configuration, connectivity or redundancy selection purposes).
 - Status of all gain frequency states, where adjustable.
 - Critical performances parameters of all travelling wave tubes. Where applicable, this shall include helix current, cathode current, or control anode voltage and status for filament, filament boost and high voltage on-off.
 - Individual load current for all RF power amplifiers and replacement heaters. In order to cope with current sensing TM allocation, grouping of load current measurements shall be reviewed with the Prime.
 - Units which have a functional sensitivity to temperature levels shall be provided with a temperature telemetry .
-

*

5. ELECTRICAL DESIGN AND INTERFACES REQUIREMENTS

5.1 ELECTRICAL DESIGN REQUIREMENTS

5.1.1 Electrical Grounding

5.1.1.1 General

Reference **ABU-SAT-GDIEE-REQ-006**

Electrical grounding and bonding is requested for all mechanical structure elements, equipment housing, thermal blanket devices:

- To prevent hazard from high potentials
- To prevent build up of static charges
- To reduce electromagnetic interference
- To protect from high voltage arcing
- To establish an Electrical Ground Reference Plane (EGRP)
- To potentially use the structure to carry primary power returns

*

The spacecraft structure will constitute a low impedance voltage reference plane named EGRP.

The PSR will be the primary power reference point where the electrical power subsystem common return is connected to the structure.

5.1.1.2 Return Grounding and Screening Requirements

5.1.1.2.1 Main Bus grounding

The negative side of the main bus shall be grounded at the electrical power subsystem distribution points, at the power supply regulator side.

Intensive use of structure return is used at system level for payload units.

Reference **ABU-SAT-GDIEE-REQ-007**

All platform equipment (power bus users) shall be compliant with option A only.

*

Reference **ABU-SAT-GDIEE-REQ-008**

Payload equipments (power bus users) shall be compliant either with Option A or Option B. Option A is the preferred configuration. Option selection (A or B) shall be brought to Prime approval

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 15 / 213

Reference **ABU-SAT-GDIEE-REQ-009**

For both option A and B, the low impedance grounding reference (defined in req. TBD) shall comply with the req. TBD.

*

Reference **ABU-SAT-GDIEE-REQ-010**

Each unit shall provide the detailed input filters electrical diagrams together with the equipment grounding diagram.

*

Option A:

Reference **ABU-SAT-GDIEE-REQ-011**

For each equipment power input, an insulation (galvanic insulation for power converters, i.e. primary to secondary insulation by means of transformers with insulated primary and secondary windings) shall be provided between primary return and structure (see Figure 6.1/1??) with impedance such that $R > 10\text{ k}\Omega$ in parallel with $C < 50\text{ nF}$; in case of non-compliance with this requirement, the supplier shall justify the use of a capacitor exceeding 50 nF.

*

Reference **ABU-SAT-GDIEE-REQ-012**

The common mode filter (balun if any or harness inductance plus common mode capacitor) is a resonant device; therefore an appropriate damping network shall limit its quality factor. (TBC)

*

Reference **ABU-SAT-GDIEE-REQ-013**

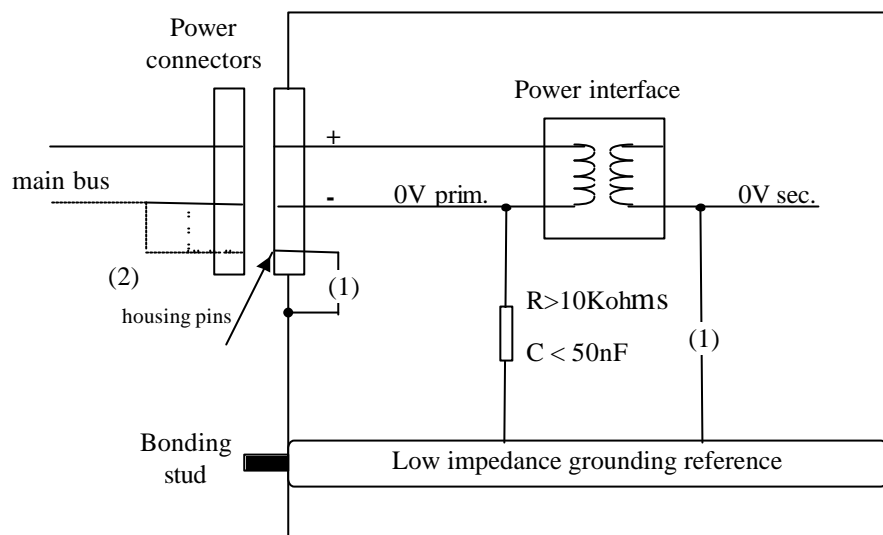
No single failure shall lead to the violation of the galvanic insulation requirements.

*

Reference **ABU-SAT-GDIEE-REQ-014**

When option A is selected, the equipment will be used either with structure return or with wire return philosophy. The structure return will be achieved by connecting together in the harness the power bus return and the housing pins of the power connector(s) (see note 2 of fig. 6.1/1). Additional housing pins shall be considered in order to meet the pin current derating.

*

Option A

(1) Low impedance bond, length less than 5cm, type and number of wires defined according to unit power consumption, as close as possible to the power transformer.

(2) structure **or** wire return **configuration** : it shall be possible to configure either wire return or structure return at connector level. Unit shall be compliant to both, and the choice of wire return shall be brought to prime approval.

FIGURE: MAIN BUS GROUNDING - Option A**Option B:**

Reference **ABU-SAT-GDIEE-REQ-015**

Primary return is grounded to the low impedance grounding reference inside unit (Primary structure return).

*

Reference **ABU-SAT-GDIEE-REQ-016**

As there might be no primary to secondary galvanic insulation, it shall be demonstrated that any single failure does not propagate to other units nor to the corresponding redundant unit (no thermal failure propagation, no over voltage exceeding specified values on all the unit interfaces, no propagation through cross-strapping).

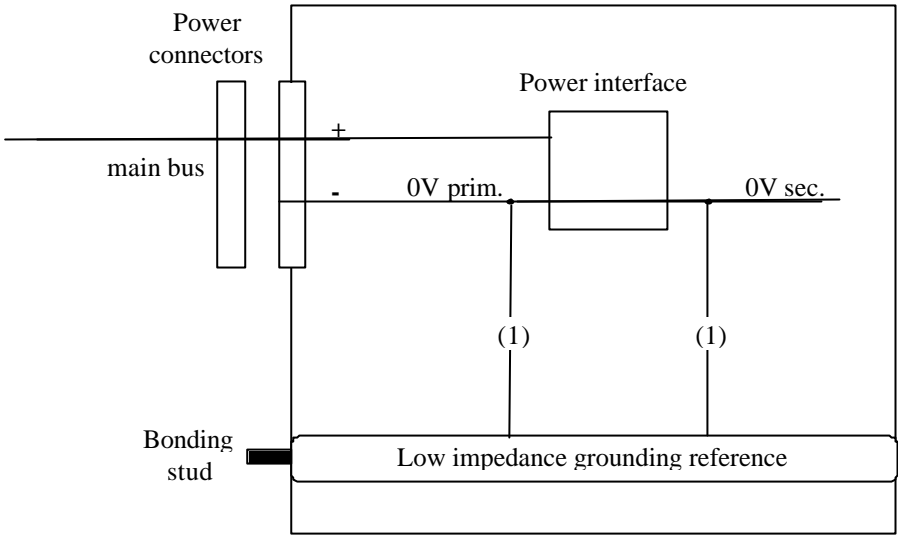
*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 17 / 213

Option B



(1) Low impedance bond, length less than 5cm, type and number of wires defined according to unit power consumption

FIGURE: MAIN BUS GROUNDING - Option B

5.1.1.2.2 Secondary supply grounding

These requirements aim at ensuring performance of the unit internal grounding, in order to master the common mode voltage internally and at interface level .

Reference **ABU-SAT-GDIEE-REQ-017**

All secondary supplies, when only used inside the equipment, shall have their return grounded through a low inductance path to a low impedance grounding reference, inside the unit (see Figure 6.1/1).

*

Reference **ABU-SAT-GDIEE-REQ-018**

The bonds used to ground the secondary supplies returns shall have a length not exceeding 5 cm, the type and number of wires being defined according to unit power consumption. . (5cm TBC)

*

Reference **ABU-SAT-GDIEE-REQ-019**

The resistance of the low impedance grounding reference shall be less than 2.5 mΩ DC between the bonding stud and any point of the low impedance grounding reference.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 18 / 213

Reference **ABU-SAT-GDIEE-REQ-020**

The internal grounding shall be designed such that the voltage drop between the bonding stud and the internal secondary OV, does not exceed 100 mV peak-to-peak d.c. to 30 MHz, when the equipment is operated with representative interfaces. This requirement shall be demonstrated by test. In case of non-compliance, a measurement using a spectrum analyser shall be provided to prime for approval. (TBC)

*

Reference **ABU-SAT-GDIEE-REQ-021**

When secondary supplies are not used only inside the equipment, the same philosophy as for requirements 17 to 21 shall apply, except when the application requires insulation; in that case the unit shall provide dedicated insulated windings used with balun transformers in order to ground the supply return at load unit level, inside the unit. (TBC)

*

Reference **ABU-SAT-GDIEE-REQ-022**

When option A is selected, the common mode current in the power lines shall be less than 100 dBμA rms at 10 kHz, decreasing with frequency with a - 20 dB/decade slope up to 30 MHz (see TBD for test set-up). (TBC)

*

5.1.1.2.3 Signal grounding (for structure return compatible units)

Reference **ABU-SAT-GDIEE-REQ-023**

Unless otherwise specified in this document or in the equipment specification, all analogue and digital logic signals shall use structure return (for structure return compatible units).

*

Reference **ABU-SAT-GDIEE-REQ-024**

In any case, signals interface design shall be compatible with a common mode specification of 0.5 V RMS from 10 kHz to 30 MHz and ± 300 mV DC. This requirement shall be demonstrated by analysis in the unit WCA (for structure return compatible units).

*

Where above requirement cannot be met or when specific design/performance requirements (such as noise immunity or cable-to-cable coupling risks) exist, dedicated return wires can be used.

5.1.1.2.4 RF Signals

Reference **ABU-SAT-GDIEE-REQ-025**

RF signals shall be carried by wave-guides, by semi-rigid coaxial cables or by flexible coaxial cables optimised for use over the operating frequency range, or any other transmission line appropriate to the Payload operational and performance requirements.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 19 / 213

Reference **ABU-SAT-GDIEE-REQ-026**

All RF components shall be designed to prohibit the occurrence of multipactor discharge when ambient pressures below 10⁻⁴ Torr have applied for times greater than 10 minutes, for instantaneous RF powers of up to 200% of the maximum operating instantaneous RF power

*

Reference **ABU-SAT-GDIEE-REQ-027**

RF components which carry power during launch and ascent shall be designed to preclude corona discharges at any pressure below 1 atmosphere

*

Reference **ABU-SAT-GDIEE-REQ-028**

Flexible coaxial cables shall be tied down to the satellite structure in such a way that the cable, inner to outer conductor dimensions will not be permanently altered if the cable experiences launch acceleration and vibrations and at intervals to be determined by the Prime Contractor

*

Reference **ABU-SAT-GDIEE-REQ-029**

Bends in coaxial cable shall be smooth and at no time shall the bend radius be less than the minimum bend radius stated by the cable manufacturer

*

Reference **ABU-SAT-GDIEE-REQ-030**

Semi-rigid cables shall, where possible, have inner and outer conductors formed of the same type of material. Where this is not practicable, the maximum differential expansion over the operational temperature range, between the inner and outer conductor of any cable, shall not exceed 0.2 mm

*

Reference **ABU-SAT-GDIEE-REQ-031**

The maximum strains imposed by connectors and connecting equipments by differential expansion between semi-rigid cable and wave guide and the spacecraft structure shall be reduced to tolerable levels by incorporating strains reducing devices e.g. bends in semi-rigid cables and bends or flexible wave guide where appropriate in wave guide runs.

*

5.1.1.3 Electrical bonding

Reference **ABU-SAT-GDIEE-REQ-032**

The bonding and grounding resistances shall be measured with a 4-point method, with a d.c. current of 1A.

*

5.1.1.3.1 Equipment housing bonding

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03
 Page 20 / 213

Reference **ABU-SAT-GDIEE-REQ-033**

All active equipment shall be provided with a bonding stud.

*

Reference **ABU-SAT-GDIEE-REQ-034**

The DC resistance in either direction between any metallic part of the equipment housing and the bonding stud shall be less than 5 mΩ (see fig. TBD).

*

Reference **ABU-SAT-GDIEE-REQ-035**

The DC resistance between bonding stud and power connectors housing pins (See fig. TBD) shall be lower than 30 mΩ but sized in accordance with primary current return (current derating shall be applied).
 (TBC)

*

Reference **ABU-SAT-GDIEE-REQ-036**

This connection, from housing pins to the bonding stud, shall withstand without stress a DC current of at least 4 times the maximum user current. (TBC)

*

Reference **ABU-SAT-GDIEE-REQ-037**

The performance impacts of the primary power lines grounding through the housing pins (additional voltage drop w.r.t $\Phi 0$, power dissipation, EMC through common impedance) shall be considered at unit level. (TBC)

*

If the bonding stud is only used for potential reference (when the unit structure is not used as an internal low impedance grounding reference, but only concerned by ESD grounding or cable shields grounding), other bonding methods (e.g. mounting feet) could be submitted to Prime approval.

Reference **ABU-SAT-GDIEE-REQ-038**

For a unit internally redundant, using Option B for primary bus grounding, two bonding studs shall be provided.

*

For information:

The DC resistance, between the equipment bonding stud and the structure is less than 2.5mΩ under 1 Adc measurement.

5.1.1.3.2 Shielding Connection to the EGRP

Reference **ABU-SAT-GDIEE-REQ-039**

Multi-point grounding to the Electrical Ground Reference Plane (EGRP) shall be provided if necessary.

*

Bus users primary power connectors, shall have at least 2 pins connected to the equipment housing (housing pins). Those housing pins shall only be used for primary power return connection to the structure, the connection being performed in the harness, when option A of requirement TBD is selected.

*

For other connectors, screen/shield pins (if any) shall not be used. The connection of the harness shields to the EGRP shall be performed at both ends through the connector body/screws, so that the shields currents do not flow inside the equipment. Each equipment connector body shall provide contact to the bonding stud with impedance less than 10 mΩ (see fig. TBD). The shielding lineic resistance shall be less than 150 mΩ/m.

*

All thermal insulation blankets shall be grounded to the equipment or to the spacecraft structure by an impedance of less than 100 Ω between any of the conductive layers and the equipment or spacecraft structure. The provisions for ESD protection shall also apply. (TBC)

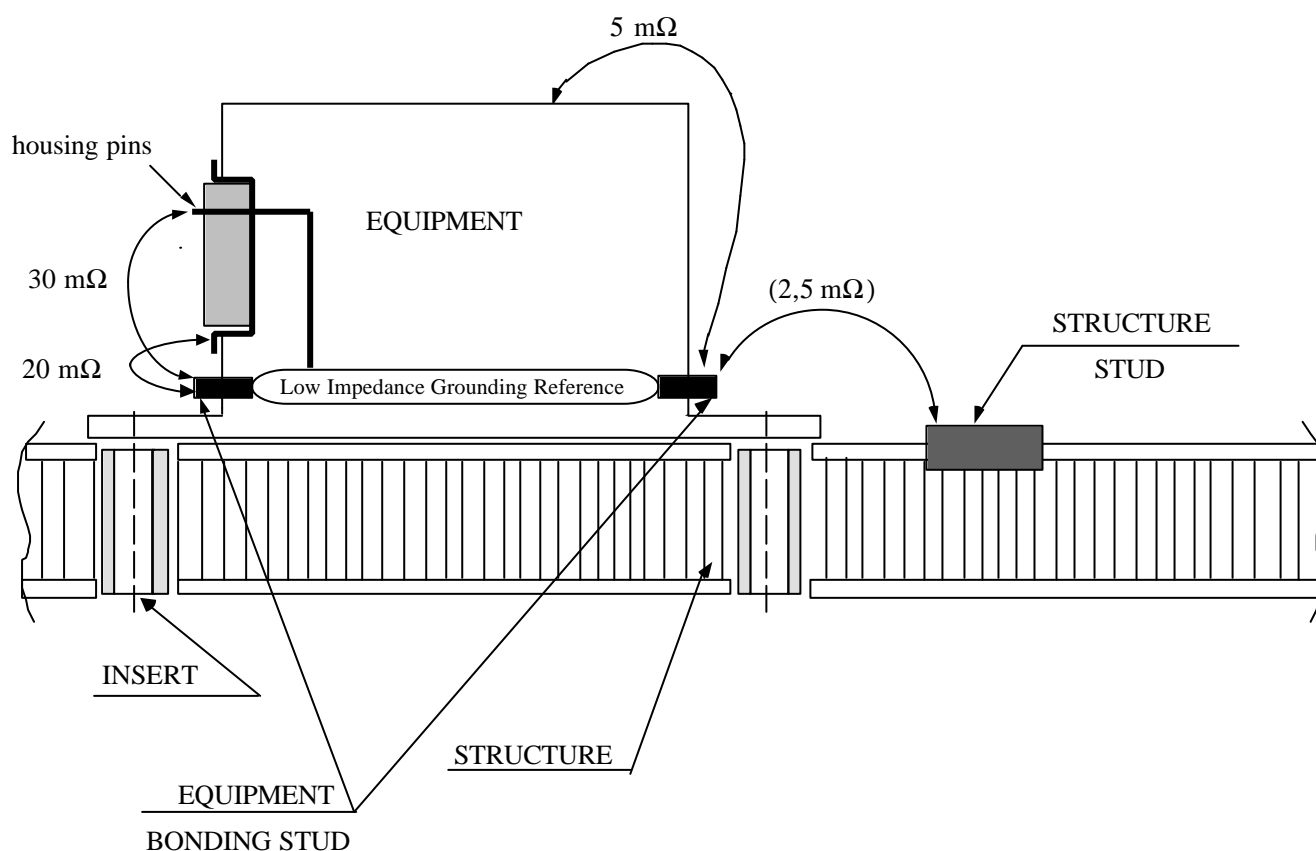


FIGURE TBD: ELECTRICAL BONDING

5.1.1.3.4 Electrostatic Cleanliness REQUIREMENTS

5.1.1.3.4.1 Reduction of ESD occurrence risk

During and after launch, the spacecraft will be surrounded by low-density plasma of high-energy electrons and protons. On any spacecraft insulated surfaces the electrons will build up a charge that will discharge when the voltage breakdown of the insulating materials is reached.

In order to minimise the effects of ESD, the general design principle is that all space facing surface shall be electrically conductive and reliably connected to spacecraft structure. Specific design requirements to satisfy the principles are as follows :

- a. All external (fully exposed) surface above 5cm² shall be electrostatically conductive and grounded to the Spacecraft structure; the surface resistance shall be less than 1E+9 O/sq.
- b. the bulk resistance shall be less than :
 - 1E+11 O.m for a max thickness of 6mm, when fully exposed to space environment (no shielding, corresponding to a max irradiation flux of 180pA/cm² at material level)
 - 1E+12 O.m for a max thickness of 5mm, when only protected from space environment by a standard MLI (75µm shielding, corresponding to a max irradiation flux of 20pA/cm² at material level)
 - 1E+13 O.m for a max thickness of 15mm, when protected from space environment by a minimum 1mm shielding (unit chassis + spacecraft structure), corresponding to a max irradiation flux of 0.72pA/cm² at material level.
 - In case of non-compliance to these requirements (Resistivity & thicknesses), the contractor shall assess by irradiation tests that there is no detrimental effect to the unit. Any deviation to this process shall be submitted to prime for approval, in case of prime refusal, the contractor shall replace the dielectric material by a compliant one.
- c. All external/internal metallic parts whose surface is higher than 1cm² (even very small ones such as metallic labels, connector brackets, the EPC and heaters base plates (or doublers), the heat pipes, the tyraps) and intrinsically conductive parts (like carbon) shall be grounded to the main spacecraft by a resistance much lower than 1MΩ and typically 100kΩ.
- d. Blankets shall be grounded to the structure with at least 2 bonding straps and any point on a blanket shall be within 1 m of a bonding strap. The bonding strap shall be grounded to the structure by a proven technique such as a wire that is as short as possible . All external (on walls, Antennas, Battery, Fluid loop...) and internal (IMUX, OMUX, TWT, CPS, Battery...) Multi-layers Insulation shall be grounded to the structure by a resistance less than 100 Ω. The area of individual thermal blankets shall not exceed 2 square meters. Adjacent blankets shall be separately grounded to structure (no daisy chain)
- e. Optical Solar Reflectors shall be bonded using an electrical conductive adhesive.

*

White PCBZ & PSG120/121FD, black ELECTRODAG 501 and conductive BLACK AEROGLAZE Z306/307 paints have demonstrated good performance in order to dissipate the electrostatic charges.

5.1.1.3.4.2 External materials submitted to Prime approval

ESD occurrence risks will be encountered in the situation here below :

Use of Perforated Aluminised Teflon (SSM) and the use of standard Teflon (FEP, PTFE, FLPO, TEFZEL)

Uncoated Kapton (or Aluminized Kapton thickness > 25µm) is generally unacceptable due to high resistivity. *(However, In continuous sunlight application, if less than 130 µm thick, Kapton is sufficiently photoconductive for use.)*

Use of epoxy glass,

Silica cloth,

Metallic floating parts (wire, connector, strap, metallic part on non-conductive Velcro).

Triple junction point (triple contact between dielectric, vacuum & metal; ex uncoated conductors) shall be strictly avoided : conductors shall be isolated from environment by a dielectric film thickness <25µm.

#

The use of non-compliant materials shall be submitted to Prime EMC/ESD authority for approval (System analysis shall be performed, taking into account with Spacecraft shielding, exposed surface, insulator thickness, in order to assess max transmitted flux)

#

If compliance with the above ESD requirements (043 & 044) cannot be achieved due to conflicting design requirements then tests shall be performed on a representative sample of the concerned surface material. Details of the procedure and the test results shall be submitted to Prime Contractor EMC authority for approval.

#

5.1.1.3.4.3 Reduction of ESD effects

The following general principles shall be applied in addition to any specific circuitry techniques:

- circuit bandwidths shall be restricted to the functional use,
- loop areas of circuits using structure return shall be minimised by routing the wires of these circuits close to the structure,
- harness shieldings shall be grounded to the Electrical Ground Reference Plane by a wire (pigtail) of 5cm length max ,
- all external harness not routed through filter connector shall shielded.
- external Top-floor harness and units protected by an ESD Screen.

#

5.1.1.3.4.4 Deep Dielectric Charging mitigation requirements

Electrostatic discharge can result from charging of dielectric and floating conductors within a spacecraft by energetic electrons ($E > 2\text{MeV}$).

In order to minimise the charging risk, the general design principle is that all metallic parts shall be electrically conductive and reliably connected to spacecraft structure, and dielectric materials resistivity and thickness selected to mitigate deep charging risk.

#

Specific design requirements to satisfy the principles are as follows :

The Subcontractor shall identify in its equipment, all the metallic $>20\text{mm}^2$ surfaces which are not always referenced to a fixed potential (track of floating PCB tracks, unused pins, cabling).

For all equipment the DDC analyses have to be performed by the Subcontractor to demonstrate design compliance to the dielectric materials selection versus bulk resistivity & thickness requirements)

#

5.1.1.3.5 Magnetic Requirements

The magnetic momentum of any fully operational equipment, electronic or others, shall not exceed 0.5 Am² in any direction. Analysis will be acceptable for demonstration of compliance except for equipments with permanent magnetic field (eg: TWT, Solenoid magnetic actuators), where test is required.

*

5.1.1.3.6 Assembly Bonding

Reference **ABU-SAT-GDIEE-REQ-047**

All metallic sub chassis, chassis and enclosures of each unit, including all connector shells and other fittings, shall be considered electrically as extensions of the EGRP. The bonding requirements are such that all satellite equipment primary and secondary structure supporting or containing electrical/electronic assemblies shall be bonded by one of the following methods, in order of preference:

- direct inherent bond by welding, brazing, soldering etc...
- direct semi-permanent bond, where clean metal areas are mated with a fastening method that exerts sufficient pressure to withstand deforming stresses, shocks and vibrations
- riveting joints where at least two rivets are driven tight per joint (TBC)
- clamped metallic fittings, normally permanent and immovable after installation
- lock-threaded devices (bolts, nuts, studs, lock-washers)
- Indirect bond, bonded to each of the members using a strap of solid flat metal of length to width ratio not exceeding 5/1. This method shall only be used with the consent of the Prime Contractor.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03
Page 25 / 213

5.1.2 Electrical Connectors

Reference **ABU-SAT-GDIEE-REQ-048**

Electrical connectors shall provide a low-impedance path for all internal wires and a low-impedance bond via the outer shell.

*

5.1.2.1 Connector Types

Reference **ABU-SAT-GDIEE-REQ-050**

The type of connectors shall be defined separately for equipment connectors, RF connectors, skin connectors and pyrotechnic connectors if applicable. The same types of connector shall be used for all equipment models.

*

Reference **ABU-SAT-GDIEE-REQ-051**

Unit mounted micro sub-miniature connectors (MDM) are forbidden for flight connectors, unless their use has been expressly agreed with Prime.

Connectors pin count shall be limited to 78 ways, unless their use has been expressly agreed with Prime.

*

5.1.2.2 Characteristics

Reference **ABU-SAT-GDIEE-REQ-052**

Connectors on the exterior of units shall be clearly and uniquely identified (refer to ICD/IDS preparation rules ref TBD + data & conf ref TBD).

*

Reference **ABU-SAT-GDIEE-REQ-053**

Pyrotechnic connectors shall be separated from other circuit connectors.

*

Reference **ABU-SAT-GDIEE-REQ-054**

Separate coaxial connectors shall be used (as required). (TBC)

*

Reference **ABU-SAT-GDIEE-REQ-055**

The housing of connectors shall be electrically connected to the unit structure.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03
Page 26 / 213

Reference **ABU-SAT-GDIEE-REQ-056**

Connectors supplying or distributing power shall be female including test connectors.

*

Reference **ABU-SAT-GDIEE-REQ-057**

Other unit mounted connectors type (male or female) shall be selected in order to avoid mismatching. (TBC)

*

Reference **ABU-SAT-GDIEE-REQ-058**

Male and female connectors shall be mechanically locked together to prevent inadvertent disconnection.

*

Reference **ABU-SAT-GDIEE-REQ-059**

The backs of connectors susceptible to the entry of moisture, fumes, contaminants and foreign objects shall be potted or otherwise sealed.

*

Reference **ABU-SAT-GDIEE-REQ-060**

Mechanical methods in conjunction with identification markings shall be employed as far as possible to prevent incorrect mating of connectors (cannon connectors can be used).

*

Reference **ABU-SAT-GDIEE-REQ-061**

Number of assembly and disassembly operations on flight connectors, including test connectors, will not exceed 50. Savers shall be used, if necessary, during integration phase.

*

REQ

The Supplier will identify the connector numbers on the interface drawing.

Unless expressly specified (e.g.TBD), connectors shall not carry both prime and redundant signals of a given functionality. Any deviation to this requirement shall be brought to prime approval, while providing the exhaustive list of connectors and signals concerned.

Reference **ABU-SAT-GDIEE-REQ-062**

On the equipment Sub-D connectors a torque of 4.5 cm kg shall be applied on each screw lock. When the harness connector is connected to the equipment, the applied torque is 3.5 cm kg. For other connectors types, the Prime shall be consulted concerning torque to be applied on screw lock. (TBC)

*

Reference **ABU-SAT-GDIEE-REQ-063**

In order to guarantee good mechanical characteristics for the bundle on the connector, the connected contacts shall never be inferior to two third of the maximum capacity.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 27 / 213

Reference **ABU-SAT-GDIEE-REQ-064**

Flame labels shall clearly identify equipment connectors that present a risk of permanent damage or failure propagation, when shorted to ground or when any two pins of that connector are shorted.

*

5.1.2.3 Connector Pin Assignment

Reference **ABU-SAT-GDIEE-REQ-065**

To establish the electrical configuration of interfaces, the Detailed Interface Handbook shall include the electrical and interface data sheets as described in TBD.

*

Screen pins can be implemented but will not be used.

Reference **ABU-SAT-GDIEE-REQ-066**

Bus user primary power connectors shall be provided with housing pins (refer to req TBD, AD TBD).

*

Reference **ABU-SAT-GDIEE-REQ-067**

The position and orientation of each connector shall be shown on an interface control drawing As per AD TBD.

*

Reference **ABU-SAT-GDIEE-REQ-068**

The number of connectors shall be kept to a minimum but using the following assignment (as per AD TBD): (TBC)

- Pyrotechnic connector (specific)
 - RF connector (specific)
 - Data bus connector(s)
 - Primary power bus connector(s)
 - Signal connector(s)
 - Test connector(s)
-

*

5.1.2.3.1 1553B Data bus connector

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 28 / 213

Reference **ABU-SAT-GDIEE-REQ-069**

Unless otherwise agreed with the Prime Contractor, the connection between a remote terminal equipment and the MIL-STD-1553 B bus stubs shall be performed via a Cannon 9 P equipment connector, according to the following pin function:

pin 1	1553 B bus prime
pin 2	not connected
pin 3	not connected
pin 4	not connected
pin 5	1553 B bus redundant
pin 6	1553 B bus prime return
pin 7	not connected
pin 8	not connected
pin 9	1553 B bus redundant return

*

Reference **ABU-SAT-GDIEE-REQ-070**

Unless otherwise agreed with the Prime Contractor, the remote terminal address definition shall be performed on a dedicated Cannon 9 S equipment connector, according to the following pin function:

pin 1	remote terminal address bit n° 4 (MSB)
pin 2	remote terminal address bit n° 3
pin 3	remote terminal address bit n° 2
pin 4	remote terminal address bit n° 1
pin 5	remote terminal address bit n° 0 (LSB)
pin 6	remote terminal address parity bit
pin 7	secondary OV
pin 8	secondary OV
pin 9	not connected

*

Reference **ABU-SAT-GDIEE-REQ-071**

Concerning remote terminal address definition pins (bits 4 to 0 and parity), a logical « 1 » level shall be obtained by floating the corresponding pin (no connection at harness connector level); adequate filtering shall be provided inside the unit on those signals. A logical « 0 » level shall be obtained by connecting the corresponding pin to the secondary OV pin at harness level; the current in each remote terminal address definition pin shall not exceed 10 mA when programmed to logical level « 0 ».

*

Reference **ABU-SAT-GDIEE-REQ-072**

This connector definition shall apply to all remote terminal equipments that are not internally redundant.

*

Reference **ABU-SAT-GDIEE-REQ-073**

For internally redundant equipments, two sets of data bus connectors shall be implemented, one for the prime Remote Interface Unit (RIU), and the other one for the redundant RIU.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03
Page 29 / 213

5.1.2.3.2 Primary power bus connector

Reference **ABU-SAT-GDIEE-REQ-074**

The primary power bus input lines for DC/DC converters shall be assigned on a dedicated connector type.

*

Reference **ABU-SAT-GDIEE-REQ-075**

Unless otherwise agreed with the Prime Contractor, a Cannon 15 P way connector, with the following pin allocation shall be implemented:

pin 1	Main bus CV	
pin 2	Main bus CV	
pin 3	spare	
pin 4	spare	
pin 5	spare	
pin 6	spare	
pin 7	spare	
pin 8	spare	
pin 9	OV Main bus	
pin 10	OV Main bus	
pin 11	spare	
pin 12	Housing	
pin 13	spare	
pin 14	spare	
pin 15	Housing	

*

Otherwise, power pin allocation remains under Prime approval.

Reference **ABU-SAT-GDIEE-REQ-076**

For internally redundant equipment, at least two power bus connectors shall be implemented (one for nominal functions and another one for redundant functions).

*

Reference **ABU-SAT-GDIEE-REQ-077**

Additional pins (for main bus CV, OV main bus and housing) shall be used in order to meet pin current derating rules.

*

Reference **ABU-SAT-GDIEE-REQ-078**

In case of power bus protection inside the unit (i.e. when fuse protection outside the unit is not chosen), double insulation requirements impose a different pin allocation with sufficient spacing between power pins and power return / housing pins (applicable to distribution units **and** high power units).

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03
 Page 30 / 213

5.1.2.4 Test Connectors

5.1.2.4.1 Definitions

Reference **ABU-SAT-GDIEE-REQ-079**

Test point return: test points shall be referenced to their ground reference inside unit; in the case where floating is required (at unit or EGSE level), the test point return shall be considered as a test point.

*

For information::

- Test point: point used either to get information used in the satellite without affecting its operation, or to inject a stimulus affecting its operation.
- Occasional AIT test points: test points used during integration and complementary satellite test; they are not necessarily connected to EGSE but shall be accessible without breaking the functional harness.
- Functional permanent AIT test points: test points used during all satellite on ground tests, and included in umbilical links towards EGSE. These are then vital functional signals used to start and basically operate the satellite.
- Recurrent permanent AIT test points: test points used during satellite recurrent tests, and connected to EGSE. These non vital links are used to characterise the satellite operation.
- Restricted equipment test points: test points used at equipment test level, which use is forbidden or strongly not recommended for AIT (safety, unprotected). Restricted use during the first integration.
- Standard equipment test points: test points used at equipment test level, which use is authorised for AIT.
- Signal test point: test point with current less than 0.1A in nominal, failure or short cases.
- Power test point: test point with current greater than 0.1A in nominal case towards EGSE (source or load).
- Voltage test point: signal test point with low source impedance with regards to the receiver impedance.
- Current test point: signal test point with high source impedance with regards to the receiver impedance.

5.1.2.4.2 Test connectors classification

Reference **ABU-SAT-GDIEE-REQ-080**

Functional and test connectors shall be segregated.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 31 / 213

Reference **ABU-SAT-GDIEE-REQ-081**

Nevertheless, « functional permanent AIT test points » and « restricted equipment test points » must be available on functional connectors, except if the test point is susceptible to EMC/ESD perturbations that could generate unit performance degradation; in that case, those test points shall be implemented on separate test connectors and protected with metallic covers.

*

Reference **ABU-SAT-GDIEE-REQ-082**

To test the performance of the system or subsystems when completely integrated onto the satellite, dedicated points shall be available on specific equipment AIT connector(s) (if equipment is concerned); the AIT connectors concern the « occasional AIT test points » and the « recurrent permanent AIT test points » that must not be implemented on functional connectors.

*

Reference **ABU-SAT-GDIEE-REQ-083**

The test points necessary to test the unit by itself shall be available on specific equipment test connector(s); this concerns the « standard equipment test points ».

*

Reference **ABU-SAT-GDIEE-REQ-084**

AIT and Test specific connectors shall be easily accessible and uniquely designated.

*

5.1.2.5 Test Points

5.1.2.5.1 AIT test point need identification

For information::

« Satellite function » is understood as a hardware or software functional subset that can be isolated upstream and downstream, in order to replace it by an equivalent subset (this is the case of cold redundancies), or to be passivated without altering the subset operation (this is the case of hot active redundancies). A function can encompass several equipments, or concern down to equipment parts.

Tests will generate stimulus and monitor the effects in return; stimulus and effects are mostly electrical.

These AIT test points shall be provided when a « satellite function » is identified by common consent between AIT and the Prime Contractor, and shall provide the adequate commandability and observability of the function.

A hardware test point (stimuli) shall be provided each time a software information in the control loop cannot be modified.

These test points shall cover as a minimum:

- The emulation of attitude sensors, temperatures, currents, voltages, according to the nominal operation of the satellite,
- The active hardware or software protections according to the abnormal operations of the satellite.

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03

Page 32 / 213

These functions are generally included in the on-board controls, that cannot be activated during tests (e.g. satellite rotation, satellite attitude for a given sensor, extreme temperature,...).

The corresponding test points shall then allow stimulating the on-board control and measuring the effects, with a maximum use of on-board hardware and software.

Reference **ABU-SAT-GDIEE-REQ-085**

All tests, recurrent or not, performed to demonstrate the correct operation and the integrity of the satellite functions (including safety, hot active redundancies check-out) shall be possible without breaking flight harness, except when duly justified.

*

Reference **ABU-SAT-GDIEE-REQ-086**

The effect of a functional stimuli test point shall be observable in unit telemetry.

*

5.1.2.5.2 Test points design requirements

The goal of the following requirements is to protect the satellite equipments against the ground test operation most frequent errors, and to define the EGSE failure domain. Failure is allowed but shall remain fail safe with respect to the satellite.

Reference **ABU-SAT-GDIEE-REQ-087**

If there is no cost/mass impact, a good way to limit the damage risk between EGSE and unit is to encourage stimuli generation or built-in self-test, inside the unit itself.

*

These requirements are applicable to specific AIT and Test connectors only (commonly named test connectors hereafter).

Reference **ABU-SAT-GDIEE-REQ-088**

The test interfaces shall be compatible and meet performance specifications with EGSE to spacecraft distance over 60m for specific signals as addressed in the equipment specification.

*

Reference **ABU-SAT-GDIEE-REQ-089**

A test point shall be either of "signal" type or of «power» type and identified as such in the ICD/IDS.

*

Reference **ABU-SAT-GDIEE-REQ-090**

A signal test point shall be either of «current» type or of «voltage» type and identified as such in the ICD/IDS.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 33 / 213

Reference **ABU-SAT-GDIEE-REQ-091**

As far as possible, equipment test connectors shall be female; this requirement remains valid in case of bi-directional power test points. Nevertheless, priority shall be given to avoid mismating.

*

Reference **ABU-SAT-GDIEE-REQ-092**

Mix of « signal » and « power » test points shall be avoided as far as possible on the same connector. Nevertheless, in case of power injection on a power test point, the signal test points allowing the control of the injected voltage shall be provided on the same connector.

*

Reference **ABU-SAT-GDIEE-REQ-093**

Equipments shall not exhibit any part at a voltage higher than 100V, that can be in direct contact with AIT people.

*

Reference **ABU-SAT-GDIEE-REQ-094**

Where test connectors are provided, these should be protected by metallic covers to provide protection against mechanical damage when not in use (particle tightness). The test connectors shall be shielded from EMI prior to launch. Protections covers of all test connectors shall be part of equipment delivery.

*

Reference **ABU-SAT-GDIEE-REQ-095**

Test points on multi-pin connectors shall be designed to withstand without causing damage, permanent voltages up to 10 % or 2 Volts (whichever is the greater) above the highest voltage on that connector, under zero impedance. As far as possible this voltage limit shall be extended to 100V. This voltage may be the output voltage from that unit (short of any two pins on that connector) or the expected maximum test input voltage. Permanent short of these points to ground shall not cause damage. The equipment operation, including test points, shall resume when the short is removed.

*

Reference **ABU-SAT-GDIEE-REQ-096**

Test points shall not generate, under any failure case, voltages up to 30 % above the highest nominal voltage on that connector.

*

Reference **ABU-SAT-GDIEE-REQ-097**

Test points shall be designed to withstand without causing damage, permanent currents up to twice the nominal current. Test points wiring shall withstand up to four times the maximum current on that connector.

*

Reference **ABU-SAT-GDIEE-REQ-098**

Test points shall not generate, under any failure case or short condition, currents up to twice the nominal current.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 34 / 213

Reference **ABU-SAT-GDIEE-REQ-099**

The equipment design shall allow without equipment damage, the supplies switching off (EGSE and internal to spacecraft) without any sequential order constraint.

*

Reference **ABU-SAT-GDIEE-REQ-101**

If fuses are used to protect test points (if current requirements cannot be met), the equipment shall withstand without causing damage the fuse clearing time under any short impedance.

*

Reference **ABU-SAT-GDIEE-REQ-102**

For requirements 94 to 101, transient currents and voltages shall remain in the equipment parts safe operating area.

*

Reference **ABU-SAT-GDIEE-REQ-103**

RF test ports shall be accessible without dismounting RF shield or thermal blankets.

*

Reference **ABU-SAT-GDIEE-REQ-104**

Exclusive use of test points shall be identified in the unit User Manual, in the case when critical test points should not be used simultaneously.

*

5.1.2.6 Connector Savers

Reference **ABU-SAT-GDIEE-REQ-105**

Connector savers shall be delivered with the unit (for payload units only).

*

Reference **ABU-SAT-GDIEE-REQ-106**

Connector savers shall be provided for all functional and test port. Connector savers shall be compatible with flight hardware, e.g. gold-plated. The savers shall remain in position for all electrical and environmental tests but removed for mass property measurements. Connector savers shall be shielded or removed for specific radiated interference tests, when these are likely to compromise the test. Saver connectors removal shall be carried out under P.A. control

*

Reference **ABU-SAT-GDIEE-REQ-107**

Connector savers shall be screw-locked in position during mechanical testing.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03
 Page 35 / 213

5.1.3 Magnetic Requirements

Reference **ABU-SAT-GDIEE-REQ-108**

The magnetic momentum of any fully operational equipment, electronic or others, shall not exceed 0.5 Am² in any direction. Analysis will normally be acceptable for demonstration of compliance except for equipment which are specifically magnetic.

*

5.1.4 Double Insulation requirements

The double insulation requirements depends on the accurate identification of:

- The way insulation is performed (thickness, gap, materials) between two electrically conductive elements at different potentials
- The conceivable variations of the thickness / gap
- The possibility of insulation loss due to external pollution (metallic particles, ...)

Terminology:

Invariable gap: when the physical distance between two electrically conductive elements is not subject to significant variations or changes, whatever the constraints applied to the unit or part of the unit.

Variable gap: when the physical distance between two electrically conductive elements can be subject to variations or changes, according to the constraints applied to the unit or part of the unit (environmental tests, AIT operations, changes with time, use of insulation materials, ...).

Rigid insulating material: strong, resistant, non-porous, etc.

Non-Rigid insulating material: flexible, thinness (kapton, choterm, glue, varnish, etc.)

Reference **ABU-SAT-GDIEE-REQ-110**

Case A: Invariable gap, and gap > 1mm

The double insulation requirements ask for at least one insulating material (rigid or not); the selection of a non rigid insulating material is authorised if it is resistant whatever the constraints undergone during lifetime (manufacturing processes, AIT operations, environmental tests, launch and in-orbit environment operation). In this case of invariable gap, the minimum physical distance between two electrically conductive elements shall be greater than 1mm. (TBC)

*

Reference **ABU-SAT-GDIEE-REQ-111**

Case B: Variable gap, or gap < 1mm

In case of Variable gap, or when the physical distance between two electrically conductive elements is less than 1mm, the double insulation requirements ask for two insulating materials including one rigid insulating material. The non-rigid insulating material shall be resistant whatever the constraints undergone during lifetime (manufacturing processes, AIT operations, environmental tests, launch and in-orbit environment operation). (TBC)

*

REQ

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 36 / 213

The supplier shall provide a document that presents the solutions retained to comply and that demonstrates the compliance to the double insulation requirements; this document shall be submitted to Prime approval.

REQ

The double insulation is mandatory between any added metallic part (e.g. patches for radiation purpose) and any signal or supply. (TBC)

Examples of double insulation implementation (as guidelines):

- Pins inside connectors: case A
 - Double insulation requested between pins for example
 - Invariable gap due to ceramic
 - Insulating material due also to ceramic
- Connector connections: case B
 - Double insulation requested between pins and wires for example
 - Variable gap due to flexible wires
 - Two insulating materials due to jackets on connections, and wire outer covering
- PCB connections < 1mm: case B
 - Double insulation requested between solder joints and/or solder joints and metallic cover for example
 - Two insulating materials due to varnish on each solder joint
 - Two insulating materials due to kapton sheet and varnish for solder joints
- PCB tracks < 1mm: case B:
 - Double insulation requested between tracks for example
 - Two insulating materials due to epoxy and varnish
- Relay fixed on PCB: case A
 - Double insulation requested between relay case and PCB metallic chassis for example
 - Insulating materials due to epoxy and screw insulation and mechanical spacing (chassis + bleeding resistor)
- Board to board: case A
 - Double insulation requested between boards components and/or boards tracks
 - Invariable gap due to metallic chassis
 - Insulation performed by a dielectric cover

Application of double insulation requirements:

Reference **ABU-SAT-GDIEE-REQ-112**

The double insulation requirements concern the following elements:

- Power conductors up to, and including, the power bus protection.

- All cross-strapped signals from source to load (e.g. TC matrices, TM matrices, external supplies, etc.)
- Any element where insulation loss would result in electrical failure propagation (e.g. primary to secondary insulation loss)
- Any element where insulation loss would result in mission loss or degradation (e.g. majority voting)

*

5.2 ELECTRICAL INTERFACE REQUIREMENTS

5.2.1 Power interface

REQ

As a general rule, any power converter shall demonstrate by tests a stability margin greater than 60° & 10dB. (TBC)

5.2.1.1 Main bus voltage

The main bus voltage is controlled by the PSR in sunlight from the solar arrays, and in eclipse from the battery.

Reference **ABU-SAT-GDIEE-REQ-113**

At the loaded input connector of user, the nominal bus voltage is:

- Max. DC bus voltage : 102 V
- Min. DC bus voltage: 98V

The unit shall not exhibit failure, malfunction or unintended responses when subjected to a sine wave signal with the following characteristics :

- 2Vr.m.s. from 30 Hz to 1 KHz, decreasing by 20 db/decade up to 2 KHz
- 1 Vr.m.s from 2 KHz to 50 MHz

The voltage injected into the primary power leads shall be tuned at a sweep rate of 1 octave per minute, with at least 4 frequency check-ups per decade (ex. 1, 3 , 5 , 7 MHz) if no specific frequencies are specified.

The injected current can be limited to 1 A r.m.s, but under prime approval.

*

5.2.1.2 Current and Voltage ripple

Reference **ABU-SAT-GDIEE-REQ-114**

Equipment shall not inject on the power main bus, current ripple exceeding requirements of figure (metre figure page 120 de la DIET). (TBC)

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03

Page 38 / 213

Reference **ABU-SAT-GDIEE-REQ-115**

Equipments are required to meet full performance when the power main bus presents the voltage ripple defined in AD TBD (TBC)

*

5.2.1.3 Transients

5.2.1.3.1 Transient due to load switching

Units' switch-on induce load current variations, resulting in transient power bus voltage transients.

Reference **ABU-SAT-GDIEE-REQ-116**

Units shall be switched On in a sequential way only: multiple unit simultaneous switch-on is forbidden.

*

Reference **ABU-SAT-GDIEE-REQ-117**

For a step load, the bus voltage disturbance at bus user connector will not exceed $\pm 3\%$ with a leading or a falling edge rate of 50V/ms, followed by an exponential recovery time of less than 5 ms. The repetition rate of the transient due to load switching will not exceed 10Hz (TBC)

*

5.2.1.3.2 Transients due to fuse clearing event

During such events, the bus voltage will be within hatched areas - 100% to $\pm 10\%$ according to figure TBD.

Reference **ABU-SAT-GDIEE-REQ-118**

Platform equipment shall remain fully operational in case of a 1 ms power drop from 100V with 50V/ms minimum primary voltage slope at recovery, according to figure TBD.

*

Reference **ABU-SAT-GDIEE-REQ-119**

For power drops of up to 45 ms, all users are not required to meet performance parameters under these conditions, but must ensure that they survive the event and that no over stressing of the system occurs during or recovering from it, so that proper operations can resume (autonomously or not) after the power bus transient, with nominal performance.

These power fluctuation requirements are related to fuse blowing or to an instantaneous short circuit occurring on the power line.

The tests (plug in current test) shall be performed when the bus voltage starts from 0V to nominal voltage (100V) with $dV/dt \gg 1 \text{ V} / \mu\text{s}$.

The current drain when the power bus returns to its nominal voltage shall follow the criteria:

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 39 / 213

$I^2 dt < A$

DC power demand of the unit	A (fuse type: AEM P600L)	Fuse
P < 25W	$10^{-3} / 2$	≈ 1 A
25W < P < 50W	$4 \times 10^{-3} / 2$	≈ 2 A
50W < P < 120W	$2.5 \times 10^{-2} / 2$	≈ 5 A
P > 120W	1 / 2	≈ 10 A
TBD	TBD	≈ 15 A

The unit input current shall be recorded and included in the test report.

*

Reference ABU-SAT-GDIEE-REQ-120

Applicable to all spacecraft- units, all software and configuration data (e.g. RAM, registers) integrity shall be guaranteed during at least 100 ms with 0V power bus voltage, in order to be insensitive to the specified transients. (TBC: SMU)

*

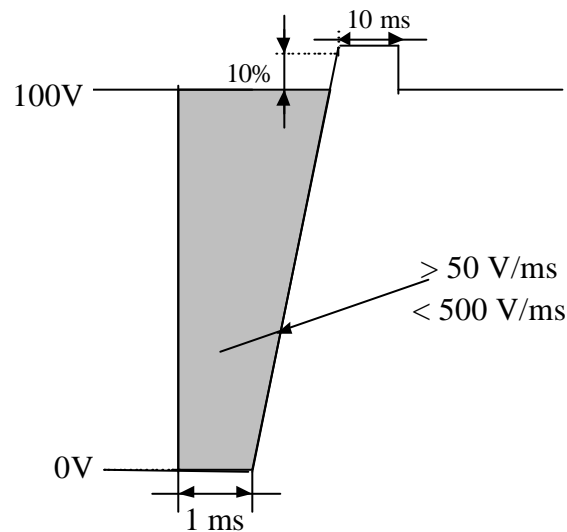
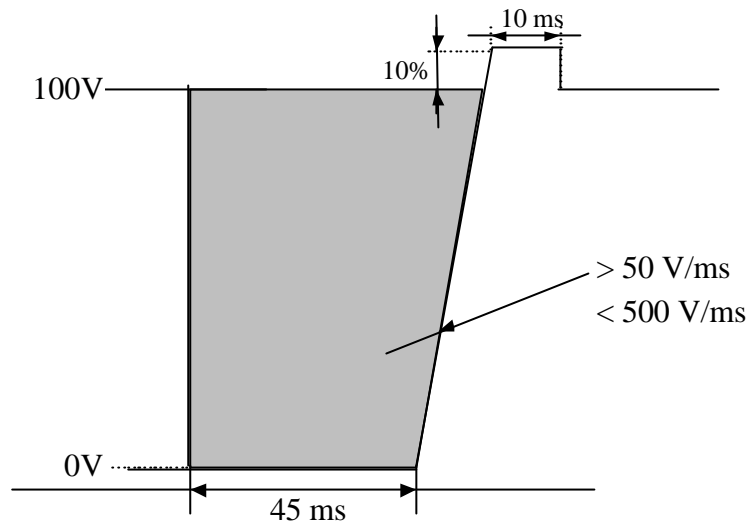


FIGURE: Transient due to fuse clearing

5.2.1.4 Abnormal Modes

REQ

Any power bus user shall provide a protection against main bus voltage polarity inversion, so that the unit will not be stressed (the use of parallel diodes is authorised, if in any case of main bus polarity inversion, the input power circuit from connectors to the protection diodes, can withstand without degradation a permanent 10A current). (TBC)

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 41 / 213

Reference **ABU-SAT-GDIEE-REQ-121**

All equipment shall not be stressed when power bus voltage is between 0V and 100V -0V +1V,, whatever duration and settling rate, or with over voltage up to 110V V during 10 ms. Fuse derating shall be met under these conditions.

*

Reference **ABU-SAT-GDIEE-REQ-122**

Under/Over Voltage Detection shall be implemented.

*

Reference **ABU-SAT-GDIEE-REQ-123**

For payload equipment, the following requirements apply:

- Full performances shall be achieved when the bus voltage is in the range 100V -0V +1V (voltage regulation precision) + 1V RMS (maximum bus voltage ripple) + 0V/-1V (range of power distribution voltage drop)
- The under voltage protection characteristics are:
 - Threshold: 94V +0V/-1V
 - Filtering at detection: 5ms minimum
 - Response time: 5ms maximum from detection to complete switch off
 - Restart shall be performed by external command only

*

Reference **ABU-SAT-GDIEE-REQ-124**

The platform equipment shall continue to operate functionally when the power bus voltage goes down to a voltage of 70 V DC, in the same conditions as under normal bus voltage, with the exception that the telemetry transmitter performance may be degraded by no more than 3 dB in output power and $\pm 10\%$ modulation index. (TBC)

*

Some critical platform units may have more stringent low voltage specified value in their equipment specification.

Reference **ABU-SAT-GDIEE-REQ-125**

There shall be no turn-off mode for the command subsystem. (TBC)

*

Reference **ABU-SAT-GDIEE-REQ-126**

For the bus voltage range defined in this document or any conceivable environmental conditions shall not result in spurious command generation or execution. (TBC)

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03

Page 42 / 213

5.2.1.5 Main bus protection

The general principle for the main power bus is that it is generated in such a manner that it is single point failure free at the distribution point (i.e. no failure of a part or insulation can cause the loss of the power bus) to ensure the bus remains reliable when users are connected to it.

Reference **ABU-SAT-GDIEE-REQ-127**

The users of the main bus shall protect the bus from overload caused by equipment failure.

*

Reference **ABU-SAT-GDIEE-REQ-128**

Protection shall be either by current limiting or by fuses, combined with double insulation between the power distribution point and the limiting device.

*

Reference **ABU-SAT-GDIEE-REQ-129**

The integrity of the double insulation shall be verifiable.

*

Reference **ABU-SAT-GDIEE-REQ-130**

If compliance with requirement 128 is implemented by any automatic means other than fusing or current limiting, a provision for ground override shall be made.

*

Reference **ABU-SAT-GDIEE-REQ-131**

Current limitation - If current limitation is chosen, the following requirements shall apply:

- After any equipment failure, the user shall limit the current consumption to 1.5 time the maximum Steady state current within 1 ms.
- For loads above 30 Watts, the current limiter shall initiate an automatic turn-off within 5 seconds.

*

Reference **ABU-SAT-GDIEE-REQ-132 (à ségréguer)**

Fuses - When fuses are used to protect the bus:

- The input relay or switch of the unit shall be sized to switch twice the manufacturer's fuse rating current.
- Fuses shall not be implemented inside equipment, except for distribution equipments, batteries & PSR
- Fuses shall be placed such that required fuse blowing current is available to the fuse.
- The fuse temperature shall be considered in the range [-40°C; +85 °C]. (TBC)
- Fuses in vacuum shall have a current derating according to ADTBD.
- For surge current, a margin ratio of at least 4 shall be considered with respect to the fuse manufacturer data.

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 43 / 213

- The fuse sizing shall include unit power off, all operational modes of the unit (e.g. including EHT switching on and off for TWTA payload units), and abnormal modes (§5.2.1.4) and all surge current situations (e.g. non exhaustive list: inrush current at switch on, with or without precharged filter; surge currents induced by §5.2.1.3 transients with maximum voltage rate of 500 V/ms and whatever the transient duration from 0ms to 45ms; surge currents induced by abnormal modes of §5.2.1.4)

The use of fuse shall be submitted to complementary analysis taking into account the fact that under short circuit condition on the main bus (or a loss of the main bus voltage), the charge stored in the DC/DC input filter ($1/2 CxV^2$) will be lost in the short circuit impedance inducing a power surge in the inline fuse.

- The fuse rating current shall not exceed 15 A, unless with the prior consent of the Prime Contractor.
- Redundant fuses may be used only with the prior consent of the Prime Contractor.
- Fuses which are used to protect any primary bus from primary power user failure, shall comply with the following requirement: any fuse shall blow in vacuum when energised for 45 ms with 4 times the fuse current rating, under all qualification environmental conditions.
- As far as possible, the fuses type shall be MEPCOPAL P600L; any other type choice shall be justified.

*

REQ

When current is subjected to significant variations (such as internally thermally regulated equipments, or as resistive loads) with respect to those conditions, the details of current variation shall be given (such as levels and duration, dissipation versus skin temperature, or consumption versus voltage).

Reference **ABU-SAT-GDIEE-REQ-133**

The Supplier shall be responsible for the fuse rating sizing, that shall be submitted to Prime for approval.

*

Reference **ABU-SAT-GDIEE-REQ-134**

The following form shall be fulfilled by the equipment designer each time a protection is needed (power bus, transformer output, telecommands, telemetries, internal functions ...) in order to:

- to assess internal fuse sizing,
- to define spacecraft centralised protection,
- to size external switching elements if any,
- to ensure compatibility of internal switching w.r.t. centralised protection,

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 44 / 213

OVERALL FUNCTION	Name of the function or set board e.g. :CVA or heater group 8
REF	Reference in the board part list for internal fuses e.g. :F10
IF(A)	Fuse rating e.g. : 2A
VF(v)	Fuse Max voltage e.g. : 125V
MANUFACTURER	Manufacturer's name and fuse type e.g. : MEPCOPAL P600L 125-2
FUSE FUNCTION	Describe the function of the fuse e.g. : Bus input protection or Capacitor S.C. failure protection
STATUS	I (internal to the unit) or O (outside the unit : centralised protection)
TYPE OF LOAD	R (resistive like heaters) with value R/L (coil) with characteristics @ 25°C P=cte (converter) with value (W) and inductor characteristics
Inom(A) / V(v)	Maximum steady state current w.r.t. nominal voltage and low voltage if applicable e.g. :0.5A/100V 0.54A/95V 0.6"A/80V 0.71A/20V
I _{max} (A) / t (ms)	Max worst case current w.r.t. voltage including pulsed load like telecommand, motor drive during the corresponding duration t. e.g. : 0.45A / 50ms @ 100V
INRUSH	Measured profile of primary (first connection), secondary (start up) and bus transient recovery inrush current if applicable I=f(t) at extreme voltage (70V, 80V,90V and 100V) with a dV/dt>1V/μs. (simulated profile acceptable at the beginning)
SWITCHING	To identify when existing if a mechanical switching at unit level or an electronic switching is compliant with the selected fuse according to the present document requirements e.g. :GP250 (2A/100V) or Electronic ON/OFF ...
Nber OF SWITCHINGS	Number of switching expected at unit level if applicable e.g. :1/week or none or N/A
OTHER PROTECTIONS	To identify all other protections in series (upstream or downstream) with thresholds and timings Under Voltage UV Overcurrent OVI OverVoltage OVV This shall be indicated even if no fuse is concerned e.g. : Main bus UV 20V/20ms 15V OVI 1A/<1ms
ELECTRICAL SCHEMATIC	Electrical schematic of parts around the fuse (e.g. input filter) with their value

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03

Page 45 / 213

Reference **ABU-SAT-GDIEE-REQ-135**

When fuse sizing is driven by transient margin and leads to a static sizing derating factor lower than 20%, the equipment design shall be modified to lower inrush current.

*

Reference **ABU-SAT-GDIEE-REQ-136**

For units with power consumption above 300 Watts on a given power line, the Prime Contractor shall be consulted on the manner in which the load shall protect the power bus. For those units, the failure modes leading to EMC perturbations on the power bus shall be clearly identified and provided with quantitative current effects, and submitted for Prime approval. In any case of failure, the unit current ripple shall not exceed the unit conducted emissions specification +6 dB.

*

Reference **ABU-SAT-GDIEE-REQ-137**

No single failure in the spacecraft including failures of wiring, connectors, etc., shall open or short the main power bus or affect definitely the normal operation of the spacecraft (Single Point of Failure), other than the possible loss of the load path where the failure occurred, provided that the corresponding function is redounded (and not affected by the failure).

*

Reference **ABU-SAT-GDIEE-REQ-138**

All functions with primary or secondary referenced interfaces shall withstand without stress (ratings can be reached) a dc common mode voltage from -20V to +20V for whatever duration with respect to the electrical ground reference (mechanical structure, chassis, secondary 0V). This requirement is applicable whatever ON or OFF state of the unit. (TBC)

*

5.2.2 Data Handling Interfaces for payload units

This part defines the requirements for all signals between data bus subscribers and users: High Level Command (HLC), Very High Level Command (VHLC), High Power Command (HPC), 16-bit Memory Load Command (ML), Direct Telecommand (DTC), Direct Telemetry (DTM), Analogue acquisition (ANA), temperature/resistor acquisition (TEMA/RESA), Bi-level acquisition (TM BL N), switch closure relay status acquisition (TM BL D/S), and Low Speed Serial Bus Interface (LSSB).

Emitted signals concern source equipments and received signals concern load equipments in this part.

Reference **ABU-SAT-GDIEE-REQ-139**

The telecommands and switch closure acquisitions matrix allocation (implementation inside the matrix) shall be flexible; any hypothesis of row or column grouping shall be agreed with Prime.

*

Reference **ABU-SAT-GDIEE-REQ-140**

The command interface circuit design shall be such as to ensure that no single failure of its components, when all possible failure modes are considered, shall allow a short circuit condition to be 'seen' across the telecommand input connection and the return, or between either of the pins and chassis.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03
Page 46 / 213

5.2.2.1 General Requirements and conventions

Reference **ABU-SAT-GDIEE-REQ-141**

The following requirements and conventions shall be applied:

- Timing:
 - Signal duration: time between crossing points of fall and rise time to 50% of the measured full amplitude.
 - Signal rise, fall time: maximum time between 10% and 90% of the nominal voltage swing.
 - Delay between 2 signals: time between the voltage crossing point 50 % of the full amplitude level.
- Driver characteristics shall be considered at the level of the source equipment output connector; harness voltage drop will be specified for each case.
- For serial transmission, MSB is transmitted first.
- Care should be taken to ensure that input levels do not exceed manufacturer's rating even when units are un-powered.
- The receiver interface design shall permit the power-on of unit without damage when the electrical interfaces are not terminated or driver unit is off.
- Any receiver interface shall be provided with a low pass filter of cut off frequency less than 2kHz, unless inconsistent with functional operation.

*

Reference **ABU-SAT-GDIEE-REQ-142**

For HLC, HPC & DTC, the following requirements and conventions shall be applied:

- The command lines (rows and columns) shall be double insulated inside equipment; the user shall not impose any potential or grounding reference on any row or column with an impedance lower than 500 kΩ.. The capacitance between any row and EGRP, and between any column and EGRP, at load side, shall not exceed 50 pF.
- All telecommands, except ML commands, are matrix telecommands. All telecommand users shall provide two diodes in series with the commanded device at any matrix node, and shall not implement quenching diodes at user side. If the command user is not redounded (e.g. non redundant payload switch), the 2 diodes shall be replaced by a diode network allowing the diode function whatever any single failure .

*

Reference **ABU-SAT-GDIEE-REQ-143**

For TMBLD and DTM; the following requirements and conventions shall be applied:

- The user shall not impose any potential or grounding reference on any row or column with an impedance lower than 500 kΩ.. The capacitance between any row and EGRP, and between any column and EGRP, at load side, shall not exceed 500 pF. The capacitance between row and column, at load side, shall not exceed 50 pF.

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03

Page 47 / 213

- The matrix switch closure acquisition are generated through a matrix organisation. Two diodes shall be provided in series with each switch.

*

5.2.2.2 High-level command (HLC)

HLC commands are dedicated to all units, except RF switches.

The command signal is a differential single positive voltage pulse (one row is pulled up to a positive voltage and one column is pulled down the secondary 0V so that only the device at the node of the activated row and column is commanded) distributed to the user for relay driving or general logic control application.

Reference **ABU-SAT-GDIEE-REQ-144**

The HLC duration that shall be considered is 48 ms \pm 5 ms.

*

5.2.2.2.1 HLC Signal source characteristics

Reference **ABU-SAT-GDIEE-REQ-145**

The unit shall comply with the following HLC signal source characteristics:

- Type of source: matrix power drivers
- Output voltage: measured at the source equipment output connector between a row and a column when loaded by the load defined in 5.2.2.2.2-a))
- True state « 1 »: $+22\text{ V} < U1 < +29\text{ V}$ during the command
- False state during inductive load energy restitution (100ms max.), the row and column voltages with respect to EGRP, will be:
 - $-2\text{ V} < \text{Row voltage} < +29\text{ V}$ (+30.8V in case of failure)
 - $0\text{ V} < \text{Column voltage} < +47\text{ V}$
 - These voltages are seen by all the matrix users connected on the same row or the same column.
 - After inductive load energy restitution, the driver false state sink current shall not exceed 100 μA .
- At any time, the differential voltage between row and column is thus in the range - 49V to +29V (+30.8V in case of failure).
- Signal shape see figure 6.2 / 2
- Harness voltage drop $< 1.0\text{ V}$
- Failure cases:
 - The load shall withstand a true state voltage of +30.8V with nominal HPC telecommand duration.
 - The load shall withstand a telecommand duration of up to 10 seconds

5.2.2.2.2 HLC Signal load characteristics (user side)

Reference **ABU-SAT-GDIEE-REQ-146**

The unit shall comply with the following HLC signal source characteristics on user side:

- Load impedance $60\ \Omega$ min., $5\ \text{k}\Omega$ max.; in parallel with $1\ \text{nF}$ max; plus 2 diodes in series.
- The command shall not be executed (user load not susceptible) when a $+40\ \text{V}$ row voltage is applied while the column is connected to secondary OV through an uncharged $10\ \text{nF}$ capacitor. The compliance shall be demonstrated by analysis or test showing that this transient energy does not lead to command execution.
- ON/OFF commands of a given equipment or function shall not share the same return (column) unless authorised by the FMECA analysis results.

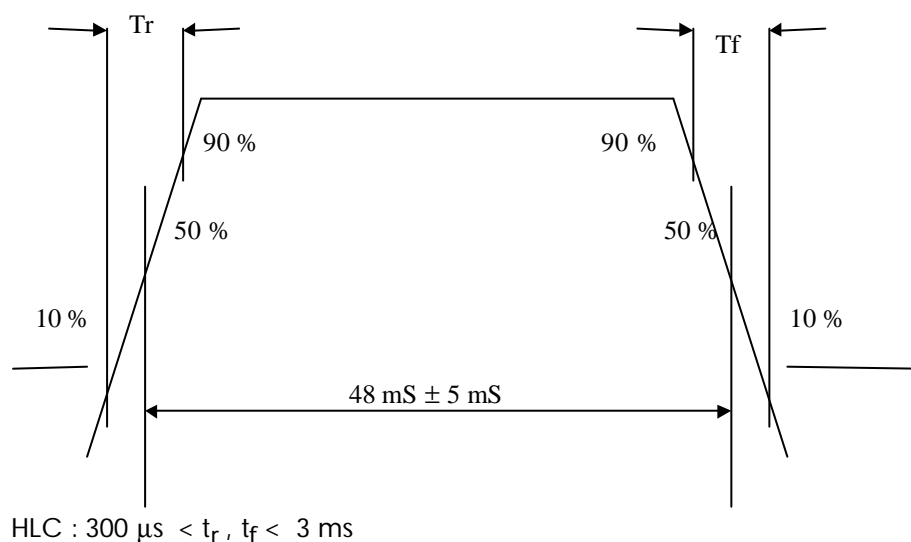


FIGURE: HIGH-LEVEL COMMAND: SIGNAL WAVEFORM AND TIMING DIAGRAM

5.2.2.3 High power command (HPC)

The command signal is a differential positive voltage single pulse (one row is pulled up to a positive voltage and one column is pulled down to the secondary OV so that only the device at the node of the activated row and column is commanded) distributed to the T coaxial and wave-guide switches of the payload (matrix organisation).

5.2.2.3.1 HPC Signal source characteristics

Reference **ABU-SAT-GDIEE-REQ-150**

The unit shall comply with the following HPC signal source characteristics:

- Type of source: matrix power drivers
- Output voltage: measured at the source equipment output connector between a row and a column when loaded by the load defined in §5.2.2.3.2
- True state « 1 » $+22\text{ V} < U1 < +29\text{ V}$ during the command
- False state during inductive load energy restitution (100ms max.), the row and column voltages, with respect to EGRP, will be:
 - $-2\text{ V} < \text{row voltage} < +30.8\text{V}$
 - $0\text{V} < \text{column voltage} < +47\text{ V}$
 - These voltages are seen by all the matrix users connected on the same row or the same column
 - After inductive load energy restitution, the driver false state sink current shall not exceed 100 μA .
- At any time, the differential voltage between row and column is thus in the range -49V to +30.8V
- Signal shape see figure 6.2/4
- Harness voltage drop $< 1.5\text{V}$
- Failure cases:
 - The load shall withstand a true state voltage of +40V with nominal telecommand duration.
 - The load shall be in an unambiguous state when commanded with HLC telecommand

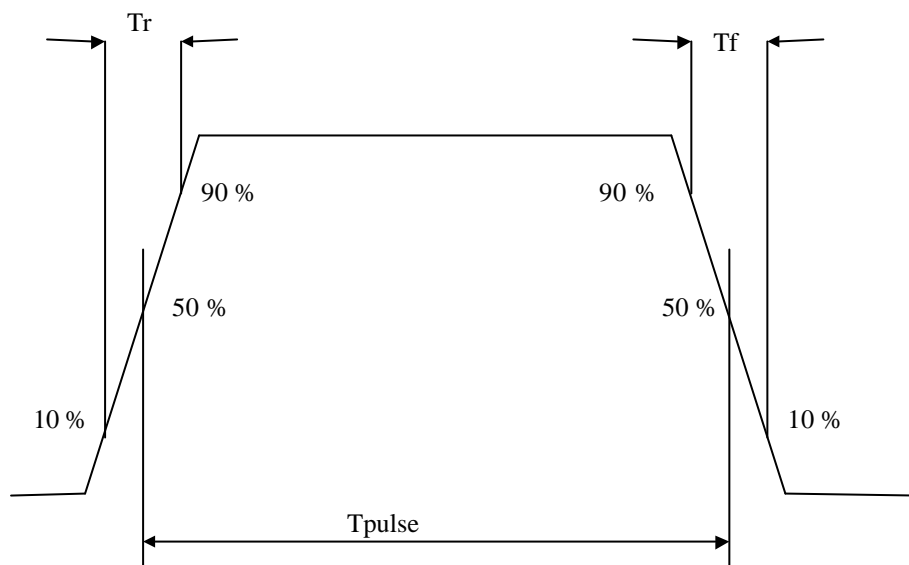
*

5.2.2.3.2 HPC Signal load characteristics (user side)

Reference **ABU-SAT-GDIEE-REQ-151**

The unit shall comply with the following HPC signal source characteristics (user side):

- Load impedance $56\ \Omega$ min., 5 k Ω max.; in parallel with 1 nF max; plus 2 diodes in series.
- The command shall not be executed (user load not susceptible) when a +40V row voltage is applied while the column is connected to secondary 0V through an uncharged 10 nF. The compliance shall be demonstrated by analysis or test showing that this transient energy does not lead to command execution.
- ON/OFF commands of a given equipment or function shall not share the same return (column) unless authorised by the FMECA analysis results.



HPC : $T_{pulse} = 750 \text{ ms} \pm 10 \text{ ms}$

FIGURE: HIGH-POWER COMMAND: SIGNAL WAVEFORM AND TIMING DIAGRAM

*

5.2.2.4 16-bit serial memory load command (ML)

Refer to §5.2.2.9 of this document for the Low Speed Serial Bus (LSSB) requirements.

5.2.2.5 Single Ended Analogue Acquisition (ANA SE)

The analogue acquisition signal appears in the form of a voltage varying within two defined limits. The voltage to be acquired is periodically sampled and will be numerically coded on 12 bits over the full scale range, with a full performance of 8 bits.

5.2.2.5.1 ANA SE Signal source characteristics (at generation side)

Reference **ABU-SAT-GDIEE-REQ-152**

The unit shall comply with the following ANA SE signal source characteristics:

- type: voltage source
- Voltage range: 0 to + 5 V
- Output impedance: $R_s < 1 \text{ k}\Omega$
- Protections:
 - Short circuit: a permanent short circuit to ground shall not cause any damage, nor shall it affect the performance of any part than the output concerned.
 - Over voltage: the application of a $\pm 16 \text{ V}$ over voltage (through a $4 \text{ k}\Omega$ resistor) on the output line of the analogue source shall not damage the source. In any case of source single failure, the source output voltage shall remain in the $\pm 16 \text{ V}$ range.

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03

Page 51 / 213

- Emission noise shall be less than 200mVpp (20 MHz bandwidth measurement) .
- The output shall not be susceptible (no offset no stress) when a signal 400 mVpp square wave 1 MHz is injected.
- Signal reference: the analogue acquisition reference shall be connected at generation level, to the chassis of the equipment (EGRP). Single-ended analogue acquisitions shall use structure return.

*

5.2.2.5.2 Signal load characteristics (at acquisition side)

Reference **ABU-SAT-GDIEE-REQ-153**

The unit shall comply with the following ANA SE signal source characteristics (at acquisition side):

- The receiver input impedance shall be greater than 100 k Ω .
- Each analogue signal acquisition interface shall include a first order low pass filter, with a cut-off frequency in the range from 10Hz to 2kHz.
- The interface shall withstand input voltages in the range from -16V to +16V.
- When the input voltage is between -16V and 0V, or between +5V and +16V, the analogue to digital conversion chain shall provide a full scale saturation corresponding respectively to 0V and +5V.

*

5.2.2.6 Temperature (TEMA) and Resistance Switch Position (RESA) Acquisition

This signal is obtained from a thermistor or a resistor located in the equipment which temperature or resistance is to be monitored.

Reference **ABU-SAT-GDIEE-REQ-154**

The thermistor or resistor shall be isolated within the equipment with respect to its chassis by at least 10M Ω .

*

Reference **ABU-SAT-GDIEE-REQ-155**

The thermistor or resistor shall not be conditioned (polarisation) inside the equipment.

*

Reference **ABU-SAT-GDIEE-REQ-156**

The thermistor or resistor shall be in the range 900 Ω to 400k Ω .

*

Reference **ABU-SAT-GDIEE-REQ-157**

For temperature acquisition, the sensor accuracy shall be better than 1°C in the range -20°C to +85°C.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03

Page 52 / 213

Reference **ABU-SAT-GDIEE-REQ-158**

The preferred thermistor part is FENWALL 526-31-BS09-153 (variant 32 part number MMS) corresponding to TEMA1E 15k Ω @ 25°C negative temperature coefficient. Other thermistor types shall be submitted to the Prime approval.

*

Sets of resistors may be connected by auxiliary telemetry switches to generate a resistance signal indicating the set position of RF switches.

Reference **ABU-SAT-GDIEE-REQ-159**

The Resistance Acquisition (RESA) signal shall be handled exactly as for the thermistor signals. A maximum of 16 levels on a given RESA shall not be exceeded.

*

5.2.2.7 Bi-level acquisition (TMBL NE)

5.2.2.7.1 General

Each bi-level digital channel is used to acquire a status bit. The bi-level digital information is presented in the form of a voltage signal which can take the following two distinct values:

Reference **ABU-SAT-GDIEE-REQ-160**

The logical level « 1 » shall correspond to positive voltage

*

Reference **ABU-SAT-GDIEE-REQ-161**

The logical level « 0 » shall correspond to zero voltage.

*

5.2.2.7.2 TMBL NE Source characteristics (generation side)

Reference **ABU-SAT-GDIEE-REQ-162**

The unit shall comply with the following TMBL NE signal source characteristics (at generation side):

- « 0 » logical level V0 (loaded through the encoder input): $0\text{ V} < V0 < + 0.5\text{ V}$
- « 1 » logical level V1 (loaded through the encoder input): $+ 3.5\text{ V} < V1 < + 5.5\text{ V}$
- Output impedance: $R_s < 10\text{ k}\Omega$.
- Protections:
 - Short circuit: a permanent short circuit to ground shall not cause any damage, nor shall it affect the performance of any part than the output concerned.
 - Over voltage: the application of a $\pm 16\text{ V}$ over voltage (through a 4k Ω resistor) on the output line of the analogue source shall not damage the source. In any case of source single failure, the source output voltage shall remain in the $\pm 16\text{ V}$ range.

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03

Page 53 / 213

-
- Emission noise shall be less than 200mVpp (20 MHz bandwidth measurement).
 - The output shall not be susceptible (no logical state change or stress) when a signal 400 mVpp square wave 1 MHz is injected.
 - Signal reference: The bi-level acquisition reference shall be connected at generation level, to the chassis of the equipment (EGRP). Structure return shall be used.
-

*

5.2.2.8 Switch closure acquisition (TM BL D/S)

5.2.2.8.1 Matrix switch closure acquisition (TM BL D)

Matrix switch closure acquisition (differential contact) will be performed via a matrix acquisition structure.

Typical acquisition pulse duration = 40 ms corresponding to matrix row voltage pulse, at the end of which the acquisition is sampled.

The contact measure furnished by the indicator allows to check the corresponding commands.

The switch closure matrix organisation is not compatible with active (0-5V) bi-level TM.

Reference **ABU-SAT-GDIEE-REQ-163**

The contact characteristics that shall be considered are:

- the user shall provide two diodes in series with the switch
 - continuous current capability > 4 mA
 - leakage current (OFF state) < 10 μ A
 - the voltage drop (when status is ON) generated by a 4 mA current shall not exceed 2.4V (including the voltage drop of the 2 serial diodes) at user side
 - maximum transient current < 20 mA
 - maximum polarisation voltage: + 20V
 - signal reference: the status and status return lines shall be isolated from equipment chassis or any potential reference as per §5.2.2.1
 - The use of optocouplers is strongly not recommended, and shall be brought to Prime knowledge for analysis and approval .
-

*

5.2.2.8.2 Single ended switch closure acquisition (TM BL S)

Direct switch closure acquisition will not be performed via a matrix acquisition structure, but with dedicated circuits referenced to the secondary 0V.

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 54 / 213

Reference **ABU-SAT-GDIEE-REQ-164**

The contact characteristics shall be the same as for §5.2.2.8.1 except for the following requirements:

- the direct switch closure acquisition return shall be connected at switch side, to the chassis of the equipment
 - the switch shall not provide two diodes in series with the switch contact, but only the switch contact.
 - continuous current capability > 1mA
 - contact resistance: ON state < 200 Ω
 - OFF state > 1M Ω
-

*

5.2.2.9 Low Speed Serial Bus (LSSB)

Reference **ABU-SAT-GDIEE-REQ-165**

Units on LSSB shall be compliant to the following LSSB characteristics as described in the present chapter.

*

5.2.2.9.1 General Description

The purpose of the serial bus is to allow serial data transfer between one bus controller (BC) or source equipment (master) to several user terminals (UT) or slave equipments.

Two different data transfers can be identified:

- Serial command: a 16 bit word is sent by the bus controller to the terminals
- Serial Telemetry (Acquisition): two 16 bit words are sent repeatedly by one terminal to the bus controller

The bus consists of five differential lines:

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 55 / 213

SAMPLE_CMD	Validates the shift clock during serial commands	Source : Controlle r	Destination : All terminals
SAMPLE_ACQ	Validates the shift clock during serial telemetry acquisitions	Source : Controlle r	Destination : All terminals
CK	Shared clock sent during serial commands and serial telemetry acquisitions to synchronise the data transfer	Source : Controlle r	Destination : All terminals
DATA OUT	Mono-directional data bus passing serial command data towards all the terminals under the control of the bus controller	Source : Controlle r	Destination : All terminals
DATA IN	Mono-directional data bus passing telemetry data to the controller under the control of one terminal, controlled by one terminal during telemetry data acquisition	Source : One terminal	Destination : Bus controller

Each of the four differential lines from the bus controller to the terminals has the architecture shown in the following figure:

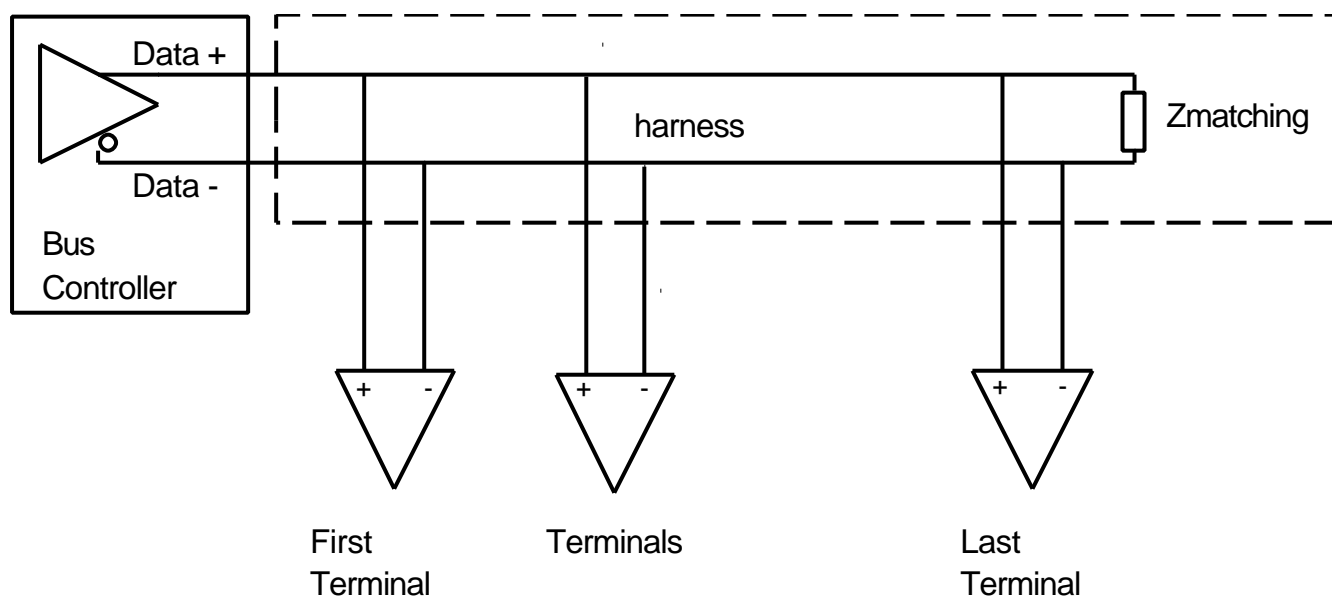


Figure: Architecture of CK, SAMPLE-CMD, SAMPLE-ACQ and DATA OUT lines

The single differential line from each terminal to the bus controller has the architecture shown in the following figure:

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 56 / 213

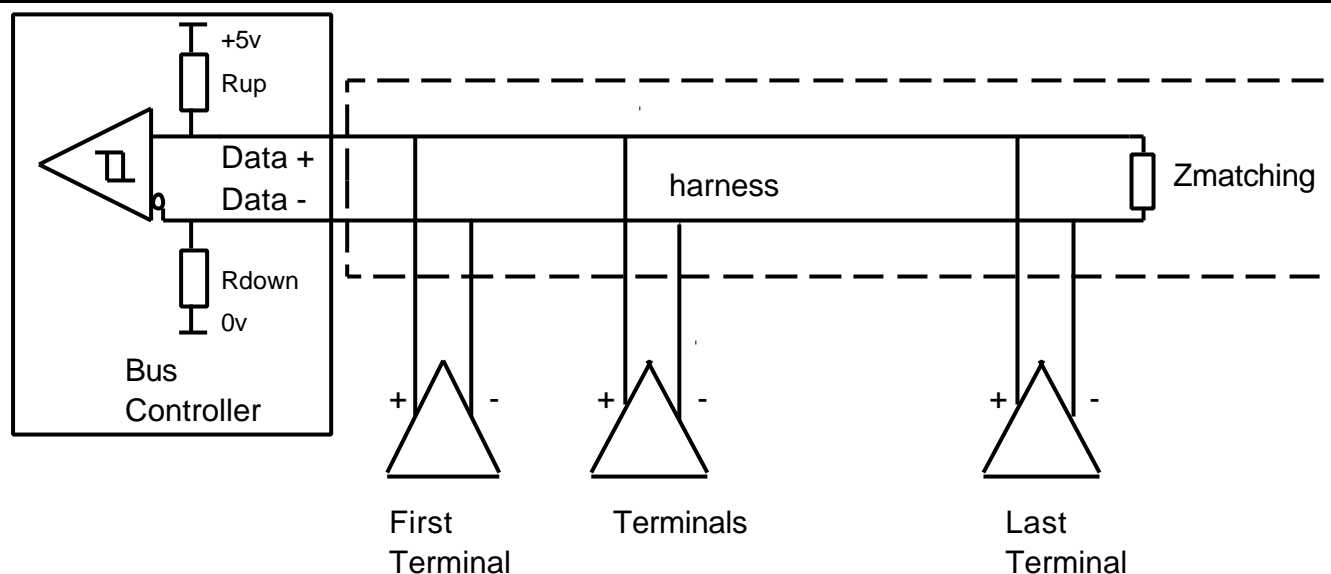


Figure: Architecture of DATA IN line

5.2.2.9.1.1 CK, SAMPLE-CMD, SAMPLE-ACQ and DATA OUT lines

Each of the four differential lines from the bus controller to the terminals, at its source, can have 3 functional states as defined in figure "Bus voltage definition" (Bus controller powered):

- High state (logic level 1)
- Low state (logic level 0)
- Undefined state
- When un-powered, the bus controller functional state will be defined as the so-called OFF state. Each terminal destination can be in 3 different states as defined in figure "Bus voltage definition"
- High state detected (logic level 1)
- Low state detected (logic level 0)
- Transient state (hysteresis zone)

In all these cases, the receiving terminal voltage is determined by the single source when the source is active, and lies in the inactive Hysteresis Zone when the source is inactive.

5.2.2.9.1.2 DATA IN Line

The single differential line from each terminal to the bus controller, at its source, can have two functional states as defined in figure "Bus voltage definition"

- Low state (logic level 0)
- Tri-state or OFF state (inactive state)
- When un-powered, the terminal functional state will be defined as the so-called OFF state.
- The bus controller destination can be in 3 different states as defined in figure "Bus voltage definition"

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 57 / 213

- High state detected (logic level 1)
- Low state detected (logic level 0)
- Transient state (hysteresis zone)

In this case, the receiving bus controller voltage is determined by any one terminal source when the source is actively in the low state, and by its own internal configuration when an active terminal source is in the high state, or when all terminal sources are inactive. In proper operation, only one source will be active, and the architecture shown allows the parallel connection of all the terminals to the one DATA IN bus.

The bus signals shall be compliant with the following functional definition:

- The SAMPLE -CMD, the SAMPLE-ACQ and the CK signals shall be driven by the bus controller in the high state when active, and in the low state when inactive.
- The DATA-OUT signal shall be a logic « 1 » when driven in the high state by the bus controller or a logic « 0 » when in the low state.
- The DATA-IN signal shall be a logic « 1 » when in the tri-state from any terminal and a logic « 0 » when driven in the low state by a terminal.

For future growth, the bus controller shall be able to change the SAMPLE-CMD and SAMPLE-ACQ level convention.

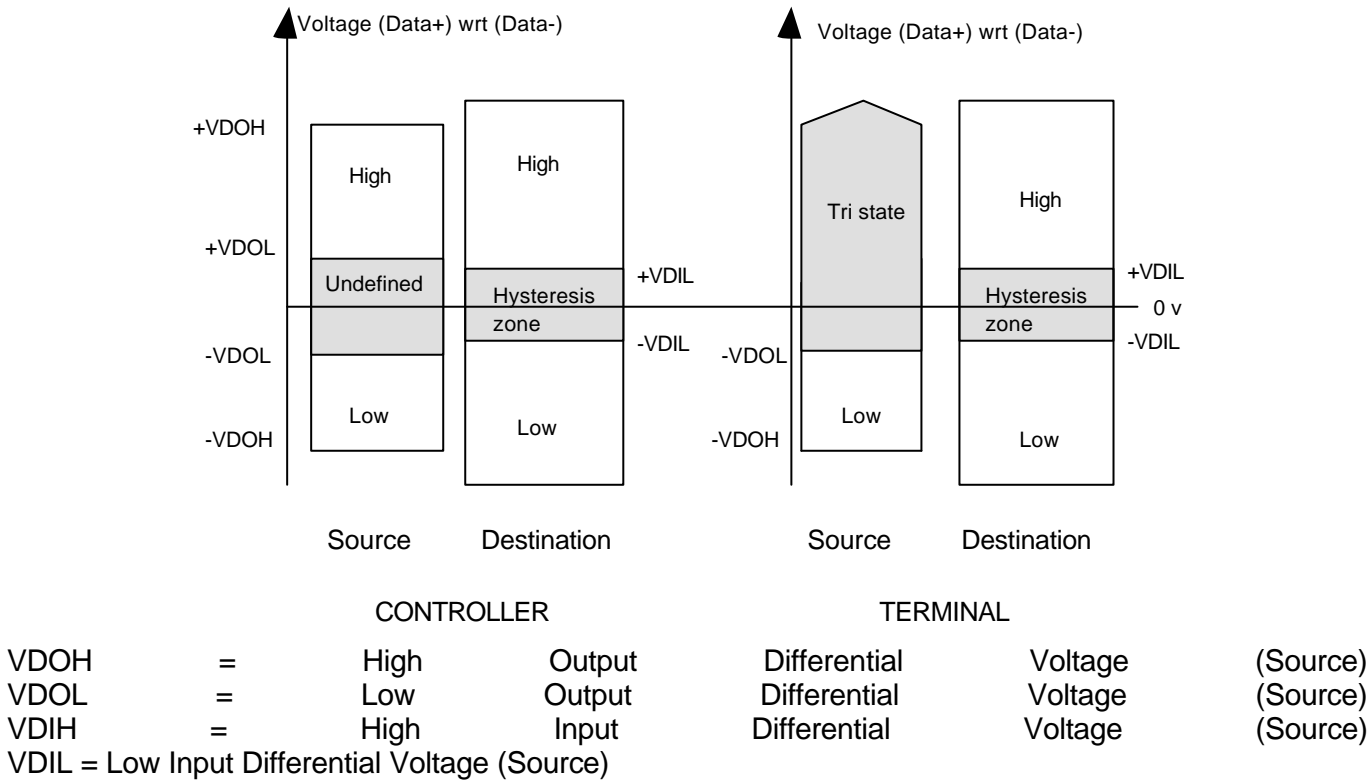


Figure : Bus Voltage Definition

5.2.2.9.2 Electrical Signals Characteristics

5.2.2.9.2.1 Source transmitter

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 58 / 213

Each transmitter shall meet the following specification.

5.2.2.9.2.1.1 Common characteristics

Max differential output voltage: $|V_{DOH}|$ 5.5 V

Min differential output voltage: $|V_{DOL}|$ 1.5 V

Fault voltage emission: +/- 8V max.

Over voltage susceptibility An application on any bus line of an over voltage +/- 16V via an impedance of

1 k Ω in the range DC to 1 MHz shall not damage the transmitter (whatever the ON or OFF state) or cause any failure propagation on source equipment or towards the destination users.

5.2.2.9.2.1.2 Specific bus controller characteristics

Transmitter type: Differential driver

Output load: Up to 32 terminal receivers

Level « 1 » (Data + voltage) - (Data - voltage) > +VDOL for all load conditions (32 terminal receivers and matching impedances)

Level « 0 » (Data + voltage) - (Data - voltage) < -VDOL for all load conditions (32 terminal receivers and matching impedances)

OFF state differential: SAMPLE-CMD line: - 0.3 V to + 0.3 V output voltage level: Other lines: -VDOL to + VDOL

No emission level: Once equipment has been initialised, the transmitter output level shall be level « 0 » in the case of no data emission

Transmitter short circuit: A permanent short circuit due to harness or output protection failure circuit between each output line and the source equipment ground or between output differential lines shall not damage the transmitter or cause any failure propagation on source equipment.

5.2.2.9.2.1.3 Specific terminal characteristics

Transmitter type: Differential driver

Level « 1 »: Transmitter in tri-state or OFF state

Level « 0 »: (Data + voltage) - (Data - voltage) < -VDOL for all load conditions (Bus controller receiver, matching load and others terminal emitters)

Output leakage current: +/- 10 μ A transmitter in tri-state or OFF

Output capacitance: C_{out} < 20 pF

Single failure: No failure propagation towards the redundant terminal bus shall occur in the event of a transmitter single failure. Failure propagation probability on the bus shall be lower than 1 fit over the mission

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03

Page 59 / 213

Transmitter short circuit: A permanent short circuit between each output line and the source equipment ground and between output differential lines shall not damage the transmitter or cause any failure propagation on source equipment or towards the redundant terminal bus.

Bus contention: The emitter shall withstand an abnormal simultaneous terminal emission on the DATA IN bus

No emission level : Once equipment initialised, the transmitter output level shall be the tri-state.

5.2.2.9.2.2 Receiver characteristics

5.2.2.9.2.2.1 Common characteristics

Receiver type: Differential

Threshold voltage: $|VDIL| = 1 \text{ V max}$

Input impedance : $R_{in} > 50 \text{ k}\Omega$ on each input line (excluding bus controller pull-up and pull down resistors)

Input capacitance: $C_{in} < 20 \text{ pF}$

Noise immunity: A minimum input hysteresis of $0,6 \text{ V (+/- } 0.3\text{V)}$ shall be guaranteed

Common mode voltage: All the receiver performances shall be maintained with a maximum common mode voltage of $\pm 5 \text{ V}$ in the range DC to 1 MHz. (rectangular signal, maximum rise time 50 nsec).

5.2.2.9.2.2.2 Specific bus controller characteristics

Receiver type: Differential

Pull up resistor: A pull up resistor of $150 \Omega \pm 5 \%$ shall be connected between the Data in + input line and the bus controller internal 5V. This resistor shall withstand a continuous short circuit between the Data In + line and the ground.

Pull down resistor: A pull down resistor of $150 \Omega \pm 5 \%$ shall be connected between the Data in - Input line and the bus controller internal ground. This resistor shall withstand a continuous short circuit between the Data In - line and a +5v supply.

Pull up/down config.: These resistors shall be configurable at board level.

Single failure: No failure propagation on source terminal equipment shall occur in the event of a receiver interface single failure (input serial impedance case)

Input voltage range: The receiver, without pull-up and pull-down resistors, shall withstand an input voltage in the range -16V to $+16\text{V}$.

5.2.2.9.2.2.3 Specific terminal characteristics

Single failure: No failure propagation towards the redundant terminal bus shall occur in the event of a transmitter single failure. Failure propagation probability on the bus shall be lower than 1 fit over the mission.

Noise immunity: When the receiver is in its hysteresis range, its output shall not change if no input differential voltage is applied.

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03
 Page 60 / 213

Input impedance: The input resistors shall be matched to 1 %

Input current: The input offset current shall be in the range $[-75\mu\text{A}, +75\mu\text{A}]$ for either one of the inputs when submitted to a voltage in the range $[-5\text{V}, +10\text{V}]$

Input offset current: The input offset current shall be in the range $[-1\mu\text{A}, +1\mu\text{A}]$ (Input Connected to ground)

Input voltage range: The receiver shall withstand an input voltage in the range -16V to $+16\text{V}$.

5.2.2.9.2.3 Terminal Equipment Bus Selection

Every terminal bus user shall be connected to prime and redundant (A and B) serial buses. The connection to each bus shall be made via an independent hardware interface.

The terminal user shall only process commands and respond to telemetry acquisition requests received via one bus at a time. Selection of bus A or bus B by the terminal equipment shall be performed by one of the two methods, either as a result of external configuration control or by an autonomous selection process.

Any failure occurring on one bus or on one command or telemetry bus interface shall not propagate to the redundant bus, or to the selection mechanism, so as to prevent its use.

5.2.2.9.2.3.1 External Configuration Control

In the case of external configuration control, switches within each terminal equipment shall be used to perform the selection between operation with A or B serial buses. The switches shall be controlled by external pulse commands.

5.2.2.9.2.3.2 Autonomous Bus Selection

In the case of autonomous bus selection, the terminal equipment shall select operation with either bus A or bus B.

The terminal user equipment shall select the bus that is currently, or most recently, active.

In the event of any single point failure occurring on one bus, the selection process shall ensure that the user terminal is maintained via the remaining operational bus.

Bus selection shall be performed on the rising edge of the SAMPLE-CMD signal.

Once the bus has been selected, the terminal bus user shall use the A (respectively B) signals for CK, DATA OUT, DATA IN, SAMPLE-ACQ, SAMPLE -CMD.

5.2.2.9.2.4 Bus Harness

The equipment shall be connected to the bus controller via a harness with the characteristics defined below. All command and telemetry interfaces shall operate within specification under these conditions.

- Harness type: 1 twisted shielded pair bifilar AWG 26 for each differential CLK, SAMPLE-CMD, SAMPLE-ACQ, DATA OUT and DATA IN line.
- Max length: $< 8\text{ m}$
- Shielding: The harness shielding shall be connected to the structure at grounding brackets level (both sides) externally of the equipment

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

- User number: 1 to 32 terminals may be connected on the bus in daisy chain
- Terminal or bus controller:
 - stub length: < 0.3 m (from bus connection to input circuits)
 - Matching stub length: < 0.5 m (from bus connection to matching impedances)
 - Matching impedance: These impedances are connected at the extremity of the cables away from the bus controller (the other extremity is the bus controller). For all the lines except the DATA IN, the impedance is a capacitance of 10 nF in series with a 57Ω +/- 5% resistor. For the DATA IN line the impedance is a 300Ω +/- 5% resistor. This resistor shall withstand a continuous dissipation of 0.5 W.

5.2.2.9.3 Timing Requirements

The figures specify the timings at Transmitter output level (Tr) and at Receiver input level (R).

5.2.2.9.3.1 General Sequence

The timing between two data transfer blocks (signal on the same bus), at terminal input level, is shown in the following figure:

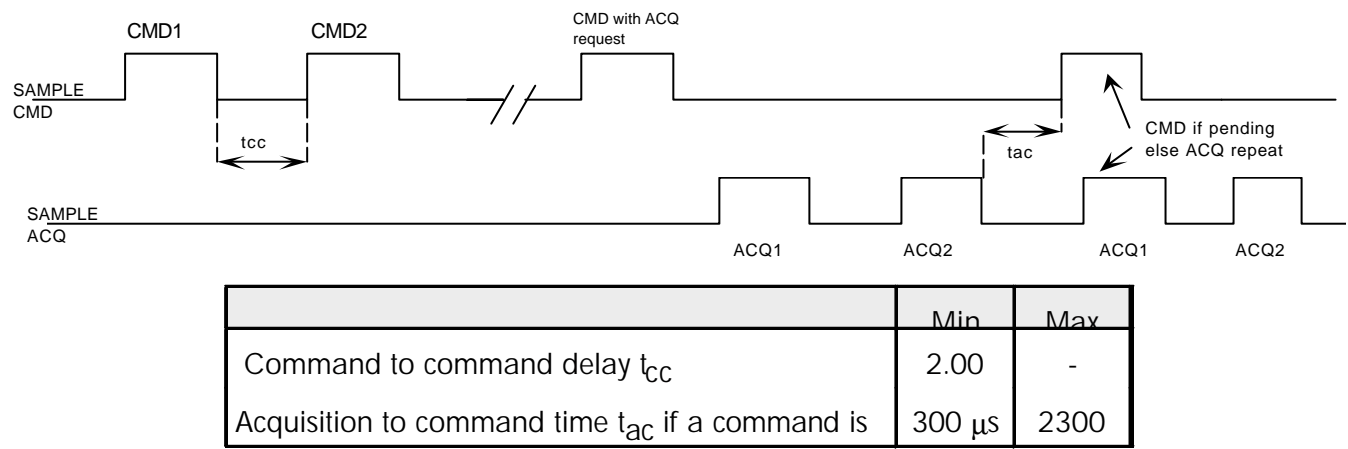


Figure: DATA TRANSFER BLOCK TIMING

5.2.2.9.3.2 Serial Commands

The timing of the 16-bit serial command signals shall be as shown in the following figure and Table.

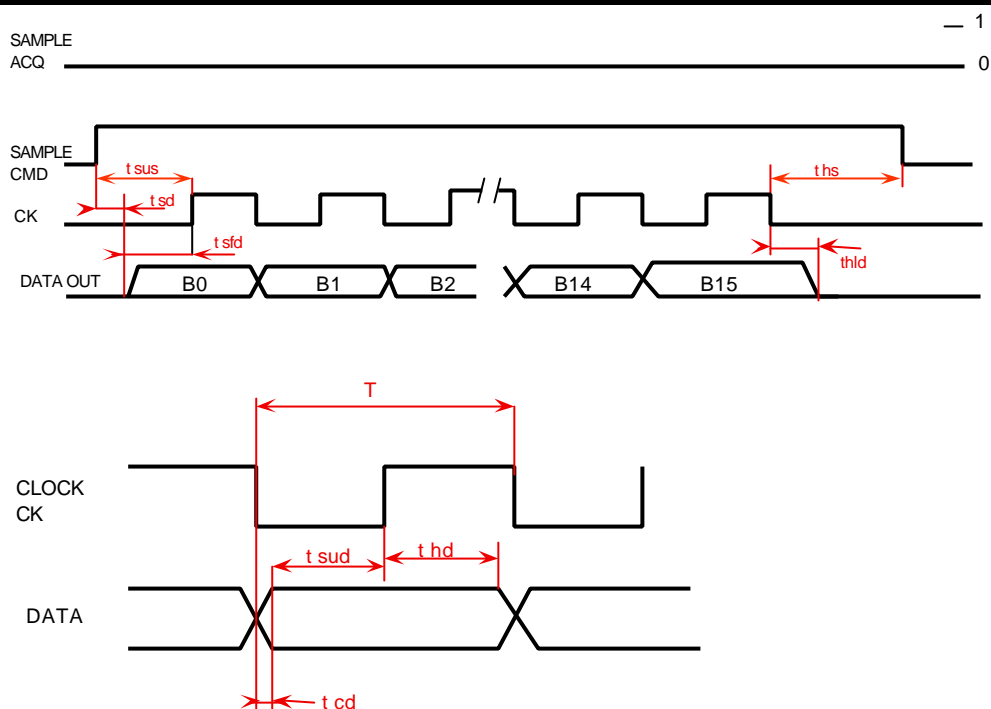


Figure: SERIAL COMMAND BIT TIMING

The serial interface shall operate over the whole range of the time T shown in the following table:.

		Bus Controller			Terminal		
		Min ms	Max ms	Type	Min ms	Max	Type
Transfer clock period	T	60	1000	Tr			
Sampling signal set up time	tsus	420	2500	Tr	400	2520	R
Sampling signal hold time	ths	45	240	Tr	30	260	R
Data signal set up time	tsud	NA	NA	Tr	10	1.05*T	R
First data set up time	tsfd	NA	NA	Tr	10	1000	R
Data signal hold time	thd	25	NA	Tr	20	1.05*T	R
Last data signal hold time	thld	- 5	40	Tr	- 10	60	R
Clock to data time	tcd	- 5	10	Tr	NA	NA	R
Sampling signal to first data	tsd	0	100	Tr	NA	NA	R
Clock duty cycle	DC	45%min	55%ma	Tr	NA	NA	R

Table: TIMING DEFINITIONS FOR SERIAL COMMAND DATA TRANSFER

Bit B0 is sent first and is the MSB of the received command data.

5.2.2.9.3.3 Serial Telemetry Acquisition

The timing of the serial telemetry acquisition signals shall be as shown in the following figure and Table.

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

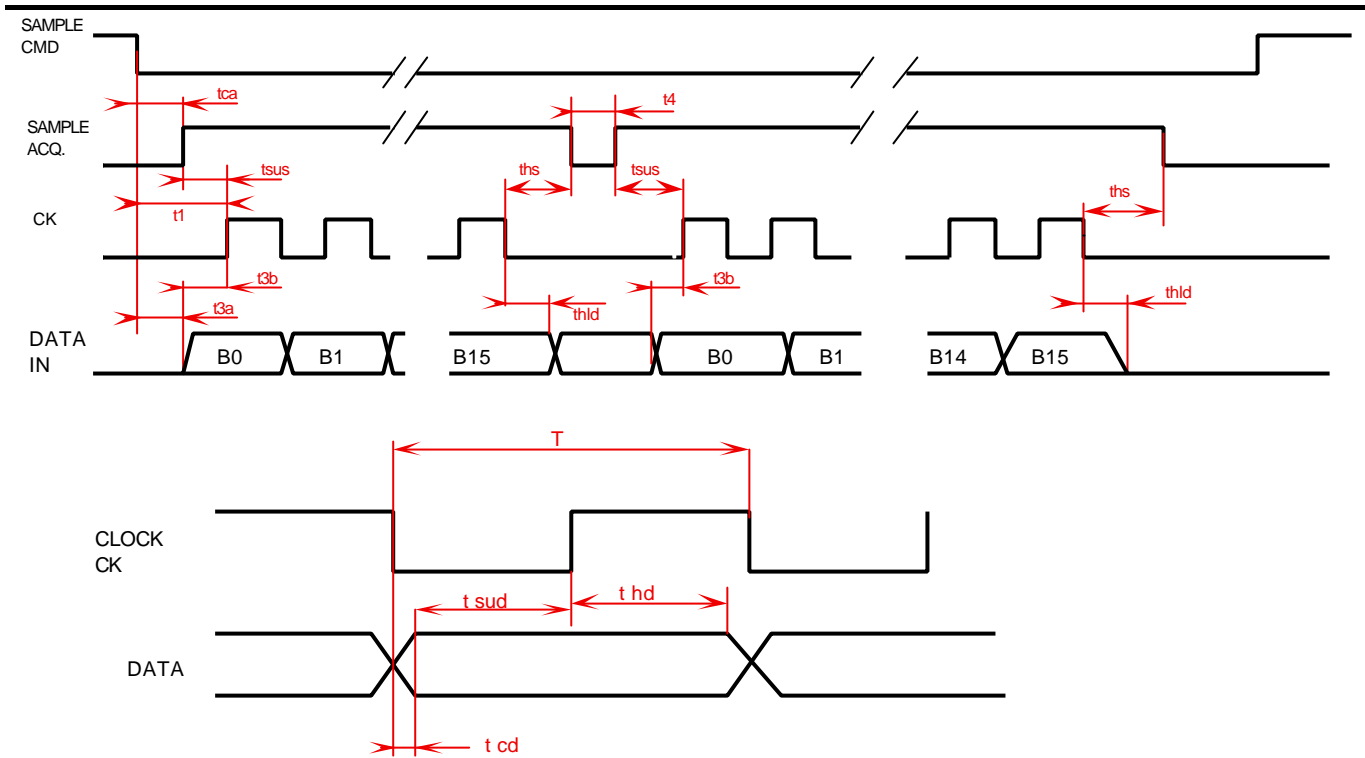


Figure: SERIAL TELEMETRY ACQUISITION BIT TIMING

After a controller request a 32 bit word is transferred from the terminal to the controller, although the 32 bits may be regarded as two separate telemetry words of 16 bits for operational purposes.

The serial interface shall operate over the whole range of the time T shown in the following Table.

		Bus Controller			Terminal		
		Min μ s	Max μ s	Type	Min μ s	Max	Type
Transfer clock period	T	60	1000	Tr			
	t1	2000	3500	Tr	2000	3510	R
	tsus	420	2500	Tr	400	2520	R
t1-t3b	t3a	NA	NA	R	0	2300	Tr
	t3b	10	2000	R	NA	NA	Tr
Duration between acquisitions	t4	1950	2300	Tr	2000	2350	R
	thld	- 5	+ 40	R	0	T/2	Tr
	ths	45	240	Tr	30	260	R
	tsud	10	-	R	20	NA	Tr
	thd	10	-	R	20	NA	Tr
	tcd	NA	NA	R	0	5	Tr
tca=t1-tsus	tca	300	2500	R	NA	NA	Tr
Clock duty cycle	DC	45%min	55%ma	Tr	NA	NA	R

Table: TIMING DEFINITIONS FOR SERIAL TELEMETRY DATA TRANSFER

The SAMPLE-ACQ signal will be available for optional use by the terminal.

Bit B0 shall be sent first and shall be the MSB of the first 16 bit word and of the second 16 bit word.

5.2.2.9.4 Protocol

This section considers that selection of prime or redundant bus has been performed as described in §5.2.2.9.2.3.

On reception of all 16 bits of a command word, and prior to performing the address check, the user terminal equipment shall compute an even parity bit value from bits 0 to 14. It shall compare the computed parity with the received value of bit 15. The received command word shall be considered validated on equality.

If the computed and received parity are not equal, the invalid command shall be ignored. The parity error shall be memorised and a Parity Error Flag (PEF) inserted into telemetry for command verification purposes.

If a parity error occurs then the PEF shall remain set to indicate the parity error event until it has been transmitted in telemetry. Once it has been transmitted then the PEF shall be reset.

After the parity validation has been successfully completed, the user terminal equipment shall then proceed to check the embedded address (as described in section 6.2.2.10.5.2.). If the received command address is equal to its hard-wired address then the user terminal equipment shall proceed to decode the user data. If the address are not identical then the command shall be ignored.

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 65 / 213

As the parity check is performed prior to determining the address validity, all user terminal interfaces on the bus shall set their PEF if they detect a parity error. If the parity error is within the received command then the error will be common to all user terminals on the bus. If only one interface sets its PEF then the parity error is within that interface.

The structure of each command is defined in paragraph 6.2.2.10.5. The contents of the 10 bit user data field shall be defined by the user and as such may differ between different bus user applications.

The bus user shall define the contents of the command data field so as to reserve some bus commands as user telemetry acquisition requests, from the bus controller. As a minimum the bus shall interpret one command data field code as a bus controller request for telemetry verification of the command data received by the user.

Following the reception of a validated command containing a telemetry request and until the reception of the next command, the user terminal shall enable the continuous transmission of the requested telemetry data to the bus controller via the DATA IN bus line.

Throughout the continuous and repetitive transmissions of the requested telemetry, the telemetry data contents shall be constantly refreshed to provide a real time monitoring function of the telemetered parameters.

Telemetry transmission following the occurrence of the telemetry acquisition request shall commence with the next clock pulse following the end of the telemetry acquisition request command.

The acquisition of telemetry consists of the bus controller acquiring 32 bits of telemetry data from a single user terminal which the user terminal transmits as two 16 bits data words. The contents of these data words are defined by the user.

The contents of the two data words may be identical to each other or their contents may be different. The contents of the two data words may be fixed or they may be selectable by a user defined decoding of the telemetry acquisition request commands.

Whilst the Telemetry Clock signal is active on the bus, and in the presence of the Telemetry Strobe signal, the two word telemetry transmission sequence (ACQ1 & ACQ2), shall be repetitively transmitted onto the DATA IN bus.

On the next reception of any command, and prior to parity check or address validation, the transmission of telemetry shall be disabled on the DATA IN bus line, and control of the bus shall be relinquished to the Command Interface.

In the case of memory dump need, the prime shall be contacted.

5.2.2.9.5 Command Structure

5.2.2.9.5.1 Bit Allocation

The allocation of the 16 bits in the command word will be as defined in the next table.

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 66 / 213

BIT POSITION	FUNCTION
0 to 4	Embedded Address
5 to 14	User Data
15	Parity Bit

Table: Command Word Bit Allocation

5.2.2.9.5.2 Embedded Address

The five bits of the Embedded Address shall be termed EB 0 to 4 taking Bit 0 as the first received bit (MSB).

Bit 0 = Embedded Address Bit EBO

Bit 1 = Embedded Address Bit EB1

Bit 2 = Embedded Address Bit EB2

Bit 3 = Embedded Address Bit EB3

Bit 4 = Embedded Address Bit EB4

The terminal equipment interface shall compare each bit of the embedded Address, EA 0 to EA 4, with a corresponding hardwired local Address, HWA 0 to HWA 4, available at unit connector level, and process the user data information contained in bits 8 to 14 when all 5 bits match.

Bit 0 EA 0 compared with hardwired bit HWA 0

Bit 1 EA 1 compared with hardwired bit HWA 1

Bit 2 EA 2 compared with hardwired bit HWA 2

Bit 3 EA 3 compared with hardwired bit HWA 3

Bit 4 EA 4 compared with hardwired bit HWA 4

Concerning the remote terminal address pins definition (HWA0 to HWA4), this definition shall be performed at harness level according to the following rule:

- a logical « 1 » level shall be obtained by floating the corresponding pin (no connection at harness connector level); adequate filtering shall be provided inside the unit on those signals,
- a logical « 0 » level shall be obtained by connecting the corresponding pin to the secondary 0V pins at harness level.

In applications where less than the maximum number of user terminals are employed, the all zero and all ones embedded command address codes should be avoided as they correspond to a bus failure case.

5.2.2.9.5.3 User data

Bit 5 to bit 14 are to be defined by the terminal equipment.

The user shall nevertheless manage at least one binary code to provide a Telemetry Acquisition Request to provide verification of received bus commands.

5.2.2.9.5.4 Parity Bit

Bit 15 shall be used as a parity bit (Even Parity), as defined in Protocol section.

5.2.2.9.6 Telemetry Structure

The user terminal equipment shall provide 32 bits of telemetry data in the form of two 16 bits telemetry data words in response to telemetry acquisition request commands from the bus controller. The contents of the two telemetry data words shall be defined by the user.

The contents of these telemetry data words may be fixed or may be selectable by the user decoding of the data field contents of the telemetry acquisition request commands from the bus controller. This decoding shall be defined by the user.

Following the reception of a validated command containing a telemetry request and until the reception of the next command, the user terminal shall enable the continuous transmission of the requested telemetry data. The telemetry data contents shall be regularly refreshed to provide a real time monitoring function of the telemetered parameters. On the next reception of any command, and prior to parity check or address validation, the transmission of telemetry shall be relinquished to the Command interface.

5.2.2.9.6.1 Command Verification Telemetry

The equipment connected on the serial bus shall provide verification of received commands via telemetry.

The command verification telemetry shall include the Embedded address of the terminal equipment and a Parity Error Flag.

The Embedded address shall be assigned to bits 0 to 4 of the command verification telemetry word.

The Parity Error Flag shall be assigned to bit 15 of the command verification telemetry word.

5.2.2.9.6.2 Functional Telemetry

The equipment connected on the serial bus shall provide sufficient telemetry data to allow the verification and monitoring of all equipment internal functions.

The user shall define the content of the functional telemetry data word.

Reference **ABU-SAT-GDIEE-REQ-166**

*

5.2.2.10 1553B Data Bus

The following requirements are related to the MIL-STD-1553 B system bus protocol at subscriber equipments levels, in terms of addressing capability, exchange type, dwell interruptibility, providing a protocol as standard as possible, which complies with the various constraints linked to each subscriber type. The following requirements only concern dumb slave subscribers (i.e. apart from slave computer).

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 68 / 213

Interface requirements concerning slave computers (« intelligent » subscribers) are presented in spec for the high level I/F between data handling & remote computers (ref TBD).

Reference **ABU-SAT-GDIEE-REQ-167**

Each system bus subscriber equipment shall comply with the MIL-STD-1553B + Notice 2 standard(RD03).

*

Reference **ABU-SAT-GDIEE-REQ-168**

Each subscriber shall be connected to both prime and redundant system buses.

*

Reference **ABU-SAT-GDIEE-REQ-169**

In normal operation, only one system bus is active at a time, and each powered subscriber shall answer to or accept the messages corresponding to its Remote Terminal (RT) address only.

*

Reference **ABU-SAT-GDIEE-REQ-170**

*

Reference **ABU-SAT-GDIEE-REQ-171**

Each powered subscriber shall be in Remote Terminal configuration only; therefore, the dynamic bus control mode command shall not be used and be ignored by all the subscribers.

*

Other mode commands can be used.

Reference **ABU-SAT-GDIEE-REQ-172**

Each subscriber shall be compatible with transformer coupling (long stub).

*

Reference **ABU-SAT-GDIEE-REQ-173**

Each 1553B remote terminal shall provide, for each system bus (prime and redundant), a long stub DC reference to the equipment chassis ground (EGRP), in order to avoid stub charging and arcing due to space environment. This reference shall be performed at the centre tap of the coupling transformer inside the equipment, at stub side, with a DC impedance greater than 100 k Ω but less than 1 G Ω .

*

Reference **ABU-SAT-GDIEE-REQ-174**

No single failure shall lead to an unreferenced stub potential: impedance shall be less than 1 G Ω even in case of any single failure (e.g. redundancy can be obtained by 2 resistors in parallel).

*

Reference **ABU-SAT-GDIEE-REQ-175**

The implementation of the option to analyse illegal commands is not required, but the design must be able to withstand the existence of these undefined commands without causing the remote terminal internal errors or data bus system problems. The general philosophy is to « respond in form », in other words, according to the protocol as if it was legal.

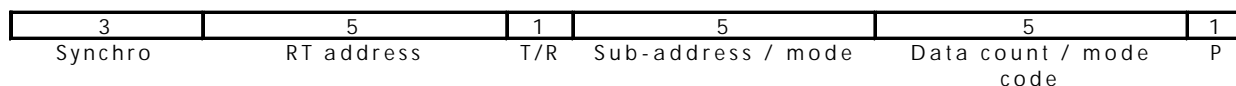
*

5.2.2.10.1 1553B message format -Addressing capability

Transfers on the 1553B bus will be performed in a single controller environment (the SCU is the single data bus master). All transfers are therefore initialised under the central computer control. Most transfers of command type, will be thus performed with the « Controller-to-RT (Remote Terminal) transfer » format; the other class of transfers of command type refers to « mode command » transfers (specific commands as the self-test, the status word transmission, coupler configuration,...): see RD03.

Reference **ABU-SAT-GDIEE-REQ-176**

The structure of the « Controller-to-RT » transfer format is as follows:



*

Reference **ABU-SAT-GDIEE-REQ-177**

The RT addressing capability (number of potential subscribers) amounts to 31 subscribers: the RT address « 31 »(11111) is reserved by the standard for broadcast commands.

*

The Prime Contractor will make the RT address allocation to each equipment.

Reference **ABU-SAT-GDIEE-REQ-178**

The RT address shall be programmable at data bus connector level, as defined in §5.1.2.3.1.

*

Reference **ABU-SAT-GDIEE-REQ-179**

The direct sub-addressing capability (number of possible sub-addresses) is 29 (29 in command and 29 in acquisition); the sub-addresses « 31 » (11111) and « 32 » (00000) are reserved by the standard for mode commands, and the sub-address « 30 » (11110) is reserved by the standard (notice 2) for coupler self-testing (data wrap-around). But the dwell requirements (leading to the sub-address MSB use for the distinction between normal and dwell acquisitions) bring this number down to 14 available sub-addresses.

*

Reference **ABU-SAT-GDIEE-REQ-180**

The block transfer capability is given by the following field of 5 bits (Data count/mode code), indicating the number of data words included in the transfer; the block transfer capability is therefore brought up to 32 words.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03

Page 70 / 213

Reference **ABU-SAT-GDIEE-REQ-181**

This field is also used for mode commands decoding when the sub-address is « 31 » or « 32 ».

*

This field does not allow to extend the sub-address field since the Alphabus application requires a direct access to each command / acquisition point, this requirement being imposed by the dwell.

5.2.2.10.2 Sub-addressing capability needs

According to the equipment type, the sub-addressing need may be very different and may be compatible or not with the direct sub-addressing capability of the MIL-STD-1553B standard.

Reference **ABU-SAT-GDIEE-REQ-182**

In case of incompatibility, the transfers related to acquisitions shall be managed by double transfers.

*

A first transfer of « Controller to-RT » type with a single data word will allow to define the end-address level that is required and to start up acquisition sequencing, and a second transfer of « RT-to-controller » type will allow to retrieve the acquisition result, as indicated by the diagram below:

1 st transfer	Receive Command	Data 1	**	Status	#
2 nd transfer	Transmit Command	**	Status	Data 2	#

- Data 1: data word associated to the Receive command, defining the end-address and starting acquisition
- Data 2: data word associated to the Transmit command, acquisition result

** response time: > 4μs and < 12μs

inter-message gap (IMG) ≥ 30μs

The minimum time between the end of the first transfer status and the beginning of the second transfer is then 30μs. More generally, the delay between the end of any transfer and the beginning of the following one can be 30μs minimum.

5.2.2.10.3 1553B Subscriber Protocol

The aim of this section is to define the protocol in terms of messages structure on the 1553B bus towards the subscriber equipments of the avionics.

There are 2 kinds of subscribers:

-
- Standard subscriber: MIL-STD-1553B Document is fully applicable. Communication is performed with messages structure in accordance.
- Complex subscribers: concerns specific subscribers (as PLIU) which require a specific protocol. Such subscribers shall use the indirect sub-addressing, with acquisitions performed with double transfer.
-

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 71 / 213

5.2.2.10.3.1 1553B Protocol for the complex subscribers

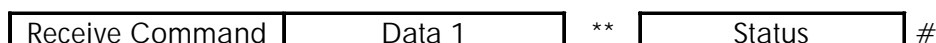
Reference **ABU-SAT-GDIEE-REQ-192**

Complex subscriber shall comply with the following protocol structure.

*

The structure of each message is described here below for commands and acquisitions:

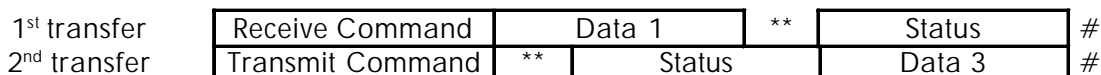
Commands: LSC and HLCD



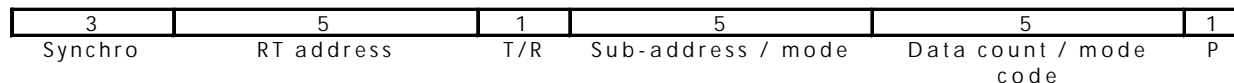
Commands: ML, HLCP, VHLC, HPC



Acquisitions: BIL, AS8, AS16, ANA



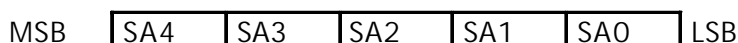
The structure of a command word (receive command or transmit command) is recalled here:



The « RT address » field has been defined in the req TBD

The T/R bit is set to '0' in the case of a receive command and to '1' in the case of a transmit command.

The sub-address field is defined as follows:



The SA4 bit (MSB) of the sub-address field (SA4 to SA0) is, as seen above, reserved for normal/dwell distinction. (D=0, dwell acquisition; D=1, normal acquisition). As this bit is useful for acquisitions only, the transfers related to commands shall not decode it (X means that the SCU can set this bit indifferently to '0' or '1').

The SA3 to SA0 bits will be used for coding the different types of commands as described in the following table.

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 72 / 213

SA4	SA3	SA2	SA1	SA0	Command		
0	0	0	0	0	Forbidden		
X	0	0	0	1	Memory Load command	(ML)	
X	0	0	1	0	Long Switch closure on/off	(LSC)	48 ms
X	0	0	1	1	High-level on/off command	(HLCD)	48 ms
D	0	1	0	0	Digital Bi-level data acquisition	(BIL)	
D	0	1	0	1	16-bit serial digital data	(AS16)	
D	0	1	1	0	8-bit serial digital data	(AS8)	
D	0	1	1	1	Analogue data acquisition	(ANA)	
X	1	0	0	0	Very high level command	(VHLC)	100
X	1	0	1	0	High power command	(HPC)	550
X	1	0	1	1	HLC payload command	(HLC P)	48 ms

Recall:

- the sub-addresses '00000' and '11111' are reserved for mode command
- the sub-address '11110' is reserved for data-wrap-around test
- X: can be indifferently '0' or '1'; D = '0': Dwell acquisition; D = '1': Normal acquisition

The Data count / Mode code field, associated to ML, LSC, HLC, VHLC, HPC, BIL, AS16, AS8, and ANA transfers allows to determine the number of data words associated to the transfer.

The value of this field is defined in the following table for each transfer:

Command	Data count
ML (Receive command)	0 0010
LSC and HLCD (Receive command)	0 0001
HLCP, VHLC, HPC (receive command)	0 0010
BIL, AS8, AS16, ANA (Receive command)	0 0001
BIL, AS8, AS16, ANA (Transmit command)	0 0001

The structure of a data word is defined here below:

3	16	1
Synchro	Data	P

For all « Receive command » transfers defined at the beginning of the section 6.2.2.13.4.1., the Data 1 word will include the end-address corresponding to this command/acquisition.

A theoretical addressing capability of 65536 channels is therefore available.

Practically, it could be interesting, in order to simplify the decoding at the subscriber level, to partition this 16-bit Data 1 word according to the different applications.

For Memory Load Commands, the Data 1 word corresponds to the ML channel address as defined above, and the Data 2 word corresponds to the actual information of the ML command.

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 73 / 213

For the 2nd transfer of acquisitions (transmit command), the Data 3 word (result of acquisition) will be sent back in response by the subscriber (single 16-bit word).

SUMMARY (for complex subscribers)

LSC commands

Receive Command	Data 1 (end address)	**	Status	#
-----------------	----------------------	----	--------	---

⇓

	XXXXX	0	X0010	00001	P
Synchro	RT address	T/R	Sub-address / mode	Data count / mode code	

HLCD commands

Receive Command	Data 1 (end address)	**	Status	#
-----------------	----------------------	----	--------	---

⇓

	XXXXX	0	X0011	00001	P
Synchro	RT address	T/R	Sub-address / mode	Data count / mode code	

ML command, HLCP, VHLC, HPC

Receive Command	Data 1 (end address)*	Data 2 (ML data or end address*)	**	Status	#
-----------------	-----------------------	----------------------------------	----	--------	---

⇓

	XXXXX	0	YYYYY	00010	P
Synchro	RT address	T/R	Sub-address / mode	Data count / mode code	

with

YYYYYY=X0001 for ML

YYYYYY=X1000 for VHLC

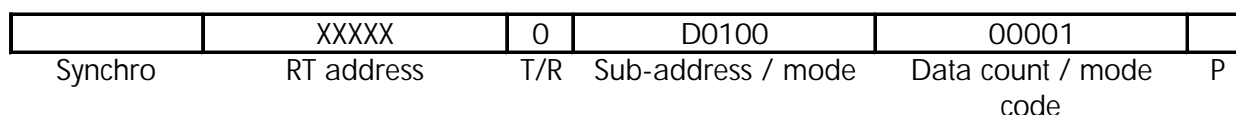
YYYYYY=X1010 for HPC

YYYYYY=X1011 for HLCP

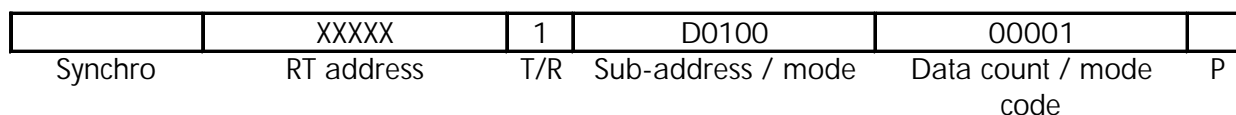
* For HLCP, VHLC, and HPC, the receive command is constituted by two data words, in order to have the possibility to send 4 commands simultaneously. The 32 bits of end address correspond then to 4x8 bits, with each « 8 bits » defined as follows:

All « 8 bits » are set to « 0 » in case of « no command »

1 st transfer	Receive Command	Data 1 (end address)	**	Status	#
--------------------------	-----------------	----------------------	----	--------	---



2 nd transfer	Transmit Command	**	Status	Data 3 (result)	#
--------------------------	------------------	----	--------	-----------------	---



For ANA acquisitions, the Data3 word (result) shall be as follows:



- XXXXX = RT Address
- X: indifferently '0' or '1'
- D bit of sub-address field:
 - D='1' normal acquisition
 - D='0' dwell acquisition

5.2.2.10.3.2 *Standard 1553B Protocol*

The SB4000 1553 type is a long stub.

ALPHABUS

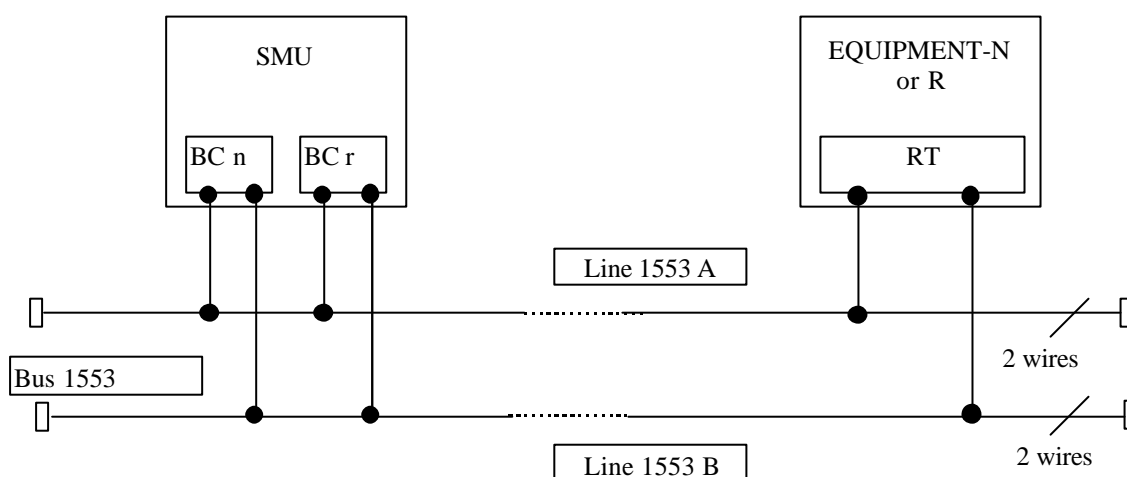
REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03

Page 75 / 213

REQ.

Among redundancy options authorized by the MIL-STD-1553B Document, the following definitions have been selected and apply for each equipments , nominal and redundant:

- One 1553 line is one pair of twisted wires.
- One 1553 bus is composed of two 1553 lines, one called line A and the other called line B.
- Each Bus Coupler (BC n and BC r) located in the computer (SMU) shall control the two 1553 lines (A and B).
- Each Equipment connected to the 1553 bus receives therefore the two 1553 lines (A and B) through dedicated Remote Terminals (RT n and RT r)



5.2.2.10.4 Timing constraints

REQ

Acquisition performances shall be met whatever acquisition sequence order with IMG between any 2 different channels. For a given channel, the maximum dwell interrogation rate shall apply.

Reference **ABU-SAT-GDIEE-REQ-194**

For a given subscriber, all command types can be sent with only the inter-message gap (IMG) ($> 30 \mu s$) between two commands.

*

The time gap between the single commands is defined below (in ms):



ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 76 / 213

2 nd command 	ML/ acq	HLC	HPC
1 st command 			
ML/acq	IMG	IMG	IMG
HLC	IMG	100	100
HPC	IMG	1000	1000

Reference **ABU-SAT-GDIEE-REQ-195**

Concerning the acquisitions (transmit command transfer) performed on a simple subscriber, the result shall be immediately ready for transmission in the given transfer (data word following the status word).

*

5.2.2.11 **OBDH Data Bus**

The OBDH-485 shall comply the « Data Bus Network Electrical and Protocol Specification ».

SBF 6AV2 AS SP 338

5.2.3 Data handling interfaces for platform units

5.2.3.1 COMMAND INTERFACE

5.2.3.1.1 *Commands types*

These commands types are :

a. Low level commands (LLC) :

- Low Priority Commands (LPC) issued by the PFDIU and from ground through umbilical interface
- High Priority Commands (HPC) issued by the Central Reconfiguration Module (CRM) and the Processing Module (PM) inside the SMU.

b. High Level commands (HLC) :

Time and current extended LLC issued by the PFDIU.

c. Memory Load command (MLC) :

Synchronous 16 bit serial data command issued by the SMU

ALPHABUS

REFERENCE: ABU-JPT-SP-563
 DATE: 30/04/2004
 ISSUE: 03

Page 77 / 213

5.2.3.1.1.1 High priority command definition

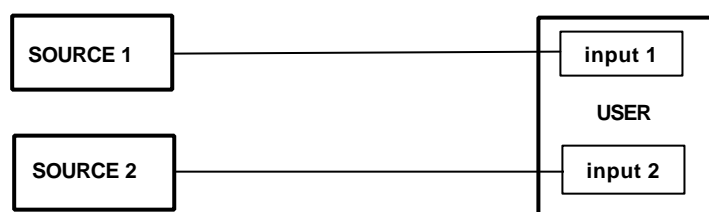
A command is considered as a high priority command if there is :

- several sources (two or three)
- one command user

These commands are identified in the relevant subsystem or unit specification.

REQ.

As a general rule, the user shall provide two separated and isolated command inputs as shown below to avoid current circulation onto the structure between source 1 and source 2.

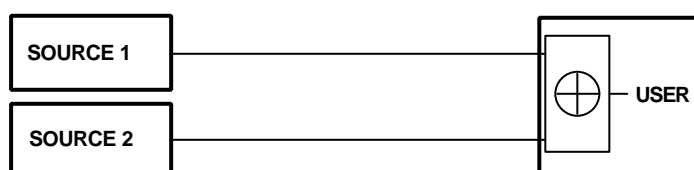


REQ.

However, possible exception could be accepted in the following conditions :

- the commands at source side are isolated from the ground structure (i.e matrix command)
- the command sources are issued from different PCB inside the same equipment.

The user should provide at least two or three 'OR'-ed inputs per command as defined here below :

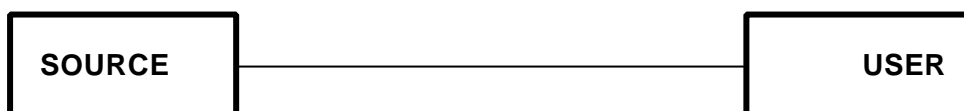


5.2.3.1.1.2 Low priority command definition for one user

A command is considered as a low priority command if there is :

- one source for the command
- one command user

These commands are identified in the relevant subsystem or unit specification.



The low priority commands are all commands not listed in « high priority commands » paragraph.

5.2.3.1.1.3 Low priority command definition for two users in cold redundancy

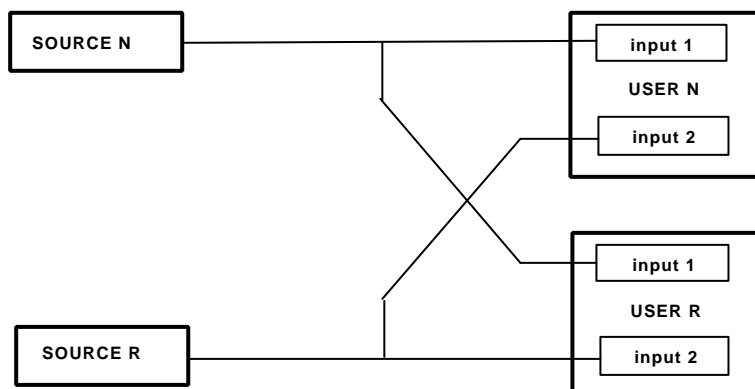
A command is considered as a low priority command in cold redundancy if there is :

- two sources for the command in cold redundancy
- two command users in cold redundancy

These commands are identified in the relevant subsystem or unit specification.

REQ.:

As a general rule, the user shall provide two separated and isolated command inputs as shown below to avoid current circulation onto the structure between source 1 and source 2.



REQ.

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

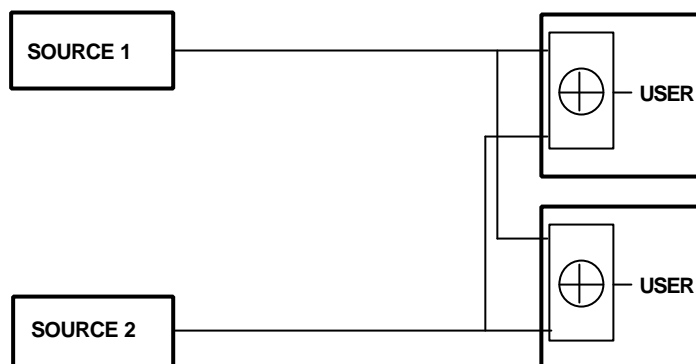
ISSUE: 03

Page 79 / 213

However, possible exception could be accepted in the following conditions :

- the commands at source side are isolated from the ground structure (i.e matrix command)
- the command sources are issued from different PCB inside the same equipment.

The user should provide at least two or three 'OR'-ed inputs per command as defined here below :



5.2.3.1.2 Critical commands

REQ.

Critical command execution, which may cause loss of mission or performance shall be identified and protected against spurious commands and handling errors of ground control, by a reference of 2 independent commands

5.2.3.1.3 LOW LEVEL AND HIGH LEVEL COMMANDS (LLC & HLC)

5.2.3.1.3.1 Matrix command definition

HLC and LLC commands are generated through matrix row and column drivers. One row pulled up to a positive voltage and one column pulled down to the secondary 0v in order to command only the device at the node of the activated row and column.

The command signal is a differential voltage pulse distributed to the user for :

- relay driving or general logic control application with low level commands
- payload waveguide relay driving with high level commands

In this part, emitted signals concern source equipments and received signals concern load equipments.

- command signal waveform is defined **Figure** :Matrix Command Signal Waveform
- Low Level electrical characteristics are presented in **Table** :LLC Electrical Characteristics
- High Level electrical characteristics are presented in **Table** :HLC Electrical Characteristics

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 81 / 213

5.2.3.1.3.1.1 Source side requirements

REQ.

matrix row and column shall be located on separated connectors.

REQ.

each node of the matrix shall be activated by a nominal or a redundant separated telecommand circuits (nominal and redundant lines are connected together as shown § 5.2.3.1.3.1.3) .

REQ.

redundancy concept shall be selected to minimize single points failure and to optimize ON/OFF command reliability.

REQ.

the command lines (rows and columns) shall be double insulated inside the equipment and no failure propagation shall occur between rows, between columns or between row and column. The integrity of the double insulation shall be verifiable following unit integration on the spacecraft.

REQ.

in case of failure, the active command output (row or column output) shall be in a high impedance state.

REQ.

matrix command (LLC and HLC) outputs shall be protected by a current limiting device

REQ.

the current limiting device status shall be monitored by telemetries in order to identify the origin of the failure.

REQ.

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03

Page 82 / 213

command line (rows and columns) shall be insulated from the mechanical ground inside each nominal and redundant source equipments through 1 M Ω bleeder resistor (one resistor per row and per column).

REQ.

row and column command circuitries shall have their OV référence isolated from the mechanical ground through 1 M Ω inside each nominal and redundant source equipments.

REQ.

this 1 M Ω bleeder resistor shall support a permanent voltage of 102 V dc

REQ.

positive voltage commands shall be connected to the matrix row through a serial diode.

REQ.

command return line shall be connected to matrix column.

REQ.

ON/OFF command duration may range from 40 ms to 530 ms (TBC) without initial affectation in order to fullfill LLC and HLC requirements. The pulse duration shall be programmed

REQ.

row and column switches shall be closed after the pulse during the demagnetisation of the relay coil.

REQ.

only one command shall be activated at the same time ; simultaneously commands are not allowed.

REQ.

Only one row and one column shall be activated per command and per matrix

5.2.3.1.3.1.2 Receiver side requirements

REQ.

all telecommand users shall provide two diodes in series with the commanded device at any matrix node.

REQ.

for receiver interface with relay coil, two parallel free wheel diodes shall be implemented in parallel with the relay coil at user side.

When the time constant of relay (L/R) is inferior to 1ms for LLC or 5ms for HLC, the diodes could be non implemented in the receiver interface.

REQ.

for receiver interface with opto-couplers, the light emitting diode shall be in series with a current limiting resistor.

REQ.

the users shall not overload the source during normal operation

REQ.

each command row and column line shall be insulated from the mechanical ground inside the receiver equipments (user side).

REQ. the receiver shall provide a galvanic isolation between the input interface and the signal electronic circuitry (use of relay coil or opto-coupler).

REQ.

the user shall not impose any potential or grounding référence on any row or column.

REQ.

the receiver interface design shall permit the unit power on/off without damage when the electrical interfaces are not terminated or driver unit is off.

REQ.

care should be taken to ensure that input levels don't exceed manufacturer's rating, even when units are unpowered.

ALPHABUS

REFERENCE: ABU-JPT-SP-563
DATE: 30/04/2004
ISSUE: 03
Page 84 / 213

REQ.

each switch shall be connected to the matrix node through a twisted wire.

REQ.

switch positive voltage commands shall be connected to matrix row

REQ.

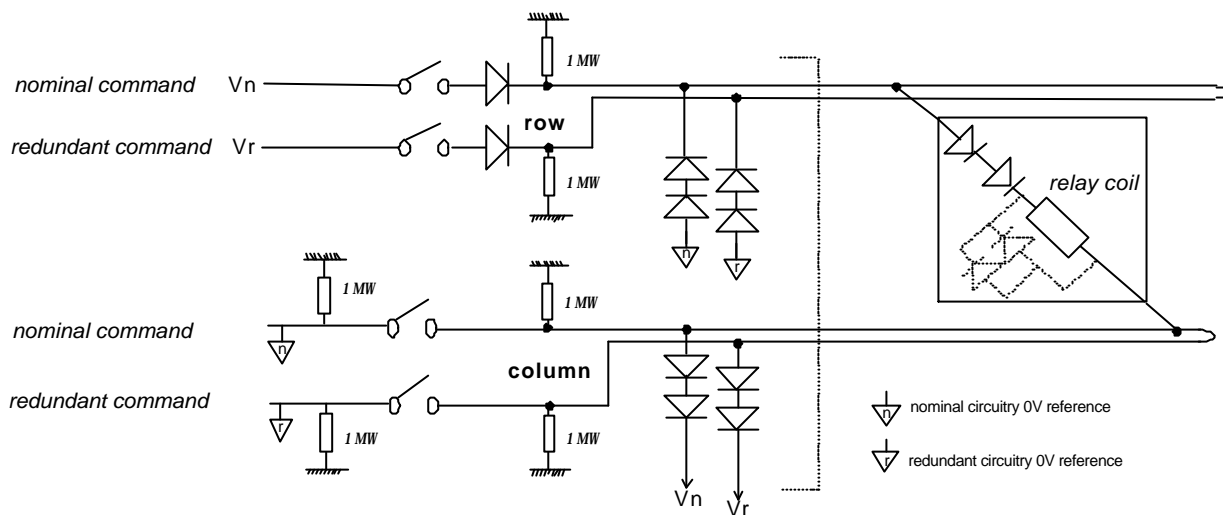
switch command return line shall be connected to matrix column.

REQ.

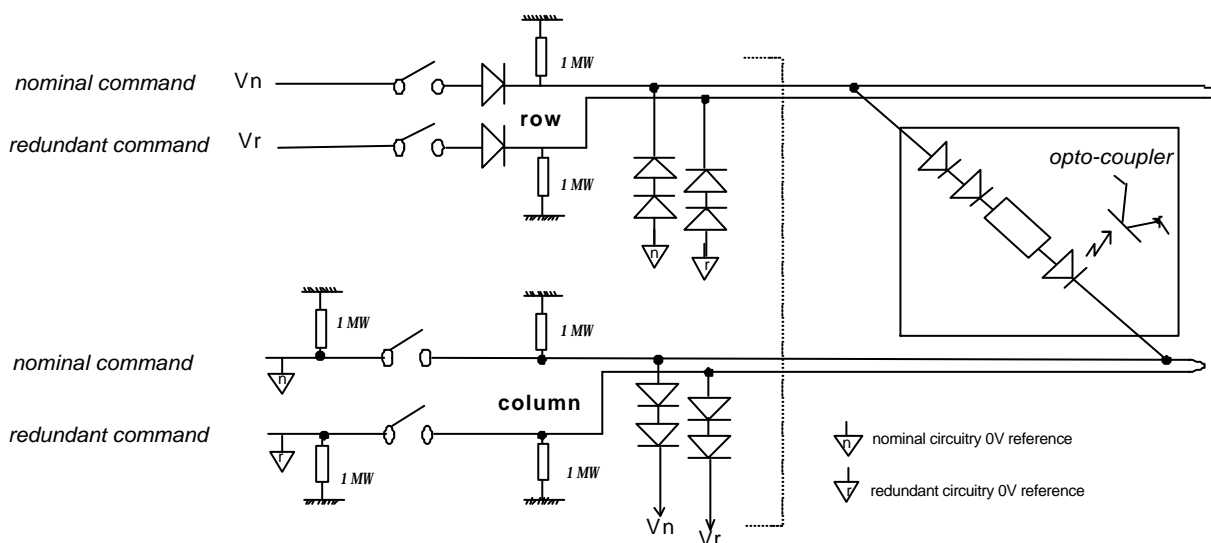
Receiver command input definition shall be compliant with § 5.2.3.1.1

5.2.3.1.3.1.3 Matrix command schematics

Req-1 : Relay interface



Req-2 : Opto coupler interface



5.2.3.1.3.1.4 Matrix command harness concept

REQ.

The basis definition of the matrix harness shall be unshielded lines assembled into one bundle in order to limit magnetic loop between the row (hot line) and the column (return line).

REQ

Each row or column line coming from the nominal function shall be routed in chain to several receivers before returning back to the redundant function. Each matrix node is thus simultaneously connected to the nominal and the redundant function.

An example is given **Figure** :Example of a 3x3 matrix commands harness concept with a 3 x 3 matrix organisation drivers.

REQ.

The bundle shall be rooted near the ground plane (< 1cm).

REQ.

Command matrix harness shall be compliant with connectors and cabling general requirements included in this document.

REQ.

Care shall be taken when connecting to the matrix nodes several switches with the same common ground référence ; those equipment shall share the same column.

REQ.

Equipment switches shall be connected to the matrix row and column lines through intermediate connectors with a mounting plug.

REQ.

Nominal and redundant switches shall not be located on the same intermediate connector

REQ.

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 87 / 213

Intermediate connectors shall be mounted on brackets.

REQ.

The intermediate connector shall be a socket contacts connector and the mounting plug a pin contacts connector.

REQ.

Very high integrated connector (ex : MDM or AMP 104) shall not be used.

The two following requirements are useless if the short circuit between adjacent pins never occurs.

REQ.

Two different rows or columns shall not be set on two adjacent pins on the intermediate connector.

REQ.

Two columns of matrix row contacts shall be separated by one matrix column contacts on the intermediate connector

REQ.Case 1 :

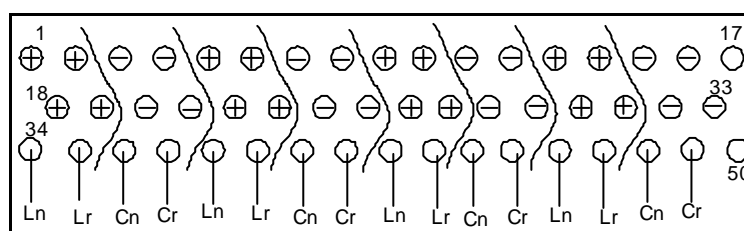
Taking into account requests 11 and 12, row and column pins arrangement on the intermediate connector shall be as shown in **Figure** :Intermediate 50 pins connector arrangement and **Figure** :Intermediate 78 pins connector arrangement for a 50 and a 78 pins connector.

On a 50 contacts connector, the maximum pins used for :

- row lines is 2 x 4 contacts (nominal + redundant lines) \Rightarrow 8 pins
- column lines is 2 x 4 contacts (nominal + redundant lines) \Rightarrow 8 pins
- switch commanded contacts is 32 (16 commands).
- 2 contacts not used

On a 78 contacts connector, the maximum pins used for :

- row lines is 2 x 5 contacts (nominal + redundant lines) \Rightarrow 10 pins
- column lines is 2 x 5 contacts (nominal + redundant lines) \Rightarrow 10 pins
- switch commanded contacts is 50 (25 commands).
- 8 contacts not used



ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 88 / 213

Figure -: INTERMEDIATE 50 PINS CONNECTOR ARRANGEMENT

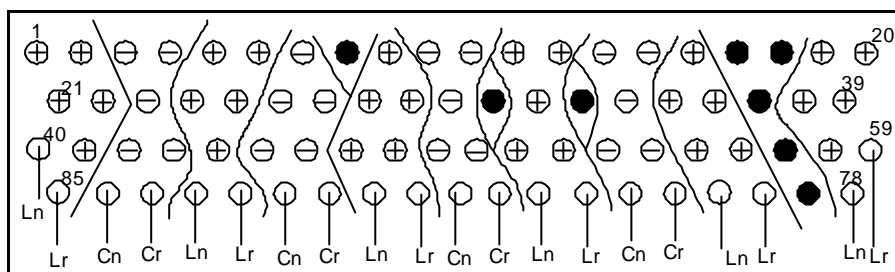


Figure -: INTERMEDIATE 78 PINS CONNECTOR ARRANGEMENT

Case 2 :

Without taking into account requests 11 and 12, row and column pins arrangement on the intermediate connector shall be made without any constraints.

On a 50 contacts connector, the maximum pins used for :

- * column lines is 2 x 4 contacts (nominal + redundant lines) \Rightarrow 8 pins
- * row lines is 2 x 4 contacts (nominal + redundant lines) \Rightarrow 8 pins
- * switch commanded contacts is 32 (16 commands).
- * 2 contacts not used

On a 78 contacts connector, the maximum pins used for :

- * row or column lines is 2 x 7 contacts (nominal + redundant lines) \Rightarrow 14 pins
- * row or column lines is 2 x 4 contacts (nominal + redundant lines) \Rightarrow 8 pins
- * switch commanded contacts is 56 (28 commands).
- * 0 contacts not used

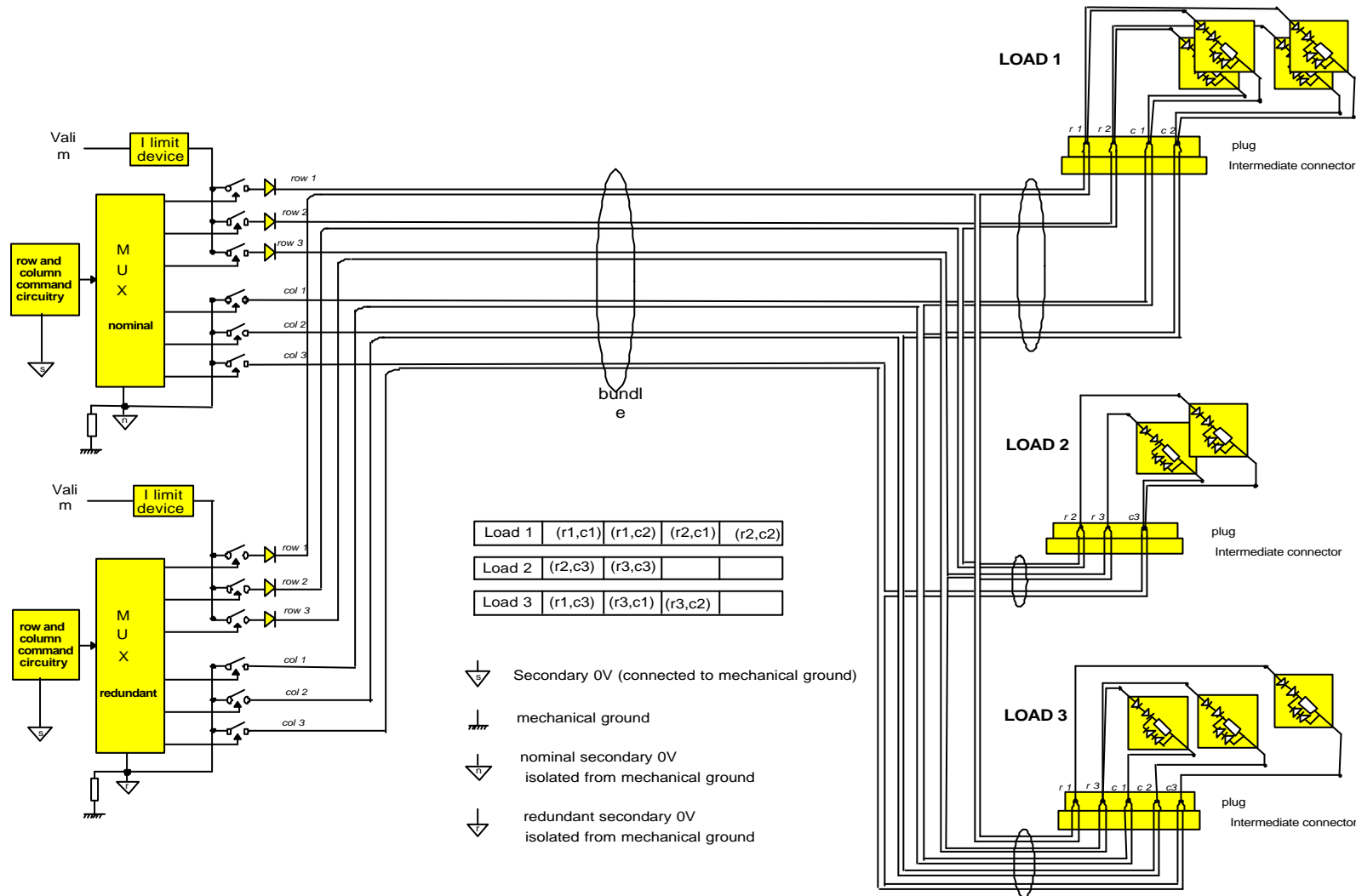


Figure : EXAMPLE OF A 3 X 3 MATRIX COMMANDS HARNESS CONCEPT

5.2.3.1.3.2 Single commands definition

The command signal is a single positive voltage pulse, distributed to the user on a dedicated line for :

- relay driving or general logic control application with low level commands
- payload waveguide relay driving with high level commands

Emitted signals concern source equipments and received signals concern load equipments in this part.

- command signal waveform is defined **Figure** :Matrix Command Signal Waveform
- Low Level electrical characteristics are presented in **Table** :LLC Electrical Characteristics
- High Level electrical characteristics are presented in **Table** :HLC Electrical Characteristics

5.2.3.1.3.2.1 Source side requirement

REQ.

LLC returns shall be referenced to secondary ground of the source equipment.

REQ.

HLC returns shall be referenced to primary ground of the source equipment

REQ.

A minimum of one return pin per two commands is required

REQ.

The source circuitry design shall be such that any single failure in the source does not cause the loss of both nominal and redundant source outputs

REQ.

Redundancy concept shall be selected to minimize single points failure and to optimize ON/OFF command reliability
no failure propagation shall occur between command lines. The integrity of the double insulation shall be verifiable following unit integration on the spacecraft.

5.2.3.1.3.2.2 Receiver side requirements

REQ.

Input return lines directed by commands shall be electrically separated from all the users circuits. User input type shall be differential.

REQ.

As a general rule, the user shall provide one input per command source. In case of several sources, the inputs shall be separated and isolated from one to another as defined in § 5.2.3.1.1.

REQ.

The nominal and the redundant commands returns for shall be electrically separated. Any exception shall be submitted to prime for approval.

REQ.

The receiver interface design shall permit the unit power-on and off without damage when the electrical interface is not terminated or driver unit is off.

REQ.

The receiver shall provide a galvanic isolation between the input interface and the signal electronic circuitry (use of relay coil or opto-coupler) .

REQ.

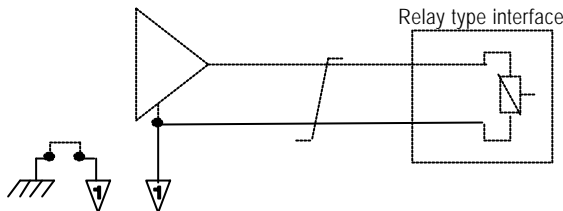
The user circuitry design shall be such that any single failure in the user does not cause the loss of the command.

REQ.

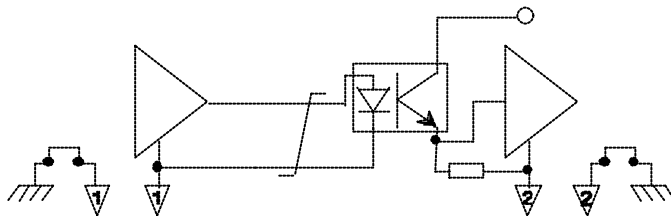
The users shall not overload the source during normal operation.

5.2.3.1.3.2.3 LLC single command schematics

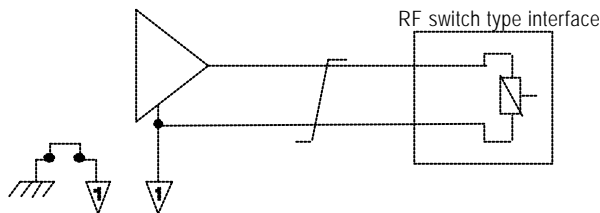
Req-1 : Relay interface



Req-2 : Optocoupler interface



5.2.3.1.3.2.4 HLC single command schematics



5.2.3.1.3.2.5 Single command harness concept

REQ.

The basis definition of the harness shall be a unshielded twisted pair for each line with the active signal and its return .

REQ.

If the user needs several commands, active signals could be grouped with one return inside pairs (from 2-wire pairs until 5-wire pairs).

5.2.3.1.3.3 Failures management

REQ.

Unpowered requirements

Unpowered equipments shall not be damaged and degraded in their performances when command signals are applied.

The unpowered standby equipment shall not affect the active unit.

REQ.

Single failure effect

Any single failure shall not cause the loss of more than one of the two redundant users or one of the two circuit outputs.

Each input shall be sufficiently decoupled (fault propagation) from each input/ output :

- normal condition (powered equipment, without failure)
- unpowered equipment
- unpowered equipment and with any one failure.

REQ.

Compliance

Each source shall be sufficiently decoupled from each other to not have the loss of more than 4 commands at the same time.

The compliance with this requirement shall be proven by analysis.

5.2.3.1.3.4 Command signal characteristics

5.2.3.1.3.4.1 Command signal waveform

- signal duration (T_d) : time between crossing points of rise and fall time to 50% of the full amplitude
- signal rise/fall time (T_r ; T_f) : maximum between 10% and 90% of the nominal voltage swing
- delay between 2 signals : time between the voltage crossing point at 50% of the full amplitude level
- closed time T_c : Command duration with switch closed
- late time T_l : Duration between end of pulse and switch opening

5.2.3.1.3.4.1.1 Classic Command

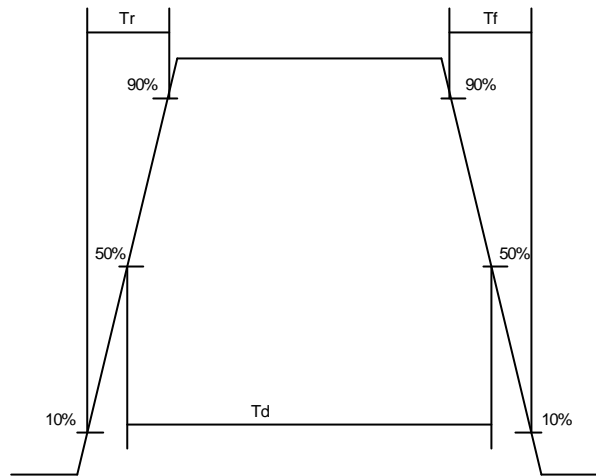


Figure : COMMAND SIGNAL WAVEFORM

5.2.3.1.3.4.1.2 Matrix Command

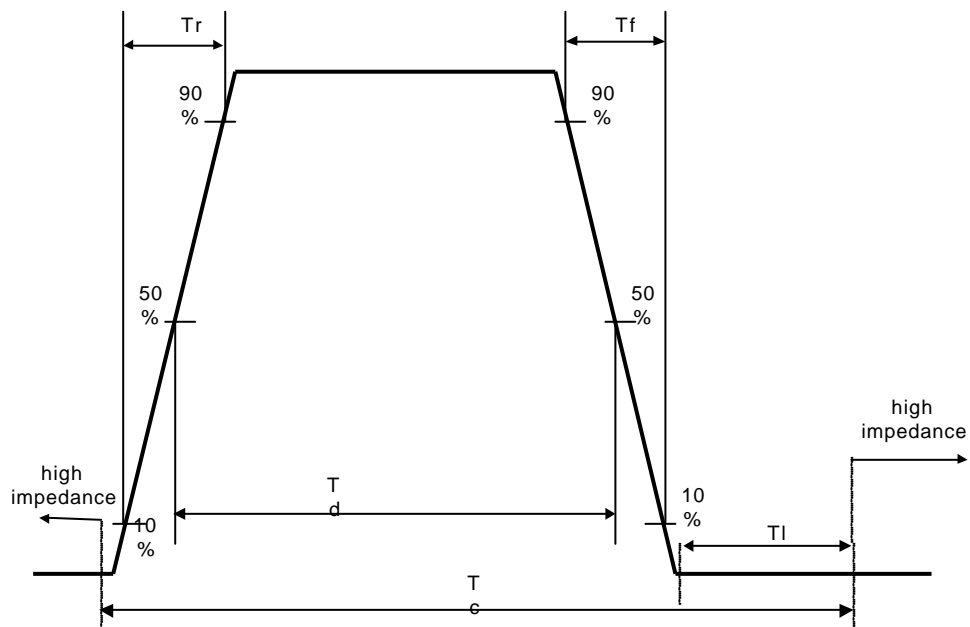


Figure : MATRIX COMMAND SIGNAL WAVEFORM

5.2.3.1.3.4.2 LLC electrical parameters

REQ.

The LLC commands shall comply these LLC electrical characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
A	TYPE			
Req-1	Output type	Differential		for matrix drivers organisation
Req-2	Output type	Single ended		for single LL command
Req-3	Input type		Differential	
Req-4	Transfer	DC COUPLER	DC COUPLER	
B	VOLTAGE			
Req-1	Discrete low « 0 » voltage	-2 V / +4V	impedance : 11k Ω	passive level
Req-2	Discrete high « 1 » voltage	26 V (+3V / - 4V)		active level (1)
Req-3	Threshold		13V +/-2V	
Req-4	Permanent Fault Voltage Emission	-3V \leq fault \leq 33 V	$\geq -5 \text{ V} / \leq 40 \text{ V}$	
Req-6	Permanent Fault Voltage Tolerance	$\geq -5 \text{ V} / \leq 40 \text{ V}$	-3V \leq fault \leq 33 V	
Req-5	Transient Fault Voltage Emission	- 30 V/400 mA/50 ms	$\geq -5 \text{ V} / \leq 40 \text{ V}$	
Req-7	Transient Fault Voltage Tolerance	$\geq -5 \text{ V} / \leq 40 \text{ V}$	- 50 V / 50 ms	maximum source Current : < 400mA
C	CURRENT			
Req-1	Driving capability	> 180 mA		
Req-2	Load current (relay)		2 mA \leq load \leq 180 mA	high level
Req-3	Load current (opto-coupler)		2 mA \leq load \leq 20 mA	high level
Req-4	Overcurrent	\leq 400 mA		
Req-5	short circuit between 2 outputs	withstand		
D	IMPEDANCE			
Req-1	Impedance ON		120 Ω \leq R \leq 11k Ω	
Req-2	Impedance OFF	\geq 10 k Ω \pm 10%	120 Ω \leq R \leq 11k Ω	
Req-3	Sink Impedance	\geq 10 k Ω \pm 10%		
Req-4	Capacity		100 pF max / 10 kHz	500 pF for harness
Req-5	Filter frequency		\leq 10 kHz	

(1) Active level is measured at the source equipment output connector when loaded by the nominal load defined in D-Req-1 in parallel with 600 pF :

- between a row and a column for matrix drivers organisation
- between the positive line and its return for single command

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 96 / 213

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
E	TIME			
Req-1	Rise Time (Tr)	$50 \mu s \leq Tr \leq 500 \mu s$		
Req-2	Fall Time (Tf)	$50 \mu s \leq Tf \leq 600 \mu s$		
Req-3	« On » duration (Td)	$40 ms \leq Td \leq 50 ms$		
Req-4	Max Closed duration (TI)	$TI \leq 25 ms$		Matrix requirement
F	MATRIX COMMAND GROUNDING AND ISOLATION			
Req-1	between row / column lines and Chassis	$1 M\Omega // < 100 pF$	$\geq 1 M\Omega$	one $1 M\Omega$ resistor per row and per column at source side
Req-2	between row and column command circuitry 0Vs and Chassis	$1 M\Omega // < 100 pF$		
Req-3	between row / column lines and receiver electrical circuitry		galvanic isolation	use of relay coil or opto-coupler at user side
G	SINGLE COMMAND GROUNDING AND ISOLATION			
Req-1	from secondary Ground (0Vs)	connected	galvanic isolation	use of relay coil or opto-coupler at user side
Req-2	Chassis	isolated ($\geq 1 M\Omega$)	isolated ($\geq 1 M\Omega$)	at source side, the isolation value is valid when the stud is disconnected
H	SPECIFIC REQUIREMENT			
Req-1	serial diode in matrix command organisation	At least one serial diode on the positive output (row line output)	two diodes in series with the commanded device	
Req-2	serial diode in single command organisation		At least one serial diode on the positive input	
Req-3	number of pins for return lines			see § 5.2.3.11 page 208

Table: LLC ELECTRICAL CHARACTERISTICS

5.2.3.1.3.4.3 HLC electrical parameters

REQ.

The HLC commands shall comply these HLC electrical characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
A	TYPE			
Req-1	Output type	Differential		for matrix drivers organisation
Req-2	Output type	Single ended		for single HL command
Req-3	Input type		Differential	
Req-4	Transfer	DC COUPLER	DC COUPLER	
B	VOLTAGE			
Req-1	Discrete low « 0 » voltage	-2 V / +4V	impedance : 11k Ω	passive level
Req-2	Discrete high « 1 » voltage	26 V (+3V / - 4V)		active level *
Req-3	Discrete high « 1 » voltage	26 V (+3V / - 8V)		
Req-4	Threshold		13V +/-2V	
Req-5	Permanent Fault Voltage Emission	-3V \leq fault \leq 33 V	$\geq -5 \text{ V} / \leq 40 \text{ V}$	
Req-7	Permanent Fault Voltage Tolerance	$\geq -5 \text{ V} / \leq 40 \text{ V}$	-3V \leq fault \leq 33 V	
Req-6	Transient Fault Voltage Emission	- 30 V 1A 600 ms	$\geq -5 \text{ V} / \leq 40 \text{ V}$	
Req-8	Transient Fault Voltage Tolerance	$\geq -5 \text{ V} / \leq 40 \text{ V}$	- 50 V / 600 ms	Maximum source current <1A
C	CURRENT			
Req-1	Driving capability	> 675 mA		
Req-2	Load current		2 mA \leq load \leq 500 mA	high level
Req-3	Overcurrent	\leq 1 A		
Req-4	short circuit between 2 outputs	withstand		
D	IMPEDANCE			
Req-1	Impedance ON		43 Ω \leq R \leq 11k Ω	
Req-2	Impedance OFF	\geq 10 k Ω \pm 10%	43 Ω \leq R \leq 11k Ω	
Req-3	Sink Impedance	\geq 10 k Ω \pm 10%		
Req-4	Capacity		100 pF Max / 10 kHz	500 pF for harness
Req-5	Filter frequency		\leq 10 kHz	

* Active level is measured at the source equipment output connector when loaded by the nominal load defined in D-Req-1 in parallel with 600 pF :

- between a row and a column for matrix drivers organisation
- between the positive line and its return for single command

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
E	TIME			
Req-1	Rise Time (Tr)	$50 \mu s \leq Tr \leq 500 \mu s$		
Req-2	Fall Time (Tf)	$50 \mu s \leq Tf \leq 600 \mu s$		
Req-3	« On » duration (Td)	$500 ms \leq Td \leq 530 ms$		
Req-4	Max Closed duration (TI)	$TI \leq 125 ms$		Matrix requirement
F	MATRIX COMMAND GROUNDING AND ISOLATION			
Req-1	between row / column lines and Chassis	$1 M\Omega // < 100 pF$	$\geq 1 M\Omega$	one $1 M\Omega$ resistor per row and per column at source side
Req-2	between row and column command circuitry 0V and Chassis	$1 M\Omega // < 100 pF$		
Req-3	between row and column lines and receiver electrical circuitry		galvanic isolation	use of relay coil or opto-coupler at user side
G	SINGLE COMMAND GROUNDING AND ISOLATION			
Req-1	from primary Ground (Ovp)	Circuit referenced to Ovp	galvanic isolation	use of relay coil or opto-coupler at user side
Req-2	from secondary Ground	galvanic isolation	galvanic isolation	
Req-3	from Chassis	$\geq 1 M\Omega // \leq 50 nF$	$\geq 1 M\Omega$	
H	SPECIFIC REQUIREMENT			
Req-1	serial diode in matrix command organisation	At least one serial diode on the positive output (row line output)	two diodes in series with the commanded device	
Req-2	serial diode in single command organisation		At least one serial diode on the positive input	
Req-3	number of pins for return lines			see § 5.2.3.11 page 208

Table: HLC ELECTRICAL CHARACTERISTICS

5.2.3.1.4 MEMORY LOAD COMMAND (MLC)

5.2.3.1.4.1 Command Definition

The purpose of the memory load command (or 16-bit serial load command) interface is to transfer a 16-bit data word, in serial form, to an user.

The interface consists of clock, address and data signals shall use SBDL interface. The three signals are sent by the Data Handling Equipment to the user.

Outside the data transfer period, ML Data is in logical « 0 » state

Outside the data transfer period, ML Address & ML/DS Clock is in logical « 1 » state.

Address :

The address signal is a single negative voltage pulse distributed to the user on one dedicated line. For each MLC location in the user, one dedicated address line shall be provided.

Clock :

One clock signal is provided to each user. The clock signals are delivered simultaneously to all users. For each data transfer, 2 bursts of 8 clock pulses are generated on the clock line. Only one clock is provided to an user for telemetry and telecommand.

REQ.

The falling edge is the active edge.

Data :

One data line is provided to each user. The data are a 16-bit word code. The data are delivered simultaneously to all users, connected to the same unit.

First Bit :

The data word shall be shifted out of the source with the MSB, bit 0 first.

The MSB shall be present t7 after the falling edge of the address pulse.

Acquisition :

The shifting of data will take place Thold_TX after the falling edge of the clock pulses.

5.2.3.1.4.2 Conventions

Time duration :

time between crossing points of rise and fall time to 50% of the full amplitude.

Signal rise and fall times :

The rise and fall times of a signal are defined as the time between 10% and 90% of the measured voltage swing.

Signal skew :

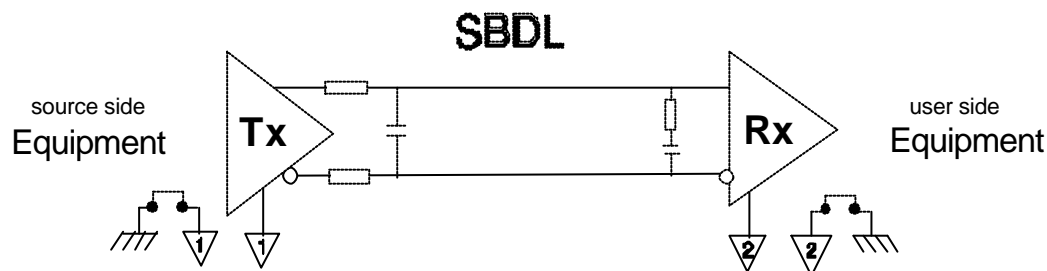
The timing skew between two signals is defined as the time between the instants when the voltage crosses 50% of the measured full amplitude.

Measurements :

Measurements are made at the user input level.

5.2.3.1.4.3 MLC schematics

for Address, Data and Clock



MLC Electrical characteristics

REQ.

Although the SBDL line is symmetrical, the two shall be identified as « non-inverted line » and « inverted line » and shall use differential lines (drivers/receivers).

The status of the signal is defined as true (logical « 1 ») when the non-inverted line has a positive voltage level w.r.t. the inverted line, i.e. when the non inverted line is at a high voltage level and the inverted line is at a low voltage level . The status of the signal is false (logical « 0 ») when the non-inverted line has a negative voltage with respect to the inverted line, i.e. when the non-inverted line is at a low level and the inverted line is at a high level.

Memory load command characteristics are detailed :

- * **Table** : SBDL Characteristics pa**Table** : Memory Load command timing
- * **Figure** : Memory load command signal waveform diagram

REQ.

The MLC commands shall comply the SBDL electrical characteristics .

5.2.3.1.4.4 MEMORY LOAD COMMAND TIMING

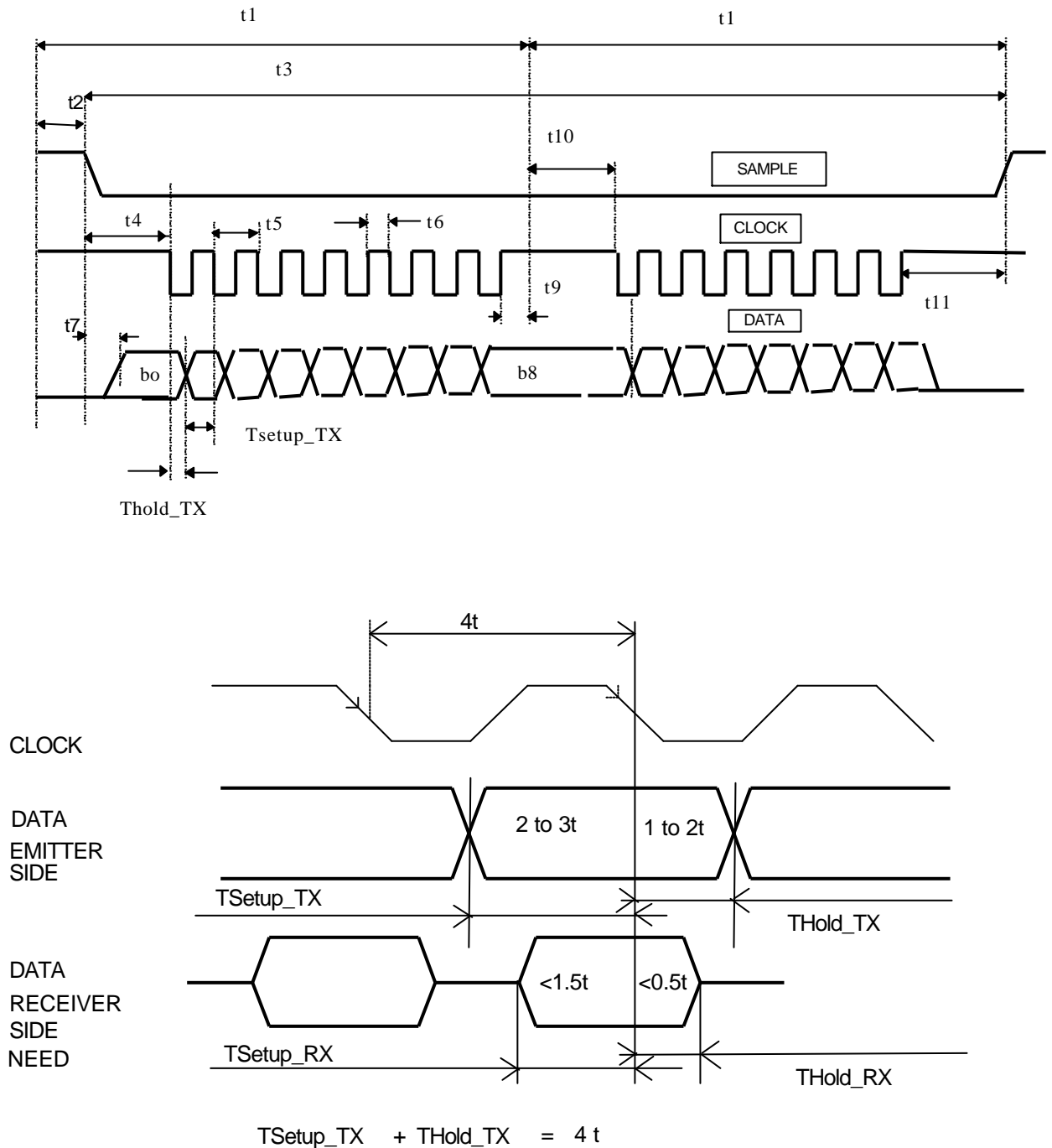


Figure : MEMORY LOAD COMMAND SIGNAL WAVEFORM DIAGRAM

TIMING		
t	Référence time	$1/(2^{20}) \text{ sec} = 0.954 \mu\text{s}$
t1	Transfer half duration	$64t \pm t$
t2	Sample Inactive state duration	$4t \pm t$
t3	Sample active state duration	$124t \pm t$
t4	Sample to clock delay	$28t \pm t$
t5	Clock period	$4t \pm 0.1t$ (262144 Hz)
t6	Active to inactive edge of clock delay	$2t \pm 0.6t$ (*)
t7	Sample to data delay	$< 4t$
t9	inactive edge clock to half transfer delay	$> 1.5t$
t10	Half transfer to clock	$32t \pm 2t$
t11	inactive edge clock to transfer end	$> 1.5t$
Tsetup_TX	Data present to clock (emitter side)	$2t \text{ to } 3t$
Thold_TX	Clock to data end (emitter side)	$1t \text{ to } 2t$
Tsetup_RX	Data present to clock (receiver side)	$< 1.5t$
Thold_RX	Clock to data end (receiver side)	$< 0.5t$
Tskew	falling to rising edge delay	$< 100 \text{ ns}$

Table: MEMORY LOAD COMMAND TIMING

Differential propagation between signals of a MLC shall not be taken into account

(*) the rising edge jitter is acceptable inside the specification. This edge shall not be used.

5.2.3.1.5 SBDL ELECTRICAL CHARACTERISTICS

REQ.

The SBDL interfaces shall comply the following characteristics:

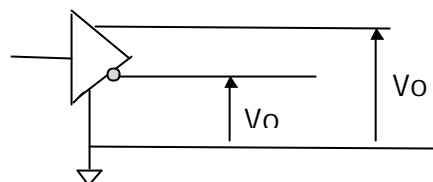
Code	PARAMETERS	SOURCE SIDE (transmitter)	USER SIDE (receiver)	COMMENT
A	TYPE			
Req-1	Output type	balanced driver		balanced driver output
Req-2	Input		Differential	
Req-3	Transfer	DC COUPLER	DC COUPLER	
B	VOLTAGE			
Req-1	Low level output voltage (VOL)	0V to 0.5V		(1)
Req-2	High level output voltage (VOH)	4 V to 5.5V		(1)
Req-3	Low level differential output voltage	-5.5 V to -3.5 V		when loaded by the nominal load defined in D-Req 3
Req-12	High level differential output voltage	3.5 V to 5.5 V		when loaded by the nominal load defined in D-Req 3
Req-4	Logical « 0 »		see (2)	measured between true and inverted line
Req-5	Logical « 1 »		see (2)	measured between true and inverted lines
Req-6	Common mode emission	see (3)	see (3)	
Req-7	common mode immunity		see (4)	
Req-8	Permanent Fault Voltage Emission	-15V to 15V		through 120 Ω
Req-9	Permanent Fault Voltage Emission		-15V to 15V	through 4.7 KΩ
Req-10	Overvoltage Tolerance	-16V to 16V		through 4.7 KΩ
Req-11	Overvoltage Tolerance		-16V to 16V	through 120 Ω
C	CURRENT			
Req-1	deleted		deleted	
Req-2	Overcurrent	≤ 100 mA		
D	IMPEDANCE			
Req-1	power on differential Impedance	120Ω ± 10%		
Req-2	power off differential Impedance	≤ 10 KΩ		
Req-3	AC differential Impedance		120 Ω in series with 1nF	

Req-4	DC in line series resistor		$\geq 4.7 \text{ K}\Omega$ In case of DC differential impedance non compliance	the value is related to each receiver input
Req-5	DC differential Impedance		$\geq 2 \times 4.7 \text{ K}\Omega$	

Code	PARAMETERS	SOURCE SIDE (transmitter)	USER SIDE (receiver)	COMMENT
E	FAIL SAFE PROTECTION			
Req-1	short circuit fail safe		implemented	see D-Req 4
Req-2	open circuit fail safe		implemented	use of line bias resistors
F	TIME			
Req-1	Rise Time (Tr)	$200\text{ns} \leq \text{Tr} \leq 1\mu\text{s}$		
Req-2	Fall Time (Tf)	$200\text{ns} \leq \text{Tf} \leq 1\mu\text{s}$		
G	GROUNDING AND ISOLATION			
Req-1	from Secondary Ground (OVs)	Circuit is referenced to OVs	Circuit is referenced to OVs	
Req-2	from Primary Ground	Isolated	Isolated	for interface referenced to secondary OV, the isolation
Req-3	from chassis	$\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	$\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	value is valid when the stud is disconnected

Table : SBDL CHARACTERISTICS

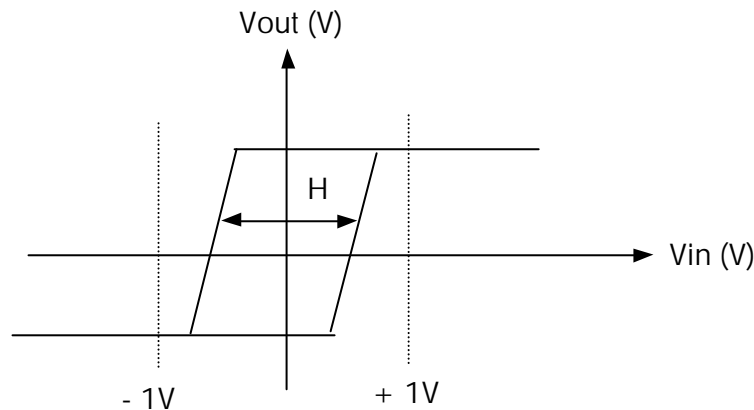
- 1) measurements are performed on each driver output line as defined below, with respect to the equipment ground and when loaded by the nominal load defined in D-Req 3



$$V_{OL} \leq V_O \leq V_{OH}$$

- (2) Two solutions are acceptable for the receiver :

- * use a classical differential receiver with the following characteristics



- The hysteresis H has to be greater than 0.8V
- The high level threshold has to be under 1V and the low level threshold has to be above -1V (differential measure).

- * use the differential line receiver **HS-26C(T)32MS** specially designed for such applications.

(3) * The common mode voltage requirement refers to the ripple voltage impressed on both the inverted and non inverted line, when measured with respect to the equipment chassis.

- * Conducted emission shall be less than $\pm 1,4 V_p$ from 30 Hz to 150 KHz, decreasing by 20db per decade up to 50 Mhz.

(4) * The common mode voltage is related to chassis ground.

- * The interfaces shall not be susceptible to a 3.5 Vrms sine wave injected from 30 Hz to 300 KHz, decreasing by 20 db per decade up to 1Mhz and 1 Vrms from 1 Mhz to 50Mhz.

5.2.3.2 TELEMETRY INTERFACE

5.2.3.2.1 Telemetry channel types

The telemetry channel types are :

- a. Analog Channel (AN)
- b. Digital Serial Channel 16-bit (DD or DS16)
- c. Digital Bi Level Channels (DB)
- d. Digital relay channels (DR)
- e. Thermistors Power Supply and Conditioning (TH)
- f. Emergency and alarm (TBC)

5.2.3.2.2 Analog channels

5.2.3.2.2.1 Analog channels definition

The information is presented in the form of a voltage varying between two defined boundaries. This voltage is sampled regularly, analog to digital converted in the encoders and issued as an 8-bit TM word.

5.2.3.2.2.2 Analog channels states

Two states are defined for the encoder input :

- during acquisition : the encoder input gate is opened
- outside acquisition : the encoder input gate is closed

5.2.3.2.2.3 Analog channels accuracy

REQ.

The system accuracy of the analog channels shall be better than ± 1 % of full scale.

The accuracy of the analog channel signal conditioning in the source shall be as specified in the corresponding subsystem specification but shall be limited to ± 0.5 % of full scale.

The overall A/D conversion accuracy including sampling error quantization error plus offset shall be less than ± 0.5 % of full scale.

5.2.3.2.2.4 Analog channels coding

REQ.

The analog to digital conversion shall use the following formula :

U is the voltage to be measured

Z is a digital binary coded value between 0 and 255

$$Z = \frac{U - 10mV}{20mV} \quad \text{rounded to the next higher integer}$$

5.2.3.2.2.5 Source side requirements

REQ.

Analog channels shall be referenced to secondary ground inside the source equipment.

Analog channels shall not be referenced to primary ground inside the source equipment.

REQ.

Separated returns for nominal and redundant channels shall be provided

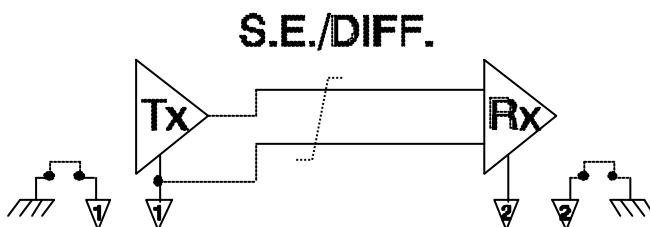
5.2.3.2.2.6 User side (or receiver side) requirements

REQ.

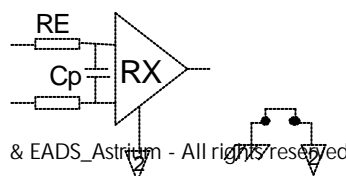
Analog channels shall be completely isolated from any other return (primary ground or mechanical ground) inside the user equipment. Differential receiver is required.

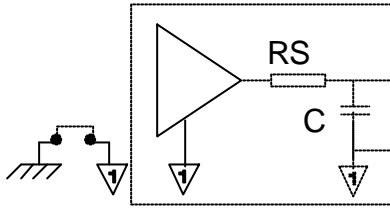
5.2.3.2.2.7 Analog channels schematics

« standard » analog channel



Parameter definition





5.2.3.2.2.8 Analog channels characteristics

REQ.

The analog telemetry shall comply these analog electrical characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
A	TYPE			
Req-1	Output type	Single ended		
Req-2	Input type		Differential	
Req-3	Transfer	DC COUPLER	DC COUPLER	
B	VOLTAGE			
Req-1	Range	0 V / 5.12V		
Req-2	Common mode		(1)	
Req-3	Fault Voltage Emission	$\pm 15 \text{ V}$	$\pm 15 \text{ V}$	
Req-4	Fault Voltage Tolerance	$\pm 17 \text{ V}$	$\pm 17 \text{ V}$	

(1) * The common mode voltage is related to chassis ground.

* The interfaces shall not be susceptible to a 3.5 Vrms sine wave injected from 30 Hz to 300 KHz, decreasing by 20 db per decade up to 1Mhz and 1 Vrms from 1 Mhz to 50 Mhz.

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
C	CURRENT			
Req-1	Over-current	$\leq 15 \text{ mA}$		permanent
D	IMPEDANCE			
Req-1	impedance ON	$R_s \leq 5 \text{ K}\Omega$ in parallel with $100 \text{ nF} \leq C \leq 1 \text{ }\mu\text{F}$ $(R_s \times C \geq 0,1 \text{ ms})$	$\geq 1 \text{ M}\Omega$ (gate on) $\geq 1 \text{ M}\Omega$ (gate off)	
Req-2	impedance OFF	$R_P \leq 100 \text{ k}\Omega$ (2)	$\geq 1 \text{ M}\Omega$	
Req-3	Receiver input Capacity		100 pF Max	500 pF for harness
Req-4	DC in line series resistor		$R_e \geq 3 \text{ K}\Omega$	value related to each receiver input
Req-5	deleted		deleted	
Req-6	Receiver filter Capacity		$C_p \geq 10 \text{ nF}$	
E	GROUNDING AND ISOLATION			
Req-1	from secondary ground (0Vs)	connected	$\geq 1 \text{ M}\Omega$	the isolation at user side is between the input lines and the secondary ground (0Vs)
Req-2	chassis	$\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	$\geq 1 \text{ M}\Omega$	the isolation at source side is valid when the stud is removed
G	SPECIFIC REQUIREMENT			
Req-1	number of pins for return lines			see § 5.2.3.11 page 208

Table: ANALOGIC TELEMETRY CHARACTERISTICS

(2) Rp is the OFF impedance between positive output and the ground

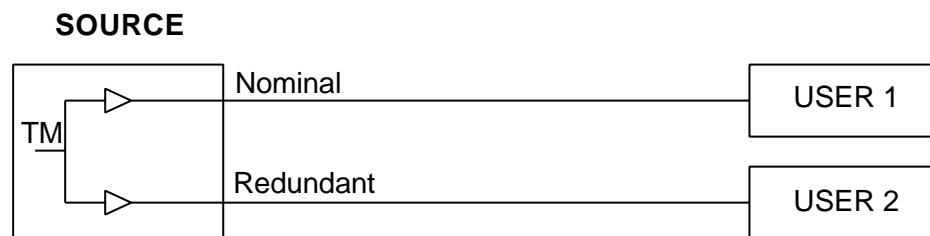
5.2.3.2.2.9 Analog channels interconnection

5.2.3.2.2.9.1 High-priority telemetry signal

5.2.3.2.2.9.1.1 High-priority telemetry definition

A telemetry is considered as a high priority telemetry if there is :

- two outputs of this telemetry in hot redundancy
- two inputs on encoder equipments



These telemetries are identified in the relevant subsystem or unit specification.

5.2.3.2.2.9.1.2 High-priority telemetry harness

The basic definition of the harness shall be a unshielded twisted pair for each line with the active line and its return.

If the source furnishes several telemetries, active signals could be grouped with one return inside pairs (from 2-wire until 5-wire pairs)

5.2.3.2.2.9.1.3 High-priority telemetry fail-safe requirements

REQ.

The source circuitry design shall be such that any single failure in the source does not cause the loss of both redundant telemetry signal outputs.

REQ.

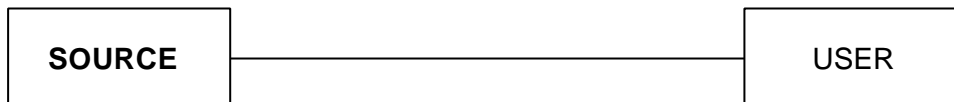
The user circuitry design shall be such that any single failure in the users does not cause the loss of both redundant telemetry signal.

5.2.3.2.2.9.2 Low priority telemetry signal

5.2.3.2.2.9.2.1 Low priority telemetry definition

A telemetry is considered as a low priority telemetry if there is :

- one output of this telemetry
- one input on encoder equipment



These telemetries are identified in the relevant subsystem or unit specification.

5.2.3.2.2.9.2.2 Low-priority telemetry harness

REQ.

The basic definition of the harness shall be a unshielded twisted pair for each line with the active line and its return.

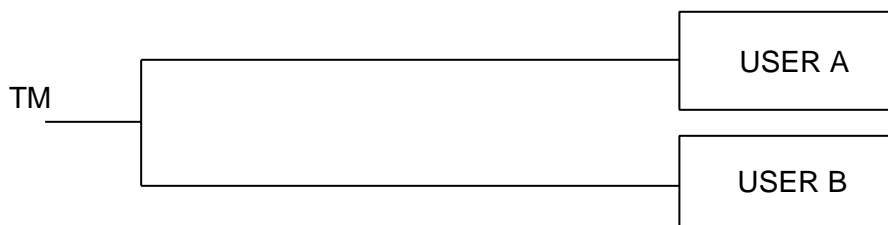
If the source furnishes several telemetries, active signals could be grouped with one return inside pairs (from 2-wire until 5-wire pairs).

5.2.3.2.2.9.3 Cold redundancy

5.2.3.2.2.9.3.1 Cold redundancy definition

A telemetry is considered as a cold redundancy telemetry if there is :

- two separate outputs for the same telemetry
- two separate inputs on encoder equipment



5.2.3.2.2.9.3.2 Cold redundancy telemetry

These telemetries are identified in the relevant subsystem or unit specification.

5.2.3.2.2.9.3.3 Cold redundancy telemetry harness

REQ.

The basic definition of the harness shall be a unshielded twisted pair for each line with the active line and its return.

If the source furnishes several telemetries, active signals could be grouped with one return inside pairs (from 2-wire until 5-wire pairs)

5.2.3.2.2.9.3.4 Cold redundancy telemetry fail-safe requirements

REQ.

The source circuitry design shall be such that any single failure in the source does not cause the loss of both redundant telemetry signal outputs.

The user circuitry design shall be such that any single failure in the users does not cause the loss of both redundant telemetry signal.

5.2.3.2.3 DIGITAL Bi-level channel

5.2.3.2.3.1 Digital Bi-Level channel telemetry definition

The digital bi-level information shall be presented by the source in the form of a voltage that can assume only two distinct values, an on-level (« ONE » level) and an off level (« ZERO » level).

Each digital bilevel corresponds to one bit of the PCMtelemetry message.

5.2.3.2.3.2 Digital Bi-Level trade-off

If several Digital Bi-Level Channels are used by one equipment the substitution by DS or DD channels shall be traded.

5.2.3.2.3.3 Source side requirements

REQ.

Digital Bilevel shall be referenced to secondary ground inside the source equipment
Other design (Primary ground référence, ...) shall be submitted to Prime approval.

REQ.

Separated returns for nominal and redundant channels shall be provided

5.2.3.2.3.4 User side (or receiver side) requirements

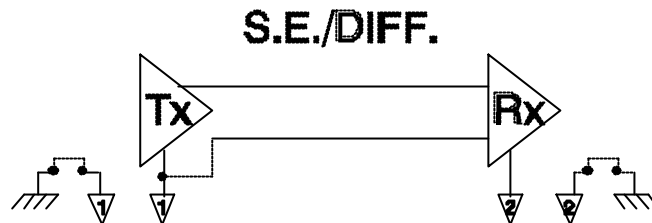
REQ.

Digital Bilevel channels shall be completely isolated from any other return inside the user equipment.

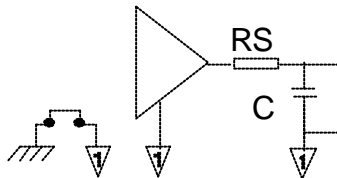
REQ.

The number of channels using the same return shall be limited to 4

5.2.3.2.3.5 Digital Bi-Level channel telemetry schematics



Parameter definition



5.2.3.2.3.6 Digital Bi-Level channel telemetry characteristics

REQ.

The digital bi-level telemetry shall comply these digital bi-level electrical characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
A	TYPE			
Req-1	Output type	Single ended		
Req-2	Input type		Differential	
Req-3	Transfer	DC COUPLER	DC COUPLER	
B	VOLTAGE			
Req-1	Low level output voltage (discrete "0")	0V to 0.5V		When loaded by the nominal load defined in D-Req 1 at source side
Req-2	High level output voltage (discrete "1")	+ 3.5V to + 10V		When loaded by the nominal load defined in D-Req 1 at source side
Req-3	common mode		(1)	
Req-3	Fault Voltage Emission	± 15 V	± 15 V	
Req-4	Fault Voltage Tolerance	± 17 V	± 17 V	

C	CURRENT			
Req-1	Over-current	$\leq 10 \text{ mA}$		permanent

(1) * The common mode voltage is related to chassis ground.

* The interfaces shall not be susceptible to a 3.5 Vrms sine wave injected from 30 Hz to 300 KHz, decreasing by 20 db per decade up to 1Mhz and 1 Vrms from 1 Mhz to 50Mhz.

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
D	IMPEDANCE			
Req-1	impedance ON	$R_s \leq 5 \text{ K}\Omega$ in parallel with $100 \text{ nF} \leq C \leq 1 \text{ }\mu\text{F}$ $(R_s \times C \geq 0,1 \text{ ms})$	$\geq 220 \text{ K}\Omega$ (gate on) $\geq 220 \text{ K}\Omega$ (gate off)	
Req-2	impedance OFF	$R_P \leq 100 \text{ K}\Omega$	$\geq 1 \text{ M}\Omega$	(2)
Req-3	Capacity		100 pF max	500 pF for harness
E	GROUNDING AND ISOLATION			
Req-1	from secondary ground (OVs)	connected	isolated ($\geq 1 \text{ M}\Omega$)	the isolation at user side is between the input lines and the secondary ground (OVs)
Req-2	chassis	isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	isolated ($\geq 1 \text{ M}\Omega$)	the isolation at source side is valid when the stud is removed
G	SPECIFIC REQUIREMENT			
Req-1	number of pins for return lines			see § 5.2.3.11 page 208

Table : DIGITAL BILEVEL TELEMETRY CHARACTERISTICS

(2) Rp is the OFF impedance between positive output and the ground

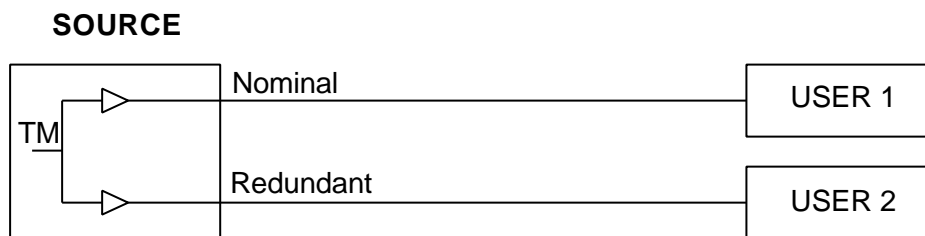
5.2.3.2.3.7 Digital Bilevel channels interconnection

5.2.3.2.3.7.1 High-priority telemetry signal

5.2.3.2.3.7.1.1 High-priority telemetry definition

A telemetry is considered as a high priority telemetry if there is :

- two outputs of this telemetry in hot redundancy
- two inputs on encoder equipments



These telemetries are identified in the relevant subsystem or unit specification.

5.2.3.2.3.7.1.2 High-priority telemetry harness

REQ.:

The basic definition of the harness shall be a unshielded twisted pair for each line with the active line and its return.

If the source furnishes several telemetries, active signals could be grouped with one return inside pairs (from 2-wire until 5-wire pairs).

5.2.3.2.3.7.1.3 High-priority telemetry fail-safe requirements

REQ.

The source circuitry design shall be such that any single failure in the source does not cause the loss of both redundant telemetry signal outputs.

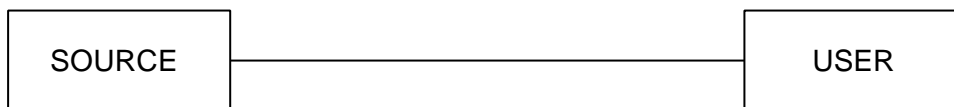
The user circuitry design shall be such that any single failure in the users does not cause the loss of both redundant telemetry signal.

5.2.3.2.3.7.2 Low priority telemetry signal

5.2.3.2.3.7.2.1 Low priority telemetry definition

A telemetry is considered as a low priority telemetry if there is :

- one output of this telemetry
- one input on encoder equipment



These telemetries are identified in the relevant subsystem or unit specification.

5.2.3.2.3.7.2.2 Low-priority telemetry harness

REQ.

The basic definition of the harness shall be a unshielded twisted pair for each line with the active line and its return.

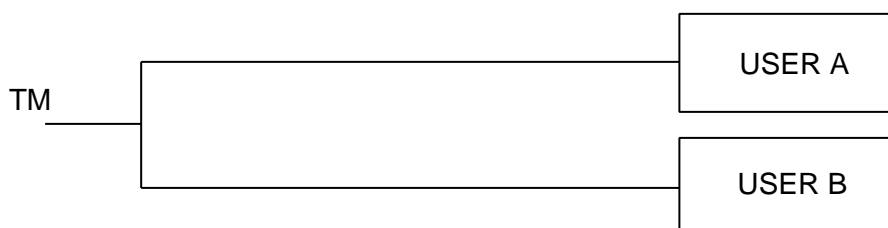
If the source furnishes several telemetries, active signals could be grouped with one return inside pairs (from 2-wire until 5-wire pairs)

5.2.3.2.3.7.3 Cold redundancy

5.2.3.2.3.7.3.1 Cold redundancy definition

A telemetry is considered as a cold redundancy telemetry if there is :

- two separate outputs
- two separate inputs on encoder equipment



5.2.3.2.3.7.3.2 Cold redundancy telemetry

These telemetries are identified in the relevant subsystem or unit specification.

5.2.3.2.3.7.3.3 Cold redundancy telemetry harness

REQ.

The basic definition of the harness shall be a unshielded twisted pair for each line with the active line and its return.

If the source furnishes several telemetries, active signals could be grouped with one return inside pairs (from 2-wire until 5-wire pairs)

5.2.3.2.4 DIGITAL switch closure channel telemetry

The Digital relay acquisition also called DR shall be used to transmit a relay or a switch status signal.

5.2.3.2.4.1 Digital switch closure telemetry types

5.2.3.2.4.1.1 High-priority telemetry signal

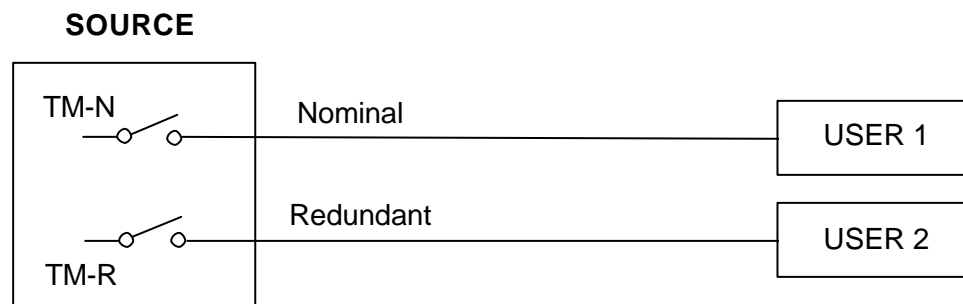
A telemetry is considered as a high priority telemetry if there is :

- two outputs of this telemetry in hot redundancy
- two inputs on encoder equipments

These telemetries are identified in the relevant subsystem or unit specification.

REQ.

The source shall provide two separated and isolated switch closure status.

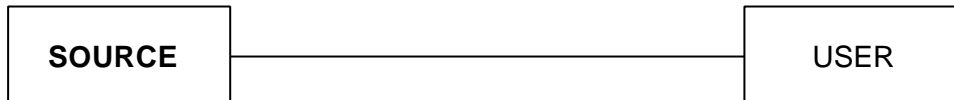


5.2.3.2.4.1.2 Low priority telemetry signal

A telemetry is considered as a low priority telemetry if there is :

- one output of this telemetry (one contact)
- one input on encoder equipment

These telemetries are identified in the revelant subsystem or unit specification.

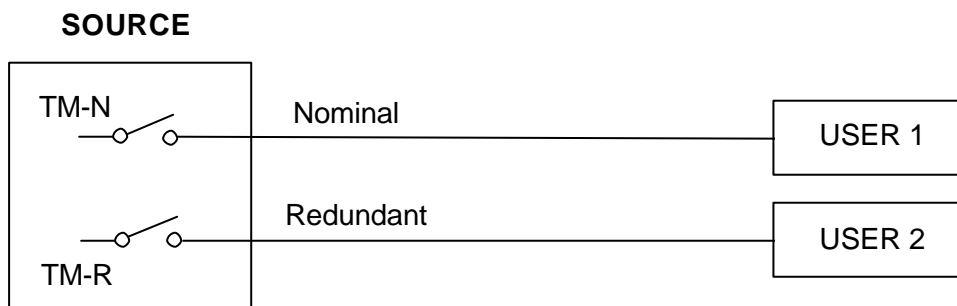


5.2.3.2.4.2 Cold redundancy definition

A telemetry is considered as a cold redundancy telemetry if there is :

- two separate outputs
- two separate inputs on encoder equipment

These telemetries are identified in the revelant subsystem or unit specification.



5.2.3.2.4.3 Matrix switch closure acquisition definition

The matrix switch closure acquisitions are performed through a matrix organisation. One row is pulled up to a positive voltage and the switch closure status is acquired on the column.

The matrix switch closure organisation is not compatible with active bi-level telemetries.

The basic configuration is a 8 rows x 4 column matrix organisation.

5.2.3.2.4.3.1 Source side requirements

Source side is related to the switch closure location

REQ.

All users shall provide two diodes in series with the switch closure device at any matrix node.

REQ.

Each row and column line shall be insulated from the mechanical ground inside the source equipment

REQ.

The source equipment shall provide a galvanic isolation between the switch closure (contact or opto-coupler transistor) lines and the source electrical circuitry

REQ.

The source equipment shall not impose any potential or grounding référence on any row or column.

REQ.

Each switch closure shall be connected to the matrix node through a twisted wire.

5.2.3.2.4.3.2 Receiver (or user) side requirements

Receiver side correspond at one hand to the switch closure polarisation outputs and at the other hand to the switch closure acquisition input.

REQ.

Matrix row and column shall be located on separated connectors.

REQ.

Each node of the matrix switch closures shall be polarised by a nominal or a redundant separated interrogation command circuits and each set of switch closure status shall be selected by the nominal or the redundant acquisition input circuits
The nominal and redundant lines are connected together as shown in § 5.2.3.2.4.3.3

REQ.

Redundancy concept shall be selected to minimize single points failure and to optimize the status acquisition reliability

REQ.

The matrix row and column lines shall be double insulated inside the equipment and no failure propagation shall occur between rows, between columns or between row and column.
The integrity of the double insulation shall be verifiable following unit integration on the spacecraft.

REQ.

In case of failure, the concerned row output or the concerned column acquisition input shall be in a high impedance state. The design shall be such that any single failure does not cause the loss of both nominal and redundant interfaces.

REQ.

The polarisation outputs of the matrix switch closure shall be protected by a current limiting device

REQ.

The current limiting device status shall be monitored by telemetries in order to identify the origin of the failure.

REQ.

Matrix switch closure row lines shall be isolated from the mechanical ground inside each nominal and redundant source equipments through 1M Ω bleeder resistor (one resistor per row)

REQ.

Matrix switch closure polarisation and acquisition circuitries shall have their OV référence isolated from the mechanical ground through 1M Ω inside each nominal and redundant receiver equipments.

REQ.

This 1 M Ω bleeder resistor shall support a permanent voltage of 102 V dc

REQ.

The matrix acquisition pulse duration shall be at least 20 ms .

REQ.

Only one row shall be selected per interrogation.

REQ.

The matrix acquisition input interfaces shall not overload the source during normal operation and 16 status (column lines, worst case) could be acquired simultaneously

REQ.

Closed contact shall correspond to the TM « ZERO » level and open contact to the TM « ONE » level.

Note

The closed contact could correspond to an equipment unpowered or powered.

For each equipment, the definition of the TM logic shall be defined .

REQ.

The receiver side shall be safe to these failure cases of the source :

- Relay :

Permanent blockage : open or closed

Blocked in an intermediate position

Short circuit between the contact and the mechanical ground

Short circuit between contacts : 100V on the source contact

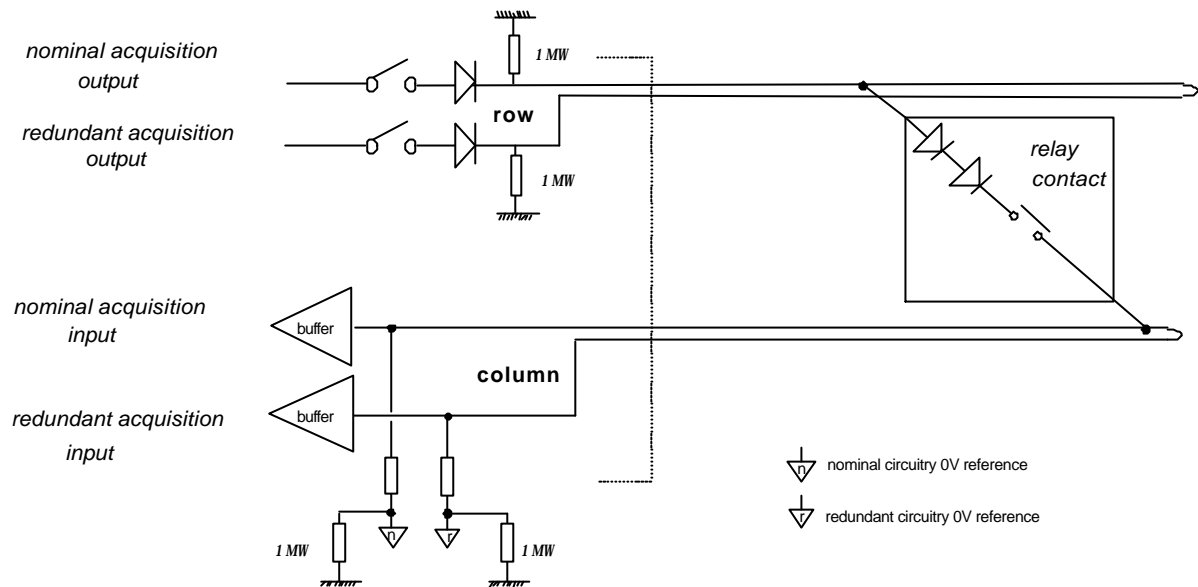
- Opto couplers :

Collector / emitter short circuit

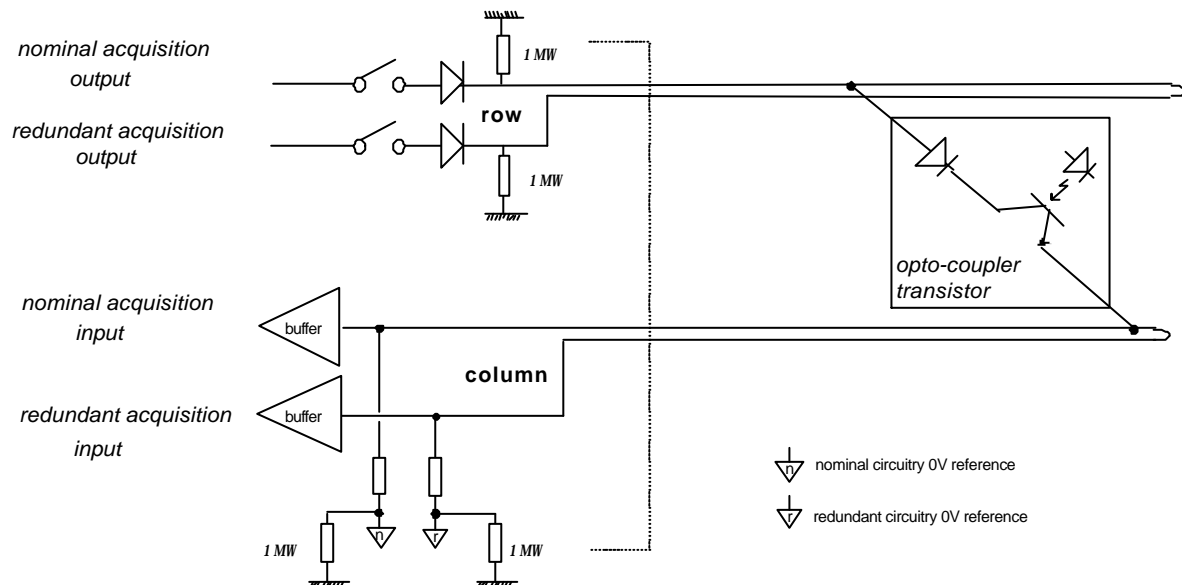
Collector / emitter open circuit

5.2.3.2.4.3.3 Switch closure matrix acquisition schematics

Req-1 : Relay contact interface



Req-2 : Opto coupler transistor interface



5.2.3.2.4.3.4 Matrix switch closure harness concept

REQ.

The basis definition of the matrix switch closure harness shall be unshielded lines assembled into one bundle in order to limit magnetic loop between the row lines and the column lines.

REQ.

Each row or column line coming from the nominal receiver PCB shall be rooted in chain to several switch closures (source equipment) before returning back to the redundant receiver PCB. Each matrix node is thus simultaneously connected to the nominal and the redundant PCB. An example is given Figure with a 3 x 3 switch closure matrix organisation.

REQ.

The bundle shall be rooted near the ground plane (< 1cm).

REQ.

Matrix switch closure harness shall be compliant with connectors and cabling general requirements included in this document

REQ.

Equipment switch closures shall be connected to the matrix row and column lines through intermediate connectors with a mounting plug.

REQ.

nominal and redundant switch closures shall not be located on the same intermediate connector

REQ.

intermediate connectors shall be mounted on brackets.

REQ.

the intermediate connector shall be a socket contacts connector and the mounting plug a pin contacts connector (50 or 78 pins connector are recommended)

REQ.

Very high integrated connector (ex : MDM or AMP 104) shall not be used.

The two following requirements are useless if the short circuit between adjacent pins never occurs.

REQ.

Two different rows or columns shall not be set on two adjacent pins on the intermediate connector.

REQ.

Two columns of matrix row contacts shall be separated by one matrix column contacts on the intermediate connector (i.e **Figure** :Intermediate 50 pins connector arrangement and **Figure** :Intermediate 78 pins connector arrangement for a 50 and a 78 pins connector.).

REQ.

Case 1 :

Taking into account requests 10 and 11, row and column pins arrangement on the intermediate connector shall be as shown in **Figure** :Intermediate 50 pins connector arrangement and **Figure** :Intermediate 78 pins connector arrangement for a 50 and a 78 pins connector.

On a 50 contacts connector, the maximum pins used for :

- * row lines is 2 x 4 contacts (nominal + redundant lines) \Rightarrow 8 pins
- * column lines is 2 x 4 contacts (nominal + redundant lines) \Rightarrow 8 pins
- * switch commanded contacts is 32 (16 commands).
- * 2 contacts not used

On a 78 contacts connector, the maximum pins used for :

- * row lines is 2 x 5 contacts (nominal + redundant lines) \Rightarrow 10 pins
- * column lines is 2 x 5 contacts (nominal + redundant lines) \Rightarrow 10 pins
- * switch commanded contacts is 50 (25 commands).
- * 8 contacts not used

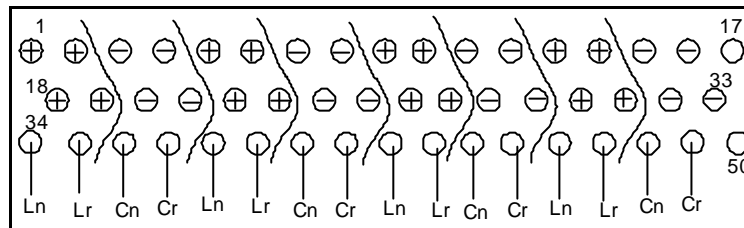


Figure : INTERMEDIATE 50 PINS CONNECTOR ARRANGEMENT

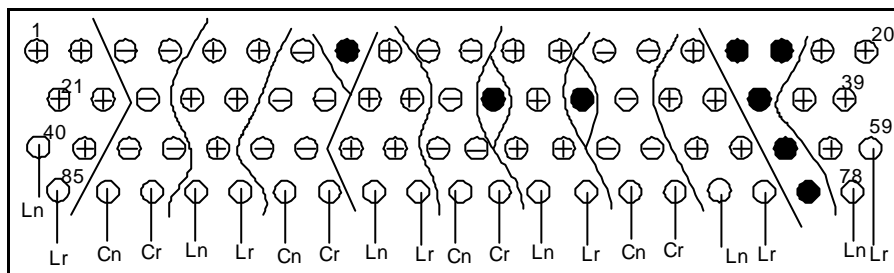


Figure : INTERMEDIATE 78 PINS CONNECTOR ARRANGEMENT

Case 2 :

Without taking into account requests 10 and 11, row and column pins arrangement on the intermediate connector shall be made without any constraints.

On a 50 contacts connector, the maximum pins used for :

- * column lines is 2 x 4 contacts (nominal + redundant lines) \Rightarrow 8 pins
- * column lines is 2 x 4 contacts (nominal + redundant lines) \Rightarrow 8 pins
- * switch commanded contacts is 32 (16 commands).
- * 2 contacts not used

On a 78 contacts connector, the maximum pins used for :

- * row or column lines is 2 x 7 contacts (nominal + redundant lines) \Rightarrow 14 pins
- * row or column lines is 2 x 4 contacts (nominal + redundant lines) \Rightarrow 8 pins
- * switch commanded contacts is 56 (28 commands).
- * 0 contacts not used

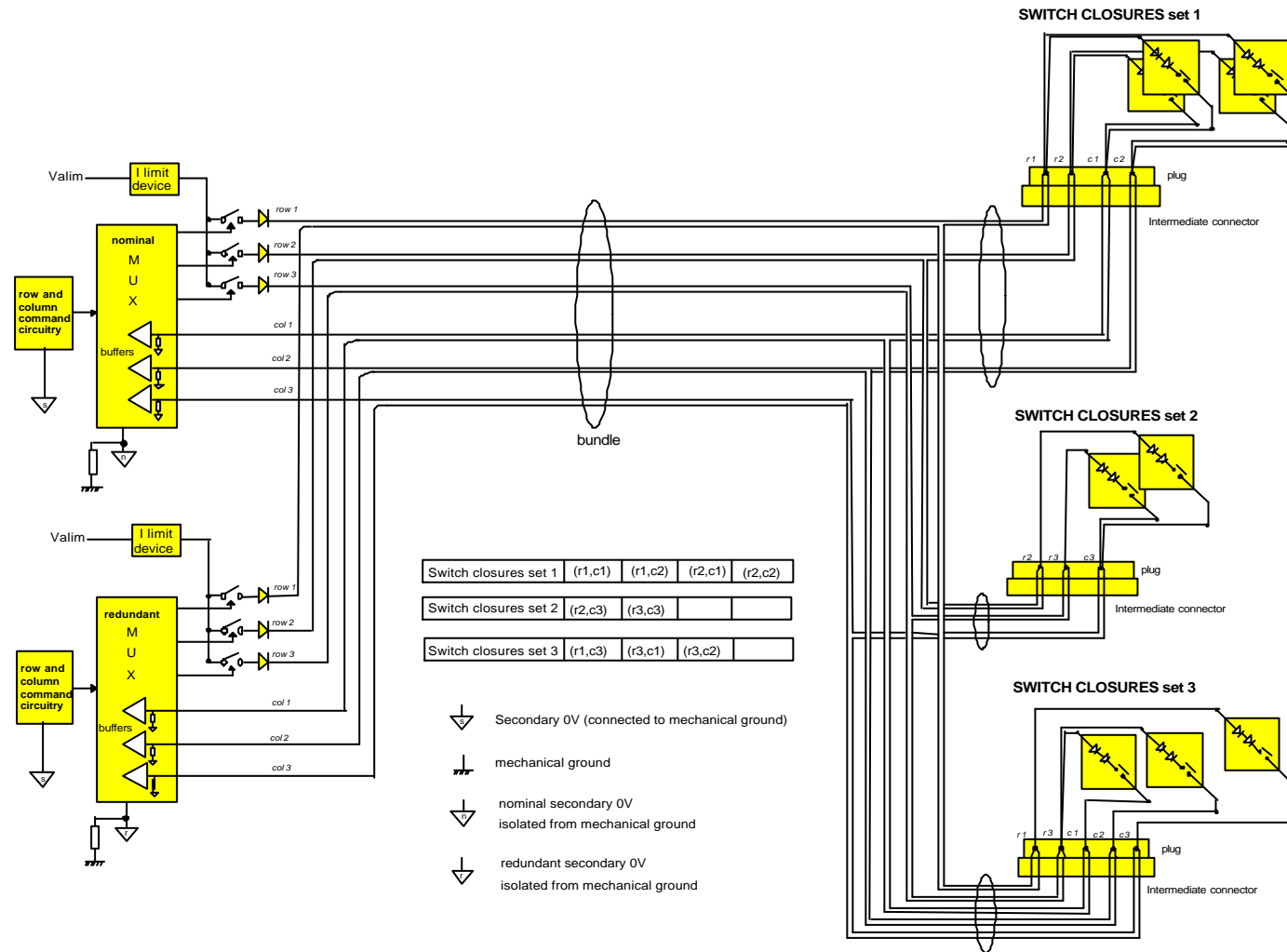


Figure 5.2.3-A : EXEMPLE OF A 3 X 3 MATRIX COMMANDS HARNESS CONCEPT

5.2.3.2.4.4 Single ended switch closure acquisition definition

REQ.

Direct switch closure acquisition will not be performed via a matrix acquisition structure, but via a dedicated circuits referenced to the secondary OV.

REQ.

The digital relay information shall be presented by the contact position with two possible states :

- closed contact corresponding to the TM « ZERO » level
- open contact corresponding to the TM « ONE » level

Each digital relay corresponds to one bit of the PCMtelemetry message.

REQ.

If several Digital relay Channels are used by one equipment the substitution by Digital serial channels or RUBI shall be traded.

5.2.3.2.4.4.1 Source side requirements

Source side is related to the switch closure location.

REQ.

Digital switch closure channels shall be completely isolated from any other return inside the source equipment

REQ.

The source equipment shall provide a galvanic isolation between the switch closure lines and the source electrical circuitry

REQ.

Separated returns for nominal and redundant channels shall be provided.

5.2.3.2.4.4.2 Receiver (or user) side requirements

Receiver side correspond to the switch closure acquisition inputs

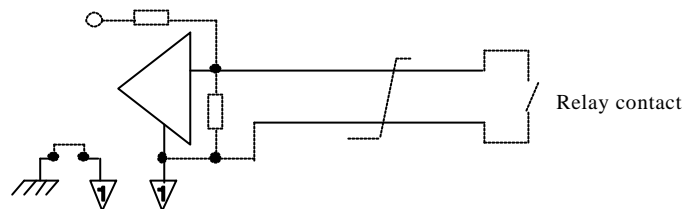
REQ.

Digital relay shall be referenced to the secondary ground inside the user equipment
Other design (Primary ground référence, ...) shall be submitted to Prime approval.

5.2.3.2.4.4.3 Digital relay channel telemetry schematics

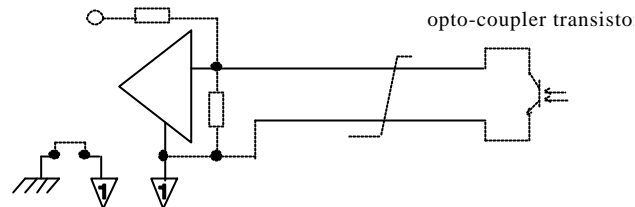
REQ.

Relay contact interface



REQ.

Opto-coupler transistor interface



5.2.3.2.4.4.4 Single ended switch closure harness concept

REQ.

The basic definition of the harness shall be a unshielded twisted pair for each line with the active line and its return.

If the source provides several telemetries, the active signals could be grouped with one return inside the bundle (from 2 wires until 5 wires pairs)

5.2.3.2.4.5 Digital relay channel telemetry characteristics

REQ.

The digital relay telemetry shall comply these digital relay electrical characteristics :

Code	PARAMETERS	SOURCE SIDE DR	USER SIDE PCB	COMMENT
A	TYPE			
Req-1	Output type	differential balanced lines		
Req-2	Input type		differential	for matrix organisation
Req-3	Input type		Single ended	for single ended acquisition
Req-4	Transfer	DC COUPLER	DC COUPLER	
B	VOLTAGE			
Req-1	contact capability	17 V		permanent, ON or OFF
Req-2	Fault voltage emission		<17V	
Req-3	Drop voltage («ON state »)	≤ 3V		- relay : 2 diodes + 1 relay contact - opto : 1 diode + 1 transistor junction
C	CURRENT			
Req-1	contact capability 'ON'	$I \geq 5\text{mA}$	$1\text{mA} < I < 5\text{mA}$	permanent
Req-2	contact capability 'OFF'	200µA / 17V		permanent
Req-3	Nominal Current limitation		<5mA	permanent, per contact
Req-4	Fault Current emission		<50mA	500 ms, per contact

D	RELAY IMPEDANCE			
Req-1	Relay contact : impedance open	$\geq 10 \text{ M}\Omega$	$\leq 100 \text{ k}\Omega$	
Req-2	Relay contact : Impedance closed	$\leq 1 \text{ }\Omega$	$\leq 100 \text{ k}\Omega$	
Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
E	TIME			
Req-1			deleted	
Req-2			deleted	
Req-3	Minimum acquisition duration		Ton $\geq 10 \text{ ms}$	corresponding to the current establishment in the line
Req-4	Acquisition duration (Td)		Ta $\geq 20 \text{ ms}$	applicable for matrix organisation
F	MATRIX COMMAND GROUNDING AND ISOLATION			
Req-1	between row / column lines and Chassis	$\geq 1 \text{ M}\Omega$	$1 \text{ M}\Omega // < 100 \text{ pF}$	one $1 \text{ M}\Omega$ resistor per row at user side
Req-2	between electrical circuitry 0Vs and Chassis		$1 \text{ M}\Omega // < 100 \text{ pF}$	
Req-3	between switch closure lines and the electrical circuitry	galvanic isolation		use of relay contact or opto-coupler transistor at source side
G	SINGLE COMMAND GROUNDING AND ISOLATION			
Req-1	from secondary Ground (0Vs)	galvanic isolation	connected	use of relay contact or opto-coupler transistor at source side
Req-2	Chassis	isolated ($\geq 1 \text{ M}\Omega$)	isolated ($\geq 1 \text{ M}\Omega$)	at user side, the isolation value is valid when the stud is disconnected
H	SPECIFIC REQUIREMENT			
Req-1	serial diode in matrix command organisation	two diodes in series with the switch closure device	At least one serial diode on the positive output (row line output)	
Req-3	number of pins for return lines			see § 5.2.3.11 page 208

Table : DIGITAL RELAY TELEMETRY CHARACTERISTICS

5.2.3.2.5 Digital serial channels : DS16

5.2.3.2.5.1 Definition

The function of this interface is to transfer in a serial form a 16-bit data word from the user to the Data Handling subsystem.

The interface consists of clock, sample and data signals shall use SBDL interface.

Outside the data transfer period, DS Data is in logical « 0 » state

Outside the data transfer period, DS Sample & ML/DS Clock is in logical « 1 » state.

Sampling signal

The sampling signal is negative voltage pulse distributed to the TLM source on a dedicated line, defining the time period during which the transfer of a serial 8-bit or 16-bit data word will take place.

For one 8-bit or 16-bit word, one sampling signal line will be provided to the user.

Clock

One clock signal is provided to each user.

The clock signals are delivered simultaneously to all subject users . For each 8-bit (or 2 x 8-bit) data word transfer, a burst of 8 (or 2 x 8) clock pulses is generated on the clock line. Only one clock is provided to an user for telecommand and telemetry.

REQ.

The falling edge is the active edge.

Data

One data line is provided by the user to the Data Handling subsystem.

Via these lines, the TLM data shall be clocked out to the Data Handling subsystem in NRZ-L code. The data shall be clocked out with the MSB first.

REQ.

The MSB shall be present (t7) after the falling edge of the sampling pulse signal. The first clock pulse shall move the (MSB-0) bit into the MSB position at the output driver. This shifting of data shall take place with a delay time (Thold_TX) after the falling edge of the clock pulse.

5.2.3.2.5.2 Conventions

Time duration :

The time duration is defined at 50% of the measured full amplitude.

Signal rise and fall times :

The rise and fall times of a signal are defined as the time between 10% and 90% of the measured voltage swing.

Signal skew :

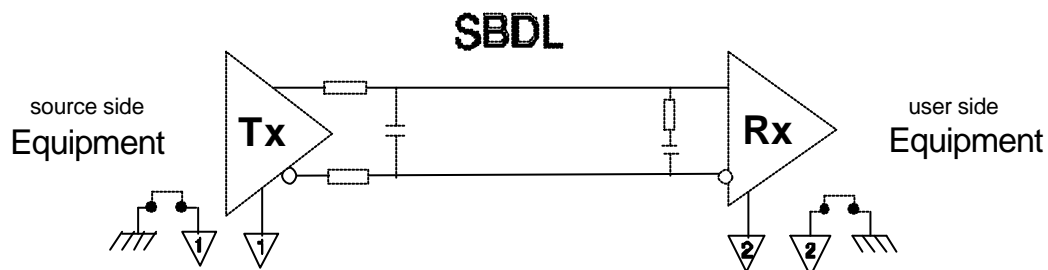
The timing skew between two signals (between inverted and non-inverted lines) is defined as the time between the instants when the voltage crosses 50% of the measured full amplitude.

Measurements :

Measurements are made at the user input level.

5.2.3.2.5.3 Digital serial telemetry schematics

for Sample, Data and Clock



5.2.3.2.5.4 Corresponding TC

REQ.

The MLC and the corresponding verification Digital Serial Telemetry shall be identical words.

5.2.3.2.5.5 Digital serial Electrical characteristics

REQ.

Although the SBDL line is symmetrical, the two shall be identified as « non-inverted line » and « inverted line » and shall use differential lines (drivers/receivers).

Digital serial telemetry characteristics are detailed :

- * **Table** :SBDL Characteristics and **Table** :Digital Serial Telemetry timing
- * **Figure** :TBC and **Figure** :Digital Serial 16-bit telemetry signal waveform diagram
- * **Figure** :Digital Serial 16-bit telemetry signal detailed waveform diagram

REQ.

The digital serial telemetry shall comply the SBDL characteristics.(**Table** : SBDL CHARACTERISTICS)

5.2.3.2.5.6 digital serial telemetry TIMING

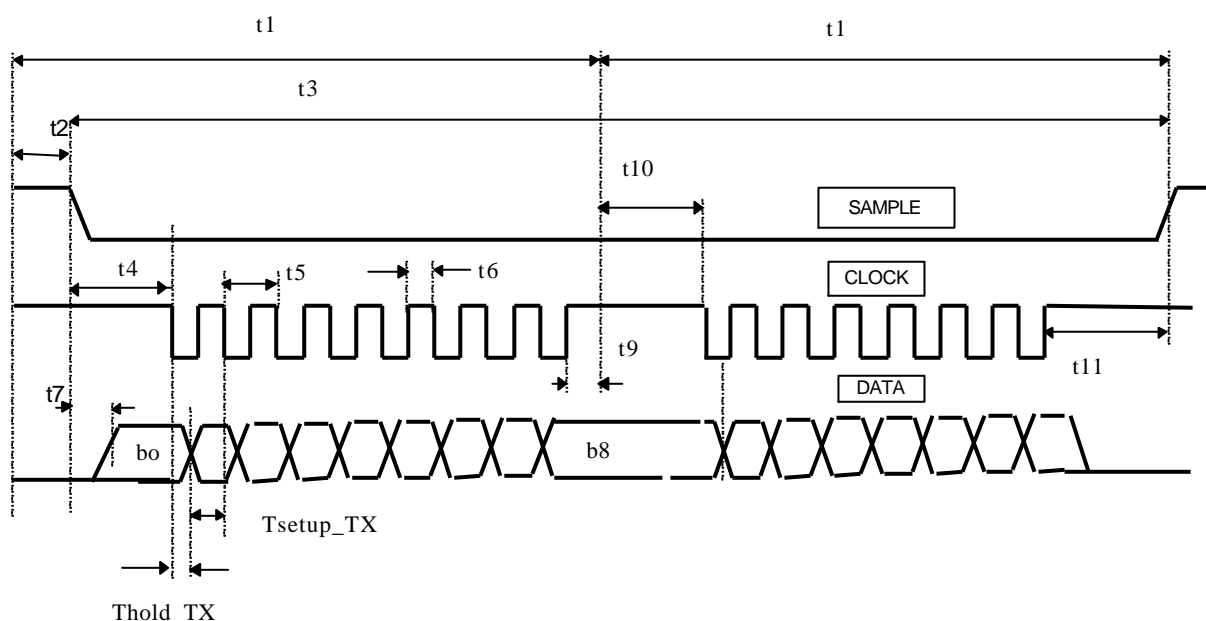


Figure : DIGITAL SERIAL 16-BIT TELEMETRY SIGNAL WAVEFORM DIAGRAM

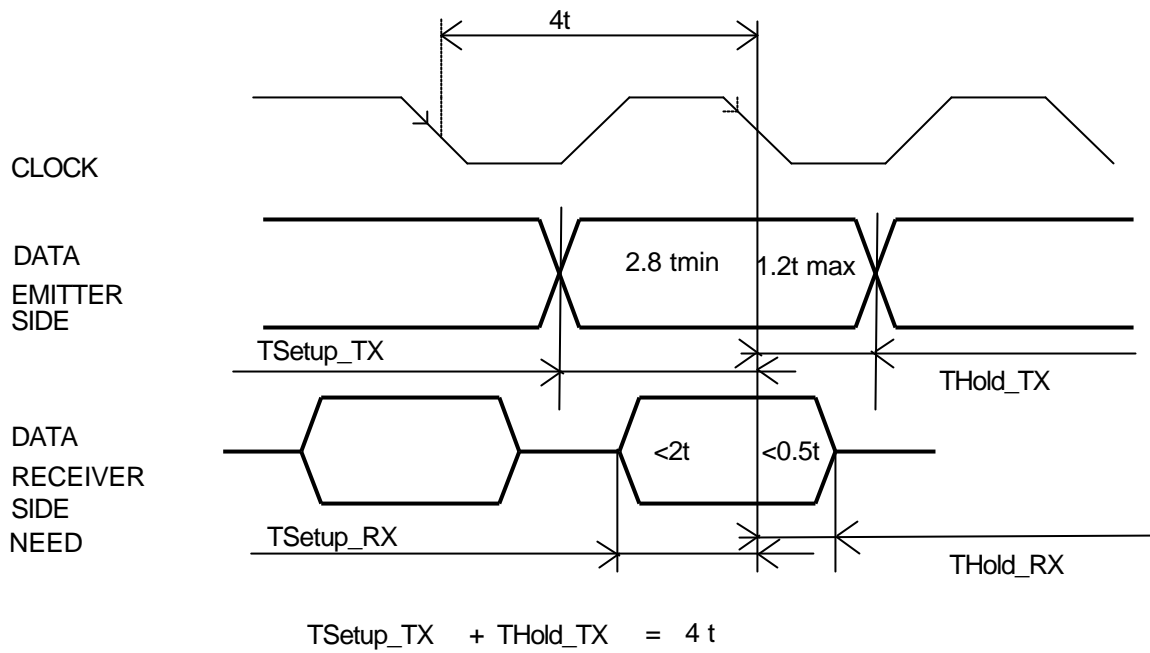


Figure: DIGITAL SERIAL SIGNAL DETAILED WAVEFORM DIAGRAM

TIMING		
t	Référence time	$1/(2^{20}) \text{ sec} = 0.954 \mu\text{s}$
t1	Transfer half duration	$64t \pm t$
t2	Sample Inactive state duration	$4t \pm t$
t3	Sample active state duration	$124t \pm t$
t4	Sample to clock delay	$28t \pm t$
t5	Clock period	$4t \pm 0.1t$ (262144 Hz)
t6	Active to inactive edge of clock delay	$2t \pm 0.6t$ (*)
t7	Sample to data delay	$< 4t$
t9	inactive edge clock to half transfer delay	$2t \pm 0.6t$
t10	Half transfer to clock	$32t \pm 2t$
t11	inactive edge clock to transfer end	$> 1.5t$
Tsetup_TX	Data present to clock (emitter side)	$> 2.8t$
Thold_TX	Clock to data end (emitter side)	$< 1.2t$
Tsetup_RX	Data present to clock (receiver side)	$< 1.5t$
Thold_RX	Clock to data end (receiver side)	$< 0.5t$
Tskew	falling to rising edge delay	$< 100 \text{ ns}$

Table : DIGITAL SERIAL TELEMETRY TIMING

Differential propagation between signals of a DS shall not be taken into account

(*)the rising edge jitter is acceptable inside the specification. This edge shall not be used.

5.2.3.2.5.7 Digital Serial channels interconnection

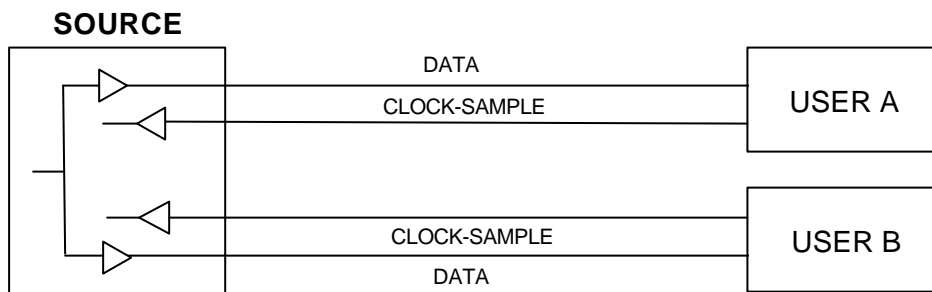
5.2.3.2.5.7.1 High-priority telemetry signal

5.2.3.2.5.7.1.1 High-priority telemetry definition

A telemetry is considered as a high priority telemetry if there is :

- two outputs of this telemetry in hot redundancy
- two inputs on encoder equipments

These telemetries are identified in the relevant subsystem or unit specification.



5.2.3.2.5.7.1.2 High-priority telemetry harness

REQ.

The basic definition of the harness shall be a shielded 2-wire twisted pair for each line with the active line and its return

5.2.3.2.5.7.1.3 High-priority telemetry fail-safe requirements

REQ.

The source circuitry design shall be such that any single failure in the source does not cause the loss of both redundant telemetry signal outputs.

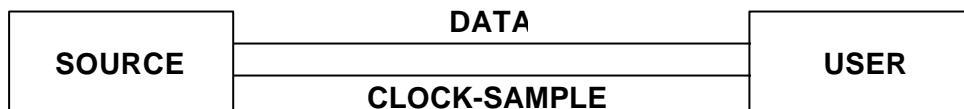
The user circuitry design shall be such that any single failure in the users does not cause the loss of both redundant telemetry signal.

5.2.3.2.5.7.2 Low priority telemetry signal

5.2.3.2.5.7.2.1 Low priority telemetry definition

A telemetry is considered as a low priority telemetry if there is :

- one output of this telemetry
- one input on encoder equipment



5.2.3.2.5.7.2.2 Low-priority telemetry

These telemetries are identified in the relevant subsystem or unit specification.

5.2.3.2.5.7.2.3 Low-priority telemetry harness

REQ.

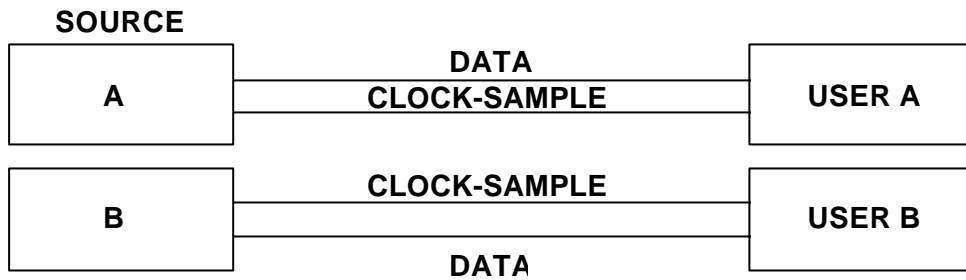
The basic definition of the harness shall be a shielded 2-wire twisted pair for each line with the active line and its return.

5.2.3.2.5.7.3 Cold redundancy

5.2.3.2.5.7.3.1 Cold redundancy definition

A telemetry is considered as a cold redundancy telemetry if there is :

- two separate outputs
- two separate inputs on encoder equipment



5.2.3.2.5.7.3.2 Cold redundancy telemetry

These telemetries are identified in the relevant subsystem or unit specification.

5.2.3.2.5.7.3.3 Cold redundancy telemetry harness

REQ.

The basic definition of the harness shall be a shielded 2-wire twisted pair for each line with the active line and its return.

5.2.3.2.6 Thermistors power supply and conditioning (TH)

5.2.3.2.6.1 Thermistors type

These channels are used to supply power, adaptation and amplification to thermistors :

DESIGNATION	TYPE	Temperature range	Corresponding R range
FENWAL	GB42	- 55 °C to + 155 °C	960 K Ω to 0.33 K Ω
or equivalent	526-31AN09-153	- 55°C to + 200°C	960 K Ω to 0.142K Ω
GULTON or Victory Engineering	34 TD 25	- 55 °C to + 125 °C	421 K Ω to 0.13 K Ω
ROSEMOUNT	118 MF	- 190 °C to + 180 °C	0.4 K Ω to 3.5 K Ω
ROSEMOUNT	118 MF	- 50 °C to + 400 °C	1.5 K Ω to 5 K Ω
Thruster thermistor	PT200	- 200 °C to + 520 °C	37.04 to 575.23 Ω

5.2.3.2.6.1.1 Type : GB42 or equivalent

The 25°C value is 15000 ohms.

Temperature(°C)	resistance (k.ohms)	temperature(°C)	resistance (k.ohms)
-55	957,0	55	4,923
-45	503,7	65	3,53
-35	276,2	75	2,57
-25	157,2	85	1,908
-15	92,6	95	1,43
-5	56,3	105	1,09
5	35,3	115	0,844
15	22,7	125	0,659
25	15,0	135	0,521
35	10,13	145	0,416
45	6,99	155	0,335
160	0,3024	185	0,1863
165	0,2733	195	0,1556

The nominal range value for this thermistor is between -55°C and + 150°C.

AMF are using the extended range between 150 °C and 200°C.

Resistance tolerance :

+/- 9.0 % to 1 % of R between -55°C and 0°C

+/- 1.0 % of R between 0°C and 155°C

+/- 1.0 % to 1.5% of R between 155°C and 200°C

5.2.3.2.6.1.2 Type : Gulton 34 TD 25 or equivalent

Maximum ratings :

current : 29 mA (recommended nominal maximum operating current : 1 mA)

power : 0.1 W at 25°C

temperature(°C)	resistance (k.ohms)	temperature(°C)	resistance (k.ohms)
-55	408,34	35	2,608
-45	197,88	45	1,7362
-35	100,81	55	1,1814
-25	53,74	65	0,8203
-15	29,85	75	0,5805
-5	17,21	85	0,4168
5	10,269	95	0,3055
15	6,321	105	0,2275
25	4	115	0,172
		125	0,1317

Resistance Accuracy : (at « zero » power)

+/- 3.3 % of R at -55.0°C

+/- 0.65 % of R at +70.0°C

+/- 1.53 % of R at 125.0°C

5.2.3.2.6.1.3 Type : ROSEMOUNT 118MF Platinum resistance

The 118 MF type are Platinum Thermistors.
The model « 2000 ohms at 0°C » shall be considered.

Maximum ratings :

current : 10 mA (recommended nominal maximum operating current : 1 mA)

power : 0.1 W at 25°C

temperature(°C)	resistance (ohms)	temperature(°C)	resistance (ohms)
-200	343,69	100	2779,8
-160	689,2	140	3085,2
-120	1026,44	180	3386,9
-80	1356,2	220	3684,9
-40	1680,2	260	3979,2
0	2000	300	4269,6
		340	4556,8
40	2314,7	380	4812
80	2625,7	400	4980

Resistance tolerance :

+/- 3% for -190 to -100°C range

+/- 2% for -100 to +400°C range

5.2.3.2.6.1.4 Thruster thermistor(PT200)

The PT200 type are Platinum Thermistors.
The model « 200 ohms at 0°C » shall be considered.

Maximum ratings :

current : 10mA

power : 0.1W

temperature(°C)	resistance (ohms)	Resistance tolerance (%)	temperature(°C)	resistance (ohms)	Resistance tolerance (%)
-200	37,04	3,4	80	261,79	2
-180	54,19	2,9	100	277,01	2
-160	71,09	2,6	140	307,17	2
-140	87,75	2,3	180	336,96	2
-120	104,22	2,3	220	366,38	2
-100	120,51	2	260	395,42	2
-80	136,65	2	300	424,1	2
-60	152,66	2	340	452,41	2
-40	168,54	2	380	480,35	2
-20	184,32	2	400	494,18	2
0	200	2	440	521,57	2
20	215,59	2	480	548,59	2
40	231,08	2	520	575,23	2
60	246,48	2			

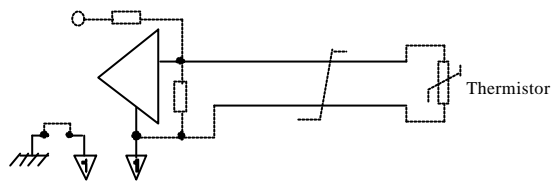
5.2.3.2.6.2 Thermistors schematics

REQ.

Both sides of the thermistor shall be completely isolated inside the equipment.

REQ.

The harness shall use unshielded **twisted** 2-wire pairs.



5.2.3.2.6.3 Thermistors channel telemetry characteristics

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
A	TYPE			
Req-1	Output type	differential balanced lines		
Req-2	Input type		Single ended	
Req-3	Transfer	DC COUPLER	DC COUPLER	
B	CURRENT			
Req-1	recommended maximum operating current	$\leq 1 \text{ mA}$		
C	IMPEDANCE			
Req-1	input impedance		$\leq 1 \text{ K}\Omega$	
D	GROUNDING AND ISOLATION			
Req-1	from secondary ground (OVs)	galvanic isolation	grounded	
Req-2	from primary ground	isolated ($\geq 1 \text{ M}\Omega$)	isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	at user side the isolation value is valid when the stud is disconnected
Req-3	from chassis	isolated ($\geq 1 \text{ M}\Omega$)	isolated ($\geq 1 \text{ M}\Omega$)	

Table: THERMISTOR TELEMETRY CHARACTERISTICS

5.2.3.3 Umbilical Strap

REQ.

The electrical characteristics of umbilical strap shall be as follows :

Code	PARAMETERS	SOURCE SIDE	USER SIDE (strap)	COMMENT
A	TYPE			
Req-1	Output type	Single ended		
Req-2	Input type		differential	
B	IMPEDANCE			
Req-1	Impedance open	$\leq 100 \text{ k}\Omega$	$\geq 10 \text{ M}\Omega$	separated
Req-2	Impedance closed	$\leq 100 \text{ k}\Omega$	$\leq 10 \text{ }\Omega$	not separated

Table: UMBILICAL STRAP CHARACTERISTICS

5.2.3.4 TTC : TRANSCEIVER SIGNALS INTERFACE

5.2.3.4.1 Transceiver TC

REQ.

The SMU shall interface 2 TTC RF parts (from the RT transceivers) in hot redundancy. The PM shall perform decoding of packets TC (CCDS format : ESA PSS 04-107) a 4Kb/s.

The SMU shall be compliant with the Digital serial electrical interfaces .

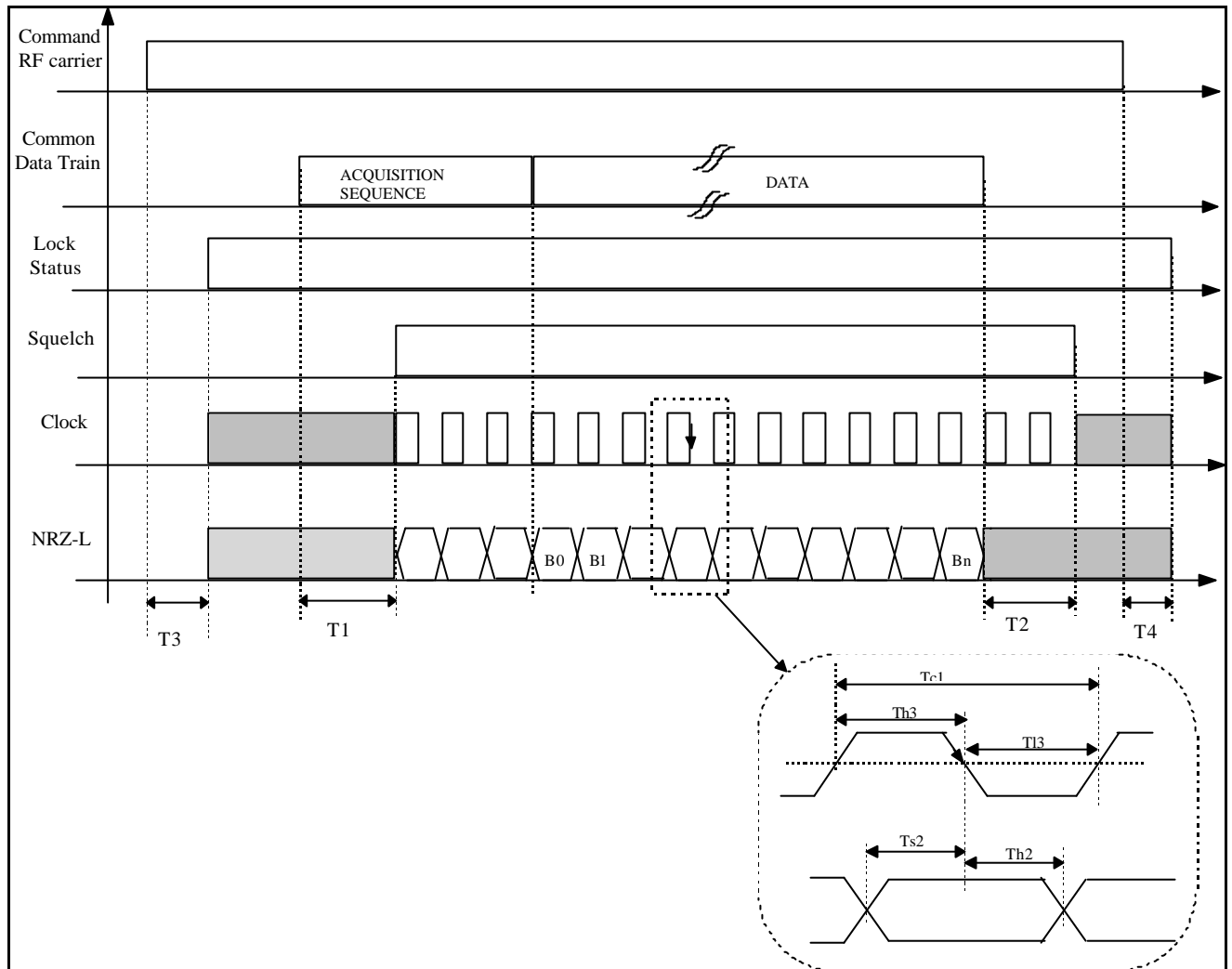


Figure: NRZ-L TC TIMING

T1 : £ 168 bits duration

1 bit duration £ T2 £ 128 bits duration

T3 & T4 £ 100ms

Tc1 (Bit clock period) = 1 Bit rate + /-5%

Th3 (TC bit clock high level duration at 50% edge) : $\geq 60\mu s$

Tl3 (TC bit clock low level duration at 50% edge) : $\geq 60\mu s$

Ts2 (Set-up time from NRZ DATA bit stable to clock falling edge (sampling edge)) : $\geq 10\mu s$

Th3 (Hold time from clock falling edge to NRZ DATA bit change) : $\geq 20\mu s$

The above described interface is used to transmit from the receiver to the SMU the following signal : SQUELCH , CLOCK , DATA

Notes :

The bit clock is running as soon as Lock Status is 'high' and it will run until Lock Status falls to 'low'.

REQ.

Data Validation shall be the clock falling edge.

REQ.

The bit clock stability shall be better than +/- 5% as soon as SQUELCH is high and until SQUELCH falls to low.

REQ.

The clock performances shall be met at least during one bit duration before the first transmitted and after the last transmitted .

REQ.

The interfaces shall comply two signal types :

- Nominal interfaces : RS422 standard with SBDL electrical characteristics.
- Backup interfaces : single ended version.

5.2.3.4.2 TRANSCEIVER TM video signals

REQ.

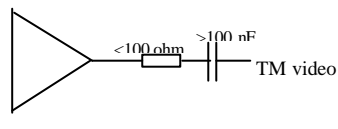
The TM video signals shall comply the following characteristics :

Code	PARAMETERS	Transmitter side SMU	Receiver side	COMMENT
A	TYPE			
Req-1	Output type	single ended		
Req-2	Input type		differential	
Req-3	Type of Modulation	PCM(NRZ-L)/BPSK	PCM(NRZ-L)/BPSK	
Req-4	Waveform	Filtered quasi sine wave	Filtered quasi sine wave	
B	VOLTAGE			
Req-1	output AC voltage	$3V \pm 5.7\%$ peak to peak		
Req-2	DC Fault Voltage Emission	$-1V < U < 10V$	$\pm 17V$ in series with > 2k Ω	
Req-3	DC Fault Voltage Tolerance	$\pm 17V$ in series with > 2k Ω	$-1V < U < 10V$	
C	IMPEDANCE			
Req-1	output impedance (1)	< 100 Ω in series with > 100nF		
Req-2	input impedance		> 10k Ω // < 500pF	
D	SPECIFIC REQUIREMENT			
Req-1	TM sub-carrier frequency	65536 Hz	65536 Hz	upgrade : 32768Hz
Req-2	TM sub-carrier frequency stability	$\pm 10^{-4}$		
Req-3	TM bit rate	4096 bit/s or 8192 bit/s	4096 bit/s or 8192 bit/s	
Req-4	Phase plot accuracy	$\pm 2^\circ$		Difference between theoretical and real phase
Req-5	group delay variations	< 1 μ s peak to peak		
Req-6	Amplitude distortion	< 1 dB peak to peak		
Req-7	signal to noise ratio	65 dBHz		

Code	PARAMETERS	Transmitter side SMU	Receiver side	COMMENT
Req-8	Spurious and Harmonics	<ul style="list-style-type: none"> • <-20dBc : 0 < f < 220kHz • <-60dBc : f > 220kHz 32768Hz +/- 8kHz 65536 Hz +/- 8kHz [15kHz ; 30kHz] 100kHz +/- 1kHz 	<p>N/A</p> <p>N/A</p>	<p>With respect to TM sub carrier levels</p> <p>TM signal bandwidth</p> <p>TM signal bandwidth</p> <p>Ranging signals bandwidth</p> <p>Ranging signals bandwidth</p>
Req-9	phase step response accuracy	± 5% (2)		
E	FAIL SAFE PROTECTION			
Req-1	protection	short circuit proof		

Table: TM VIDEO SIGNAL CHARACTERISTICS

(1)



(2) At all times, for more than 25% of a sub-carrier period after a phase reversal, the phase of the modulated sub-carrier shall be within ±5% of a perfect signal.

5.2.3.5 UMBILICAL INTERFACE

5.2.3.5.1 Umbilical definition

Proper telemetry and telecommand PCM signals shall be routed to the umbilical connector from data handling sub-system.

These signals are :

- two separate inputs for TC (one to/from each part of the central calculator)
- two separate outputs for TM (one to/from each part of the central calculator)

5.2.3.5.2 TC (transceiver) requirements

REQ.

The TC umbilical interface shall comply the TC transceivers interface characteristics.

5.2.3.5.3 Umbilical TM (transceiver) requirements

REQ.

The umbilical TM interface shall comply the TM video signal

5.2.3.6 EMERGENCY SIGNAL

5.2.3.6.1 Emergency signal definition

REQ.

The emergency information shall be presented by the source in the form of a digital relay or a digital bi-level, the active level shall be the contact closed and the non-active level shall be the contact in high impedance.

5.2.3.6.2 Emergency signal characteristics

Two electrical types of emergency signal exists : digital relay and SBDL .

REQ.

The Emergency signal interface shall comply the SBDL electrical characteristics : **Table:** SBDL Characteristics for : STARTRACKER, IRES, AOCSP, PROP .

Others Emergency signal interface shall comply the digital relay electrical characteristics : **Table:** Digital Relay Telemetry characteristics .

REQ.

Requirements 8 to 11 (**Table:** SBDL Characteristics) are not applicable to SBDL emergency signals. The fault voltage emission and tolerance shall be $\pm 7V$

5.2.3.6.3 Emergency signals returns on source side

5.2.3.6.3.1 Emergency signals returns référence

REQ.

Emergency signal shall be referenced to secondary ground inside the source equipment. Other design (Primary ground référence, ...) shall be prohibited.

5.2.3.6.3.2 Emergency signals returns separation

REQ.

Separated returns for nominal and redundant channels shall be provided.

5.2.3.6.3.3 Emergency signal returns number

refer to chapter 5.2.3.11

5.2.3.6.4 Emergency signals returns on user side

5.2.3.6.4.1 Emergency signals returns référence

REQ.

Emergency signals shall be completely isolated from any other return inside the user equipment as specified in TBC point E1.

5.2.3.6.4.2 Emergency signals common return

REQ.

The number of channels using the same return shall be limited to 2.

5.2.3.6.4.3 Emergency signals returns number

Refer to chapter 5.2.3.11

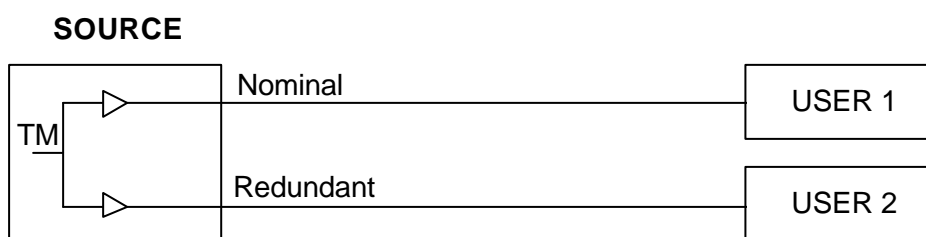
5.2.3.6.5 Emergency signals interconnection

5.2.3.6.5.1 High-priority signal

5.2.3.6.5.1.1 High-priority definition

A telemetry is considered as a high priority telemetry if there is :

- two outputs of this telemetry in hot redundancy
- two inputs on encoder equipments



5.2.3.6.5.1.2 High-priority telemetry

These telemetries are identified in the relevant subsystem or unit specification.

5.2.3.6.5.1.3 High-priority telemetry harness

REQ.

The basic definition of the harness shall be a unshielded twisted pair for each line with the active line and its return.

If the source furnishes several telemetries, active signals could be grouped with one return inside pairs (from 2-wire until 5-wire pairs).

5.2.3.6.5.1.4 High-priority telemetry fail safe requirements

REQ.

The source circuitry design shall be such that any single failure in the source does not cause the loss of both redundant telemetry signal outputs.

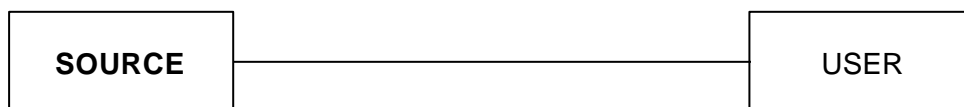
The user circuitry design shall be such that any single failure in the users does not cause the loss of both redundant telemetry signal.

5.2.3.6.5.2 Low priority telemetry signal

5.2.3.6.5.2.1 Low priority telemetry definition

A telemetry is considered as a low priority telemetry if there is :

- one output of this telemetry
- one input on encoder equipment



5.2.3.6.5.2.2 *Low-priority telemetry*

These telemetries are identified in the revelant subsystem or unit specification.

5.2.3.6.5.2.3 *Low-priority telemetry harness*

REQ.

The basic definition of the harness shall be a unshielded twisted pair for each line with the active line and its return.

If the source furnishes several telemetries, active signals could be grouped with one return inside pairs (from 2-wire until 5-wire pairs)

5.2.3.7 SYNCHRONISATION SIGNALS

The SMU provides three synchronisation signal :

- 1Hz : 1 + 1 output (1 nominal + 1 redundant)
- 10Hz : 4 + 4 output (4 nominal + 4 redundant)
- 1000Hz : 1 + 1 output (1 nominal + 1 redundant)

The 1 Hz signal period accuracy is better than $1s \pm 1\mu s$ by period.

10Hz, 1Hz clock rising transition is synchronous to 1000 Hz rising clock transitions.

REQ.

The synchronisation signals shall use the RS422 standard.

REQ.

These interfaces shall be fail safe if one of the users or the source channel failed in short circuit or in open circuit.

REQ.

The electrical characteristics are defined in the SBDL electrical characteristics

The requirements : Requirements B-Req8 to B-Req11 (: **Table:** SBDL Characteristics) are not applicable. To synchronisation signals The fault voltage emission and tolerance shall be $\pm 7V$.

REQ.

The current capability (high level) for the transmitter shall be : $> 50mA$.

REQ.

The receiver and the transmitter shall be differential and isolated from the primary ground and the chassis with a minimum impedance of $1M\Omega$ in parallel with $50nF$.

REQ.

The rise and fall time shall be : $100 ns < t < 500ns$.

5.2.3.8 ALARMS SIGNALS

Alarm signals use Emergency signal interface (§ 5.2.3.6.2). The receiver side is the SMU.

5.2.3.9 INTER SUBSYSTEMS LINKS

5.2.3.9.1 Harness definition responsibility

The links definition between two subsystems is under the Prime responsibility.

5.2.3.9.2 Design rules

REQ.

The unit and subsystems design shall not induce harness constraints in term of length (max 15m), unshielding unless justified by analysis. Exception is made with high current links where maximum length could be limited to 5 m

These links are:

- OBDH links
- Video and umbilical links
- Power links
- TM and TC links
- Emergency, Alarm signals
- Solar Array deployment signals.

5.2.3.10 Specific Interfaces

5.2.3.10.1 UPS Interfaces

The PROP will interface the equipments detailed in the following table :

	<u>NOMINAL</u>		<u>BACKUP</u>	
	RÉFÉRENCE	TENSION	RÉFÉRENCE	TENSION
<u>UPS</u>				
LAE 400N	motor DASA : S400-12 valve MOOG : 53-216	50V	motor MARQUARDT : R-4D-15 valve MARQUARDT : R-4D	50V
RCT 10N	motor DASA : S10-20 valve bi/mono MOOG : 51-219 valve bi/mono MOOG : 51-220	50V 42V	motor LEROS 10 valve bi/mono MOOG : 51-214	42V
Standard Pressure Transducer	GULTON : PA 4089	28V	SEP : 215X-S4	28V

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 166 / 213

High Accuracy Pressure Transducer	AEROQUARTZ : 7525-001(LP) and 7525-002(HP) 1475-001(LP) and 1475-002(HP)	8.5 to 12V	NEANT	
PPS				
Bistable valve	VACCO : VIC 10592	42-50V		
Standard Pressure Transducer	GULTON : PA 4089	28V	SEP : 215X-S4	28V

Table: UPS EQUIPMENTS

5.2.3.10.1.1 ABM Valve Interface

REQ.

The ABM valve interface shall comply the following characteristics :

Code	PARAMETERS	SOURCE SIDE PROP	USER SIDE ABM 53-216	USER SIDE ABM R-4D	COMMENT
A	TYPE				
Req-1	Output type	single ended			
Req-2	Input type		differential 2 coil in series	differential 2 coil in series	
B	VOLTAGE				
Req-1	Operating Voltage Range	43V<Vn< 53V	42 to 54 V	32 to 53 V	2 coil in series
Req-2	Pull-in Voltage	>39V (2 coils in series)	≤18.3V (per coil)	20V to 35V (2 coils in series)	300mV harness drop voltage
Req-3	Drop-out Voltage	<1V	≤1.5V	≤1.5V	per coil
Req-4	Holding Voltage	>16V (2 coils in series)	≤7.5V (per coil)	≤7.5V (per coil)	100mV harness drop voltage
Req-5	Fault voltage emission	<53V			
Req-6	Fault voltage tolerance		54V	53V	2 coil in series
C	POWER				
Req-1	Nominal Power consumption		29W (25V per coil)	43.5W (42V for 2 serial coils)	
D	TIME				
Req-1	Opening response time		≤30ms	<30ms	
Req-2	Closing response time		≤30ms	<10ms	
E	IMPEDANCE				
Req-1	Coil Inductance		≤350mH	<900mH	at 21°C per coil
Req-2	Coil Resistance		17.2 Ω<R<28.7 Ω	16.6 Ω<R<26.5 Ω	including temperature range
F	GROUNDING AND ISOLATION				
Req-1	Insulation resistance to from chassis	>1 MΩ	>100 MΩ	>50 MΩ	

Table : ABM INTERFACE CHARACTERISTICS

5.2.3.10.1.2 Commanding and monitoring Bi-Stable Valves

The bi-stable commands functioning are equivalent to command matrix functioning.
Electrical characteristics are different .

5.2.3.10.1.2.1 Bistable Valves interface

REQ.

The Bistable valve interface shall comply the following characteristics :

Code	PARAMETERS	SOURCE SIDE (PROP)	USER SIDE 51-214/51-220	USER SIDE 51-219	COMMENT
A	TYPE				
Req-1	Output type	single ended			
Req-2	Input type		differential	differential	bistable
B	VOLTAGE				
Req-1	Operating Voltage Range		25 to 42Vdc	32 to 51.5V	
Req-2	Pull-in Voltage	> 32V	< 32V	32 to 51.5V	
Req-3	Drop-out Voltage		< 32V	32 to 51.5V	
Req-4	Fault voltage emission	55V (50ms)			
Req-5	Fault voltage tolerance		55V (50ms)	55V	
C	POWER				
Req-1	Power consumption		< 8W	< 8.5W	
D	TIME				
Req-1	Opening/closing response time	> 15ms	< 15ms	< 15ms	50V at 21°C
E	IMPEDANCE				
Req-1	Coil Inductance		≤ 1 H	≤ 750mH	at 21°C
Req-2	Coil Resistance		260 Ω < R < 482 Ω	260 Ω < R < 485 Ω	including temperature range
F	GROUNDING AND ISOLATION				
Req-1	Insulation resistance to from chassis		> 100 MΩ	> 100 MΩ	at 20°C

Table: BI-STABLE Valve characteristics

5.2.3.10.1.2.2 PPS Valve (VACCO)

REQ.

The PPS valve interface shall comply the following characteristics :

Code	PARAMETERS	SOURCE SIDE (PROP)	USER SIDE	COMMENT
A	TYPE			
Req-1	Output type	single ended		
Req-2	Input type		differential	bistable
B	VOLTAGE			
Req-1	Operating Voltage Range	$31V < V_n < 51V$	30V to 51V	
Req-2	Fault voltage Tolerance		55V	
Req-3	Fault voltage Emission	<55		
C	POWER			
Req-1	Power consumption		42W	50V & 21°C
Req-1	Current		0.82A	
D	TIME			
Req-1	Opening/closing response time	>50ms	<50ms	50V & 21°C
E	IMPEDANCE			
Req-1	Coil Inductance		200mH	1kHz
Req-2	Coil Resistance		$47\Omega < R < 75\Omega$	including temperature range
F	GROUNDING AND ISOLATION			
Req-1	Insulation resistance to from chassis		100 M Ω	500VDC

Table: PPS VALVE CHARACTERISTICS

5.2.3.10.1.3 Mono-Stable Valves

REQ.

The mono-stable valve command shall be pulse type, with a 1ms resolution on pulse duration and on pulse start.

The mono-stables command shall operate simultaneously up to 10 valves continuously.

REQ.

Each command generated by the function shall be read back to generate a mono-stables status .

REQ.

The On time of the mono-stables shall last from 1 ms to hours with repetition frequency of 33Hz.

5.2.3.10.1.3.1 Mono-stable Valve Interface

REQ.

The Mono-stable valve interface shall comply the following characteristics :

Code	PARAMETERS	SOURCE SIDE (PROP)	USER SIDE 51-219	USER SIDE 51-214/51-220	COMMENT
A	TYPE				
Req-1	Output type	single ended			
Req-2	Input type		differential	differential	monostables
B	VOLTAGE				
Req-1	Operating Voltage Range		35V to 51.5V	25 to 42V	
Req-2	Pull-in Voltage	>36V	>35V	10V	
Req-3	Drop-out Voltage		>3V	7V	
Req-4	Fault voltage emission	55V (50ms)			
Req-5	Fault voltage tolerance		55V (30s)	55V	
C	POWER				
Req-1	Power consumption		<8.5W	<8W	
D	TIME				
Req-1	Opening/closing response time		< 2.4 ms	<2.5 ms	50V at 45°C
E	IMPEDANCE				
Req-1	Coil Inductance		≤500mH	< 1H	at 21°C
Req-2	Coil Resistance		273 Ω < R < 478 Ω	190 Ω < R < 325 Ω	including temperature range
F	GROUNDING AND ISOLATION				
Req-1	Insulation resistance to from chassis		>100 MΩ	>100 MΩ	at 20°C

Table: MONO-STABLE VALVES CHARACTERISTICS

5.2.3.10.1.4 Pressure Transducer

5.2.3.10.1.4.1 Standard pressure transducer

5.2.3.10.1.4.1.1 Supply characteristics

REQ.

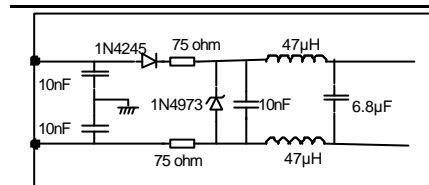
The standard pressure transducer supply interface shall comply the following characteristics :

Code	PARAMETERS	SOURCE SIDE (PROP)	USER SIDE (GULTON)	USER SIDE (SEP)	COMMENT
A	TYPE				
Req-1	Output type	single ended			
Req-2	Input type		differential	differential	
B	VOLTAGE				
Req-1	Nominal Voltage	28V	28V	28V	
Req-2	Operating Voltage Range	26.5 > Vop > 28.5V	24 to 32V	26 to 28.5V	
Req-3	Fault voltage emission	< 30V			
Req-4	Fault voltage tolerance		37V	30V	
C	CURRENT				
Req-1	Nominal Current		17mA	< 20mA	
Req-2	Input current range		16 to 20mA	/	
Req-3	Inrush Current		200 mA max, 4ms	/	100 A/s ma
D	POWER				
Req-1	Power consumption		0.408 to 0.64W	< 1W	
E	IMPEDANCE				
Req-1	Input impedance		> 1.4 kΩ	/	10 m of 26 AWG between PROP and Pressure transducer

F	GROUNDING AND ISOLATION				
Req-1	Insulation resistance from chassis		> 100 MΩ	> 100 MΩ	50V
G	TIME				
Req-1	Power On Step response off to steady state	NA	250ms		
Req-2	Power OFF step response	NA	900ms		

Table: STANDARD PRESSURE TRANSDUCER INPUT CHARACTERISTICS

Input filters :



5.2.3.10.1.4.1.2 Standard pressure transducer Telemetry characteristics

REQ.:

The standard pressure transducer telemetry interface shall comply the following characteristics :

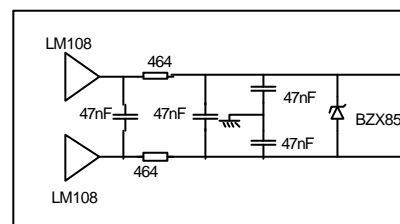
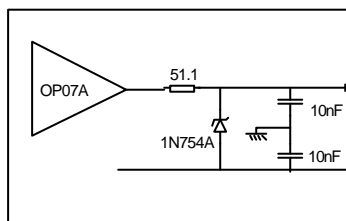
Code	PARAMETERS	SOURCE SIDE (GULTON)	SOURCE SIDE (SEP)	USER SIDE (PROP)	COMMENT
A	TYPE				
Req-1	Output type	Differential	Differential		
Req-2	Input type			Differential	
B	VOLTAGE				
Req-1	Voltage Range	0 V/ 5V	0 V/ 5V		Output noise : 20mVpp (20MHz bandwidth)
Req-2	Output voltage shift	±5mV	/		
Req-3	Common mode			(1)	
Req-4	Fault Voltage Emission	U < 15V	-1V < U < 8.2V	± 16 V	
Req-5	Fault Voltage Tolerance	+ 15 V	± 16 V	-1.5V < U < 15V	
Req-6	Ripple and noise	25mV peak			
C	CURRENT				
Req-1	short circuit current	< 30mA	5mA		

D	IMPEDANCE				
Req-1	ON Impedance	< 100 Ω	< 1k Ω	$\geq 1M\Omega$	
Req-2	OFF Impedance	< 20 k Ω	< 1k Ω	$\geq 1M\Omega$	
Req-3	Low pass filter	1kHz and 6dB/Oct			
Req-4	Capacity	deleted	deleted	deleted	
E	GROUNDING OR ISOLATION				
Req-1	from supply ground	> 100 M Ω	> 100M Ω	$\geq 1 M\Omega$	
Req-2	chassis	$\geq 100 M\Omega$	$\geq 100 M\Omega$	$\geq 1 M\Omega$	

Table: STANDARD PRESSURE TRANSDUCER TELEMETRY CHARACTERISTICS

- (1) * The common mode voltage is related to chassis ground.
- * The interfaces shall not be susceptible to a 3.5 Vrms sine wave injected from 30 Hz to 300 KHz, decreasing by 20 db per decade up to 1Mhz and 1 Vrms from 1 Mhz to 50 Mhz.

Simplified schematic (for information) :



5.2.3.10.1.4.2 High Accuracy Pressure Transducer :

Reference : 7525-001 AEROQUARTZ

5.2.3.10.1.4.2.1 Supply characteristics

REQ.

The high accuracy pressure transducer supply interface shall comply the following characteristics :

Code	PARAMETERS	SOURCE SIDE (PROP)	USER SIDE	COMMENT
A	TYPE			
Req-1	Input type		NA	
Req-2	Output type	NA		
B	VOLTAGE			
Req-1	Operating Voltage Range		9 to 25V	
Req-2	Nominal Supply Voltage	11V +/-5 %		
Req-3	Fault voltage emission	< 25V with current limitation < 15V without current limitation		
Req-4	Fault voltage tolerance		25V	
C	POWER			
Req-1	Power consumption		30mW at 8.5V 72 mW at 11V 90mW at 12V 587mW at 25V	
Req-2	Fault current	< 25 mA		cf. B Req.3
D	IMPEDANCE			
Req-1	Input resistance		≥ 800 Ω	
F	GROUNDING AND ISOLATION			
Req-1	Insulation resistance to from chassis		> 20MΩ (50V) 100nF	

Table: HIGH ACCURACY TRANSDUCER INPUT CHARACTERISTICS

5.2.3.10.1.4.2.2 Telemetries characteristics

REQ.

The high accuracy pressure transducer telemetry interface shall comply the following characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE (PROP)	COMMENT
A	TYPE			
Req-1	Output type	single ended		square wave AC coupled
Req-2	Input		Differential	
B	VOLTAGE			
Req-1	Voltage range	5Vpp +/- 0.5V	5Vpp +/- 0.25	with a 0.1µF serial capacitor 250 mV harness drop voltage
D	IMPEDANCE			
Req-1	Output Impedance	< 2 KΩ		
Req-2	Input Impedance		5kΩ < R < 10kΩ	
F	TIME			
Req-1	Full Scale (Pressure) frequency span	1.5 to 4 kHz		
Req-2	Pressure frequency range	30 to 42 kHz		
Req-3	Temperature frequency range	162 to 182 kHz		sensitivity : 45ppm/°C
G	GROUNDING AND ISOLATION			
Req-3	from chassis	> 20MΩ (50V) // 100nF	≥ 1 MΩ // < 50nF	

Table: HIGH ACCURACY PRESSURE TRANSDUCER TELEMETRIES CHARACTERISTICS

5.2.3.10.1.5 UPS Digital relay characteristics

REQ.

The UPS Digital relay interface shall comply the following characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE (PROP)	COMMENT
A	TYPE			
Req-1	Output type	differential balanced lines		
Req-2	Input type		differential	
B	VOLTAGE			
Req-1	contact capability	17 V		permanent
C	CURRENT			
Req-1	contact capability	$I > 5\text{mA}$	$1\text{mA} < I < 5\text{mA}$	permanent per closed contact
D	IMPEDANCE			
Req-1	impedance open	$\geq 10\text{ M}\Omega$	$\leq 100\text{ k}\Omega$	
Req-2	Impedance closed	$\leq 1\text{ }\Omega$	$\leq 100\text{ k}\Omega$	
E	TIME			
Req-1	Rise Time (Tr) and Fall Time (Tf)		$T_r, T_f \geq 1\text{ ms}$	
Req-2	"On" duration (Td)		$T_d \geq 20\text{ ms}$	
F	MATRIX COMMAND GROUNDING AND ISOLATION			
Req-1	between row / column lines and Chassis	$\geq 1\text{ M}\Omega$	one $1\text{ M}\Omega$ resistor per row at user side	
Req-2	between electrical circuitry OV's and Chassis		$1\text{ M}\Omega // < 100\text{ pF}$	
G	SINGLE COMMAND GROUNDING AND ISOLATION			
Req-1	from secondary Ground (OV's)	galvanic isolation	connected	use of relay contact at source side
Req-2	Chassis	isolated ($\geq 1\text{ M}\Omega$)	isolated ($\geq 1\text{ M}\Omega$)	at user side, the isolation value is valid when the stud is disconnected
H	SPECIFIC REQUIREMENT			

Req-1	serial diode in matrix command organisation	two diodes in series with the switch closure device	At least one serial diode on the positive output (row line output)	
Req-3	number of pins for return lines			see § 5.2.3.11 page 208

Table: UPS DIGITAL RELAY TELEMETRY CHARACTERISTICS

5.2.3.10.2 Heaters characteristics

5.2.3.10.2.1 General characteristics

Code	PARAMETERS	Heater	COMMENT
A	TYPE		
1	Output	differential	
B	POWER		
1	Max power	8 W/cm ²	heater surface : 15 cm ²
C	IMPEDANCE		
1	Max resistance	180 Ω/cm ² 100 Ω/cm ²	classic heaters perforated heaters tolerance ± 10%
2	Max capacitance	< 5nF	
3	Max inductance	5 μH	
D	GROUNDING AND ISOLATION		
1	from chassis	> 1000 MΩ	

Table : HEATER GENERAL CHARACTERISTICS

5.2.3.10.2.2 Heaters interface characteristics

Code	PARAMETERS	SOURCE SIDE	USER SIDE (DHP)	COMMENT
A	TYPE			
Req-1	Output	Differential		
B	POWER			
Req-1	120W heater Maximum power	120W	120W	
Req-2	80 W heater Maximum power	80W	80W	
Req-3	60 W heater Maximum power	60W	60W	
Req-4	40 W heater Maximum power	40W	40W	
Req-5	30 W heater Maximum power	30W	30W	
Req-6	15 W heater Maximum power	15W	15W	
Req-7	7 W heater Maximum power	7W	7W	
Req-8	Power Tolerance	± 10%	± 10%	except for 120W heater
Req-9	120W heater Power Tolerance	- 10%	- 10%	
Req-10	AMF Heater	30-50W	30-50W	
C	IMPEDANCE			
Req-1	Max capacitance	< 5nF		
Req-2	Max inductance	5 µH		+ 7µH Harness : twisted pair:AWG 24 or 26
Req-3	Max resistance	(1)		
D	GROUNDING AND ISOLATION			
Req-1	from Primary Ground	/	connected	
Req-2	from chassis	> 100 MΩ	≥ 1 MΩ // ≤ 50 nF	

Table: HEATER INTERFACE CHARACTERISTICS

(1) The maximum resistance is defined by the heater power.

5.2.3.10.3 Deployment, Full Step, Sinus Cosinus motors Interfaces

5.2.3.10.3.1 Mechanism Motors Interfaces

5.2.3.10.3.1.1 Bi and three phases steppers interface characteristics

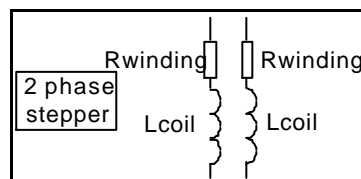
5.2.3.10.3.1.1.1 BAPTA motor interfaces

REQ.

The BAPTA interfaces (motor and Pcb) shall comply the following characteristics :

Code	PARAMETERS	BAPTA MOTOR	COMMENT
A	CURRENT		
Req-1	Current	$I < 300\text{mA}$	
B	IMPEDANCE		
Req-1	2 phase winding resistance	$60\Omega < R_{\text{winding}} < 115\Omega$	Including temperature range
Req-2	typical 2 phase winding inductance	$L_{\text{coil}} = 200\text{mH} \pm 20\%$	Including temperature range
C	GROUDING AND ISOLATION		
Req-1	Insulation resistance between windings	$> 50 \text{ M}\Omega \text{ } 250\text{V}$	
Req-2	Insulation resistance : Winding/case	$> 50 \text{ M}\Omega \text{ } 200\text{V}$	
D	FAILURE MODE		
Req-1	Insulation resistance between windings	$> 50 \text{ M}\Omega \text{ } 250\text{V}$	
Req-2	Insulation resistance : Winding/case	$> 50 \text{ M}\Omega \text{ } 200\text{V}$	

Table : BAPTA CHARACTERISTICS



For information, the 2 phase winding resistance at ambient temperature(25°C) is :

$$88\Omega < R_{\text{winding}} < 91\Omega$$

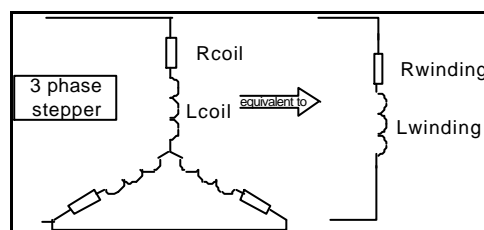
5.2.3.10.3.1.1.2 Antenna pointing motor interfaces

REQ.

The antenna pointing interfaces (motor and Pcb) shall comply the following characteristics :

Code	PARAMETERS	Antenna pointing motor	COMMENT
A	VOLTAGE		
Req-1	Voltage	26V \pm 10%	
B	IMPEDANCE		
Req-1	3 phase winding resistance	$40\Omega < R_{winding} < 120\Omega$	Including temperature range
Req-2	typical 3 phase winding inductance	L coil=20.4mH \pm 20%	Including temperature range
C	GROUDING AND ISOLATION		
Req-1	Insulation resistance between windings	> 50 M Ω 250V	
Req-2	Insulation resistance : Winding/case	> 50 M Ω 200V	
D	FAILURE MODE		
Req-1	Insulation resistance between windings	> 50 M Ω 250V	
Req-2	Insulation resistance : Winding/case	> 50 M Ω 200V	

Table : APM CHARACTERISTICS



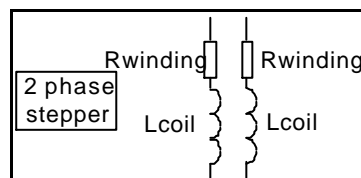
5.2.3.10.3.1.1.3 Thruster orientation motor interfaces

REQ.

The thruster orientation interfaces (motor and Pcb) shall comply the following characteristics :

Code	PARAMETERS	Thruster orientation motor	COMMENT
A	VOLTAGE		
Req-1	Voltage	26V \pm 10%	
B	IMPEDANCE		
Req-1	2 phase winding resistance	$60\Omega < R_{winding} < 120\Omega$	Including temperature range
Req-2	typical 2 phase winding inductance	L coil = 200mH \pm 20%	Including temperature range
C	GROUDING AND ISOLATION		
Req-1	Insulation resistance between windings	> 50 M Ω 250V	
Req-2	Insulation resistance : Winding/case	> 50 M Ω 200V	
D	FAILURE MODE		
Req-1	Insulation resistance between windings	> 50 M Ω 250V	
Req-2	Insulation resistance : Winding/case	> 50 M Ω 200V	

Table : TOM CHARACTERISTICS



5.2.3.10.3.1.2 Brush motor interface

REQ.

The Brush motor interfaces (motor and Pcb) shall comply the following characteristics :

Code	PARAMETERS	BRUSH MOTOR	MOTOR PCB	COMMENT
A	TYPE			
Req-1	deleted			
Req-2	deleted			
B	VOLTAGE			
Req-1	Voltage Range	$0V < U < 28 V$		
Req-2	Nominal Voltage : braking mode		$U < 9V$	
Req-3	Nominal voltage : motor mode		$6.3V \pm 5\%$	
C	POWER			
Req-1	Power consumption	3.4 W 5.1 W 8.9 W		Supply 9V at 85°C Supply 9V at 25°C Supply 10V at -50°C
D	CURRENT			
Req-1	deleted			
Req-2	deleted			
Req-3	Maximum current	$\pm 1A$	$\pm 1A$	
Req-4	Nominal Current	$-0.2A < I < 0.275A$	$-0.2A < I < 0.275A$	
E	IMPEDANCE			
Req-1	winding resistance	$9.9\Omega < R < 20.5\Omega$		Including temperature range
Req-2	winding inductance	$1mH < L < 4mH \pm 10\%$		
Req-3	deleted			
F	GROUDING AND ISOLATION			
Req-1	Insulation Impedance : Winding/case	1 nF		
Req-2	Insulation Impedance : Winding/ Winding	0.4 nF		

Table : Brush motor characteristics

5.2.3.10.3.2 Sensors Interfaces

5.2.3.10.3.2.1 Potentiometers Interfaces

REQ.

The potentiometers interfaces shall comply the following characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE (motor pcb)	COMMENT
A	TYPE			
Req-1	Output	Floating		
B	IMPEDANCE			
Req-1	deleted			
Req-2	deleted			
Req-3	Resistance range	$5\text{ k}\Omega < R < 20\text{ k}\Omega \pm 10\%$	$> 10\text{M}\Omega$	
C	POWER			
Req-1	Maximum power	1/4 W		
D	GROUDING AND ISOLATION			
Req-1	Insulation resistance : leads	$> 100\text{M}\Omega$ 100V		

Table : COARSE AND FINE POTENTIOMETER CHARACTERISTICS

5.2.3.10.3.2.2 Micro-switch Interface

REQ.:

The micro-switch interface shall comply the digital relay interface.

REQ.

The interface shall comply the two types of micro-switch :

- Normally Open
- Normally Closed

5.2.3.10.3.2.3 Optical Encoder Interface

REQ.

Code	PARAMETERS	SOURCE SIDE OPTICAL ENCODER	USER SIDE Motor Pcb	COMMENT
A	TYPE			
Req-1	Output	RS422		absolute, 12 to 24 bits
B	VOLTAGE			
Req-1	Threshold voltage		400mV	
Req-2	Power supply 1	15 V \pm 5%	15V \pm 2%	including ripple and transient
Req-3	Power supply 2	5 V \pm 5%	5V \pm 2%	including ripple and transient
Req-4	Permanent Fault Voltage Emission (Power supply 1)		\leq 16 V	
Req-5	Permanent Fault Voltage Emission (Power supply 2)		\leq 6 V	
Req-6	Line Overvoltage Tolerance	$>$ 6V	$>$ 6V	
Req-7	Line Overvoltage emission	\leq 6V	\leq 6V	through 120 Ω
C	CURRENT			
Req-1	Nominal Current Power supply 1 (+15V)	12 to 18 bits :In<20mA 18 to 21 bits :In<40mA 21 to 24 bits :In<80mA		
Req-2	Nominal Current Power supply 2 (5V)	12 to 18 bits :In<90mA 18 to 24bits :In<110mA		

D	IMPEDANCE			
Req-1	Supply 1 and 2 Capacitance value	10 μ F		

Table : OPTICAL ENCODER CHARACTERISTICS

REQ.

The PCB interface shall comply the following timing characteristics :

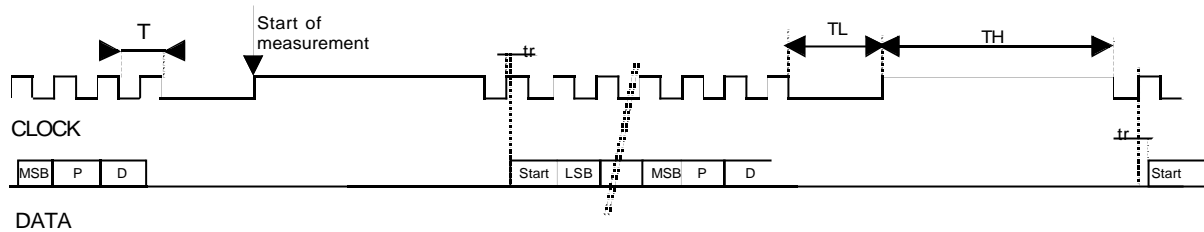


Figure: OPTICAL SERIAL OUTPUT DIAGRAM

P = Parity bit

A = Alarm bit

Clock = 2 Mhz max., 10kHz min

TL = 2T min.

	<u>12 to 14 bits</u>	<u>14 to 18 bits</u>	<u>18 to 21 bits</u>	<u>21 to 24 bits</u>
TH	7µs min.	15µs min.	25µs min.	45µs min.
tr	< 200 ns.	< 50 ns	< 50 ns	< 50 ns

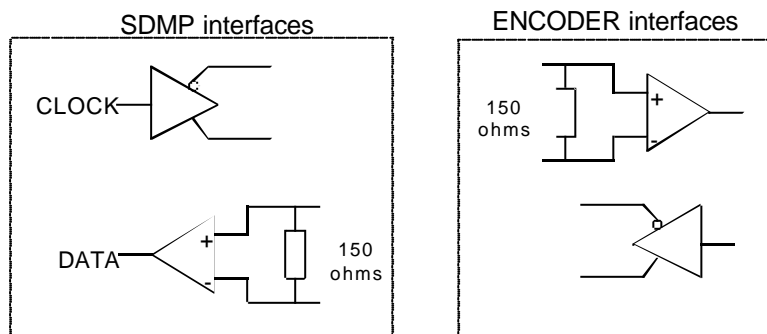


Figure: OPTICAL ENCODER ELECTRICAL INTERFACES

Truth table for parity bit

	Parity bit
If Σ of the bits at 1 (including start bit) is even then	0
If Σ of the bits at 1 (including start bit) is odd then	1

Truth table for alarm bit

	Alarm bit
No problem	0
In case of opto-electronic component ageing on the first track on the disk (only during this period) the bit becomes « 1 »	1

5.2.3.10.3.2.4 Optical switch interface

REQ.

The SDMP shall be able to supply and acquire optical switch in compliance with the following characteristics :

Parameter	Value
Redundancy	cold redundancy
Power supply (Vs)	+ 5V (DC) \pm 5%
Max. Consumption (Vs=5V)	50 mA
Output interface	open collector
Reference duration (tp)	>5ms
Switching time (td)	< 100ms

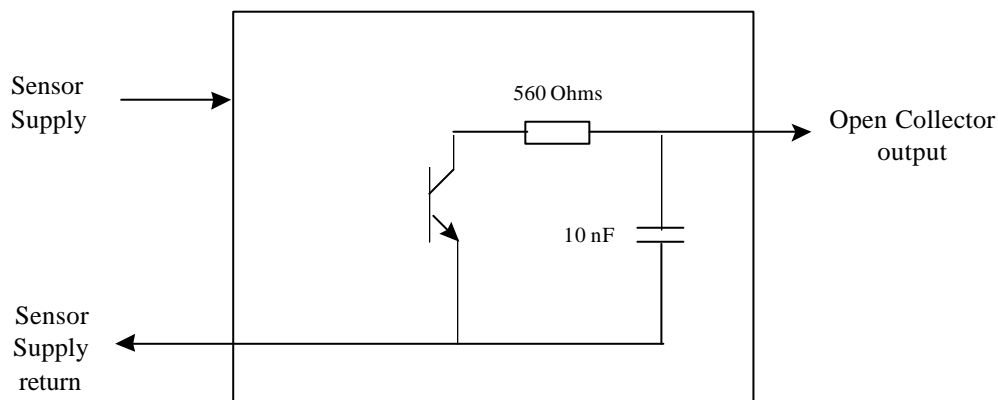


Figure : OPTICAL SWITCH ELECTRICAL INTERFACE

Rq : The output transistor is corresponding to a LM139 output transistor

REQ.

A pull-up resistor (R_c) shall be used to determine the two operating levels, according the following usage example :

Usage example with 12 V supply :

$$V_{ol} = 1.1V \text{ max } (R_c = 10 \text{ k}\Omega)$$

$$V_{oh} = 11.7V \text{ min } (R_c = 10 \text{ k}\Omega)$$

Maximum power set-up time = 50 ms.

REQ.

The maximum voltage applied to the input capacity of optical switch shall be less than 16V.

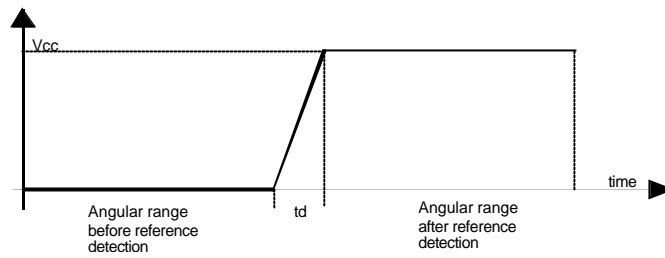


Figure : OUTPUT SIGNAL (FRONT)

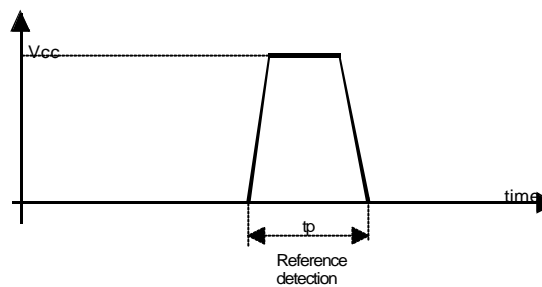
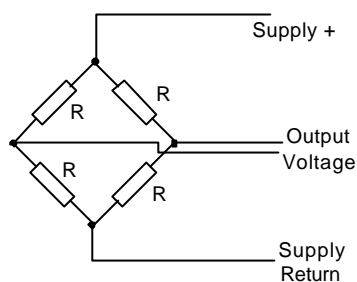


Figure: OUTPUT SIGNAL (PULSE)

5.2.3.10.3.2.5 Strain gauge

Three types of strain gauge exists :

- one type for deployment
- two types for battery



5.2.3.10.3.2.5.1 Deployment strain gauge

REQ.

The deployment strain gauge interface shall comply the following characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE (SDMP)	COMMENT
A	TYPE			
Req-1	Output	floating		
B	VOLTAGE			
Req-1	Supply voltage	10 V	10V ^{\$}	between strain gauge and SDMP : 6m of #24
Req-2	Output voltage	-20mV < Vo < + 20mV		
C	IMPEDANCE			
Req-1	gauge impedance (R)	700 Ω		Wheaston bridge
Req-2	Input telemetry impedance		> 10MΩ	

Figure : DEPLOYMENT STRAIN GAUGE CHARACTERISTICS

^{\$} The total accuracy (supply + acquisition) shall not exceed 5%.

5.2.3.10.3.2.5.2 Battery Strain gauge

REQ.

The battery strain gauge interface shall comply the following characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE (BMP)	COMMENT
A	TYPE			
Req-1	Output	floating		
B	VOLTAGE			
Req-1	Supply voltage	10 V +/- 1%	10V, +1%, -0.9%	between strain gauge and BMP : 8m of #24
Req-2	Output voltage	< +30mV		
C	IMPEDANCE			
Req-1	gauge1 impedance (R)	350 Ω		Wheaston bridge
Req-2	gauge2 impedance (R)	1000 Ω		Wheaston bridge
Req-3	Input telemetry impedance		> 10M Ω	

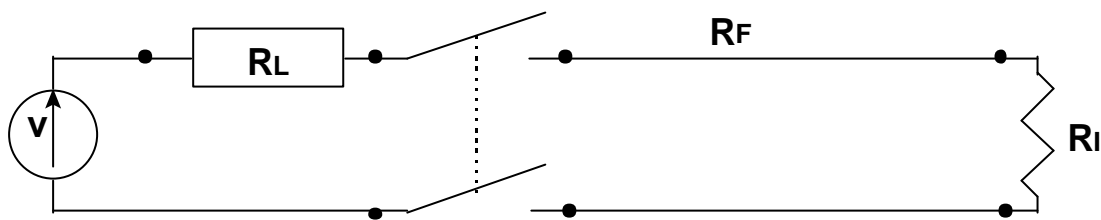
Figure : BATTERY STRAIN GAUGE CHARACTERISTICS

5.2.3.10.4 PYRO Interfaces

5.2.3.10.4.1 Initiator interface

REQ.

The electrical lines shall be composed by a current limitation resistance R_L , wire length R_F and the bridgewire initiator R_I .



R_L : current limitation resistance

R_F : wire resistance (Gauge 26 = 135.8 mOhm/m)

R_I : single bridgewire

Figure : PYRO ELECTRIC LINE

The R_L shall be specified by the SDIU Prime.

REQ.

The wire length R_F shall be between 0 m and 12m. The total length shall be twice this length so 24m.

REQ.

The single bridgewire shall be like specified by the NASA and ESA so : 1.05 ± 0.10 Ohm.

5.2.3.10.4.2 PYRO Characteristics

Code	PARAMETERS	USER SIDE	COMMENT
A	TYPE		
Req-1	Output	differential	
B	VOLTAGE		
Req-1	Nominal Voltage	20.5 V	
C	CURRENT		
Req-1	Nominal firing current	5 A	
Req-2	Minimum firing current	3.5 A	
Req-3	Max no-fire current	1A-5min 1W-5min	
Req-4	Check out current	10mA	
D	IMPEDANCE		
Req-1	bridgewire resistance	1.05 Ω +/- 0.15 Ω	
E	TIME		
Req-1	nominal impulse of ignition	< 5 ms for 5A < 10 ms for 3.5A	
F	GROUDING AND ISOLATION		
Req-1	Bonding	$\leq 2.5m\Omega$	resistance between initiator body and valve housing
Req-2	Insulation resistance	$\geq 100 M\Omega$ (50V)	R between shorted bridge wire and case

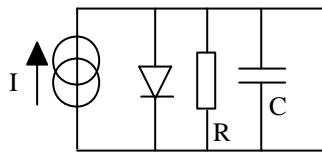
Table : PYRO CHARACTERISTICS

5.2.3.10.5 AOCS Interfaces

5.2.3.10.5.1 Coarse Sun Sensor interface

One CSS delivers 4 coarse analog detectors.

Schematic :



$R > 10 \text{ k}\Omega$

$C = 5000 \text{ pF}$ to 17000 pF on the range temperature

REQ.

The CSS interfaces (AOCSP) shall be compliant to these characteristics :

Code	PARAMETERS	SOURCE SIDE Analog detector	USER SIDE AOCSP	COMMENT
A	VOLTAGE			
Req-1	Maximum reverse voltage emission		5 V	
B	CURRENT			
Req-1	Nominal current	$0 < I < 1000 \text{ }\mu\text{A}$		
Req-2	Maximum current		10mA	
C	FAILURE MODE			
Req-1	Failure mode	<ul style="list-style-type: none"> Short circuit Open circuit Short circuit between wire + and structure Short circuit between wire - and structure 	Fail safe	

5.2.3.10.5.2 Reaction Wheel interface

Each reaction wheel have 3 commands and 4 telemetries :

Commands:

- Torque command and Torque direction (interfaced by AOCSP) : PWM format
- ON/OFF command (2 ON and 2 OFF commands) : Low level Command

Telemetries:

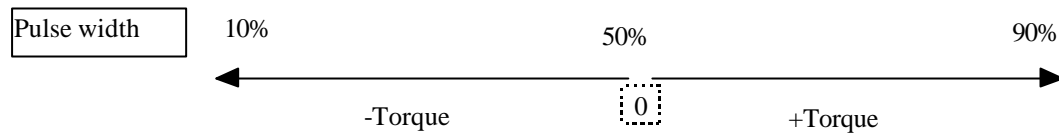
- Tachometer (interfaced by AOCSP) : Frequency format
- Speed direction (interfaced by AOCSP) : Bi-level format
- Motor current (interfaced by AOCSP) : PWM format
- ON/OFF status : Switch closure (cf chapter 6.2.5)
- Wheel NOGO (interfaced by AOCSP) : Bi-level format

Simplified schematic :



5.2.3.10.5.2.1 Torque command

Coding of torque direction and Torque Command :



REQ.

The torque command shall comply the following table :

Code	PARAMETERS	SOURCE SIDE AOCSP	USER SIDE WHEEL	COMMENT
A	CURRENT			
Req-1	Low level current (discrete "0")	0mA \pm 0.25mA		
Req-2	High level current (discrete "1")	9 mA < I _{HL} < 15.5 mA TBC		
B	VOLTAGE			
Req-1	Maximum Voltage drop		<1.9V/13mA	opto-coupler : 6N134
Req-2	Maximum differential Voltage	-1.5V < V _{diff} < 15V		
C	FREQUENCY			
Req-1	Nominal frequency	475Hz < F _{pwm} < 525Hz		
D	TIME			
Req-1	Rise/Fall time	< 50ns		150 Ω ; 600 pF
E	ISOLATION			
Req-1	from primary ground (0Vp)	connected	isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	
Req-2	chassis		isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	

Table : TORQUE TELECOMMAND CHARACTERISTICS

REQ.

The Torque command is interfaced by an optocoupleur referenced 6N 134.

5.2.3.10.5.2.2 Bi-level telemetry : Wheel direction and Wheel NOGO

REQ.

The torque direction shall comply these digital bi-level electrical characteristics :

Code	PARAMETERS	SOURCE SIDE WHEEL (1)	USER SIDE AOCSP	COMMENT
A	VOLTAGE			
Req-1	Low level differential output voltage	-5.5 V to -3.5 V		NOGO State // negative direction
Req-2	High level differential output voltage	3.5 V to 5.5 V		GO State // positive direction
Req-3	Max Fault voltage emission	-5V to +5V		
B	CURRENT			
Req-1	Current capacity	>10mA		
Req-2	Load current		<10mA	
C	IMPEDANCE			
Req-1	Series resistor		>700 Ω	
D	ISOLATION			
Req-1	from primary ground (0Vp)	connected	isolated ≥ 1 MΩ // ≤ 50 nF	
Req-2	chassis		isolated ≥ 1 MΩ // ≤ 50 nF	

Table: WHEEL NOGO/DIRECTION TELEMETRY CHARACTERISTICS

(1) The output driver is a 26C31.

Signal Logic :

- Hi="0" and Lo="1" (NOGO State // negative direction)
- Hi="1" and Lo="0" (GO State // positive direction)

The interface definition is set up so that current must flow through the optocoupler in order to establish a GO state (positive direction).

5.2.3.10.5.2.3 Bi-level telemetry : Tachometer

REQ.

The Tachometer interface shall be compliant with the following table :

Code	PARAMETERS	SOURCE SIDE WHEEL	USER SIDE AOCSP	COMMENT
A	VOLTAGE			
Req-1	Low level voltage	-12V \pm 2V		Current capacity : >15mA
Req-2	High level voltage	+12V \pm 2V		
Req-2	Fault voltage emission	\pm 15V		
B	IMPEDANCE			
Req-1	Load impedance		>400 Ω	
Req-2	Source impedance	200 Ω \pm 5% on each line		
C	TIME			
Req-1	Minimum Pulse duration	<10 μ s		
D	ISOLATION			
Req-1	from primary ground (OVp)	connected	isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	
Req-2	chassis		isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	

Table : WHEEL TACHOMETER TELEMETRY CHARACTERISTICS

REQ.

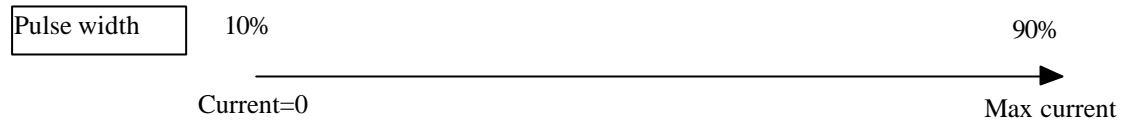
The tachometer interface (AOCSP) shall acquire between 192000 pulse per minute (3200 Hz) and 0 pulse per minute.

Note :

The wheel tachometer generate 24 pulse per revolution and the maximum speed is 8000 revolution per minute.

5.2.3.10.5.2.4 Motor current telemetry : PWM

Coding of Motor current telemetry :



REQ.

The motor current AOCSP interface shall be compliant with the following table :

Code	PARAMETERS	SOURCE SIDE WHEEL	USER SIDE AOCSP	COMMENT
A	VOLTAGE			
Req-1	Low level voltage	$0 \pm 1.5V$		
Req-2	High level voltage	$12V \pm 2V$		
B	VOLTAGE			
Req-1	Maximum Voltage drop		$2 * 1.9V/13mA$	opto-coupler : 6N134
C	IMPEDANCE			
Req-1	Load impedance		$> 400 \Omega$	
Req-2	Source impedance	$< 400 \Omega \pm 5\%$		
D	FREQUENCY			
Req-1	Nominal frequency	$10 \text{ kHz} \pm 2\text{kHz}$		
E	TIME			
Req-1	Rise/Fall Time	$< 50 \text{ ns}$		$150\Omega ; 600pF$
F	ISOLATION			
Req-1	from primary ground (0Vp)	connected	isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	
Req-2	chassis		isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	

Table : MOTOR CURRENT CHARACTERISTICS

5.2.3.11 NUMBER OF CONNECTOR PINS FOR RETURN LINES AND SHIELDING

REQ.

Each equipment shall provide as a minimum the following number of pins for the return of the different CMD and TLM signals .

N°	RETURN FOR	NUMBER OF PINS PER CONNECTOR
1	ON/OFF commands used for relays driving	2 (pin redundancy)
2	ON/OFF commands used for logic control	2 (pin redundancy)
3	MLC and DS signals (clocks, data, address)	1 per signal "inverted line of SBDL"
4	TLM data (analog, digital bi level, emergency)	2 (pin redundancy) if all TLM data are referenced to on common ground n x 2 (pin redundancy) If the TLM data are referenced to n different grounds
5	TLM data (TH)	1 per thermistor
6	TLM data (DR)	2 for nominal DR 2 for redundant DR

Table: CONNECTOR PINS FOR RETURN LINES AND SHIELDING

REQ.

Each connector for telemetry and command signals shall provide two pins which are connected with the box housing.

These two pins could be used for shields grounding if any better solution couldn't be defined (point c).

REQ.

Shields shall be connected to the connectors housing.

5.2.3.12 Data Bus interfaces

Two types of Data bus are available on SB4000 :

- OBDH - 485
- 1553

The nominal bus is OBDH - 485.

The use of 1553 bus is limited to AOCS equipments :

- Startracker
- Gyro
- IRES

5.2.3.12.1 OBDH - 485

REQ.

The OBDH-485 shall comply the « Data Bus Network Electrical and Protocol Specification ».

SBF 6AV2 AS SP 338

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 210 / 213

5.2.3.12.2 1553 BUS INTERFACE

REQ.

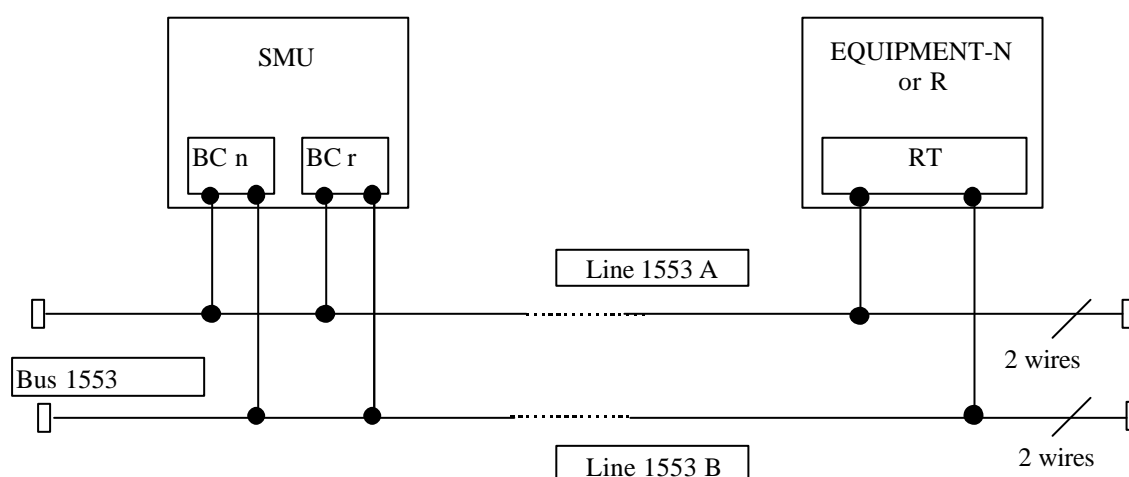
All detail 1553 bus requirements are to be found in MIL-STD-1553B Applicable Document.

The SB4000 1553 type is a long stub.

REQ.

Among redundancy options authorized by the MIL-STD-1553B Document, the following definitions have been selected and apply for each equipments , nominal and redundant:

- One 1553 line is one pair of twisted wires.
- One 1553 bus is composed of two 1553 lines, one called line A and the other called line B.
- Each Bus Coupler (BC n and BC r) located in the computer (SMU) shall control the two 1553 lines (A and B).
- Each Equipment connected to the 1553 bus receives therefore the two 1553 lines (A and B) through dedicated Remote Terminals (RT n and RT r)



6. GROUND AND FLIGHT ENVIRONMENTS

Why is this chapter here? (not practical in this document)

6.1.1 Corona

Reference **ABU-SAT-GDIEE-REQ-196**

Units ON during launch will be submitted to all pressure values between 1 bar and 0 bar. They have to be designed to operate in such an environment without any arcing (see AD03).

*

6.2 IN ORBIT ENVIRONMENT

6.2.1 Vacuum

Reference **ABU-SAT-GDIEE-REQ-197**

Exposure to a hard vacuum commensurate with orbital altitude will occur at synchronous orbit, this will be 10-10 Torr in free space, but may be as high as 0.1 Torr within the spacecraft interior. Equipments shall be designed to operate in these environments, in particular without any arcing (see AD03).

*

6.2.2 Deep Dielectric Charging

Electrostatic discharge can result from charging of dielectric and floating conductors within a spacecraft by energetic electrons ($E > 2\text{MeV}$).

Reference **ABU-SAT-GDIEE-REQ-198**

The Subcontractor shall identify in its equipment, all the metallic surfaces which are not always referenced to a fixed potential (track of PCB floating in particular equipment configuration, ...).

*

Reference **ABU-SAT-GDIEE-REQ-199**

For all equipment the DDC analyses have to be performed by the Subcontractor. The energetic electrons shall be shielded such that electric fields at boundaries or between components shall not exceed a breakdown level of 20MV/m when irradiated by a flux of 1nA/cm² (TBC). Where shielding is inappropriate, the analysis shall show that discharges, that may take place shall not affect the performance or degrade the integrity of the equipment, its components and materials.

*

ALPHABUS

REFERENCE: ABU-JPT-SP-563

DATE: 30/04/2004

ISSUE: 03

Page 212 / 213

END OF DOCUMENT