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Information Documentaire / Document Information

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SPACEBUS

Repeater and TCR unit Electrical Design and Interfaces Requirements

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DOCUMENT CHANGE RECORDS

Paragraphs Change Record (List of paragraphs modified, new or deleted)

Issue	Date	Change Record Description	Author
01	11/12/08	Initial issue based from AD01 pt4 issue 3 + DCN 200193751D, 200216227I, 200163883M, 200397196N, 200415261A	D Leportier
02	23/02/09	**req 638** is set applicable ALL_CF (§3.1) (mistake inside previous version) : req 638 = All requirements in this document shall be applicable in all satellite environmental conditions (mechanical, thermal, etc...) **req 009** is set to issue C in accordance with the approved DCN 200193751D (§ 3.5.1) req 009c = a) Nominal and redundant signals routing shall not be implemented on the same PCB or b) When nominal and redundant circuits are designed on the same PCB the two circuits shall be separated physically in order to avoid any risk of failure propagation and the corresponding PCB shall be tested : at bare PCB level at 2 times Vmax operating (with minimum voltage test at 250 V), a test duration of 20 h shall be proven at Vmax and maximum operating temperature at equipped PCB or equipment level **req 436** is modified (typo on capacitor value) **§ 6.2.7.7.3** : addition of a schematic to explain the requirements	D. Leportier

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LIST OF FIGURES

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ACRONYMS, SYMBOLS AND ABBREVIATIONS

A/D	Analog/numeric conversion
ABM	Apogee Boost Motor
AC	Alternating current
ADPM	Antenna Deployment and Pointing Mechanism
AN	TM Analog
AOCS	Attitude and Orbit Control Subsystem
AOCSP	Attitude and Orbit Control System PCB
AOCSP_NG	Attitude and Orbit Control System PCB_ New Generation
APM	Antenna Pointing Mode

AWG	American Wire Gauge
BAPTA	Bearing and Power Transfer Assembly
BBC	Bus Brick Connection
BCRB	Battery Connection Relay Box
CM	Common Mode
CRM	Central Reconfiguration Module
DB	TM Digital bi-level
DC	Direct current
DC/DC	Direct current/Direct current
DM	Differential Mode
DOCON	DOwn CONverter
DR	TM Digital Relay
DS16	TM Digital Serial 16 bit
DSPG	Distributed Single Point Grounding
EED	Electro-Explosive Devices
EGRN	Electrical Ground Reference Network
EGRP	Electrical Ground Reference Point
EGSE	Electrical Ground Support Equipment
EMC	Electro-Magnetic Compatibility
EPC	Electrical Power Conditioning
EPS	Electrical Power Subsystem
ESD	Electro-Static Discharges
HLC	High Level Command
HPC	High Priority Command
ICD	Interface Control Drawing
IDS	Interface Data Sheet
ITO	Iridium Tantale Oxyd
IRES	Infra-Red Earth Sensor
LLC	Low Level Command
LMU	Li-Ion Battery Management Unit
LNA	Low Noise Amplifier
LPC	Low Priority Command
LSB	Least Significant Bit
MLC	Memory Load Command
MLI	Multi Layer Insulator
MSB	Most Significant Bit
NRZ	Non Return to Zero
NRZ-L	Non Return to Zero Level
OBDH	On Board Data Handling

OBP	On Board Processor
OSR	Optical Surface Radiator
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PCU	Power Conditioning Unit
PFDIU	PlatForm Distribution and Interface Unit
PLDIU	Payload Distribution and Interface Unit
PROP	PROPulssion electronic (Chemical/Plasmic) PCB
PPS	Plasmic Propulsion Subsystem
PPU	Power Processing Unit
PYPGP	Pyrotechnic Pcb with GP relays
RA	Rotary Actuator
RUBI	Remote User Brick Interface
RF	Radio Frequency
RX	Receiver
S/C	Spacecraft
S/W	Software
S4DSAP	SB4000 Deployment of Solar Array PCB
SA	Solar Array
SADM	Solar Array Drive Mechanism
SADP	Solar Array and Deployment PCB
SBDL	Standard Balanced Digital Signal
SDIU	Satellite Distribution and Interface Unit
SDMP	Stepper and Deployment Motor PCB
SLI	Single Layer Insulator
SMU	Satellite Management Unit
SPF	Single Point Failure
SSM	Second Surface Mirror
STR	Star Tracker
TC	Telecommand
TCR	Telemetry, Command and Ranging
TH	Thermistor
TLM	Telemetry
TM	Telemetry
TOM	Thruster Orientation Mechanism
TTC	Tracking, Telemetry and Command
TWT	Travelling Wave Tube
TWTA	Travelling Wave Tube Amplifier
TX	Transmitter

UPCON	UP CONverter
UPS	Unified Propulsion Subsystem
w.r.t.	with respect to

Note: Applicability List

AIT	Assembly Integration & Test
ANTRACK	Antenna Tracking
AOCS	Attitude and Orbit Control Subsystem
DATAM	Data Management
FDIR	Failure Detection, Isolation and Recovery
HARNESS	-
MECHANISM	-
PAYLOAD	-
POWER	-
PROP	Propulsion Subsystem
STRUCTURE	-
TCR	Telemetry, Command and Ranging
THERM	Thermal Subsystem
ANTENNA	-
ALL CF	All Functional Chain

1. SCOPE

This document is issued from the system APPLICABLE DOCUMENT called **AD01part 4** by filtering the requirements applicable to repeater and TCR.

This document establishes the general electrical design and interface requirements for subsystem and units included in SPACEBUS 4000 systems satellites to be met to ensure their correct performance during assembly, integration, testing, storage, transportation, launch and orbital operations.

Additional design requirements related to Electromagnetic and ESD environmental conditions are provided in a separate dedicated applicable document.

NOTA : This document is issued automatically from a data base (DOORS). This is why there are some paragraphs without text or requirements. It means that these paragraphs are not applicable to repeater or TCR.

2. DOCUMENTS

2.1 Applicable documents

In case of conflict between any specification document and this applicable document, the specification document shall have precedence.

Any discrepancy shall be notified to the attention of Prime Contractor for clarification and resolution.

Denom.	Title	Doc Ref.
AD01 P1 (Part 1)	*Electrical design, interface and environmental Requirements*	SB.AS.SY.0001-1
AD02 P1 (Part 1)	*Mechanical design, interface and environmental Requirements*	SB.AS.SY.0002-1
AD03 Pa (Part a)	*Radiation Requirements*	REF-ASPI-CN-11-E
AD03 Pb (Part b)	*Space Radiation Environment Specification for Geostationnary Missions*	REF-ASPI-CN-12-E
AD13	*Safety Requirements*	REF-ASPI-CN-39-E
IRD 01	*Launcher to Satellite Interface Requirement*	SB3-ASPI-SP-0158
IRD 02	*Satellite/Ground interface Specification Part 1 - Physical Layer (C-band)*	SB4-ASPI-SP-0381
IRD 03	*Satellite/Ground interface Specification Part 2 - SB4100C1 TM/TC format & protocol*	SB4-ASPI-SP-0078
IRD 04	*Satellite/Ground interface Specification Part 3 - Command and Observability*	SB4-ASPI-SP-0320
	Data Bus Network Electrical and Protocol Specification	SBF 6AV2 AS SP 338
	MIL STD 1553B Protocol and Interface Requirements for DBN	SBF 6AV2 AS SP 504
	MIL STD 1553B "Aircraft Internal Time Division Command/Response Multiplex Data Bus", with Notice 4	

Table 1:Applicable Technical Documents and Interface Documents at Satellite system level

Denom.	Title	Doc Ref.
AD 04	*Generic Product Assurance Requirements*	REF-ASPI-AQ-21-E
AD 05	*Materials, Parts & Process Requirements*	REF-ASPI-CN-10-E
AD 06	*EEE Parts Requirements*	REF-ASPI-CN-7-E

Denom.	Title	Doc Ref.
AD 07- P1	*Reliability Requirements*	REF-ASPI-CN-9-E
AD 07- P2	*Data Base for Reliability*	REF-ASPI-CN-13-E
AD 12	*Software Eng. And PA Requirements*	REF-ASPI-CN-38-E

Table 2:Applicable Programmatics, Quality and Product Assurance Requirements Documents at Satellite system level

Denom.	Title	Doc Ref.
AD 09	*Configuration Requirements*	CAIS-ASPI-SP-0218
	Documentation Requirements	CAIS-ASPI-SP-0219
AD 10-P1	*Guide de gestion des exigences*	REF-ASPI-CN-74-E
AD 10-P2	*Spécification des règles de gestion des exigences*	REF-ASPI-CN-86-F
AD 11	*Instruction for IDS and ICD*	REF-ASPI-CN-88-E

Table 3:Applicable Programmatics and Data Configuration Requirements Documents at Satellite system level

2.2 Reference documents

The following documents listed hereinafter are for reference and information only. They have been used as basis for some requirements defined in the present specification.

Denom.	Title	Doc. Ref.
REF1	*IEEE Standard for Space Applications Module, Extended Height Format E Form Factor*	IEEE Std 1101.7-1995
REF2	*EIA-485 Standard for Electrical Characteristics of Generators and Receivers for Use in balanced digital multipoint systems (RS485 Standard), April 1983*	
REF3	*Derating Requirements Applicable to Electronic, Electrical and Electro-Mechanical Components for ESA Space Systems, Issue 2, April 1992*	PSS-01-301
REF4	*Space system engineering Standard*	ECSS-E-20B

3. GENERAL SPECIFICATIONS

3.1 Engineering specifications

Reference **SB4-SAT-AD1-P4-REQ-001 b**

The metric standard (SI - International system) shall be used for design, manufacturing and testing of systems or subassemblies.

*

Reference **SB4-SAT-AD1-P4-REQ-638**

All requirements in this document shall be applicable in all satellite environmental conditions (mechanical, thermal, etc...)

*

3.2 Electrical symbols

Possible electrical symbols used in electrical diagrams (grounding, etc…) are shown in Figure 1:

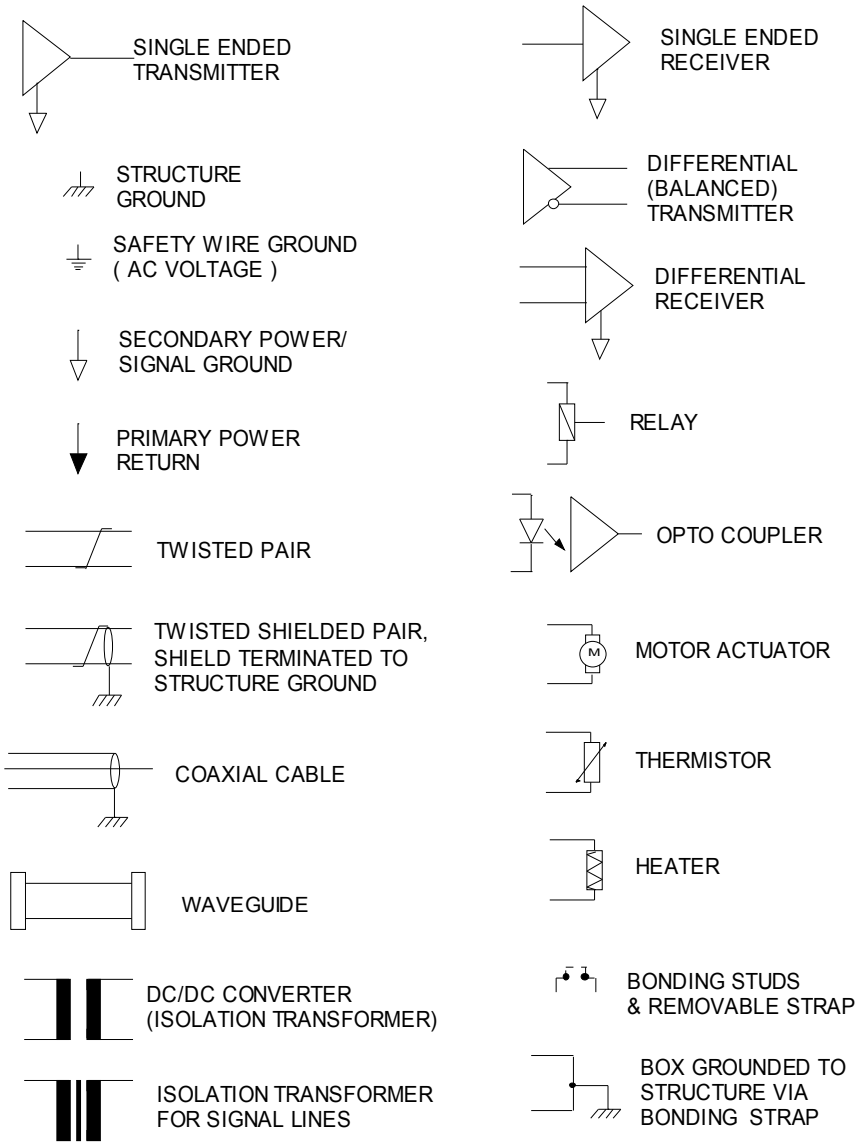


Figure 1: Symbols for electrical diagrams

3.3 Lifetime

Reference **SB4-SAT-AD1-P4-REQ-005 b**

Units and subsystems shall be designed for a 15 years lifetime after having been stored for 5 years in a protected environment and having been used for tests and integrations for 2 years.

*

3.4 Delivery

Reference **SB4-SAT-AD1-P4-REQ-610**

All unit/subsystem shall be delivered in POWER OFF status.

*

3.5 Redundancy

3.5.1 Redundancy rules

Reference **SB4-SAT-AD1-P4-REQ-544**

When redundancy is implemented in the design, any single failure leading to total or partial loss of the unit operational capability or mission shall be forbidden.

*

Reference **SB4-SAT-AD1-P4-REQ-009 c**

a)Nominal and redundant signals routing shall not be implemented on the same PCB

or

b) When nominal and redundant circuits are designed on the same PCB the two circuits shall be separated physically in order to avoid any risk of failure propagation and the corresponding PCB shall be tested :

at bare PCB level at 2 times Vmax operating (with minimum voltage test at 250 V),

a test duration of 20 h shall be proven at Vmax and maximum operating temperature at equipped PCB or equipment level

*

Reference **SB4-SAT-AD1-P4-REQ-400**

Nominal and redundant ways shall use separated connectors.

*

3.5.2 Units failure

3.5.3 Single point failure

Reference **SB4-SAT-AD1-P4-REQ-014 b**

No conductive particle, smaller than 3 mm, shall cause total or partial loss of the unit or mission.

*

Reference **SB4-SAT-AD1-P4-REQ-401 a**

All units, with nominal power consumption higher than 20W, shall always be able to switch-off in any case of failure (except in case of OFF command interface failure).

*

3.6 Test points

3.6.1 Test points requirements

Reference **SB4-SAT-AD1-P4-REQ-024 b**

The test points shall be clearly identified in the unit ICD/IDS.

*

Reference **SB4-SAT-AD1-P4-REQ-026 b**

Test points on multi-pin connectors shall be designed to withstand, without causing damage to the unit, the highest voltage on that connector unit as well as short circuits

*

Reference **SB4-SAT-AD1-P4-REQ-028 b**

Unit test connectors shall be provided with electrically conductive covers to ensure protection against electrical and mechanical damage.

*

Reference **SB4-SAT-AD1-P4-REQ-029 b**

Input test points shall be fixed in potential to avoid perturbations during operational life.

*

3.7 Identification of product

3.7.1 Identification design

Reference **SB4-SAT-AD1-P4-REQ-035 c**

deleted

*

4. ELECTRICAL ARCHITECTURE REQUIREMENTS

4.1 Grounding and isolation requirements

Grounding is the establishment of an electrically conductive path between two points to connect electrical elements of a system to the ground reference point.

4.1.1 Grounding objective

Electrical grounding and bonding is requested for all mechanical structure elements, equipment housing, thermal blanket devices and cables :

- to prevent hazard from high potentials
- to prevent build up and accumulation of electrostatic charges
- to avoid differential charge build up that could result in an electrostatic discharge
- to reduce electromagnetic interferences due to electric field or other forms of mutual coupling
- to protect from high voltage arcing
- to provide an Electrical Ground Reference Network (EGRN) used as an equipotential surface reference plane (particularly important for RF unit) to be able to withstand EMC/ESD requirements.

4.1.2 Grounding concept

The Electrical Ground Network includes the following items:

- aluminium panels (honeycomb and skins)
- launcher interface ring (this ring is the spacecraft reference point)
- internal deck interface ring
- all grounding strap (metallization) and their rivets
- all baseplates supporting equipments.

The spacecraft structure shall constitute a low impedance reference named Electrical Ground Reference Network (EGRN).

Reference **SB4-SAT-AD1-P4-REQ-411**

All metallic sub-chassis, chassis and enclosures of each unit, including all connectors' shells and other fittings, shall be considered electrically as extensions of the EGRN.

*

The grounding and bonding concept is a "returns by wires" concept with a Distributed Single Point Grounding (DSPG) configuration.

Reference **SB4-SAT-AD1-P4-REQ-412**

Each independent network (primary power distribution and secondary power distribution, ...) based on a star-point system shall be referenced to the EGRN via an one point low impedance connection.

*

Possible grounded solutions for unit secondary reference point are shown in Figure 2.

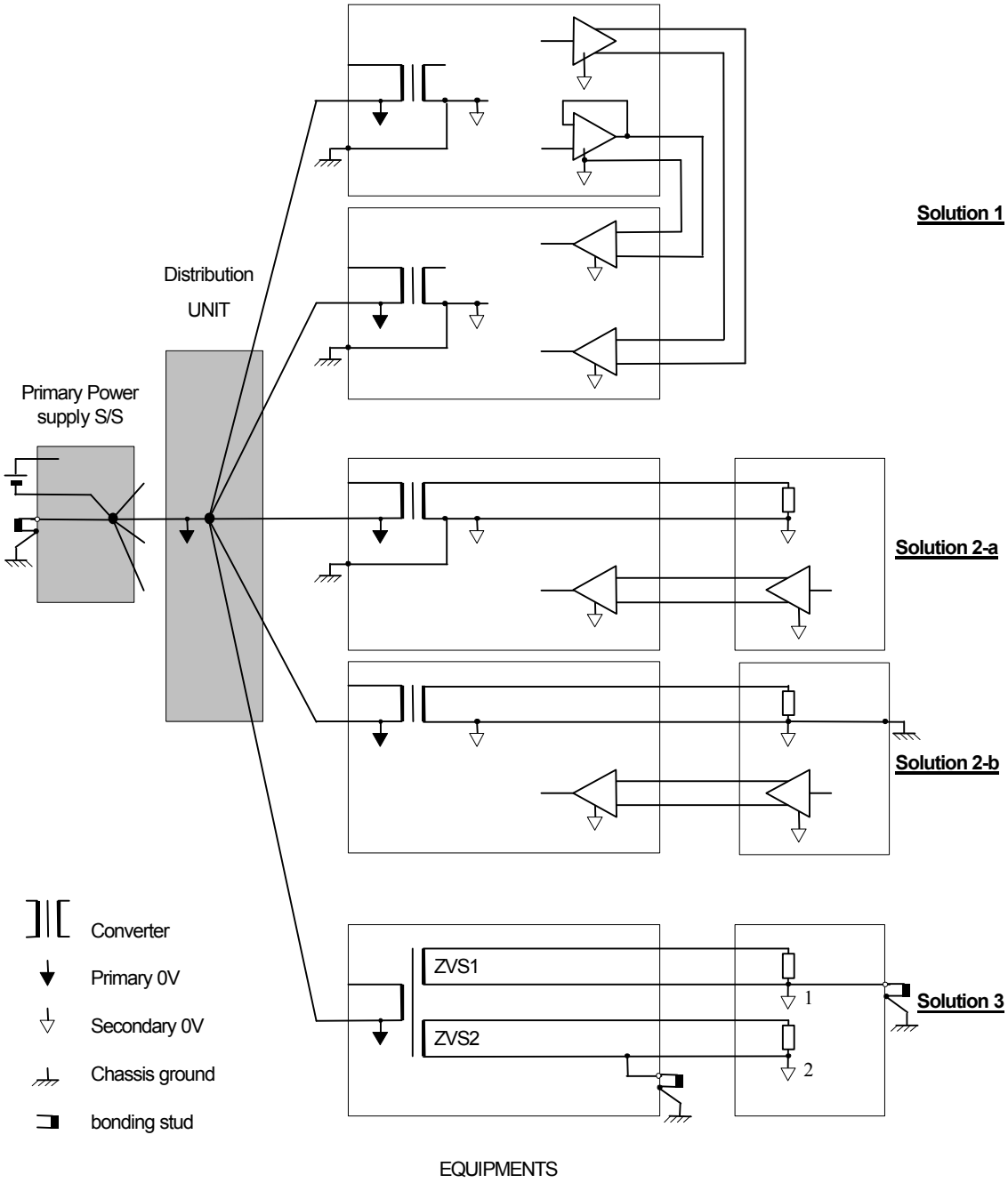


Figure 2: Basic philosophy for Distributed Single Grounding Concept

4.1.2.1 Grounding Solution 1

Reference **SB4-SAT-AD1-P4-REQ-415**

The unit secondary reference point is insulated from the secondary reference point of other units (implying the use of insulated or differential interfaces between the units). In this case, the equipment shall be grounded internally to its own housing in order to ensure a low impedance ground path.

*

4.1.2.2 Grounding Solution 2

Reference **SB4-SAT-AD1-P4-REQ-417**

The unit secondary reference point is common to several units.
In this case :

- the unit assembly shall be grounded at only one point,

*

4.1.2.3 Grounding Solution 3

Reference **SB4-SAT-AD1-P4-REQ-418**

Each unit shall provide dedicated bounding studs so that each unit secondary reference point can be grounded externally to the equipment housing. One of the grounding stud shall be insulated from the equipment structure and connected to the unit secondary reference point; the other one shall be connected directly to the chassis ground (See Figure 3).
It shall be possible to ground the unit secondary reference point by placing a bar (removable strap) between the two bounding studs.
This requirement is not mandatory for RF equipment which have an internal link.
It must be noted that the above-mentioned bounding studs is different from the bounding strap used to connect the unit case to the mechanical structure

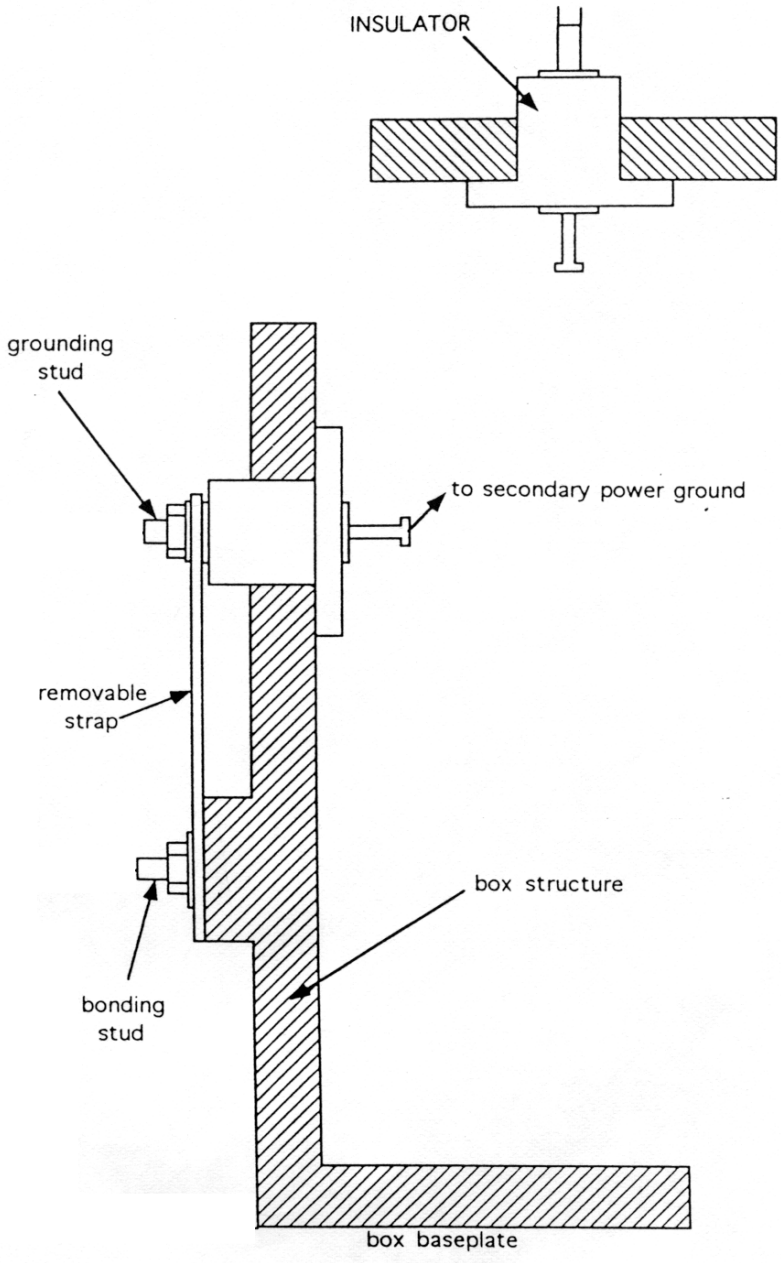


Figure 3 : Grounding of a unit secondary reference point via a bonding stud

*

Reference **SB4-SAT-AD1-P4-REQ-419**

The bar shall be supplied by the equipment manufacturer.

*

4.1.2.4 Specific Grounding Solution for matrix provided by SMU, CVICP and MAP.

4.1.3 Grounding and isolation diagram

Reference **SB4-SAT-AD1-P4-REQ-420**

An overall zero volt and grounding diagram shall be provided in the IDS for establishing functional and electromagnetic compatibility.

*

Reference **SB4-SAT-AD1-P4-REQ-421**

This diagram shall indicate any AC or DC loop, the type of isolation/insulation used, and any impedance coupling between zero volt and structure and shall be established for all Equipment and Subsystems containing electrical/electronic circuits.

*

4.1.4 Power lines grounding

Reference **SB4-SAT-AD1-P4-REQ-425**

The grounding connection impedance between the unit electrical 0V ground and its housing shall be lower than 2.5 mΩ measured under 1 Adc current and shall be lower than 100 nH.

*

4.1.4.1 Grounding of primary power bus 0V

Reference **SB4-SAT-AD1-P4-REQ-424 a**

deleted

*

4.1.4.2 Grounding of secondary power bus 0V

Reference **SB4-SAT-AD1-P4-REQ-429 a**

In case that several units are supplied from the same DC / DC converter secondary power output, the secondary 0V shall be interconnected in a starpoint system to form the secondary reference ground, except for RF units.

*

Reference **SB4-SAT-AD1-P4-REQ-431**

The high voltages necessary for the TWT's shall be considered as secondary power and shall be referenced at the EPC (via EPC structural part) and at the TWT side (via the TWT structural part).

*

Reference **SB4-SAT-AD1-P4-REQ-433 a**

The grounding path shall be designed and sized to withstand a current equal to 1.5 times the worst case fault current as limited by the unit primary power bus protection device. The following current shall be considered :

- either a primary current due a short-circuit between the primary power supply positive lines and the unit secondary reference point/mechanical ground.
- or a secondary current due to a short-circuit between a secondary power line and the secondary reference point/mechanical ground.

*

Reference **SB4-SAT-AD1-P4-REQ-435**

All transformer screen shall be grounded to chassis.

*

4.1.5 Primary and secondary power lines insulation

Reference **SB4-SAT-AD1-P4-REQ-170 a**

The primary power lines shall be transformer insulated from all secondary power.

*

Warning: During measurement rating on components must be withstood. Derating may be exceeded.

Reference **SB4-SAT-AD1-P4-REQ-436**

Insulation	isolation resistor with stray capacitance in parallel	measurement DC voltage	test conditions
Between unit primary power + (positive) input lines and structure	(>1 MΩ) // (< 600 nF)	100Vdc	unit unpowered

*

Reference **SB4-SAT-AD1-P4-REQ-631**

Insulation	isolation resistor with stray capacitance in parallel	measurement DC voltage	test conditions
Between unit primary power - (negative) input lines and structure	(>1 MΩ) // (< 600nF)	50Vdc	unit unpowered

*

Reference **SB4-SAT-AD1-P4-REQ-438**

Insulation	isolation resistor with stray capacitance in parallel	measurement DC voltage	test conditions
~~Req 3 :~~ ~~b~~etween primary power leads and secondary power leads	(>1 MΩ) // (< 50 nF)	100Vdc both polarities	* unit unpowered

*

4.1.6 High voltage units

Reference **SB4-SAT-AD1-P4-REQ-624 a**

Isolation between the highest voltage inside the equipment and thermistor, relay coil, relay contact or heater leads shall be guaranteed with 6 dB margin.

*

4.2 Bonding requirements

4.2.1 General purpose

Bonding is the establishment of a low impedance path between two metal surfaces or different structural parts.

Electrical bonds are employed for the following purposes:

- To minimize the impedance of the ground plane formed by the metallic portion of the structure.
- To assure the existence of low impedance return paths for possible failure mode-related fault current.
- To avoid the development of RF potentials between adjacent conductive surfaces raise the effectiveness of enclosure shielding.

– To provide high current capability to carry potential fault current.

Reference **SB4-SAT-AD1-P4-REQ-488 a**

To avoid discharge surfaces, each electrically conductive area larger than 5 cm2 , shall be grounded to a referenced voltage.

*

4.2.2 Bonding characteristics at unit level

Reference **SB4-SAT-AD1-P4-REQ-454**

Bonding connection	Electrical continuity
between two adjacent parts of a metal case including the resistance between any point of the case and any point of the cover or bonding point (possibly after vibration tests)	≤ 5 mΩ under 1Adc current

*

Reference **SB4-SAT-AD1-P4-REQ-459**

Bonding connection	Electrical continuity
between connector shell and unit structure	≤ 2.5 mΩ under 1Adc current

*

Reference **SB4-SAT-AD1-P4-REQ-460**

Bonding connection	Electrical continuity
between connector back-shell and connector body	≤ 5 mΩ under 1Adc current

*

4.2.3 Bonding strap characteristics

4.2.4 Harness Bonding characteristics

4.2.5 Structural Part Assembly Bonding

4.2.6 Thermal Part Assembly Bonding

4.2.6.1 General Requirements

4.2.6.2 MLI / SLI Requirements

4.2.6.3 SSM Requirements

Reference **SB4-SAT-AD1-P4-REQ-497**

The use of SSM shall be avoided.

*

4.2.6.4 OSR Requirements

4.3 Paints and coatings characteristics

Reference **SB4-SAT-AD1-P4-REQ-490 a**

Coatings (including paintings) on non conductive surface (not applicable on coating which is inside the unit)

Coatings applied on a dielectric or non-conductive surface shall be grounded to the ground reference network on the edges.
The coating surface resistivity applied on non conductive materials shall be less than 1 E9 Ω / square.

*

Reference **SB4-SAT-AD1-P4-REQ-491 a**

Coatings (including paints) on conductive surface (not applicable on coating which is inside the unit)

The coating resistivity applied on a conductive surface shall be less than 1 E9 Ω.m assuming a depth $e \leq 100$ µm.

*

4.4 Electrical connector requirements

Requirements in this chapter are applicable to:
- Satellite harness
- Harness of the units (i.e.: Reaction Wheel, ADPM...), except to Pcb's wires.

4.4.1 Connector types

Reference **SB4-SAT-AD1-P4-REQ-498**

All connectors shall be selected according to AD11.

*

Reference **SB4-SAT-AD1-P4-REQ-499**

MDM and very high density (ex.:AMP104) connectors shall not be used.

*

Reference **SB4-SAT-AD1-P4-REQ-508 a**

All connectors, not dedicated to power generation and distribution outputs, shall be pin type.

*

4.4.2 Connector characteristics

4.4.2.1 Connectors housing

Reference **SB4-SAT-AD1-P4-REQ-506 a**

deleted

*

4.4.2.2 Specific derating requirements

Reference **SB4-SAT-AD1-P4-REQ-614**

Mating and demating of each connector shall be less than 25 before unit delivery at Satellite System Integration.

*

4.4.2.3 Connector mounting requirements

Reference **SB4-SAT-AD1-P4-REQ-511**

The connectors shall be placed in such a way that connection and disconnection on one connector shall be made without any specific tool and without disconnecting the other connectors.

*

Reference **SB4-SAT-AD1-P4-REQ-512**

At least, 6mm shall be kept between two adjacent connectors.

*

Reference **SB4-SAT-AD1-P4-REQ-615**

The connectors shall be placed according to manufacturer connector requirements.

*

4.4.2.4 Connector identification

Reference **SB4-SAT-AD1-P4-REQ-518**

Each unit or bracket shall be permanently marked by visible connector identification closely adjacent to the appropriate connector in order to allow a correct mating of corresponding harness connector.

*

4.4.3 Connector savers

Reference **SB4-SAT-AD1-P4-REQ-513**

Saver connectors shall be used during integration to lower number of mating and demating cycles.

*

4.4.4 Pins characteristics

Reference **SB4-SAT-AD1-P4-REQ-515**

Lines which have a common return shall be placed on adjacent contacts to facilitate cable twisting and/or shielding (except for matrix concept).

*

Reference **SB4-SAT-AD1-P4-REQ-517**

The connected contacts on each connector shall never be inferior to two third of its maximum capacity.

*

4.4.5 Specific requirements for pyro connectors

4.5 Harness requirements

Requirements in this chapter are applicable to:
- Satellite harness
- Harness of the units (i.e.: Reaction Wheel, ADPM...), except to Pcb's wires.

4.5.1 Harness definition responsability

4.5.2 Bundles characteristics

4.5.2.1 Bundles classification

4.5.2.2 Bundles rules

4.5.3 Connectors

Reference **SB4-SAT-AD1-P4-REQ-639**

All external connectors shall include connector back-shell.
The shells shall be:

- electrically conductive
- bonded to the overall harness shield or to all the cable shields
- connected to the connector case to provide a 360° termination around the internal cable bundle

*

4.5.4 Wire specifications

4.5.4.1 Wire selection

4.5.4.2 Twisted links

4.5.4.3 Shielded links

4.5.4.4 High voltage specific derating requirements

4.5.4.5 Crimping of wires

4.5.5 Matrix harness concept

4.5.6 Specific requirements for pyro circuits

5. POWER SUBSYSTEM INTERFACES REQUIREMENTS

5.1 Power Bus Definition

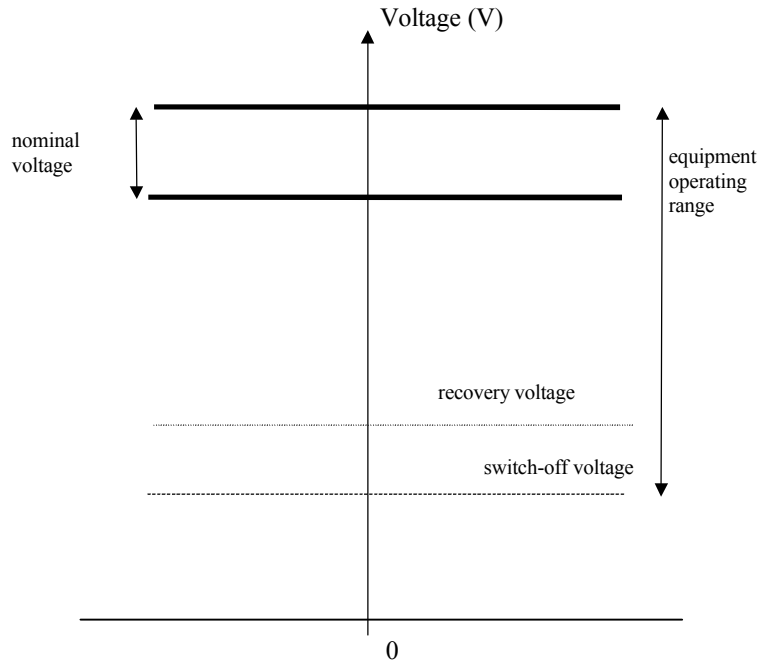


Figure 6: Equipment operating range.

5.2 Power bus nominal voltage

The power conditioning subsystem provides one regulated 100 V power bus, which is distributed to the spacecraft users.

Reference **SB4-SAT-AD1-P4-REQ-131 a**

At the loaded input connector of user, the nominal bus voltage is defined as follows :

Maximal DC bus voltage : 102V
Minimal DC bus voltage : 98V

*

5.3 Power bus operational voltage

Reference **SB4-SAT-AD1-P4-REQ-133 d**

deleted

*

5.4 Equipment operating requirements

Reference **SB4-SAT-AD1-P4-REQ-134 b**

Units shall not be affected **in their nominal performances** if the power bus voltage is under their automatic switch-off voltage level during less than 10 μs.

*

Reference **SB4-SAT-AD1-P4-REQ-135 d**

Units shall be automatically switched off as soon as the power bus voltage is under their automatic switch-off voltage level in a time range of [10 μs ,1s].

Function	AUTOMATIC Switch-Off Voltage (V)	AUTOMATICRECOVERY	RECOVERYVOLTAGE(V)
High Power Payload Units (> 20 W)	94 $\pm$ 1	NO	$\geq$ 95
PYRO Pcb / FSMP	94 $\pm$ 1	NO	$\geq$ 95
SADP/S4DSAP/PROP/CVICP	70	NO	72 $\pm$ 1
Other Platform Sub-Systems / Pcb	70	NO	72 $\pm$ 1
Low Power Payload Units (< 20W)	< 95 **or** No automatic Switch-Off voltage	NO/YES	$\geq$ 95
AOCS-UPS Units	70	NO	72 $\pm$ 1
SMU-TTC RF (RX+TX) - Ciphering Units	<70	YES	72 $\pm$ 1

Table 6: Regulated 100V, Equipment operating requirements

*

5.5 Distribution requirements

The main power bus distribution is based on a single point failure free concept at the distribution point (no failure of a part or insulation can cause the loss of the power bus).

Reference **SB4-SAT-AD1-P4-REQ-145 b**

The unit input ON/OFF relay contact shall be sized to withstand twice the current peak value corresponding to the long peak power demand.

*

5.5.1 Double insulation requirements

5.5.2 Fuses

Reference **SB4-SAT-AD1-P4-REQ-146 c**

Fuses shall not be implemented inside equipments excepted distribution units (PLDIU, PFDIU) and batteries.

*

5.5.3 High power units

5.5.4 Primary Power Line fluctuation

Reference **SB4-SAT-AD1-P4-REQ-150 b**

All users of these power lines shall safely survive any standing or fluctuation voltage in the full range 0V to 102 V and recover nominal operating performances with the bus voltage rise time to reach its nominal range of dV/dt < 1V/μsec.

*

Reference **SB4-SAT-AD1-P4-REQ-152 b**

During power bus voltage fluctuations tests, the unit under test shall be initially in a configuration which maximize the interference (ex : unit in ON state).
Units are not required to meet performance parameters under these conditions but must safely survive without any over-stressing or damage and must recover all their nominal operating performance.

*

Reference **SB4-SAT-AD1-P4-REQ-155 b**

Low speed power fluctuation (integration and hardware verification).

The test shall be performed when the bus voltage starts from 0V to nominal voltage (100V) with 20V/ms < dV/dt < 10 V/s (see figure below). During such event, the bus voltage shall be within hatched areas.

The unit input current shall be recorded and included in test report.

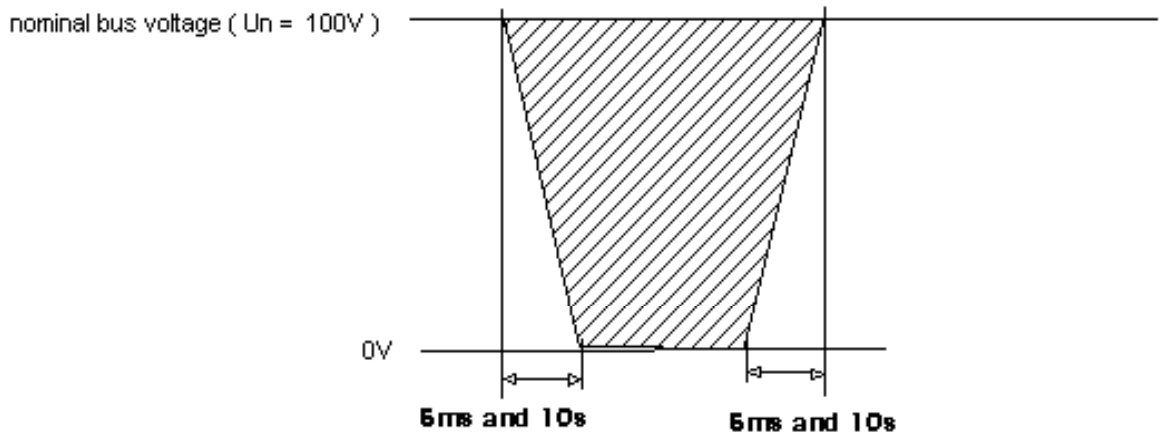


Figure 7: Low speed power bus fluctuation (low dV/dt)

*

5.6 Mean power demand

The mean power demand is defined as the maximum average power drawn from its dedicated power lines in the worst conditions.
Specifically, the maximum average is defined as the average during a period of 5 minutes shifted to any point in time where this average will yield a maximum and does not include peak power defined hereafter.

Reference **SB4-SAT-AD1-P4-REQ-161 b**

The mean power demand shall be measured in voltage nominal conditions (see chapter "Power bus nominal voltage") during a period of 5 minutes

*

5.7 Peak power demand

The long peak power demand is defined as the maximum operational average power drawn from the unit dedicated power lines in the worst .
Specifically, the maximum operational average is defined as the average during a period of 50 msec shifted to any point in time where this average will yield a maximum. Operational mode change requires specification of the average power demands per mode and duration.

Reference **SB4-SAT-AD1-P4-REQ-162 b**

The long peak power demand shall be measured in voltage nominal conditions (see chapter "Power bus nominal voltage") at worst functional case of equipment (wheel spin up, telecomand generation, etc)

*

5.8 Load current limitation

Reference **SB4-SAT-AD1-P4-REQ-164 c**

For High Power Units (> 20W), the maximum current drawn by the unit from the supply lines in case of failure, shall be limited to 1.5 times the current peak value corresponding to the long peak power demand (except during the unit ON/OFF sequence)

*

Reference **SB4-SAT-AD1-P4-REQ-642**

For Low Power Units (< 20W), the maximum current drawn by the unit from the supply lines in case of failure, shall be limited to 2 times the current peak value corresponding to the long peak power demand (except during the unit ON/OFF sequence)

*

6. SIGNAL LINE INTERFACE REQUIREMENTS

Reference **SB4-SAT-AD1-P4-REQ-442**

Signal interface shall use a return by wire concept.

*

6.1 Conventions

- Time duration :The time duration is defined at 50% of the measured full amplitude.
- Signal rise and fall times : The rise and fall times of a signal are defined as the time between 10% and 90% of the measured voltage swing.
- Measurements : Measurements are made at the unit (or harness) connector level.

6.2 Command interface

6.2.1 Commands source

6.2.2 Commands types

6.2.2.1 High priority command definition

6.2.2.2 Low priority command definition for one user

6.2.2.3 Low priority command definition for two users in cold redundancy[6.1.2.3]

6.2.3 LLC - MLC TRADE OFF

6.2.4 Command verification and protection

6.2.5 Critical commands

6.2.6 LOW LEVEL AND HIGH LEVEL COMMANDS (LLC & HLC)

6.2.7 Low Level and High Level Commands (LLC & HLC)

6.2.7.1 Matrix command definition

HLC and LLC commands are generated through matrix row and column drivers. One row pulled up to a positive voltage and one column pulled down to the secondary 0v in order to command only the device at the node of the activated row and column.
The command signal is a differential voltage pulse distributed to the user for :

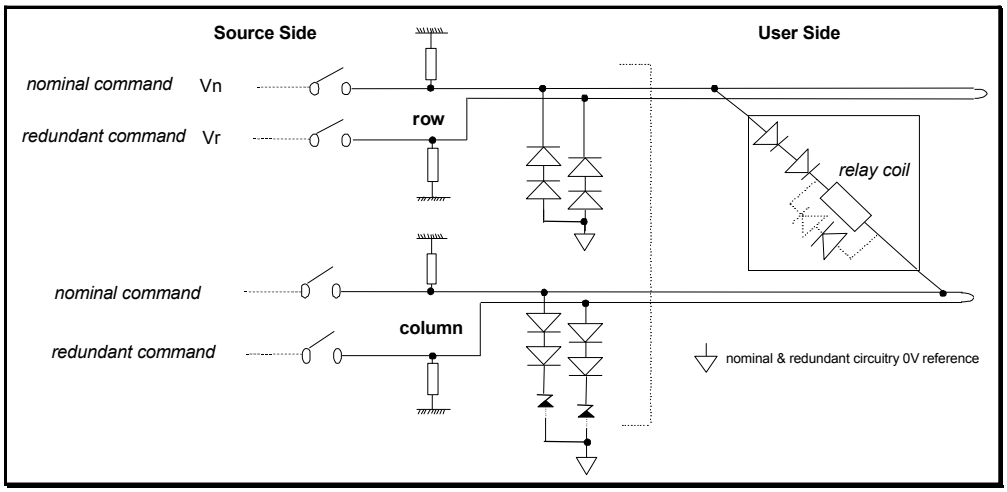
- relay driving or general logic control application with low level commands
- payload waveguide relay driving with high level commands

6.2.7.1.1 Matrix command harness concept

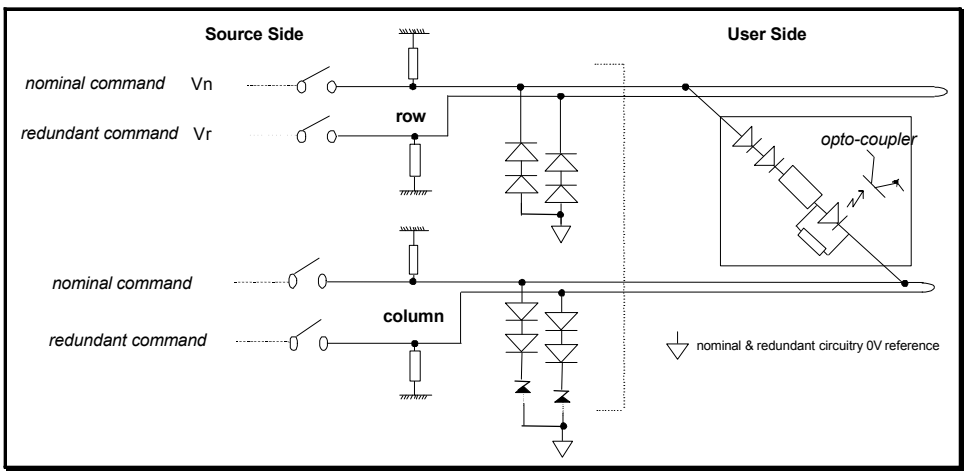
6.2.7.2 Matrix command schematics

6.2.7.3 Matrix command schematics

Relay interface



Opto coupler interface



6.2.7.4 Source side requirements

6.2.7.5 User side requirements

Reference **SB4-SAT-AD1-P4-REQ-195 a**

all telecommand users shall provide two diodes in series with the commanded device at any matrix node.

*

Reference **SB4-SAT-AD1-P4-REQ-196 d**

For user interface with relay coil (LLC), two serial free wheel diodes shall be implemented in parallel with the relay coil at user side.

When the time constant of relay (L/R) is inferior to 1ms for LLC, the diodes could be non implemented in the receiver interface.

*

Reference **SB4-SAT-AD1-P4-REQ-637 a**

For user interface with RF switch (HLC):
When the time constant of relay (L/R) is higher than 5 ms, two redounded (in parallel) free wheel diodes shall be implemented in parallel with the relay coil.
When the time constant of relay (L/R) is lower than 5 ms, two redounded (in parallel) free-wheel diode may be non implemented.
But, If at user side, free wheeling current and duration exceed Free wheeling currents and times specified in requirement SB4-SAT-AD1-P4-REQ-239 and shown in Figure 1, free-wheel diode shall be implemented

*

Reference **SB4-SAT-AD1-P4-REQ-201 b**

The user shall not impose any potential or grounding reference on any row or column.

*

6.2.7.6 Single commands definition

6.2.7.6.1 Source side requirements

6.2.7.6.2 Receiver side requirements

6.2.7.6.3 Failures management

Reference **SB4-SAT-AD1-P4-REQ-202 b**

The user interface design shall permit the unit power on/off without damage when the electrical interfaces are not fully connected.

*

Reference **SB4-SAT-AD1-P4-REQ-235 b**

Unpowered equipments shall not be damaged and degraded in their performances when command signals are applied.

*

Reference **SB4-SAT-AD1-P4-REQ-236 c**

deleted

6.2.7.6.4 HLC single command schematics

6.2.7.6.5 Single command harness concept

6.2.7.7 Command signal characteristics

6.2.7.7.1 Command signal waveform

Signal duration (Td): time between crossing points of rise and fall time to 50% of the full amplitude

Signal rise/fall time (Tr ; Tf): maximum between 10% and 90% of the nominal voltage swing

Delay between 2 signals: time between the voltage crossing point at 50% of the full amplitude level

Closed time Tc: Command duration with switch closed

Free wheeling time: Duration between end of pulse and switch opening

6.2.7.7.1.1 Classic Command

6.2.7.7.1.2 Matrix Command

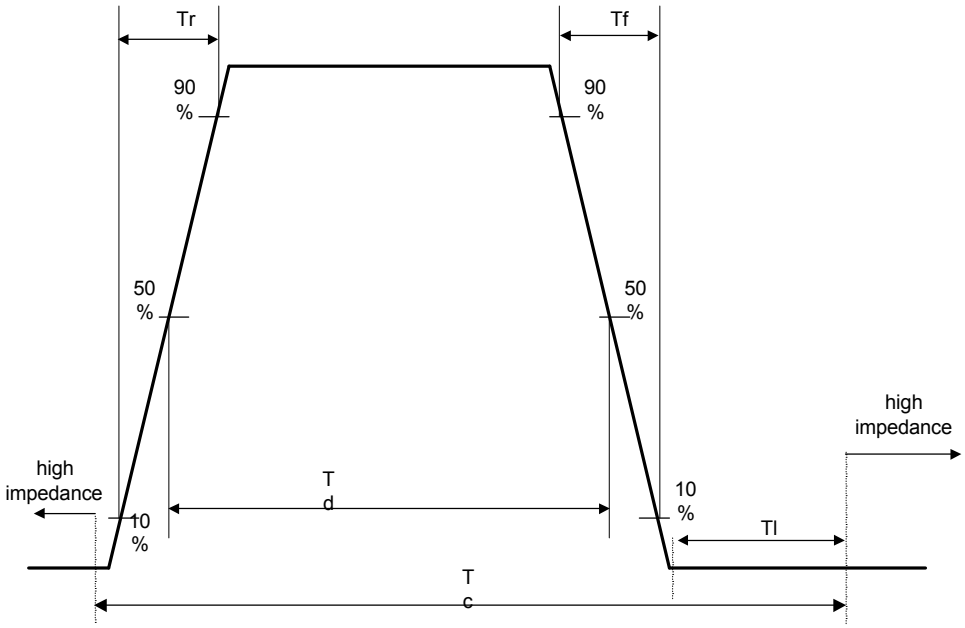


Figure 8: Matrix command signal waveform

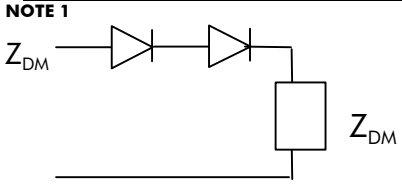
6.2.7.7.2 LLC electrical parameters

Reference **SB4-SAT-AD1-P4-REQ-238 d**

The LLC commands shall comply with these LLC electrical characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
A	***TYPE***			
Req-1	Output type	Differential		for matrix drivers organisation
Req-2	Input type		Differential	
B	**VOLTAGE**			
Req-1	DM low « 0 » voltage	-29V/ +4V	-29V / +4V	User shall also comply with Req-H1
Req-2	DM high « 1 » voltage	26 V (+3V / -2V)	26 V (+3V / -5V)	
Req-3	Threshold		7 V ≤ V_T ≤19V	
Req-4	CM Permanent Fault Voltage Emission	Not allowed	-5V < fault <40V	DM = 0
Req-5	DM Permanent Fault Voltage	Not allowed	Not allowed	
Req-6	DM Transient Fault Voltage Emission	-63 V/1 s +33V/80ms	± 2V / 25 ms	
Req-7	DM Transient Fault Voltage Tolerance	-63 V/1 s +33V/80ms	-63 V/1 s +33V/80ms	
C	**CURRENT**			
Req-1	Driving capability	> 180 mA		
Req-2	Load current		2,2 mA ≤ *load* ≤180 mA	Considering the whole DM high level voltage range
Req-3	Overcurrent	≤400 mA		
Req-4	short circuit between 2 outputs	Withstand		
D	**IMPEDANCE (Differential impedance excluding the two serial diodes (see figure NOTE 1))**			
Req-1	Impedance under DM low voltage		R≤ 9kΩ	
Req-2	Impedance during free wheeling time (TI)	<10Ω		Excluding diodes inside matrix source

NOTE 1

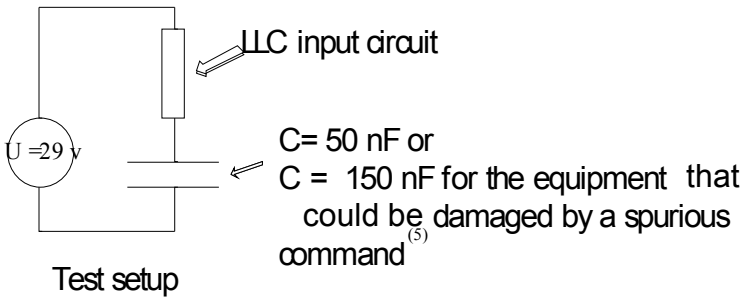


Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
E	***TIME***			
Req-1	Rise Time (Tr)	50 μs ≤ Tr ≤ 500 μs		Matrix output loaded by a user impedance in accordance with Code C and D.
Req-2	Fall Time (Tf)	1 μs ≤ Tf ≤ 600 μs		Matrix output loaded by a user impedance in accordance with Code C and D.
Req-3	« On » duration (Td)	40 ms ≤ Td ≤ 50 ms		
Req-4	Closed duration (Tl)	20 ms ≤ Tl ≤ 30 ms		Matrix requirement
Req-5	Spurious Command		Td ≤ 0,1 ms	Td = time duration
F	***MATRIX COMMAND GROUNDING AND ISOLATION*** (2)			
Req-1	Between matrix ground and Chassis: R equivalent	113 KΩ< R < 2 MΩ	> 10 MΩ	
Req-2	between one row or one column and Chassis: Equivalent Capacitance (In // R equivalent)	C_CM < 1nF	C_CM<500 pF (3)	(3) Around 10 KHz
Req-3	Between matrix ground and Chassis: C equivalent (In // R equivalent)	C_CM < 34 nF(3) (for SMU and PFDIU) C_CM < 50 nF(3) (for PLDIU)		(3) Around 10 KHz
Req-4	between row / column lines and relay or opto-coupler at user side		galvanic isolation	use of relay coil or opto-coupler at user side
H	***SPECIFIC REQUIREMENT***			
Req-1	Transient low "0" voltage	N/A	The input LLC shall not be activated with the following setup hereafter(4)	U=29V with tr 50 to 500 μs

(2) Primary and users secondary grounds shall be considered connected to chassis for measurements

Note: CM: Common mode / DM: Differential Mode

Test setup[4]



Test setup

[5] 150 nF is only applicable to Payload units.

Table 7: LLC electrical characteristics

*

Reference **SB4-SAT-AD1-P4-REQ-587**

For LLC a single return shall be allowed for a maximum of 4 LLC commands.

*

Reference **SB4-SAT-AD1-P4-REQ-588**

Each return shall be electrical insulated from other return.

*

6.2.7.7.3 HLC electrical parameters

Reference **SB4-SAT-AD1-P4-REQ-239 f**

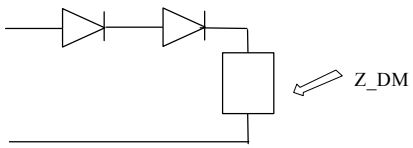
The HLC commands shall comply with these HLC electrical characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
A	***TYPE***			
Req-1	Output type	Differential		for matrix drivers organization
Req-2	Input type		Differential	
B	***VOLTAGE***			
Req-1	DM(5) low « 0 » voltage	-29 V / +4V	-29 V / +4V For voltage between –29V and 0V, the user shall guarantee no possible presence of current (presence of serial diodes). For voltage between 0V and 4 V, the user shall show no modification of mechanical, electrical and RF state with a max current of 5 mA	User shall also comply (no activation) with here below Req-H1
Req-2	DM(5) high « 1 » voltage	26 V (+3V / - 3V)	26 V (+3V/- 5.5V)	

Req-3	Threshold		The user of the HLC shall react and go to the commanded state with a maximum command threshold equals to the minimum voltage defined at B req2 (user side) With a impedance defined in D req1, the user of HLC shall not react to a command with a voltage lower that the maximum voltage defined at B req1 (user side) +1V. If the impedance of the user is lower than 120 ohms, the user of HLC shall not react to a command with a voltage lower that the maximum voltage defined at B req1 (user side) +0V.	
Req-4	CM(5) Permanent Fault Voltage Emission	Not allowed	-5V < fault < 40 v	DM(5) voltage =0
Req-5	DM(5) Transient Fault Voltage Emission	-63 V / 1s +33V/1s	± 2 V / 125 ms	
Req-6	DM(5) Transient Fault Voltage Tolerance	-63 V / 1s +33V/1s	-63 V / 1s +33V/1s	
Req-7	Voltage limitation during Tws free wheeling time	-5V < V < 0V		See figure 16
Req-8	Free wheeling voltage		-5V < V < 0V	Limited by the source when user re-inject current, see figure 16
C	***CURRENT***			
Req-1	Driving capability	> 500 mA		
Req-2	Load current		22 mA ≤ *load* ≤ 500 mA	Considering the whole DM(5) high level voltage range
Req-3	Source current limitation	≤ 1 A		
Req-4	Free Wheeling current capability during Twu	>500mA		See figure 16

Req-5	Free Wheeling current during Twu		≤500mA	See figure 16
Req-6	Free Wheeling current capability after Twu	>5mA		See figure 16
Req-7	Free Wheeling current after Twu		<5mA	See figure 16
D	**IMPEDANCE (Z_DM(5): Differential impedance excluding the two serial diodes(1))**			
Req-1	Impedance under DM(5) low voltage		R≤ 9kΩ	

(1) Schematic Definition of Z_DM :

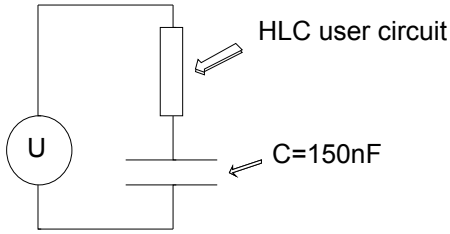


Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
E	***TIME***			
Req-1	Rise Time (Tr)	50 μs ≤ Tr ≤ 500 μs		
Req-2	Fall Time (Tf)	1 μs ≤ Tf ≤ 600 μs		N/A for a not loaded HLC output
Req-3	« On » duration (Td)	500ms ≤ Td ≤ 530ms	500ms ≤ Td ≤ 530ms	
Req-6	« On » duration (Td) for long HLC	530ms ≤ Td ≤ 1s	530ms ≤ Td ≤ 1s	
Req-7	« On » duration (Td) programmable range	15ms ≤ Td ≤ 1s		
Req-4	Free wheeling time	110ms ≤ Tws ≤ 140ms	Twu<60ms	See figure 16
Req-8	Free wheeling time for long HLC	110ms ≤ Tws ≤ 210ms	Twu<60ms	See figure 16
Req-9	Free wheeling time programmable range	15ms ≤ Tws ≤ 1s		
Req-5	Spurious Command		See here below Req H-1	No activation of the user
F	***GROUNDING AND ISOLATION*** [2]			
Req-1	Between matrix ground and Chassis: R equivalent	113 KΩ< R < 2 MΩ	> 10 MΩ	
Req-2	Between one row or one column and Chassis: Equivalent Capacitance (In // R equivalent)	C_CM[5] < 1nF	C_CM[5]<500 pF[3]	
Req-3	Between matrix ground and Chassis: C equivalent (In // R equivalent)	C_CM[5]< 50 nF[3] (for PLDIU)		
Req-4	between row / column lines and relay or opto-coupler at user side		galvanic isolation	use of relay coil or opto-coupler at user side
H	***SPECIFIC REQUIREMENT***			
Req-1	Transient low "0" voltage	N/A	The input HLC shall not be activated with the following setup [4]	

[2] Primary and users secondary grounds shall be considered connected to chassis for measurements

[3] Capacitance value shall be considered at a frequency around 10 KHz

[4] Equivalent circuit :



U=29V with rise time between 50µs to 500µs

(5) CM: Common mode / DM: Differential Mode

Table 8: HLC electrical characteristics

#	*

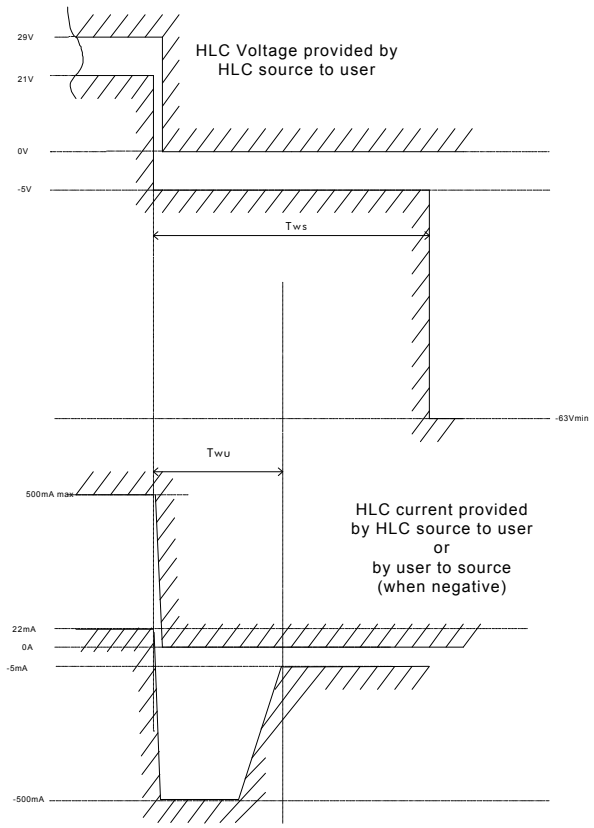


Figure 16 : HLC free wheeling chronogram

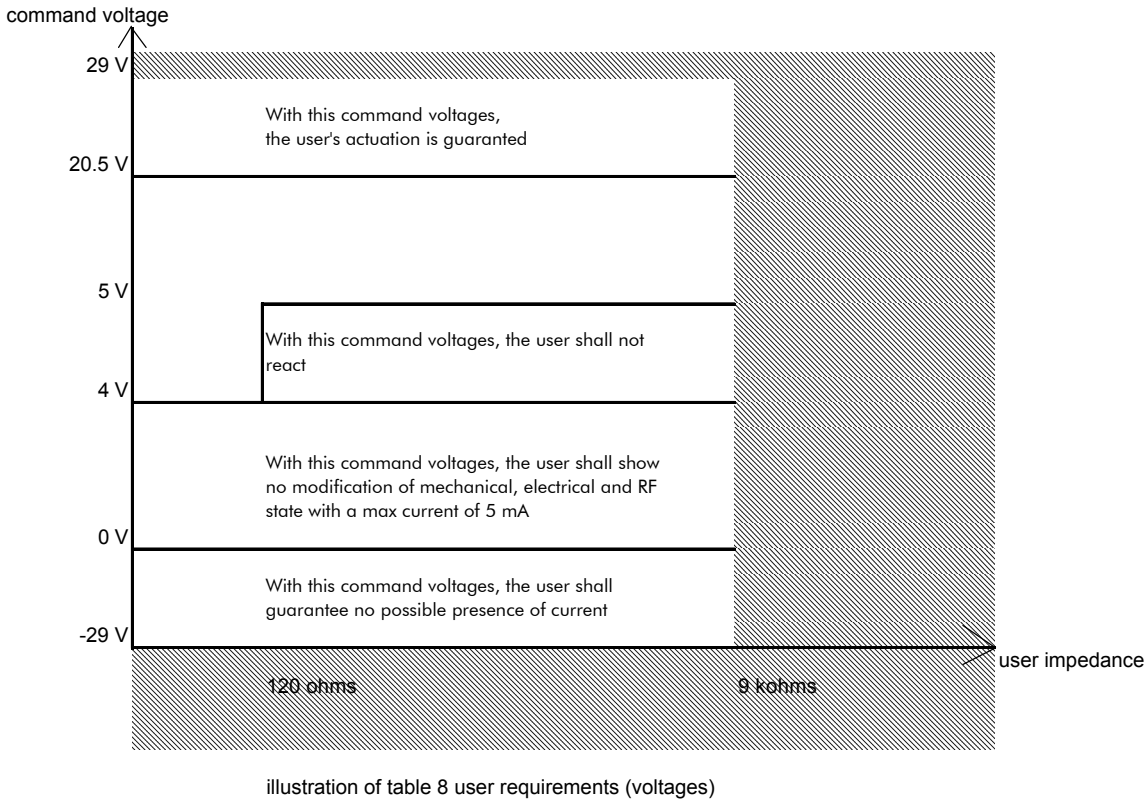


illustration of table 8 user requirements (voltages)

Reference **SB4-SAT-AD1-P4-REQ-589**

Each return shall be electrical insulated from others returns.

*

Reference **SB4-SAT-AD1-P4-REQ-590**

For HLC a single return shall be allowed for a maximum of 4 HLC commands.

*

6.2.8 SBDL Electrical Characteristics

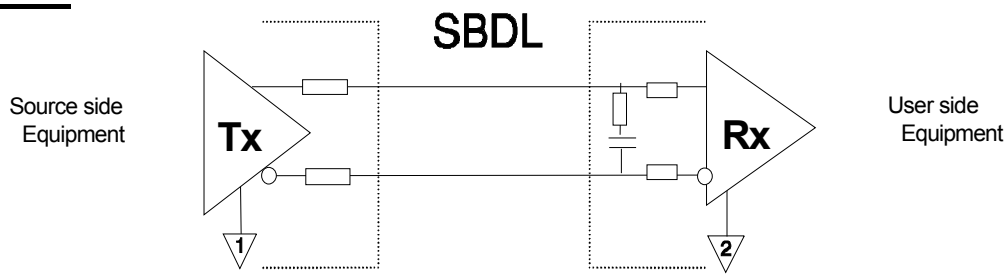
Reference **SB4-SAT-AD1-P4-REQ-626**

The following electrical characteristics shall be applied to a "point to point" connection. The cross strap of two redundant transmitters (MASTER) inside the unit (the same Pcb) is allowed.

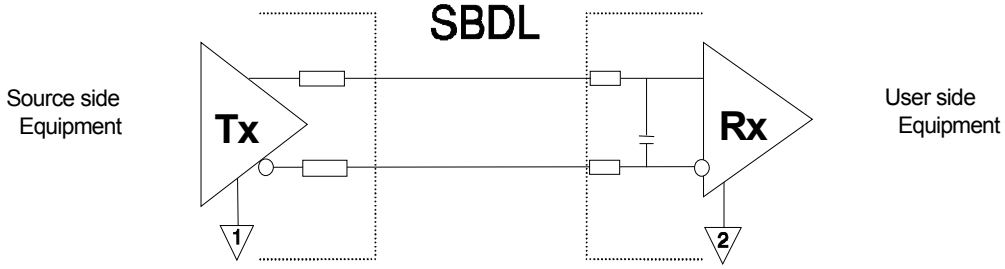
*

SBDL electrical interface is according to one of these schematics (Option1 and Option2):

OPTION 1



OPTION 2



Reference **SB4-SAT-AD1-P4-REQ-241 b**

SBDL serial link differential signals shall be identified as "non-inverted" and "inverted line".

*

Reference **SB4-SAT-AD1-P4-REQ-559**

The status of the signal shall be defined as true (logical " 1 ") when the non-inverted line has a positive voltage level w.r.t. the inverted line, i.e. when the non inverted line is at a high voltage level and the inverted line is at a low voltage level.

*

Reference **SB4-SAT-AD1-P4-REQ-560**

The status of the signal shall be defined as false (logical " 0 ") when the non-inverted line has a negative voltage with respect to the inverted line, i.e. when the non-inverted line is at a low level and the inverted line is at a high level.

*

Reference **SB4-SAT-AD1-P4-REQ-243 c**

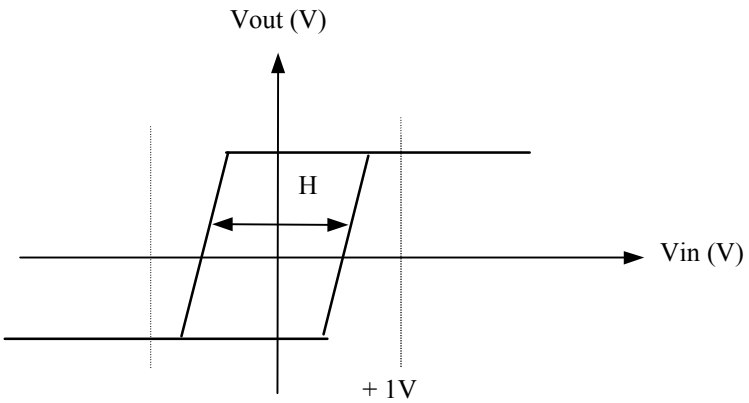
The SBDL interfaces shall comply with the following characteristics:

Code	PARAMETERS	SOURCE SIDE (transmitter)	USER SIDE (receiver)	COMMENT
A	***TYPE***			
Req-1	Output type	Differential driver or balanced driver		Differential driver required for ML16 drivers
Req-2	Input type		Differential	
B	***VOLTAGE***			
Req-1	Low level output voltage (VOL)	0V to 0.5V		D-Req4 (common mode)
Req-2	High level output voltage (VOH)	4 V to 5.5V		D-Req4 (common mode)
Req-3	Low level differential output voltage (logical 0)	-5.5 V to -3.5 V	See (1)	D-Req5
Req-4	High level differential output voltage (logical 1)	3.5 V to 5.5 V	See (1)	D-Req5
Req-5	Logical « 0 » differential threshold		-1V min	
Req-6	Logical « 1 » differential threshold		+1V max	
Req-7	CM Permanent Fault Voltage Emission	-0.5V to +7V		
Req-8	CM Permanent Fault Voltage Emission		-0.5V to +7V	through 2KΩ
Req-9	Overvoltage Tolerance (CM)	-7V to +12V		through 2KΩ
Req-10	Overvoltage Tolerance (CM)		-7V to +12V	
C	***CURRENT***			
Req-1	Current capability	20mA min. 100mA max.		Differential short circuit
D	***IMPEDANCE***			
Req-1	Power on differential Impedance	120Ω ± 10%		Serial resistor required
Req-2	Power off differential Impedance	4 KΩ min.		
Req-3	AC differential Impedance		120 Ω in series with 100 pF to 1nF max.	Option 1
Req-4	AC differential Impedance		2 x 2.2 KΩ min with 10 pF min. in parallel	Option 2 (Max. capacitor value is limited by propagation time)
Req-5	DC in line series resistor		2.2 KΩ min.	the value is related to each receiver input
Req-6	DC differential Impedance		10 KΩ min.	

Code	PARAMETERS	SOURCE SIDE (transmitter)	USER SIDE (receiver)	COMMENT
E	***TIME***			
Req-1	Rise Time (Tr)	10 ns ≤ Tr ≤ 100 ns		Measured on 120 Ω with 50pF in parallel. Only applicable to ML16/DS16
Req-2	Fall Time (Tf)	10 ns ≤ Tf ≤ 100 ns		Measured on 120 Ω with 50pF in parallel Only applicable to ML16/DS16
F	***GROUNDING AND ISOLATION***			
Req-1	from Secondary Ground (0Vs)	Circuit is referenced to 0Vs	Circuit is referenced to 0Vs	
Req-2	from Primary Ground	Isolated (> 1MΩ // 50nF)	Isolated (> 1MΩ // 50nF)	
Req-3	from chassis	Connected	Connected	

Table 9: SBDL characteristics

(1) Two solutions are acceptable for the receiver :
*use a classical differential receiver with the following characteristics



- The hysteresis H has to be greater than 0.8V
- The high level threshold has to be under 1V and the low level threshold has to be above -1V (differential measure).

* use the differential line receiver **HS-26C(T)32MS** specially designed for such applications.

*

6.2.9 Memory Load Command (ML16)

6.2.9.1 Command Definition

6.2.9.2 Conventions

6.2.9.3 MLC schematics

6.2.9.4 Memory Load Command timing

6.3 Telemetry interface

6.3.1 Telemetry users

6.3.2 Telemetry channel types

The telemetry channel types are :

a. Analog Channel (AN)
b. Digital Bi Level Channels (DB)
c. Digital relay channels (DR)
d. Digital Serial Channel 16-bit (DS16)
e. Thermistors Power Supply and Conditioning (TH)

6.3.3 Analog channels

6.3.3.1 Analog channels definition

For ADSP users the analog TM is coded in 12 bits.
For unit including BBC/RUBI device, the analog TM is coded in 10 bits.

6.3.3.2 Analog channels states

The system accuracy of the analog channels is better than ± 1 % of full scale.

6.3.3.3 Analog channels accuracy

Reference **SB4-SAT-AD1-P4-REQ-244 b**

The accuracy of the analog channel signal conditioning in the source shall be as specified in the corresponding subsystem specification but shall be limited to ± 0.5 % of full scale.

*

Reference **SB4-SAT-AD1-P4-REQ-613**

The overall A/D conversion accuracy including sampling error, quantization error plus offset shall be less than ± 0.5 % of full scale.

*

6.3.3.4 Analog channels coding

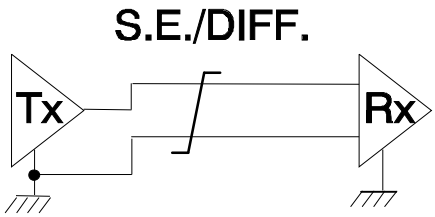
6.3.3.5 Source side requirements

6.3.3.6 User side (or receiver side) requirements

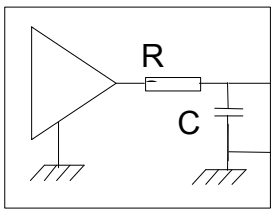
6.3.3.7 Analog channels schematics

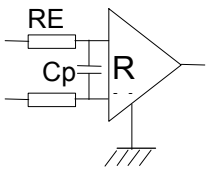
6.3.3.8 Analog channels characteristics

- Standard analog channel:



- Parameter definition:





Reference **SB4-SAT-AD1-P4-REQ-250 c**

The analog telemetry shall comply with these analog electrical characteristics:

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
A	***TYPE***			
Req-1	Output type	Single ended		
Req-2	Input type		Differential	
B	***VOLTAGE***			
Req-1	Range	0 V / 5.12V		
Req-2	Fault Voltage Emission	± 15 V	± 15 V	
Req-4	Fault Voltage Tolerance	± 17 V	± 17 V	
C	***CURRENT***			
Req-1	Over-current	≤ 15 mA		permanent
D	***IMPEDANCE***			
Req-1	impedance ON	Rs ≤ 5 KΩ in parallel with 100 nF ≤ C ≤ 1 µF (RS x C ≥ 0,1 ms)	≥ 1 MΩ	
Req-2	impedance OFF	RP ≤ 100 kΩ **(2)**	≥ 1 MΩ	
Req-3	Receiver input Capacity		100 pF Max	500 pF for harness
Req-4	DC in line series resistor		Re ≥ 3 KΩ	value related to each receiver input
Req-5	Receiver filter Capacity		Cp ≥ 10nF	
E	***GROUNDING AND ISOLATION***			
Req-1	from secondary ground (0Vs)	Connected	≥ 1 MΩ	

Table 11: Analogic telemetry characteristics

(2) Rp is the impedance between positive output and the ground when the unit (source side) is OFF.

*

6.3.3.9 Analog channels interconnection

6.3.3.9.1 High-priority telemetry signal

6.3.3.9.1.1 High-priority telemetry definition

Reference **SB4-SAT-AD1-P4-REQ-562**

The digital bi-level information shall be presented by the source in the form of a voltage that can assume only two distinct values, an on-level ("ONE" level) and an off level ("ZERO" level).

*

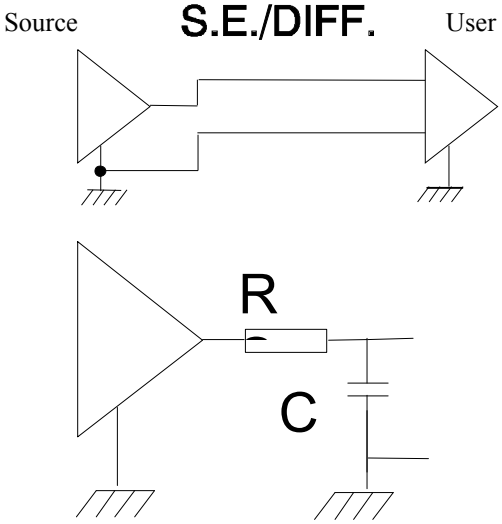
6.3.4.2 Digital Bi-Level trade-off

6.3.4.3 Source side requirements

6.3.4.4 User side (or receiver side) requirements

6.3.4.5 Digital Bi-Level channel telemetry schematics

6.3.4.6 Digital Bi-Level channel characteristics



Reference **SB4-SAT-AD1-P4-REQ-260 c**

The digital bi-level telemetry shall comply with these digital bi-level electrical characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
A	***TYPE***			
Req-1	Output type	Single ended		
Req-2	Input type		Differential	
Req-3	Transfer	DC COUPLER	DC COUPLER	
B	***VOLTAGE***			
Req-1	Low level output voltage (discrete ''0'')	0V to 0.5V		
Req-2	High level output voltage (discrete ''1'')	+3.5V to +10V		
Req-3	Fault Voltage Emission	± 15 V	± 15 V	
Req-4	Fault Voltage Tolerance	± 17 V	± 17 V	
C	***CURRENT***			
Req-1	Over-current	≤ 10 mA		permanent
D	***IMPEDANCE***			
Req-1	impedance ON	Rs ≤ 5 KΩ in parallel with 100 nF ≤ C ≤ 1 µF (RS x C ≥ 0,1 ms)	≥ 220 kΩ	
Req-2	impedance OFF	RP ≤ 100 kΩ **(2)**	≥ 1 MΩ	
Req-3	Capacitance		100 pF max	500 pF for harness
E	***GROUNDING AND ISOLATION***			
Req-1	from secondary ground (0Vs)	connected	isolated (≥ 1 MΩ)	

Table 12: Digital bilevel telemetry characteristics

(2) Rp is the impedance between positive output and the ground when the unit (source side) is OFF.

*

6.3.4.7 Digital Bilevel channels interconnection

6.3.4.7.1.1 High-priority telemetry definition

6.3.4.7.1.2 High-priority telemetry harness

6.3.4.7.1.3 High-priority telemetry fail-safe requirements

6.3.4.7.2 Low priority telemetry signal

6.3.4.7.2.1 Low priority telemetry definition

6.3.4.7.2.2 Low-priority telemetry harness

6.3.4.7.3 Cold redundancy

6.3.4.7.3.1 Cold redundancy definition

6.3.4.7.3.2 Cold redundancy telemetry harness

6.3.5 Digital switch closure channel telemetry

The Digital relay acquisition also called DR shall be used to transmit a relay or a switch status signal.

6.3.5.1 Digital switch closure telemetry types

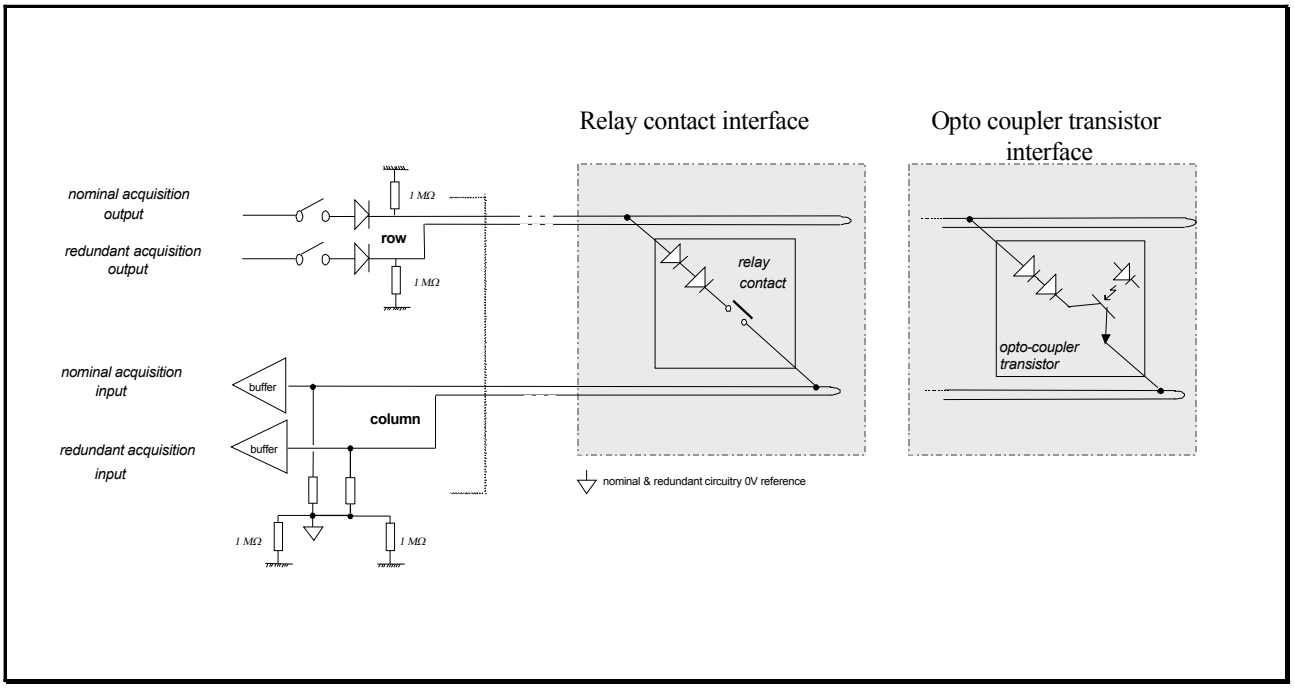
6.3.5.1.1 High-priority telemetry signal

6.3.5.1.2 Low priority telemetry signal

6.3.5.2 Cold redundancy definition

6.3.5.3 Matrix switch closure acquisition definition

The matrix switch closure acquisitions are performed through a matrix organisation. One row is pulled up to a positive voltage and the switch closure status is acquired on the column.



6.3.5.3.1 Switch closure matrix acquisition schematics

6.3.5.3.2 Source side requirements

Source side is related to the switch closure location

Reference **SB4-SAT-AD1-P4-REQ-266 b**

All source shall provide two diodes in series with the switch closure device.

*

Reference **SB4-SAT-AD1-P4-REQ-267 b**

deleted

*

Reference **SB4-SAT-AD1-P4-REQ-268 a**

The source equipment shall provide a galvanic isolation between the switch closure (contact or opto-coupler transistor) lines and the source electrical circuitry

*

Reference **SB4-SAT-AD1-P4-REQ-269 b**

The source equipment shall not impose any potential or grounding reference on any row or column.

*

Reference **SB4-SAT-AD1-P4-REQ-563**

Closed contact shall correspond to the TM "Zero" level with the unit powered or active

*

Reference **SB4-SAT-AD1-P4-REQ-564**

Open contact shall correspond to the TM "One" level with the unit unpowered or inactive

*

6.3.5.3.3 Receiver (or user) side requirements

Receiver side correspond at one hand to the switch closure polarization outputs and at the other hand to the switch closure acquisition input.

6.3.5.3.4 Matrix switch closure harness concept

6.3.5.4 Single ended switch closure acquisition definition

6.3.5.4.1 Source side requirements

6.3.5.4.2 Receiver (or user) side requirements

6.3.5.4.3 Digital relay channel telemetry schematics

6.3.5.4.4 Single ended switch closure harness concept

6.3.5.5 Digital relay channel telemetry characteristics

Reference **SB4-SAT-AD1-P4-REQ-308 c**

For matrix organization, the digital relay telemetry shall comply with these digital relay electrical characteristics :

Code	PARAMETERS	SOURCE SIDE DR	USER SIDE PCB	COMMENT
A	***TYPE***			
Req-1	Output type	differential		
Req-2	Input type		differential	for matrix organisation
B	***VOLTAGE***			
Req-1	Row min. voltage	N/A	9V	
Req-2	DM fault voltage emission	Not allowed	±17 V	
Req-3	DM fault voltage tolerance	-17 V	N/A	permanent, ON or OFF
Req-4	DM fault voltage tolerance	±17 V	N/A	permanent OFF only
Req-5	CM fault voltage emission	Not allowed	±17V	
Req-6	Drop voltage («ON state »)	≤ 3,7V at 1mA		- relay : 2 diodes + 1 relay contact - opto : 2 diodes+1 transistor junction
Req-7	CM Fault Voltage Tolerance	±17 V	±17 V	DM = 0
C	***CURRENT***			
Req-1	Contact capability 'ON'	I ≥ 1mA	0,5mA<I<5mA	Permanent, closed contact
Req-2	Contact capability 'OFF' (leakage)	<200µA @ 17V		Permanent, open contact
Req-3	Fault Current emission	N/A	<100mA	

Code	PARAMETERS	SOURCE SIDE DR	USER SIDE PCB	COMMENT
E	***MATRIX DR GROUNDING AND ISOLATION*** [1]			
Req-1	between row / column lines and Chassis	≥ 1 MΩ// <50 pF for switch** <500 pF for all the other equipment**	113 KΩ<R<10 MΩ //< 25 pF	** Only stray capacitance, no physical capacitance shall be added. Note: For Repeater Subsystem only the equivalent capacitance for one MAP equivalent matrix (contribution of all units connected) shall be lower than 33nF.
Req-2	Between matrix ground and Chassis		113 KΩ<R<10 MΩ // 10nF<C_CM<50nF for PLDIU or 10nF<C_CM<34nF for PFDIU	
Req-3	Between switch closure lines and the electrical circuitry	galvanic isolation		use of relay contact or opto-coupler transistor at source side

[1] Primary and users secondary grounds shall be considered connected to chassis for measurements

(1) Primary and users secondary grounds shall be considered connected to chassis for measurements

Table 13: Digital relay telemetry characteristics (For matrix acquisition)

*

Reference **SB4-SAT-AD1-P4-REQ-643**

A single return shall be allowed for a maximum of 4 DR telemetries

*

Reference **SB4-SAT-AD1-P4-REQ-632**

For single ended acquisition, the digital relay telemetry shall comply with these digital relay electrical characteristics :

Code	PARAMETERS	SOURCE SIDE DR	USER SIDE PCB	COMMENT
A	***TYPE***			
Req-1	Output type	differential		
Req-2	Input type		Single ended	for single ended acquisition
B	***VOLTAGE***			
Req-1	DM fault voltage emission	Not allowed	±16 V	
Req-2	DM fault voltage tolerance	±16 V	N/A	permanent OFF only
Req-3	Drop voltage («ON state ») for DR ABM / MBSV / Umbilical	≤ 4V / 400mA / 50ms		Only for ABM / MBSV / Umbilical
	Drop voltage («ON state ») for DR BSV/ SMU / PYPGP	≤ 0,5V / 10mA		Only for BSV/ SMU / PYPGP
	Drop voltage («ON state ») for DR TOM/ BAPTA / SADM	≤ 1V / < 1mA		Only for TOM/ BAPTA / SADM
C	***CURRENT***			
Req-1	Contact capability 'OFF' (leakage)	<100µA @ 5V		Permanent, open contact
Req-2	Fault Current emission	N/A	<100mA	

Code	PARAMETERS	SOURCE SIDE DR	USER SIDE PCB	COMMENT
E	***SINGLE COMMAND GROUNDING AND ISOLATION***			
Req-1	From Primary or Secondary Ground	Galvanic isolation		Not applicable to optical switches (BAPTA/SADM)
Req-2	Chassis	Isolated (≥1MΩ)		Not applicable to optical switches (BAPTA/SADM)

Table 14: Digital relay telemetry characteristics (Single ended acquisition)

*

Reference **SB4-SAT-AD1-P4-REQ-591**

For an equipment all digital relay telemetry return shall be insulated from all other digital relay telemetry return and from grounding

*

6.3.6 Digital serial channels : DS16

6.3.6.1 Telemetry definition

6.3.6.2 Conventions

6.3.6.3 Digital serial telemetry schematics

6.3.6.4 Corresponding TC

6.3.6.5 Digital serial Electrical characteristics

6.3.6.6 Digital serial telemetry timing

6.3.6.7 Digital Serial channels interconnection

6.3.6.7.1 High-priority telemetry signal

6.3.6.7.1.1 High-priority telemetry definition

6.3.6.7.1.2 High-priority telemetry harness

6.3.6.7.1.3 High-priority telemetry fail-safe requirements

6.3.6.7.2 Low priority telemetry signal

6.3.6.7.2.1 Low priority telemetry definition

6.3.6.7.2.2 Low-priority telemetry

6.3.6.7.2.3 Low-priority telemetry harness

6.3.6.7.3 Cold redundancy

6.3.6.7.3.1 Cold redundancy definition

6.3.6.7.3.2 Cold redundancy telemetry

6.3.6.7.3.3 Cold redundancy telemetry harness

6.3.7 Thermistors power supply and conditioning (TH)

6.3.7.1 Thermistors type

6.3.7.1.1 Type : GB42 or equivalent

6.3.7.1.2 Type: FENWAL or equivalent

Reference **SB4-SAT-AD1-P4-REQ-583**

The interface between receiver and the SMU shall provide (form SBDL signal): Squelch, Clock, Lock Status and Data signals.

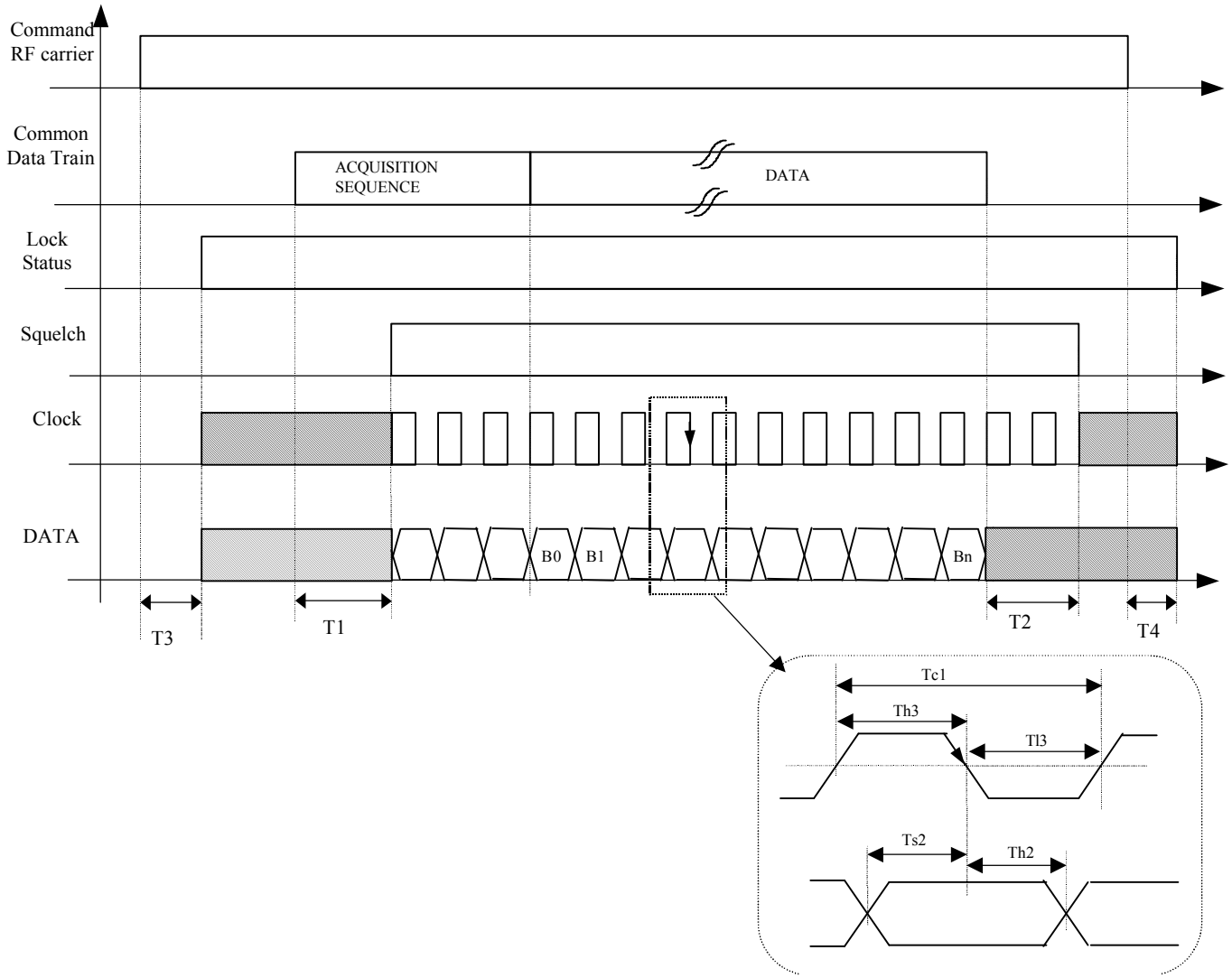


Figure 11: Signals between receiver and SMU.

T1 : ≤ *168 bits duration*

1 bit duration ≤ T2 ≤ 128 bits duration

T3 & T4 ≤ *100ms*

Tc1 (Bit clock period) = 1 Bit rate +/-5%

Th3 (TC bit clock high level duration at 50% edge) : ≥60µs

Tl3 (TC bit clock low level duration at 50% edge) : ≥60µs

Ts2 (Set-up time from NRZ DATA bit stable to clock falling edge (sampling edge)) : ≥10µs

Th2 (Hold time from clock falling edge to NRZ DATA bit change) : ≥20µs

The above described interface is used to transmit from the receiver to the SMU the following signal : SQUELCH , CLOCK , DATA

*

Reference **SB4-SAT-AD1-P4-REQ-584**

The receiver bit clock shall be running as soon as Lock Status is 'high'.

*

Reference **SB4-SAT-AD1-P4-REQ-326 b**

Data Validation shall be performed on the falling edge of the clock signal.

*

Reference **SB4-SAT-AD1-P4-REQ-327 a**

The bit clock stability shall be better than +/- 5% as soon as SQUELCH is high and until SQUELCH falls to low.

*

6.7.2 SMU / Transmitter interfaces

6.7.2.1 TRANSCEIVER TM video signals

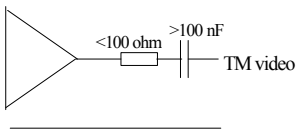
Reference **SB4-SAT-AD1-P4-REQ-330 d**

The TM video signals shall comply with the following characteristics :

Code	PARAMETERS	Transmitter side SMU	Receiver side	COMMENT
A	***TYPE***			
Req-1	Output type	single ended		
Req-2	Input type		differential	
Req-3	Type of Modulation	NRZ-L/BPSK	NRZ-L/BPSK	
Req-4	Waveform	Filtered quasi sine wave	Filtered quasi sine wave	
B	***VOLTAGE***			
Req-1	output AC voltage	3V ± 5.7% peak to peak		
Req-2	DC Fault Voltage Emission	-1V<U<10V	±17V in series with >2kΩ	
Req-3	DC Fault Voltage Tolerance	±17V in series with >2kΩ	-1V<U<10V	
C	***IMPEDANCE***			
Req-1	output impedance **(1)**	< 100Ω in series with > 100nF		
Req-2	input impedance		>10kΩ// <500pF	
D	***SPECIFIC REQUIREMENT***			
Req-1	TM sub-carrier frequency	65536 Hz	65536 Hz	upgrade : 32768Hz
Req-2	TM sub-carrier frequency stability	$\pm 10^{-4}$		
Req-3	TM bit rate	4096 bit/s or 8192 bit/s	4096 bit/s or 8192 bit/s	
Req-4	Phase plot accuracy	± 2°		Difference between theoretical and real phase
Req-5	group delay variations	< 1μs peak to peak		
Req-6	Amplitude distortion	<1 dB peak to peak		
Req-7	signal to noise ratio	65 dBHz		

Code	PARAMETERS	Transmitter side SMU	Receiver side	COMMENT
Req-8	Spurious and Harmonics	• **<-20dBc** : 0<f<220kHz • **<-60dBc :** f>220kHz 32768Hz +/-8kHz 65536 Hz +/- 8kHz [15kHz ;30kHz] 100kHz +/-1kHz	N/A N/A	 With respect to TM sub carrier levels TM signal bandwidth TM signal bandwidth Ranging signals bandwidth Ranging signals bandwidth
Req-9	phase step response accuracy	± 5% **(2)**		
E	***FAIL SAFE PROTECTION***			
Req-1	protection	short circuit proof		
F	***GROUNDING AND ISOLATION***			
Req-2	From primary ground	Isolation ≥ 1MΩ	Isolation ≥ 1MΩ	
Req-3	From chassis	Grounded	Isolation ≥ 1MΩ	

(1)



(2) At all times, for more than 25% of a sub-carrier period after a phase reversal, the phase of the modulated sub-carrier shall be within ±5% of a perfect signal.

Table 25: TM Video Signal Characteristics.

*

6.14 Heaters characteristics

6.14.1 General characteristics

6.14.2 Heaters interface characteristics

6.15 Deployment, Full Step, Sinus Cosinus motors Interfaces

6.15.1 Bi and three phases steppers interface characteristics

6.15.1.1 Antenna pointing motor interfaces

6.15.1.2 Thruster orientation motor interfaces

6.15.2 Brush motor interface

6.15.3 Sensors Interfaces

6.15.3.1 Potentiometers Interfaces

6.15.3.2 Micro-switch Interface

6.15.3.3 Optical Encoder Interface

6.15.3.4 Optical switch interface

6.15.3.5 Strain gauge

6.15.3.5.1 Deployment strain gauge

6.15.3.5.2 Battery Strain gauge

6.16 PYRO Interfaces

6.16.1 Initiator interface

6.16.2 PYRO Characteristics

6.17 AOCS Interfaces

6.17.1 Coarse Sun Sensor interface

6.17.2 Reaction Wheel interface

6.17.2.1 Torque command

6.17.2.2 Bi-level telemetry : Wheel direction and Wheel NOGO

6.17.2.3 Wheel direction and Wheel NOGO Telemetry

6.17.2.4 Bi-level telemetry : Tachometer

6.17.2.5 Tachometer telemetry

6.17.2.6 Motor current telemetry : PWM

6.18 NUMBER OF CONNECTOR PINS FOR RETURN LINES AND SHIELDING

6.19 Data Bus interfaces

Two types of Data bus are available on SB4000 :

- OBDH - 485
- 1553

The nominal bus is OBDH - 485.
The use of 1553 bus is limited to AOCS equipments :

- Startracker
- Gyro
- IRES

6.19.1 OBDH - 485

The "Data Bus Network Electrical and Protocol Specification" (SBF 6AV2 AS SP 338) document comprises the requirements to be satisfied by the OBDH-485.
(See chapter "Applicable documents")

6.19.2 1553 BUS INTERFACE

The Bus 1553 Applicable documents comprise the requirements to be satisfied by the bus 1553.
(See chapter "Applicable documents")

END OF DOCUMENT