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**SUBSYSTEM AND UNITS REQUIREMENTS - Electrical
Design and Interfaces Requirements
(AD01-P4)
SB4-6A-AS-SP-065**

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SPACEBUS

SUBSYSTEM AND UNITS REQUIREMENTS
- Electrical Design and Interfaces
Requirements
(AD01-P4)

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Service	ASP-03-SB_FIL-179_3
PMO Filière	ATTANASIO M
PMO Filière	AVENTIN O
PMO Filière	BASSALER P
PMO Filière	BAUTHIER C
PMO Filière	BENHAMOU M
PMO Filière	BENOIST E
PMO Filière	BOBAN E
PMO Filière	BRIZE L
PMO Filière	BRIZE O
PMO Filière	CORDIER P
PMO Filière	DAVID M
PMO Filière	DUCATEZ JL
PMO Filière	HERNANDO L

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CTO	PIN D
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IU/PM	CHAMPANDARD F
IU/PM	D'ADD JM
IU/PM	GEYER F
IU/PM	GIORDANO JJ
IU/PM	VERNE C
IU/PM	WAGNER C
IUEL	PRATX JM

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IUEL/IP	VIALANEIX JP
IUEL/LPE	FAURE A
IUEL/LPE	GARRAUD L
IUEL/LPE	MORENO
IUEL/LPE	SPINELLI C
IUEL/LPA	LABOURDETTE C
IUEL/LPA	LEPELTIER P
IUEL/LPA	CROQ F
DA	BOUGUET J
DA	DURAND B
DA	GARNERO P
DA	GIRAUDBIT JN
DA	VERZAT J
DBS	AIGNERAY P
DBS	COSTE O
DBS	NEYRET C
DQ	BORDEUX E
DQ	BOUVY D
DQ	CALVEL P
DQ	COSSON D
DQ	DELPET A
DQ	DEMAQUILLY D
DQ	DESPAROIR J
DQ	DODI D
DQ	FOLCO Y
DQ	PAYSSE JM
DQ	REMONDIERE O
DRD	ANDRAU M
DRD	GILBERTAS P
DRD	JOSEPH J
DRD	PORTIER J
IUIT	CAPELLI
IUIT	COUGNAUD F
IUIT	DERBES JC
IUIT	HENRY JP

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Service	ASP-03-SB_FIL-179_3
IUIT	LASFARGUES G
IUIT	PINTO M
IUSO	FRANCOIS M
IUSO	MICHAUD P
IUSO	PRUNIER C
IUSO	TORREA M
PROGRAMMES	Applicabilité SB4
PROGRAMMES	CHINASAT 9
PROGRAMMES	MODULES : Structure
PROGRAMMES	MODULES : Thermique
PROGRAMMES	MODULES : Câblages
PROGRAMMES	PROPULSION : UPS
PROGRAMMES	PROPULSION : PPS
PROGRAMMES	MECANISMES : ADM
PROGRAMMES	MECANISMES : ADPM
PROGRAMMES	MECANISMES : HRM
PROGRAMMES	MECANISMES : SADM
PROGRAMMES	AVIONIQUE : AOCS
PROGRAMMES	AVIONIQUE : EPS
PROGRAMMES	AVIONIQUE : DHS
PROGRAMMES	AVIONIQUE : FDIR
PROGRAMMES	GS (SLB)
Support Opérationnel DOORS Cannes	THONGKHAM V.
Support Opérationnel DOORS Cannes	BENILAN I.
Support Opérationnel DOORS Toulouse	CROSNIER M.
Support Opérationnel DOORS Toulouse	ALMAIDA D.

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CHANGE RECORDS

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ED.	REV.	DATES	MODIFIED D PAGES	CHANGES	APPROVAL
01	00	22/12/98		Initial issue	
02	00	05/05/99	6	3.8.1.1 Redundancy rules Req-1 :Redundancy and <u>cross-strap</u>	
			7	3.9.1.2 Access requirements Req-1 : ... <u>For SDIU, all boards shall be exchanged without</u>	
			30	5.1.2 Power bus operational voltage Req : 5.1.2.1-001, 5.1.2.2-02 : suppression of TBC	
			31	5.1.3 Equipment operating requirements Suppressions of TBC	
			32	5.1.4 Power safe line Req : 5.1.4-002 : Power safe line nominal voltage value	
			34	Req : 5.1.5-010 : Redundant fuses, <u>if necessary</u>at least <u>80%</u> of the operational... Req : 5.1.5-011 : the use of fuse rating less than <u>1 A</u> is prohibited....	
			36	5.2.1 Primary power line Addition of high and low speed power fluctuation for the 50V bus.	
			36	5.2.2 Power safe line Power safe line transient definition	
			40	6.1.2 Commands type	
			41	6.1.2.1 High priority command definition Correction of command number	
			47	6.1.6.1.2 Receiver side requirements (matrix) Req : 6.1.6.1.2.002 : New definition of the free wheeling diodes	
			49	6.1.6.1.4 Matrix command harness concept Req 11 and Req 12 applicability	
			50	Req 13 : new definition of the intermediate connectors	
			57	6.1.6.4.2 LLC electrical parameters :	
			58	global revision	
			59	6.1.6.4.3 HLC electrical parameters	
			60	global revision	
			83	Req 14 : Modification of logical levels	
			85	6.1.6.1.4 Matrix command harness concept Req 10 and Req 11 applicability	
			86	Req 12 : new definition of the intermediate connectors	

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			89	6.2.5.5 Digital relay channel telemetry characteristics C Req-2 : Nominal current limitation C Req-3 : Fault current emission	
			97 98 100	6.2.7 Thermistors power supply and conditioning Modification of thermistors definition and temperature range	
			102,103,106	6.4.1 Transceiver TC New definition of transceiver TC	
			107	6.6 Emergency signal Addition of a new electrical characteristic	
			110	6.7 Synchronisation signals : New Definition	
			125	6.11.1.1 Bi and three phases steppers interface New Definition	
			126	6.11.1.2 Brush motor interface D-Req 1 to 3 : deleted E Req-1 : winding resistance (source side) E Req-2 : winding inductance (source side)	
			127	6.11.2.2 micro-switch interface new requirement	
			128	6.11.2.3 Optical switch interface	
			129	6.11.2.4 Optical switch interface ; Nominal Vcc ; Maximum fault voltage emission	
			133-134	6.11.2.5 Strain gauge Definition of strain gauges	
			136	6.12.2 PYRO characteristics	
			137	6.13 AOCS Interfaces Definition of CSS and Wheel interfaces	
			146	6.17 Data bus interfaces definition of OBDH-485 and 1553B	
02	01	16/06/99	111	Requirements 6.9.1-001 to 6.9.1-007 deleted	
			112	6.9.2 ABM Valve interface Command Profile suppression	
			113,117	6.9.2 ABM Valve interface Modification of valves characteristics (coil inductance, resistance.....)	
			114,115 and 117	Correction of valves characteristics : Resistance value on the temperature range	
			125	6.11.1.1 Bi and three phases steppers... Power, Coil resistance and inductance correction	
			126	Brush motor resistance comment	
			127	Potentiometer power definition and impedance correction	
			128	Complementary information on the current consumption	
			133	Addition of a new schematic Suppression of the supply voltage accuracy, modification of the output voltage range	
			133/134	Parameter 'gage impedance' modified in 'gage impedance (R)'	

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02	02	01/10/99			
			13	Requirement 4.2.1-007 : suppression of TBC	
			14	Requirement 4.2.1-008 : suppression of TBC	
			15	Requirement 4.2.1-020 : suppression of TBC	
			28	Requirement 4.8-002 : suppression of TBC	
			29	5.1.1.1 Regulated 50V power bus Minimal DC bus voltage modification for payload equipments (except PLDIU)	
			31	Requirement 5.1.3-002 and table 5.1.3A ; 5.1.3B table 5.1.3A : Correction of recovery voltage Addition of BAPTA function automatic switch-off voltage table 5.1.3B : Correction of recovery voltage Addition of BAPTA function automatic switch-off voltage	
			34	Requirement 5.1.5-008 : New definition of the use of fuses inside equipments	
			57	Requirement 6.1.6.4.2-001 : transient fault voltage tolerance modification	
			59	Requirement 6.1.6.4.3-001 : transient fault voltage tolerance modification	
			65	6.1.8 SBDL Electrical characteristics Suppression of non applicable requirements	
			69	Requirement 6.2.3.5-001/b ; 6.2.3.6-001/b : Analog channels shall not be referenced to primary ground inside the source equipment	
			70-71	6.2.3.8 Analog channels characteristics new requirement : D-Req-6 specification complement	
			76-77	6.2.4.6 Digital Bi-level telemetry characteristics D-Req-1 User : Impedance ON	
			84	6.2.5.3.3 Switch closure matrix acquisition schematics Req-2 : Opto-coupler schematic modification	
			89-90	Requirement 6.2.5.5-001 : digital relay characteristics complement (opto-coupler addition)	
			104→ 105	6.4.2 TM video signals TM video characteristics correction	
			108	6.6.2 Emergency signal characteristics Specification Complement	
			111	6.7 Synchronisation signal Requirement 6.7-003/b and 6.7-006/b : Requirement complement and correction	
			115	6.9.3.1.1 Bistable valves interfaces B-Req1/2 : Voltage value correction	
			118	6.9.4.1.1 Mono-stable valves interfaces B-Req1 : Voltage value correction	

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			119→122	Requirement 6.9.5.1.1-001 and 6.9.5.1.2-001 : standard pressure transducer characteristics complement and correction	
			123-124	Requirement 6.9.5.2.1-001 : high accuracy pressure transducer characteristics complement	
			128→130	6.11.1.1 Bi and three phases steppers separation of the BAPTA, TOM and APM characteristics in three tables	
			131	6.11.1.2 Brush Motor interface A-Req1 ; A-Req 2 : deleted	
			132	6.11.2.1 Potentiometers interfaces Resistance range reduction	
			133	6.11.2.3 Optical encoder interface Addition of -15V supply	
			135	6.11.2.4 Optical switch interface Suppression of TBC and information complement	
			141	6.13.1 Coarse sun sensor Modification of capacity	
			142→146	6.13.2 Reaction Wheel interface New definition of the wheel electrical interface	
			149	Requirement 6.17.2-002 : Modification of 1553 architecture	

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ACRONYMS, SYMBOLS AND ABBREVIATIONS

A/D	Analog/numeric conversion
ABM	Apogee Boost Motor
AC	Alternating current
ADPM	Antenna Deployment and Pointing Mechanism
AN	TM Analog
AOCS	Attitude and Orbit Control Subsystem
AOCSP	Attitude and Orbit Control System PCB
AOCSP_NG	Attitude and Orbit Control System PCB_ New Generation
APM	Antenna Pointing Mode
AWG	American Wire Gauge
BAPTA	Bearing and Power Transfer Assembly
BBC	Bus Brick Connection
BCRB	Battery Connection Relay Box
CM	Common Mode
CRM	Central Reconfiguration Module
DB	TM Digital bi-level
DC	Direct current
DC/DC	Direct current/Direct current
DM	Differential Mode
DOCON	Down CONverter
DR	TM Digital Relay
DS16	TM Digital Serial 16 bit
DSPG	Distributed Single Point Grounding
EED	Electro-Explosive Devices
EGRN	Electrical Ground Reference Network
EGRP	Electrical Ground Reference Point
EGSE	Electrical Ground Support Equipment
EMC	Electro-Magnetic Compatibility
EPC	Electrical Power Conditioning
EPS	Electrical Power Subsystem
ESD	Electro-Static Discharges
HLC	High Level Command
HPC	High Priority Command
ICD	Interface Control Drawing
IDS	Interface Data Sheet
ITO	Iridium Tantale Oxyd
IRES	Infra-Red Earth Sensor

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LLC	Low Level Command
LMU	Li-Ion Battery Management Unit
LNA	Low Noise Amplifier
LPC	Low Priority Command
LSB	Least Significant Bit
MLC	Memory Load Command
MLI	Multi Layer Insulator
MSB	Most Significant Bit
NRZ	Non Return to Zero
NRZ-L	Non Return to Zero Level
OBDH	On Board Data Handling
OBP	On Board Processor
OSR	Optical Surface Radiator
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PCU	Power Conditioning Unit
PFDIU	PlatForm Distribution and Interface Unit
PLDIU	Payload Distribution and Interface Unit
PROP	PROpulsion electronic (Chemical/Plasmic) PCB
PPS	Plasmic Propulsion Subsystem
PPU	Power Processing Unit
PYPGP	Pyrotechnic Pcb with GP relays
RA	Rotary Actuator
RUBI	Remote User Brick Interface
RF	Radio Frequency
RX	Receiver
S/C	Spacecraft
S/W	Software
S4DSAP	SB4000 Deployment of Solar Array PCB
SA	Solar Array
SADM	Solar Array Drive Mechanism
SADP	Solar Array and Deployment PCB
SBDL	Standard Balanced Digital Signal
SDIU	Satellite Distribution and Interface Unit
SDMP	Stepper and Deployment Motor PCB
SLI	Single Layer Insulator
SMU	Satellite Management Unit
SPF	Single Point Failure
SSM	Second Surface Mirror
STR	Star Tracker

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TC	Telecommand
TCR	Telemetry, Command and Ranging
TH	Thermistor
TLM	Telemetry
TM	Telemetry
TOM	Thruster Orientation Mechanism
TTC	Tracking, Telemetry and Command
TWT	Travelling Wave Tube
TWTA	Travelling Wave Tube Amplifier
TX	Transmitter

UPCON	UP CONverter
UPS	Unified Propulsion Subsystem

w.r.t. with respect to

Note: Applicability List

AIT	Assembly Integration & Test
ANTRACK	Antenna Tracking
AOCS	Attitude and Orbit Control Subsystem
DATAM	Data Management
FDIR	Failure Detection, Isolation and Recovery
HARNESS	-
MECHANISM	-
PAYLOAD	-
POWER	-
PROP	Propulsion Subsystem
STRUCTURE	-
TCR	Telemetry, Command and Ranging
THERM	Thermal Subsystem
ANTENNA	-
ALL CF	All Functional Chain

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1. SCOPE

This document is the system APPLICABLE DOCUMENT called **AD01part 4** applicable to **subsystems and equipments.**

This document establishes the general electrical design and interface requirements for subsystems and equipments included in SPACEBUS 4000 systems satellites to be met to ensure their correct performance during assembly, integration, testing, storage, transportation, launch and orbital operations.

Additional design requirements related to Electromagnetic and ESD environmental conditions are provided in a separate dedicated applicable document **AD01 Part 3.**

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2. DOCUMENTS

2.1 Applicable documents

In case of conflict between any specification document and this applicable document, the specification document shall have precedence.

Any discrepancy shall be notified to the attention of Prime Contractor for clarification and resolution.

Denom.	Title	Doc Ref.
AD01 P1 (Part 1)	<i>Electrical design, interface and environmental Requirements</i>	SB.AS.SY.0001-1
AD02 P1 (Part 1)	<i>Mechanical design, interface and environmental Requirements</i>	SB.AS.SY.0002-1
AD03 Pa (Part a)	<i>Radiation Requirements</i>	REF-ASPI-CN-11-E
AD03 Pb (Part b)	<i>Space Radiation Environment Specification for Geostationary Missions</i>	REF-ASPI-CN-12-E
AD13	<i>Safety Requirements</i>	REF-ASPI-CN-39-E
IRD 01	<i>Launcher to Satellite Interface Requirement</i>	SB3-ASPI-SP-0158
IRD 02	<i>Satellite/Ground interface Specification Part 1 - Physical Layer (C-band)</i>	SB4-ASPI-SP-0381
IRD 03	<i>Satellite/Ground interface Specification Part 2 - SB4100C1 TM/TC format & protocol</i>	SB4-ASPI-SP-0078
IRD 04	<i>Satellite/Ground interface Specification Part 3 - Command and Observability</i>	SB4-ASPI-SP-0320
	<i>Data Bus Network Electrical and Protocol Specification</i>	SBF 6AV2 AS SP 338
	<i>MIL STD 1553B Protocol and Interface Requirements for DBN</i>	SBF 6AV2 AS SP 504
	<i>MIL STD 1553B "Aircraft Internal Time Division Command/Response Multiplex Data Bus", with Notice 4</i>	

Table 1: Applicable Technical Documents and Interface Documents at Satellite system level

Denom.	Title	Doc Ref.
AD 04	<i>Generic Product Assurance Requirements</i>	REF-ASPI-AQ-21-E
AD 05	<i>Materials, Parts & Process Requirements</i>	REF-ASPI-CN-10-E
AD 06	<i>EEE Parts Requirements</i>	REF-ASPI-CN-7-E
AD 07- P1	<i>Reliability Requirements</i>	REF-ASPI-CN-9-E
AD 07- P2	<i>Data Base for Reliability</i>	REF-ASPI-CN-13-E
AD 12	<i>Software Eng. And PA Requirements</i>	REF-ASPI-CN-38-E

Table 2: Applicable Programmatics, Quality and Product Assurance Requirements Documents at Satellite system level

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Denom.	Title	Doc Ref.
AD 09	Configuration Requirements	CAIS-ASPI-SP-0218
	Documentation Requirements	CAIS-ASPI-SP-0219
AD 10-P1	Guide de gestion des exigences	REF-ASPI-CN-74-E
AD 10-P2	Spécification des règles de gestion des exigences	REF-ASPI-CN-86-F
AD 11	Instruction for IDS and ICD	REF-ASPI-CN-88-E

Table 3:Applicable Programmatics and Data Configuration Requirements Documents at Satellite system level

2.2 Reference documents

The following documents listed hereinafter are for reference and information only. They have been used as basis for some requirements defined in the present specification.

Denom.	Title	Doc. Ref.
REF1	IEEE Standard for Space Applications Module, Extended Height Format E Form Factor	IEEE Std 1101.7-1995
REF2	EIA-485 Standard for Electrical Characteristics of Generators and Receivers for Use in balanced digital multipoint systems (RS485 Standard), April 1983	
REF3	Derating Requirements Applicable to Electronic, Electrical and Electro-Mechanical Components for ESA Space Systems, Issue 2, April 1992	PSS-01-301
REF4	Space system engineering Standard	ECSS-E-20B

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3. GENERAL SPECIFICATIONS

3.1 Engineering specifications

Reference **SB4-SAT-AD1-P4-REQ-001 b**

[FC Applicability: ALL CF (hardware)]

The metric standard (SI - International system) shall be used for design, manufacturing and testing of systems or subassemblies.

*

Reference **SB4-SAT-AD1-P4-REQ-638**

All requirements in this document shall be applicable in all satellite environmental conditions (mechanical, thermal, etc...)

*

3.2 Electrical symbols

Possible electrical symbols used in electrical diagrams (grounding, etc...) are shown in Figure 1:

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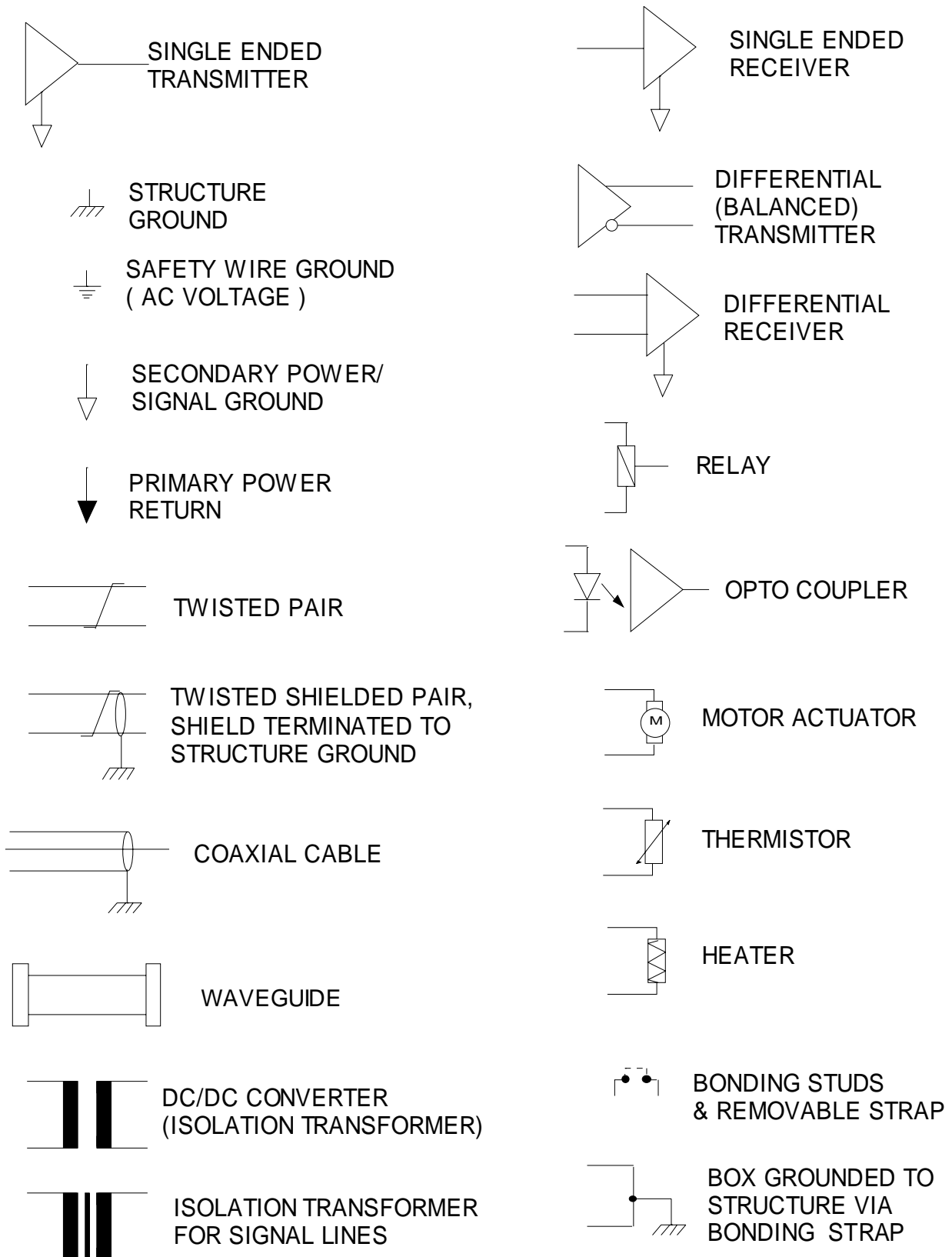


Figure 1: Symbols for electrical diagrams

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3.3 Lifetime

Reference **SB4-SAT-AD1-P4-REQ-005 b**

[FC Applicability: ALL CF (hardware)]

Units and subsystems shall be designed for a 15 years lifetime after having been stored for 5 years in a protected environment and having been used for tests and integrations for 2 years.

*

3.4 Delivery

Reference **SB4-SAT-AD1-P4-REQ-610**

[FC Applicability: ALL CF (hardware)]

All unit/subsystem shall be delivered in POWER OFF status.

*

3.5 Redundancy

3.5.1 Redundancy rules

Reference **SB4-SAT-AD1-P4-REQ-544**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, STRUCTURE, TCR, THERMAL, ANTENNA]

When redundancy is implemented in the design, any single failure leading to total or partial loss of the unit operational capability or mission shall be forbidden.

*

Reference **SB4-SAT-AD1-P4-REQ-009 b**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, STRUCTURE, TCR, THERMAL, ANTENNA]

When nominal and redundant ways are designed on the same board or device, the two functions shall be separated physically in order to avoid any risk of failure propagation.

*

Reference **SB4-SAT-AD1-P4-REQ-400**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, STRUCTURE, TCR, THERMAL, ANTENNA]

Nominal and redundant ways shall use separated connectors.

*

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3.5.2 Units failure

Reference **SB4-SAT-AD1-P4-REQ-014 b**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, STRUCTURE, TCR, THERMAL]

No conductive particle, smaller than 3 mm, shall cause total or partial loss of the unit or mission.

*

Reference **SB4-SAT-AD1-P4-REQ-401**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL]

All units, with nominal power consumption higher than 20W, shall always be able to switch-off in any case of failure.

*

3.6 Test points

Reference **SB4-SAT-AD1-P4-REQ-024 b**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL]

The test points shall be clearly identified in the unit ICD/IDS.

*

Reference **SB4-SAT-AD1-P4-REQ-026 b**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

Test points on multi-pin connectors shall be designed to withstand, without causing damage to the unit, the highest voltage on that connector unit as well as short circuits

*

Reference **SB4-SAT-AD1-P4-REQ-028 b**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL]

Unit test connectors shall be provided with electrically conductive covers to ensure protection against electrical and mechanical damage.

*

Reference **SB4-SAT-AD1-P4-REQ-029 b**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL]

Input test points shall be fixed in potential to avoid perturbations during operational life.

*

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3.7 Identification of product

Reference **SB4-SAT-AD1-P4-REQ-035 b**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

Connecting items shall be provided with mismating avoidance provisions. (identification marks or hardware design)

*

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4. ELECTRICAL ARCHITECTURE REQUIREMENTS

4.1 Grounding and isolation requirements

Grounding is the establishment of an electrically conductive path between two points to connect electrical elements of a system to the ground reference point.

4.1.1 Grounding objective

Electrical grounding and bonding is requested for all mechanical structure elements, equipment housing, thermal blanket devices and cables :

- to prevent hazard from high potentials
- to prevent build up and accumulation of electrostatic charges
- to avoid differential charge build up that could result in an electrostatic discharge
- to reduce electromagnetic interferences due to electric field or other forms of mutual coupling
- to protect from high voltage arcing
- to provide an Electrical Ground Reference Network (EGRN) used as an equipotential surface reference plane (particularly important for RF unit) to be able to withstand EMC/ESD requirements.

4.1.2 Grounding concept

The Electrical Ground Network includes the following items:

- aluminium panels (honeycomb and skins)
- launcher interface ring (this ring is the spacecraft reference point)
- internal deck interface ring
- all grounding strap (metallizations) and their rivets
- all baseplates supporting equipments.

The spacecraft structure shall constitute a low impedance reference named Electrical Ground Reference Network (EGRN).

Reference **SB4-SAT-AD1-P4-REQ-406**

[FC Applicability: STRUCTURE]

These grounding reference rails shall be implemented in the form of semi-rigid foil strips attached to the non-metallic structural elements and secured by inserts. These grounding reference rail shall be routed as close as possible to each unit mounted on the non-metallic structure.

*

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Reference **SB4-SAT-AD1-P4-REQ-407**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

Carbon fibre structural parts shall not be used as bounding path.

*

Reference **SB4-SAT-AD1-P4-REQ-410**

[FC Applicability: STRUCTURE]

The spacecraft surface fixed to the adapter shall be treated and protected in such a way that the electrical resistance between the Electrical Ground Reference Point and the adapter is kept lower than 10mΩ under 1Adc current measurement.

*

Reference **SB4-SAT-AD1-P4-REQ-411**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, STRUCTURE, TCR, THERMAL, ANTENNA]

All metallic sub-chassis, chassis and enclosures of each unit, including all connectors' shells and other fittings, shall be considered electrically as extensions of the EGRN.

*

The grounding and bonding concept is a "returns by wires" concept with a Distributed Single Point Grounding (DSPG) configuration.

Reference **SB4-SAT-AD1-P4-REQ-412**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, STRUCTURE, TCR, THERMAL, ANTENNA]

Each independent network (primary power distribution and secondary power distribution, ...) based on a star-point system shall be referenced to the EGRN via an one point low impedance connection.

*

Possible grounded solutions for unit secondary reference point are shown in Figure 2.

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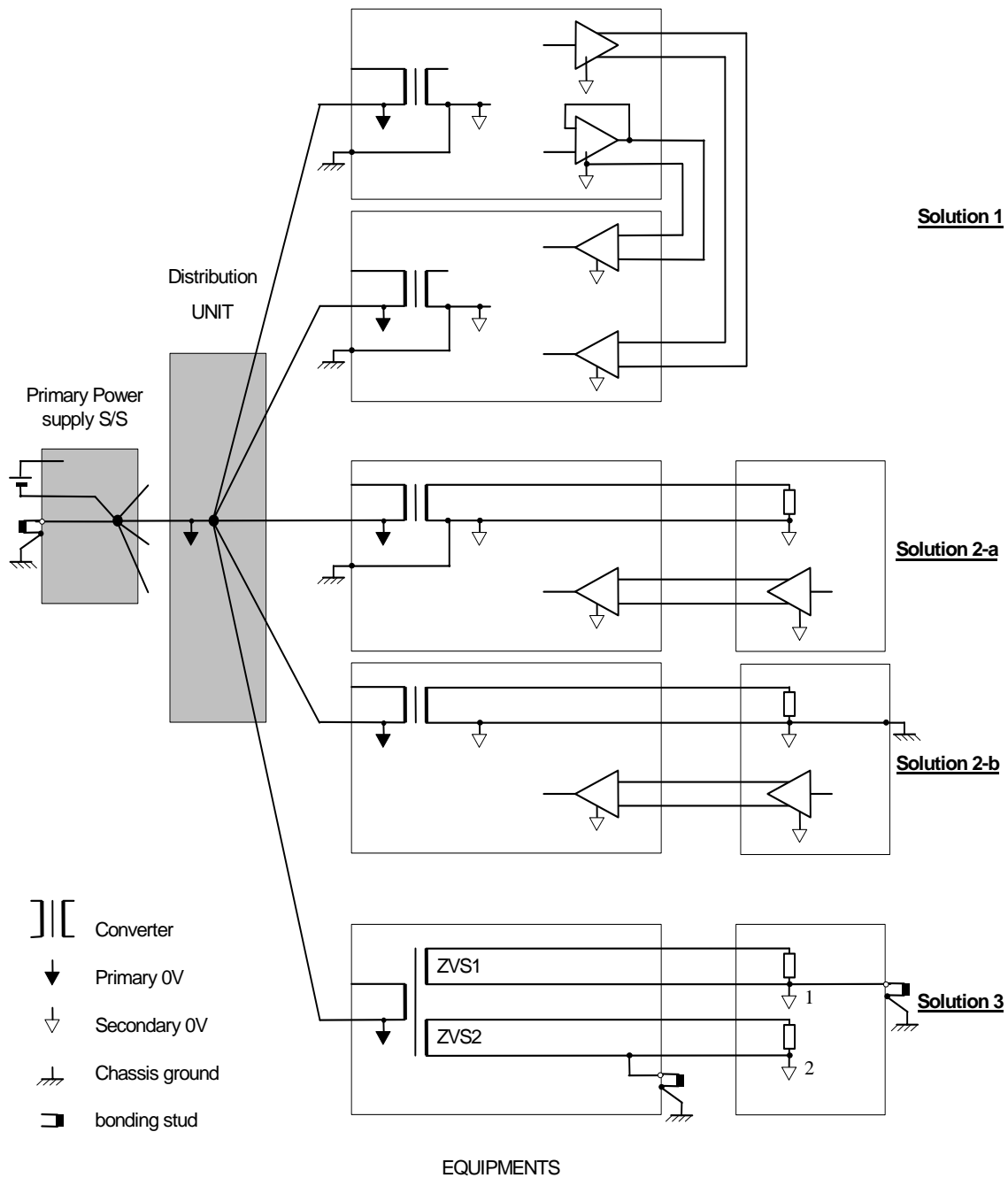


Figure 2: Basic philosophy for Distributed Single Grounding Concept

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4.1.2.1 Grounding Solution 1

Reference **SB4-SAT-AD1-P4-REQ-415**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

The unit secondary reference point is insulated from the secondary reference point of other units (implying the use of insulated or differential interfaces between the units). In this case, the equipment shall be grounded internally to its own housing in order to ensure a low impedance ground path.

*

4.1.2.2 Grounding Solution 2

Reference **SB4-SAT-AD1-P4-REQ-417**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

The unit secondary reference point is common to several units.

In this case :

- the unit assembly shall be grounded at only one point,
-

*

4.1.2.3 Grounding Solution 3

Reference **SB4-SAT-AD1-P4-REQ-418**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

Each unit shall provide dedicated bounding studs so that each unit secondary reference point can be grounded externally to the equipment housing. One of the grounding stud shall be insulated from the equipment structure and connected to the unit secondary reference point; the other one shall be connected directly to the chassis ground (See Figure 3).

It shall be possible to ground the unit secondary reference point by placing a bar (removable strap) between the two bounding studs.

This requirement is not mandatory for RF equipment which have an internal link.

It must be noted that the above-mentioned bounding studs is different from the bounding strap used to connect the unit case to the mechanical structure

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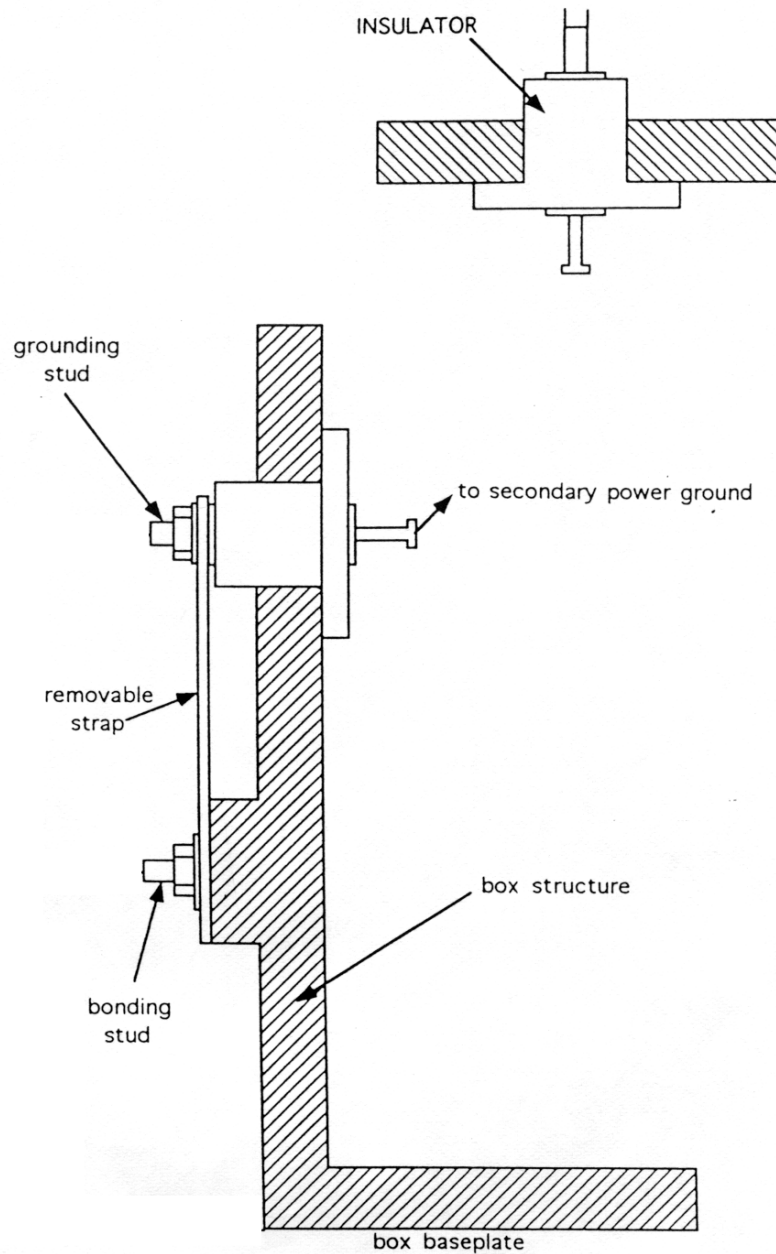


Figure 3 : Grounding of a unit secondary reference point via a bonding stud

*

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Reference **SB4-SAT-AD1-P4-REQ-419**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

The bar shall be supplied by the equipment manufacturer.

*

4.1.2.4 Specific Grounding Solution for matrix provided by SMU, CVICP and MAP.

Reference **SB4-SAT-AD1-P4-REQ-611**

[FC Applicability: DATAM]

For matrix provided by SMU, CVICP and MAP, the secondary 0Vs shall be grounded to the structure by resistors.

Note: To check resistance value (above-mentioned resistors) in concerned chapters (LLC/HLC characteristics).

*

4.1.3 Grounding and isolation diagram

Reference **SB4-SAT-AD1-P4-REQ-420**

[FC Applicability: ANTRACK, AOCS, DATAM, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL]

An overall zero volt and grounding diagram shall be provided in the IDS for establishing functional and electromagnetic compatibility.

*

Reference **SB4-SAT-AD1-P4-REQ-421**

[FC Applicability: ANTRACK, AOCS, DATAM, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL]

This diagram shall indicate any AC or DC loop, the type of isolation/insulation used, and any impedance coupling between zero volt and structure and shall be established for all Equipment and Subsystems containing electrical/electronic circuits.

*

4.1.4 Power lines grounding

Reference **SB4-SAT-AD1-P4-REQ-425**

[FC Applicability: ANTRACK, AOCS, DATAM, MECHANISMS, PAYLOAD, POWER, PROP, TCR]

The grounding connection impedance between the unit electrical 0V ground and its housing shall be lower than 2.5 mΩ measured under 1 Adc current and shall be lower than 100 nH.

*

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4.1.4.1 Grounding of primary power bus 0V

Reference **SB4-SAT-AD1-P4-REQ-423**

[FC Applicability: ANTRACK, AOCS, DATAM, MECHANISMS, PAYLOAD, POWER, PROP, TCR]

The return of all the power bus shall be grounded to the EGRN at a single grounding point located in the service module at the negative side of main bus capacitor within the power subsystem regulator.

*

Reference **SB4-SAT-AD1-P4-REQ-424**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Users of primary power shall therefore isolate the power wires from the structure

*

Reference **SB4-SAT-AD1-P4-REQ-426**

[FC Applicability: DATAM, POWER, PROP]

The power system regulator shall provide a dedicated stud to allow the primary return line grounding.

*

4.1.4.2 Grounding of secondary power bus 0V

Reference **SB4-SAT-AD1-P4-REQ-427**

[FC Applicability: ANTRACK, AOCS, DATAM, POWER, PROP, TCR]

Secondary power line returns shall be referenced to the electrical ground reference (structure) at only one location point, except for RF units.

*

Reference **SB4-SAT-AD1-P4-REQ-428**

[FC Applicability: PROP]

For PPU high voltage secondary outputs connected to the active thrusters, the secondary 0V shall be uncoupled from the mechanical ground plane by a capacitance.

*

Reference **SB4-SAT-AD1-P4-REQ-429**

[FC Applicability: ANTRACK, AOCS, DATAM, POWER, PROP, TCR]

In case that several units are supplied from the same DC / DC converter secondary power output, the secondary 0V shall be interconnected in a starpoint system to form the secondary reference ground, except for RF units.

*

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Reference **SB4-SAT-AD1-P4-REQ-430**

[FC Applicability: ANTRACK, AOCS, DATAM, POWER, PROP, TCR]

All converter secondary OV shall be insulated from one to another by design, except for RF units.

*

Reference **SB4-SAT-AD1-P4-REQ-431**

[FC Applicability: PAYLOAD]

The high voltages necessary for the TWT's shall be considered as secondary power and shall be referenced at the EPC (via EPC structural part) and at the TWT side (via the TWT structural part).

*

Reference **SB4-SAT-AD1-P4-REQ-433**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

The grounding path shall be designed and sized to withstand a current equal to 1.5 times the worst case fault current as limited by the unit primary power bus protection device. The following current shall be considered :

- either a primary current due a short-circuit between the primary power supply hot spot and the unit secondary reference point/mechanical ground.
- or a secondary current due to a short-circuit between a secondary power line and the secondary reference point/mechanical ground.

*

Reference **SB4-SAT-AD1-P4-REQ-435**

[FC Applicability: ANTRACK, AOCS, DATAM, MECHANISMS, PAYLOAD, POWER, PROP, TCR]

All transformer screen shall be grounded to chassis.

*

4.1.5 Primary and secondary power lines insulation

Reference **SB4-SAT-AD1-P4-REQ-170 a**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

The primary power lines shall be transformer insulated from all secondary power.

*

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Warning: During measurement rating on components must be withstood. Derating may be exceeded.

Reference **SB4-SAT-AD1-P4-REQ-436**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Insulation	isolation resistor with stray capacitance in parallel	measurement DC voltage	test conditions
Between unit primary power + (positive) input lines and structure	($>1\text{ M}\Omega$) // ($< 50\text{ nF}$)	100Vdc	unit unpowered

*

Reference **SB4-SAT-AD1-P4-REQ-631**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Insulation	isolation resistor with stray capacitance in parallel	measurement DC voltage	test conditions
Between unit primary power - (negative) input lines and structure	($>1\text{ M}\Omega$) // ($< 600\text{nF}$)	50Vdc	unit unpowered

*

Reference **SB4-SAT-AD1-P4-REQ-438**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Insulation	isolation resistor with stray capacitance in parallel	measurement DC voltage	test conditions
Between primary power leads and secondary power leads	($>1\text{ M}\Omega$) // ($< 50\text{ nF}$)	100Vdc both polarities	unit unpowered

*

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

Reference **SB4-SAT-AD1-P4-REQ-439****[FC Applicability:** ANTRACK, AOCS, DATAM, POWER, PROP]

Insulation	isolation resistor with stray capacitance in parallel	measurement DC voltage	test conditions
Between any unit secondary power leads and structure (Except for Payload and TTC)	(> 1 MΩ) // (< 50 nF)	100Vdc both polarities	unit unpowered stud removed Not Applicable to grounding solution 1 (See SB4-SAT-AD1-P4-REQ-415)

*

Reference **SB4-SAT-AD1-P4-REQ-440****[FC Applicability:** ANTRACK, AOCS, DATAM, POWER, PROP, TCR]

Insulation	isolation resistor with stray capacitance in parallel	measurement DC voltage	test conditions
Between secondary power leads and other unit secondary power leads Except for Payload and TTC	(> 1 MΩ) // (< 50 nF)	100Vdc both polarities	unit unpowered stud removed

*

4.1.6 High voltage units

Reference **SB4-SAT-AD1-P4-REQ-624****[FC Applicability:** PAYLOAD, PROP]

For unit including high power supplies (EPC, PPS, etc...), thermistor, relay coil, relay contact or heater leads insulation shall be guaranteed at the highest voltage level within the equipment with 6 db margin.

*

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

4.2 Bonding requirements

4.2.1 General purpose

Bonding is the establishment of a low impedance path between two metal surfaces or different structural parts.

Electrical bonds are employed for the following purposes:

- To minimise the impedance of the ground plane formed by the metallic portion of the structure.
- To assure the existence of low impedance return paths for possible failure mode-related fault current.
- To avoid the development of RF potentials between adjacent conductive surfaces raise the effectiveness of enclosure shielding.
- To provide high current capability to carry potential fault current.

Reference **SB4-SAT-AD1-P4-REQ-488**

[FC Applicability: AIT, ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, STRUCTURE, TCR, THERMAL, ANTENNA]

To avoid discharge surfaces, each electrically conductive layer shall be grounded to structure.

*

4.2.2 Bonding characteristics at unit level

Reference **SB4-SAT-AD1-P4-REQ-454**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, STRUCTURE, TCR, THERMAL, ANTENNA]

Bonding connection	Electrical continuity
between two adjacent parts of a metal case including the resistance between any point of the case and any point of the cover or bonding point (possibly after vibration tests)	$\leq 5 \text{ m}\Omega$ under 1Adc current

*

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

Reference **SB4-SAT-AD1-P4-REQ-459****[FC Applicability:** ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

Bonding connection	Electrical continuity
between connector shell and unit structure	$\leq 2.5 \text{ m}\Omega$ under 1Adc current

*

Reference **SB4-SAT-AD1-P4-REQ-460****[FC Applicability:** ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

Bonding connection	Electrical continuity
between connector back-shell and connector body	$\leq 5 \text{ m}\Omega$ under 1Adc current

*

4.2.3 Bonding strap characteristics

Reference **SB4-SAT-AD1-P4-REQ-449****[FC Applicability:** AIT, STRUCTURE]Bonding between metallic structure parts shall be direct with a minimum covering area of 1cm².

*

Reference **SB4-SAT-AD1-P4-REQ-450****[FC Applicability:** AIT, STRUCTURE]

The bounding strap length-to-width (L / w) ratio shall be less than 5 to 1 assuming a strap thickness of 0.2 mm.

If this rule can not be met, the bonding strap shall respect:

- DC ohmic resistance < 2.5 m Ω
- Inductance < 100 nH

*

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Reference **SB4-SAT-AD1-P4-REQ-451**

[FC Applicability: AIT, STRUCTURE]

The bonding strap shall be protected to avoid damage in case of bundles proximity.

*

Reference **SB4-SAT-AD1-P4-REQ-456**

[FC Applicability: AIT, STRUCTURE]

Bonding connection and strap resistance	Electrical continuity
Between the active unit ¹ (including external switches) bonding stud and the EGRN bonding point (including the bonding strap contacts) ¹ Internal or external units	$\leq 10 \text{ m}\Omega$ under 1Adc current

*

Reference **SB4-SAT-AD1-P4-REQ-596**

[FC Applicability: AIT, ANTRACK, PAYLOAD, STRUCTURE, ANTENNA]

Bonding connection and strap resistance	Electrical continuity
between the antenna feed or OMUX and the EGRN	$\leq 10 \text{ m}\Omega$ under 1Adc current

*

Reference **SB4-SAT-AD1-P4-REQ-409**

[FC Applicability: AIT, STRUCTURE]

Bonding connection and strap resistance	Electrical continuity
between the Electrical Ground Reference Point (EGRP) and any point of the Electrical Ground Reference Network (EGRN)	$\leq 50 \text{ m}\Omega$ under 1Adc current

*

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- Electrical Design and Interfaces

Requirements

(AD01-P4)

4.2.4 Harness Bonding characteristics

Reference **SB4-SAT-AD1-P4-REQ-461**

[FC Applicability: AIT, HARNESS, STRUCTURE]

Bonding connection	Electrical continuity
between overall harness shield and connector back-shell	$\leq 5 \text{ m}\Omega$ under 1Adc current

*

Reference **SB4-SAT-AD1-P4-REQ-462**

[FC Applicability: AIT, HARNESS, STRUCTURE]

Bonding connection	Electrical continuity
<u>Pyro :</u> Any part of pyro shielding and connector cover Any part of pyro shielding and EGRN	$\leq 2.5 \text{ m}\Omega$ under 1Adc current

*

4.2.5 Structural Part Assembly Bonding

Reference **SB4-SAT-AD1-P4-REQ-475**

[FC Applicability: MECHANISMS, STRUCTURE]

Bonding connection	Electrical continuity
between two mating metal structural parts (metal-to-metal assembly)	* $\leq 10 \text{ m}\Omega$ under 1Adc current * minimum contact size area $> 1 \text{ cm}^2$

*

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Reference **SB4-SAT-AD1-P4-REQ-476****[FC Applicability:** MECHANISMS, STRUCTURE]

Bonding connection	Electrical continuity
between metal part and carbon fibre part	< 100 Ω

*

Reference **SB4-SAT-AD1-P4-REQ-477****[FC Applicability:** AIT, MECHANISMS, STRUCTURE]

Bonding connection	Electrical continuity
between carbon fibre parts (panels, corners, angles)	< 100 Ω

*

Reference **SB4-SAT-AD1-P4-REQ-479****[FC Applicability:** AIT, MECHANISMS, STRUCTURE]

Bonding connection	Electrical continuity
between carbon fibre skins (face-sheets) and structure (EGRP)	< 100 Ω

*

Reference **SB4-SAT-AD1-P4-REQ-481****[FC Applicability:** ANTRACK, MECHANISMS, STRUCTURE, ANTENNA]

Bonding connection	Electrical continuity
between antenna reflector and structure (EGRP)	< 500 Ω

*

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Reference **SB4-SAT-AD1-P4-REQ-482**

[FC Applicability: MECHANISMS, STRUCTURE]

Bonding connection	Electrical continuity
between brackets, connector support and unit support and structure (EGRP)	< 100 Ω

*

Reference **SB4-SAT-AD1-P4-REQ-483**

[FC Applicability: POWER, STRUCTURE]

Bonding connection	Electrical continuity
between solar arrays housing and structure (EGRP)	< 25 K Ω

*

Reference **SB4-SAT-AD1-P4-REQ-484**

[FC Applicability: MECHANISMS, STRUCTURE]

Bonding connection	Electrical continuity
between batteries housing and structure (EGRP)	< 60 K Ω

*

Reference **SB4-SAT-AD1-P4-REQ-485**

[FC Applicability: STRUCTURE]

Bonding connection	Electrical continuity
Items not included in the EGRN (angles, corners, inserts...) and the structure (EGRP)	< 1 M Ω

*

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4.2.6 Thermal Part Assembly Bonding

4.2.6.1 General Requirements

Reference **SB4-SAT-AD1-P4-REQ-489**

[FC Applicability: AIT, STRUCTURE, THERMAL]

Conductive components which can not respect the bonding requirements specified in the following sections shall be connected to the ground reference network by a resistance lower than 1 MΩ.

*

4.2.6.2 MLI / SLI Requirements

Reference **SB4-SAT-AD1-P4-REQ-492**

[FC Applicability: AIT, STRUCTURE, THERMAL]

Each part of the MLI or SLI shall be connected to the EGRN with at least :

- one point if their area is less than 0.05 square meter.
- two points if their area is more than 0.05 square meter

*

Reference **SB4-SAT-AD1-P4-REQ-493**

[FC Applicability: AIT, STRUCTURE, THERMAL]

The DC resistance between one of these points and the EGRN close to the connection shall be less than 300 mΩ under 1Adc measurements

*

Reference **SB4-SAT-AD1-P4-REQ-494**

[FC Applicability: STRUCTURE, THERMAL]

Each MLI metallized foil shall be electrically connected to the reference point of the MLI piece.

The DC resistance between this point and any point belonging to a metallized face of any foil shall be less than 200 Ω tested at 100 mA.

*

Reference **SB4-SAT-AD1-P4-REQ-495**

[FC Applicability: AIT, STRUCTURE, THERMAL]

External MLI Kapton thickness shall be 25 μm, except for Solar Array panel insulation that shall be 50 μm.

*

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(AD01-P4)

Reference **SB4-SAT-AD1-P4-REQ-606**

[FC Applicability: THERMAL]

MLI external surfaces (space face) shall be conductive. Some limited exceptions are acceptable (Star trackers, ADPM, RF feeds, anti earth panel).

*

4.2.6.3 SSM Requirements

Reference **SB4-SAT-AD1-P4-REQ-497**

[FC Applicability: ALL CF (hardware)]

The use of SSM shall be avoided.

*

4.2.6.4 OSR Requirements

Reference **SB4-SAT-AD1-P4-REQ-582**

[FC Applicability: STRUCTURE, THERMAL]

If no ITO is used, non conductive glue shall be used

*

4.3 Paints and coatings characteristics

Reference **SB4-SAT-AD1-P4-REQ-490**

[FC Applicability: ALL CF (hardware)]

Coatings (including paintings) on non conductive surface

Coatings applied on a dielectric or non-conductive surface shall be grounded to the ground reference network on the edges.

The coating surface resistivity applied on non conductive materials shall be less than $1 \text{ E9 } \Omega / \text{square}$.

*

Reference **SB4-SAT-AD1-P4-REQ-491**

[FC Applicability: ALL CF (hardware)]

Coatings (including paints) on conductive surface

The coating resistivity applied on a conductive surface shall be less than $1 \text{ E9 } \Omega.m$ assuming a depth $e \leq 100 \mu m$.

*

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

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4.4 Electrical connector requirements

Requirements in this chapter are applicable to:

- Satellite harness
- Harness of the units (i.e.: Reaction Wheel, ADPM...), except to Pcb's wires.

4.4.1 Connector types

Reference **SB4-SAT-AD1-P4-REQ-498**

[FC Applicability: ALL CF (hardware)]

All connectors shall be selected according to AD11.

*

Reference **SB4-SAT-AD1-P4-REQ-499**

[FC Applicability: ALL CF (hardware)]

MDM and very high density (ex.:AMP104) connectors shall not be used.

*

Reference **SB4-SAT-AD1-P4-REQ-507**

[FC Applicability: ANTRACK, AOCS, DATAM, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL]

All connectors dedicated to power generation and distribution outputs shall be socket type.

*

Reference **SB4-SAT-AD1-P4-REQ-508**

[FC Applicability: ANTRACK, AOCS, DATAM, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL]

All other connector shall be pin type.

*

4.4.2 Connector characteristics

4.4.2.1 Connectors housing

Reference **SB4-SAT-AD1-P4-REQ-506**

[FC Applicability: AIT, ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

The housing of connectors shall be electrically connected to the unit structure.

*

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4.4.2.2 Specific derating requirements

Reference **SB4-SAT-AD1-P4-REQ-510**

[FC Applicability: AIT, ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

Mating and demating of each connector shall be less than 25 at Satellite System Integration.

*

Reference **SB4-SAT-AD1-P4-REQ-614**

[FC Applicability: AIT, ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

Mating and demating of each connector shall be less than 25 before unit delivery at Satellite System Integration.

*

4.4.2.3 Connector mounting requirements

Reference **SB4-SAT-AD1-P4-REQ-511**

[FC Applicability: AIT, ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

The connectors shall be placed in such a way that connection and disconnection on one connector shall be made without any specific tool and without disconnecting the other connectors.

*

Reference **SB4-SAT-AD1-P4-REQ-512**

[FC Applicability: AIT, ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

At least, 6mm shall be kept between two adjacent connectors.

*

Reference **SB4-SAT-AD1-P4-REQ-615**

[FC Applicability: AIT, ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

The connectors shall be placed according to manufacturer connector requirements.

*

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4.4.2.4 Connector identification

Reference **SB4-SAT-AD1-P4-REQ-518**

[FC Applicability: AIT, ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

Each unit or bracket shall be permanently marked by visible connector identification closely adjacent to the appropriate connector in order to allow a correct mating of corresponding harness connector.

*

4.4.3 Connector savers

Reference **SB4-SAT-AD1-P4-REQ-513**

[FC Applicability: AIT, ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

Saver connectors shall be used during integration to lower number of mating and demating cycles.

*

4.4.4 Pins characteristics

Reference **SB4-SAT-AD1-P4-REQ-515**

[FC Applicability: AIT, ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

Lines which have a common return shall be placed on adjacent contacts to facilitate cable twisting and/or shielding (except for matrix concept).

*

Reference **SB4-SAT-AD1-P4-REQ-517**

[FC Applicability: AIT, ANTRACK, AOCS, DATAM, HARNESS, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

The connected contacts on each connector shall never be inferior to two third of its maximum capacity.

*

4.4.5 Specific requirements for pyro connectors

Reference **SB4-SAT-AD1-P4-REQ-501**

[FC Applicability: ANTRACK, DATAM, HARNESS, MECHANISMS, POWER, PROP, STRUCTURE, ANTENNA]

Pyrotechnic circuit connectors shall be separated from all other circuit connectors

*

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

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Reference **SB4-SAT-AD1-P4-REQ-502**

[FC Applicability: ANTRACK, DATAM, HARNESS, MECHANISMS, POWER, PROP, STRUCTURE, ANTENNA]

Pyrotechnic circuit connectors shall have a stainless steel shell or suitable electrically conductive finish

*

Reference **SB4-SAT-AD1-P4-REQ-503**

[FC Applicability: ANTRACK, DATAM, HARNESS, MECHANISMS, POWER, PROP, STRUCTURE, ANTENNA]

Pyrotechnic circuit connectors shall complete the shell-to-shell connection before the pins connect

*

Reference **SB4-SAT-AD1-P4-REQ-504**

[FC Applicability: ANTRACK, DATAM, HARNESS, MECHANISMS, POWER, PROP, STRUCTURE, ANTENNA]

Pyrotechnic circuit connectors shall provide for 360° shield continuity at connector side

*

Reference **SB4-SAT-AD1-P4-REQ-505**

[FC Applicability: ANTRACK, DATAM, HARNESS, MECHANISMS, POWER, PROP, STRUCTURE, ANTENNA]

Pyrotechnic circuit connectors shall provide for 360° shield continuity at bundle side without gaps (minimum 85% of optical coverage)

*

4.5 Harness requirements

Requirements in this chapter are applicable to:

- Satellite harness
- Harness of the units (i.e.: Reaction Wheel, ADPM...), except to Pcb's wires.

4.5.1 Harness definition responsibility

The subsystem internal harness definition is under system responsibility. Nevertheless, specific requirements may be submitted by the co-contractor.

The links definition between two subsystems is under the Prime responsibility.

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(AD01-P4)

4.5.2 Bundles characteristics

4.5.2.1 Bundles classification

Reference **SB4-SAT-AD1-P4-REQ-519**

[FC Applicability: HARNESS, STRUCTURE]

The spacecraft harness (excluding RF coaxial cable and waveguide) shall be divided into four classes

Class 1	Power	If all class1 (A to D) respect the notes all lines shall be assembled in one bundle. For heater power lower than 15W, common routing with TM/TC are accepted.
Class 1A	primary power lines, PPS and heaters (P>15W)	
Class 1B	secondary power lines (Camp/EPC)	The class1B shall be separated from class1A, except in of these lines are shielded.
Class 1C	Solar Array/power supply link (PCU)	
Class 1D	Batteries/power supply link (PCU) AND Safe Line	
Class 1E	Motors supply lines (BAPTA-M, SADM, APMM, Solar Array deployment motors in HKU, WDE-MW, AOCSP-MW, SEPTA M/SADP...).	All class 1 E (motors supply lines) must be shielded. Any deviation must be submitted to prime approval. SA power strain gauge (SEPTA M/SADP) shall be routed with Class 1C (these lines are only used at the beginning of the satellite flight).
Class 2	Non sensitive signals	
Class 2A	TC signals (HL, LL, valves command TVC) TM signals (Thermistors, AN, DB, DR, valves statuts TVS, TM APMM, TM Bapta/SADM)	For the class2A, when using Relay Switch Module (RDU) or MAP (PLDIU), harness gauge must be verified in order to respect harness voltage drop and input switch voltage. Maximum resistance of harness line at 80°C: with MAP, up to 6 Ohm (taken into account a double failure in the harness); with RSD up to 2,8 Ohm.
Class 2B	Others non sensitive signals.	
Class 3	Electro-Explosive Device (EED) interface signals	Electro-Explosive Device (EED) interface signals i.e. between the EED itself and the last arming or firing relay
Class 4	Sensitive signals	
Class 4A	shielded links PSSE-PSSH, OBCU-IRES, AOCSP-CSS	
Class 4B	Sensitive analog signals (other signals), Video links (TM/TC between CDMU/SMU and TTCRF RX/TX), batteries pressure, batteries cells voltage, signal from SAPT, LAPT, HAPT	Class4B shall be separated from all class with a distance minimum of 5cm except for shielded links. SA signal strain gauge shall be routed with Class 1E.
Class 4C	OBDH ans 1553 links	

Table 4: Spacecraft harness classification.

*

Reference **SB4-SAT-AD1-P4-REQ-520**

[FC Applicability: HARNESS, STRUCTURE]

Wires falling into one class shall be assembled into one bundle.

*

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Reference **SB4-SAT-AD1-P4-REQ-521**

[FC Applicability: HARNESS, STRUCTURE]

Under-classes inside class 1 shall be separated from themselves.

*

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(AD01-P4)

4.5.2.2 Bundles rules

Reference **SB4-SAT-AD1-P4-REQ-522**

[FC Applicability: HARNESS, STRUCTURE]

The routing of bundles shall respect the minimal distance shows in Figure 4.

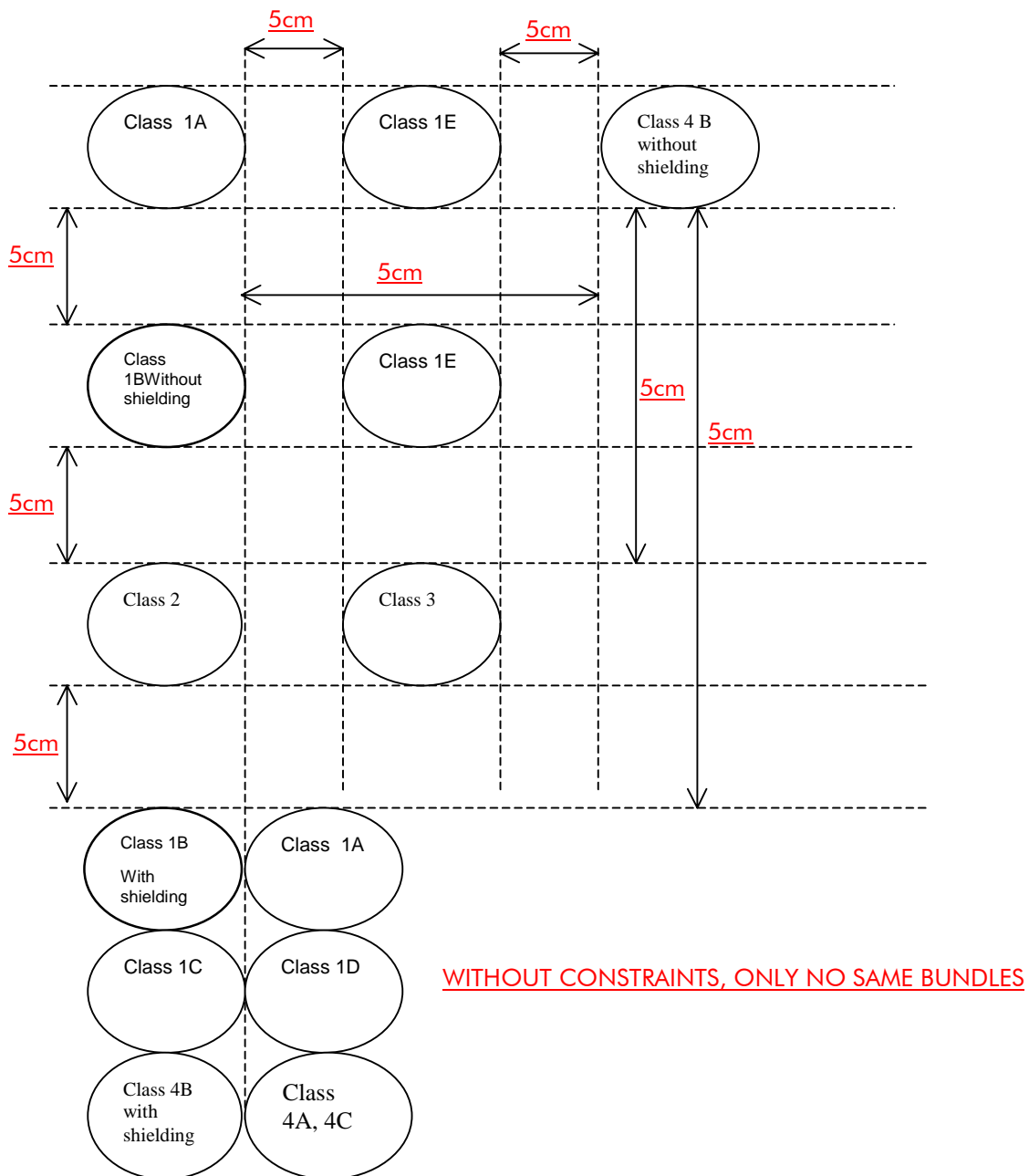


Figure 4: Routing of several bundles

*

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Reference **SB4-SAT-AD1-P4-REQ-523****[FC Applicability:** HARNESS, STRUCTURE]

The different cables and cable bundle shall be routed as close as possible to the structure (preferably at a distance less than 1 cm).

*

Reference **SB4-SAT-AD1-P4-REQ-524****[FC Applicability:** HARNESS, STRUCTURE]

All shielded lines (class 1,2 and 4) may be assembled with any other unshielded lines (without limitation) except at the terminal; at this level the different kinds of class must be separated from any other type for 150 mm length minimum upstream the terminal (see Figure 5). Between the terminal and 150mm upstream the terminal, the distance between shielded classes must be at a minimum 1 cm (except for Pyro lines class 3).

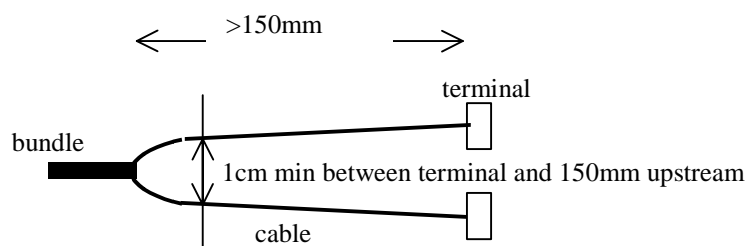


Figure 5: Class separation at the terminal

*

Reference **SB4-SAT-AD1-P4-REQ-525****[FC Applicability:** HARNESS, STRUCTURE]

Where bundles of different classes must cross each other the crossing angle shall be approximately 90 degrees.

*

Reference **SB4-SAT-AD1-P4-REQ-526****[FC Applicability:** HARNESS, STRUCTURE]

Where closer distances between categories than those shown in Figure 4 cannot be avoided, shield shall be added along the commonly routed paths or metallic barriers between adjacent bundles.

*

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Reference **SB4-SAT-AD1-P4-REQ-539**

[FC Applicability: HARNESS, STRUCTURE]

The mechanical and wiring harness layout shall be such that circuit access and ease of dismantling is provided.

*

Reference **SB4-SAT-AD1-P4-REQ-540**

[FC Applicability: HARNESS, STRUCTURE]

Routing shall enable accessibility of shielded terminations, grounded connections and allow easy connector mating.

*

Reference **SB4-SAT-AD1-P4-REQ-541**

[FC Applicability: HARNESS]

The bundle diameter shall be less than 5 cm.

*

4.5.3 Connectors

Reference **SB4-SAT-AD1-P4-REQ-509**

[FC Applicability: ALL CF (hardware)]

Pin and socket connectors shall be mechanically locked together, to prevent inadvertent disconnection.

*

Reference **SB4-SAT-AD1-P4-REQ-514**

[FC Applicability: HARNESS]

Connector pins and sockets shall be removable on the harness connectors.

*

Reference **SB4-SAT-AD1-P4-REQ-623**

[FC Applicability: HARNESS]

The shielding pigtail length shall be less than 3 cm in all cases. In case of impossibility an EMC/ESD back-shell must be added.

*

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Reference **SB4-SAT-AD1-P4-REQ-639**

[FC Applicability: ANTRACK, AOCS, HARNESS, MECHANISMS, PAYLOAD, PROP, THERMAL, ANTENNA]

All external connectors shall include connector back-shell.

The shells shall be:

- electrically conductive
 - bonded to the overall harness shield or to all the cable shields
 - connected to the connector case to provide a 360° termination around the internal cable bundle
-

*

4.5.4 Wire specifications

4.5.4.1 Wire selection

Reference **SB4-SAT-AD1-P4-REQ-619**

[FC Applicability: HARNESS]

The AWG wire shall be selected to withstand the fuse size.

*

Reference **SB4-SAT-AD1-P4-REQ-537**

[FC Applicability: HARNESS]

Copper wires smaller than AWG 28 (diameter 0.32 mm) shall not be used.

*

Reference **SB4-SAT-AD1-P4-REQ-538**

[FC Applicability: HARNESS]

Aluminium wires smaller than AWG 22 shall not be used.

*

4.5.4.2 Twisted links

Reference **SB4-SAT-AD1-P4-REQ-528**

[FC Applicability: HARNESS]

All active wire(s) shall always be twisted around its return wire, except for primary power lines (PCU/Batteries, PCU/SDIU, PCU/BCRB/Batteries), in this case the harness routing minimises the wire loop.

*

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Reference **SB4-SAT-AD1-P4-REQ-529**

[FC Applicability: HARNESS]

When several lines share the same return line, the whole bundle shall be twisted with its return.

*

4.5.4.3 Shielded links

Reference **SB4-SAT-AD1-P4-REQ-600**

[FC Applicability: HARNESS]

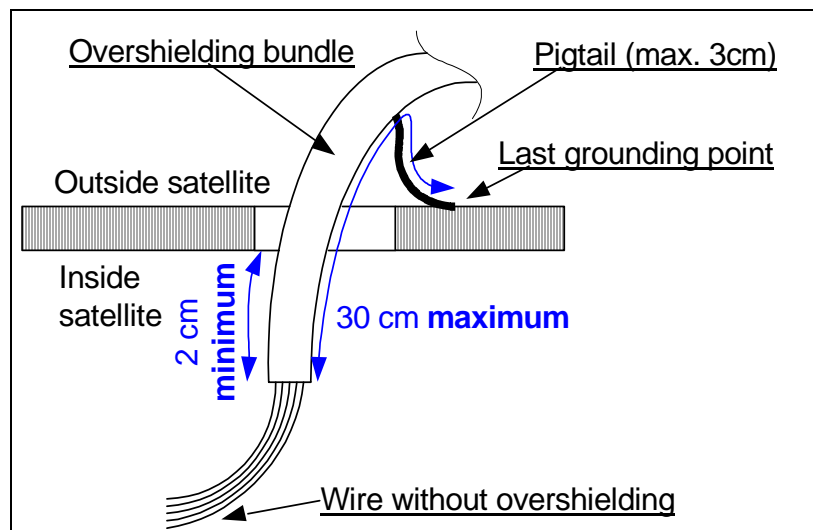
All links between outside and inside the spacecraft shall be over shielded on their external part (except for solar array).

*

Reference **SB4-SAT-AD1-P4-REQ-640**

[FC Applicability: HARNESS]

When the external overshielded wire is going inside the satellite, the overshield shall respect the distances shown in the following figure:



*

Reference **SB4-SAT-AD1-P4-REQ-641**

[FC Applicability: HARNESS]

External shields with ribbons shall be grounded to the EGRN every 40 cm maximum by bonding of 3cm (5cm maximum).

*

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Reference **SB4-SAT-AD1-P4-REQ-533**

[FC Applicability: HARNESS]

The use of shielded wires shall only occur inside the spacecraft when specified in the relevant subsystem specification.

*

Reference **SB4-SAT-AD1-P4-REQ-534**

[FC Applicability: HARNESS]

Shields shall be connected to connector housing at both ends.

*

Reference **SB4-SAT-AD1-P4-REQ-535**

[FC Applicability: HARNESS]

Each harness connector shall be able to support a grounding grid for shielding purposes.

*

Reference **SB4-SAT-AD1-P4-REQ-545**

[FC Applicability: HARNESS]

For ML16 and DS16 harness shall be shielded.

*

4.5.4.4 High voltage specific derating requirements

Reference **SB4-SAT-AD1-P4-REQ-532**

[FC Applicability: HARNESS]

For high voltage cables, the maximum ac voltage or ripple shall not exceed 5% of the dc rating.

*

4.5.4.5 Crimping of wires

Reference **SB4-SAT-AD1-P4-REQ-542**

[FC Applicability: HARNESS]

A maximum of two wires shall be crimped together at one connector contact according to qualification rules.

*

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4.5.5 Matrix harness concept

Reference **SB4-SAT-AD1-P4-REQ-205 b**

[FC Applicability: AOCS, DATAM, HARNESS, PAYLOAD, POWER, PROP, TCR]

Matrix command positive voltages shall be connected to matrix row.

*

Reference **SB4-SAT-AD1-P4-REQ-206 b**

[FC Applicability: AOCS, DATAM, HARNESS, PAYLOAD, POWER, PROP, TCR]

Matrix command return line shall be connected to matrix column.

*

Reference **SB4-SAT-AD1-P4-REQ-208 b**

[FC Applicability: AOCS, DATAM, HARNESS, PAYLOAD, POWER, PROP, TCR]

The basis definition of the matrix harness shall be unshielded lines.

*

Reference **SB4-SAT-AD1-P4-REQ-209 c**

[FC Applicability: AOCS, DATAM, HARNESS, PAYLOAD, POWER, PROP, TCR]

Each row or column line coming from the nominal function shall be routed in daisy chain to several receivers before returning back to the redundant function.

*

4.5.6 Specific requirements for pyro circuits

Reference **SB4-SAT-AD1-P4-REQ-536**

[FC Applicability: ANTRACK, DATAM, HARNESS, MECHANISMS, POWER, PROP, ANTENNA]

For pyro, shielded twisted pairs shall be used.

*

Reference **SB4-SAT-AD1-P4-REQ-543**

[FC Applicability: ANTRACK, DATAM, HARNESS, MECHANISMS, POWER, PROP, ANTENNA]

For pyro lines, only one wire per contact shall be used.

*

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5. POWER SUBSYSTEM INTERFACES REQUIREMENTS

5.1 Power Bus Definition

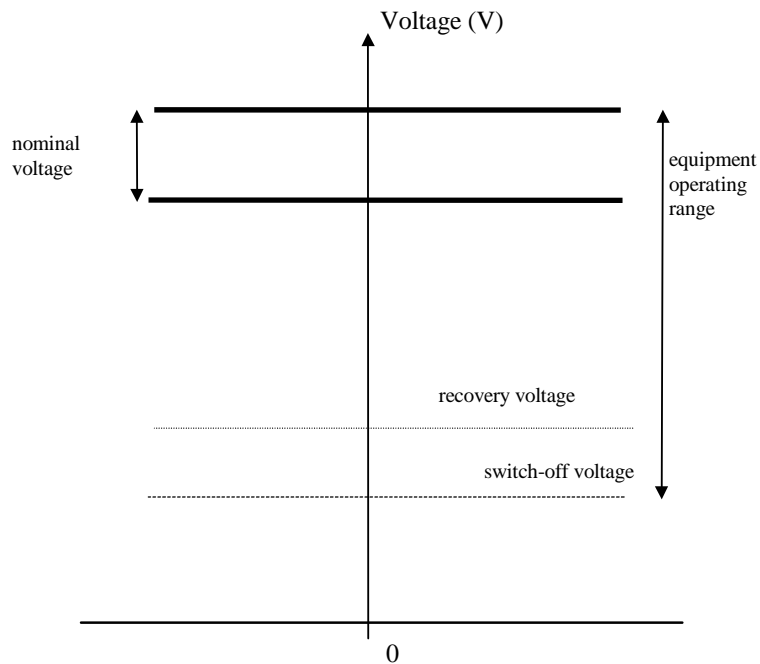


Figure 6: Equipment operating range.

5.2 Power bus nominal voltage

The power conditioning subsystem provides one regulated 100 V power bus, which is distributed to the spacecraft users.

Reference **SB4-SAT-AD1-P4-REQ-131 a**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, PAYLOAD, POWER, PROP, TCR, THERMAL]

At the loaded input connector of user, the nominal bus voltage is defined as follows :

Maximal DC bus voltage : 102V

Minimal DC bus voltage : 98V

*

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5.3 Power bus operational voltage

Reference **SB4-SAT-AD1-P4-REQ-133 c**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

The DC/DC of spacecraft equipment shall be able to operate according to the following voltage.

Function	DC MIN VOLTAGE (V)
High Power Payloads Units (> 20W)	95
PYRO Pcb / FSMP	95
SADP/S4DSAP	70
Other Platform Sub-systems	70
Low Power Payloads Units (< 20W)	95
AOCS-UPS	70
SMU / TTC RF (TX + RX) - Ciphering Units	70

Table 5: Regulated 100V Power bus operating voltage limits

*

5.4 Equipment operating requirements

Reference **SB4-SAT-AD1-P4-REQ-134 b**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Units shall not be affected **in their nominal performances** if the power bus voltage is under their automatic switch-off voltage level during less than 10 μ s.

*

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Reference **SB4-SAT-AD1-P4-REQ-135 c**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Units shall be automatically switched off if the power bus voltage is under their automatic switch-off voltage level during more than 10 μ s

Function	AUTOMATIC Switch-Off Voltage (V)	AUTOMATIC RECOVERY	RECOVERY VOLTAGE(V)
High Power Payload Units (> 20 W)	94 \pm 1	NO	\geq 95
PYRO Pcb / FSMP	94 \pm 1	NO	\geq 95
SADP/S4DSAP/PROP/CVICP	70	NO	72 \pm 1
Other Platform Sub-Systems / Pcb	70	NO	72 \pm 1
Low Power Payload Units (< 20W)	< 95 or	NO/YES	\geq 95
	No automatic Switch-Off voltage	YES	\geq 95
AOCS-UPS Units	70	NO	72 \pm 1
SMU-TTC RF (RX+TX) - CIPHERING Units	< 70	YES	72 \pm 1

Table 6: Regulated 100V, Equipment operating requirements

*

5.5 Distribution requirements

The main power bus distribution is based on a single point failure free concept at the distribution point (no failure of a part or insulation can cause the loss of the power bus).

Reference **SB4-SAT-AD1-P4-REQ-139 a**

[FC Applicability: DATAM, POWER, PROP]

The main bus protection shall be either by current limiting device or by fuses, combined with double insulation between the power distribution point and the limiting device.

*

Reference **SB4-SAT-AD1-P4-REQ-145 b**

[FC Applicability: AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

The unit input ON/OFF relay contact shall be sized to withstand twice the current peak value corresponding to the long peak power demand.

*

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5.5.1 Double insulation requirements

Reference **SB4-SAT-AD1-P4-REQ-616**

[FC Applicability: DATAM, HARNESS, POWER, PROP, STRUCTURE]

Double insulation shall be implemented by at least two independent layers of insulating materials

*

Reference **SB4-SAT-AD1-P4-REQ-464**

[FC Applicability: DATAM, HARNESS, POWER, PROP, STRUCTURE]

All power lines located between power generation (Batteries or solar array or umbilical) and circuit protections installed inside the conditioning and distribution boxes (BCRB, PCU and SDIU) shall present a double insulation.

*

Reference **SB4-SAT-AD1-P4-REQ-617**

[FC Applicability: DATAM, HARNESS, POWER, PROP, STRUCTURE]

All power lines located between power generation (Batteries or solar array or umbilical) and circuit protections installed inside the high power units (PPU ...) shall present a double insulation.

*

Reference **SB4-SAT-AD1-P4-REQ-618**

[FC Applicability: DATAM, HARNESS, POWER]

Battery cells voltage monitoring lines and power pyro lines shall present a double insulation.

*

Reference **SB4-SAT-AD1-P4-REQ-465**

[FC Applicability: DATAM, HARNESS, POWER, PROP]

All power lines inside power units (PCU, PPU, BCRB, Battery, Solar Array, SADM, SDIU) shall be double insulated.

*

5.5.2 Fuses

Reference **SB4-SAT-AD1-P4-REQ-146 c**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, PAYLOAD, POWER, PROP, TCR, THERMAL]

Fuses shall not be implemented inside equipments excepted distribution units (PLDIU, PFDIU) and batteries.

*

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Reference **SB4-SAT-AD1-P4-REQ-147 b**

[FC Applicability: DATAM, POWER, PROP]

The fuse rating shall not exceed 15A

*

Reference **SB4-SAT-AD1-P4-REQ-148 c**

[FC Applicability: DATAM, POWER, PROP]

In case of use of wire fuses, they shall be redounded. The redundant fuse shall be used with a serial resistance. The value of this resistance shall be such that at least 75 % of the operational current pass through the nominal fuse.

*

Reference **SB4-SAT-AD1-P4-REQ-149 c**

[FC Applicability: DATAM, POWER, PROP]

For 100V regulated power bus, the use of fuse rating less than 1A is prohibited.

*

5.5.3 High power units

Reference **SB4-SAT-AD1-P4-REQ-603**

[FC Applicability: PROP]

For high power units (>500W), input protection shall be implemented and it shall limit the maximum power consumption to 2 times the mean power demand.

*

5.5.4 Primary Power Line fluctuation

Reference **SB4-SAT-AD1-P4-REQ-150 b**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, PAYLOAD, POWER, PROP, TCR, THERMAL]

All users of these power lines shall safely survive any standing or fluctuation voltage in the full range 0V to 102 V and recover nominal operating performances with bus voltage rise time to reach its nominal range of $dV/dt < 1V/\mu\text{sec}$.

*

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Reference **SB4-SAT-AD1-P4-REQ-152 b****[FC Applicability:** ANTRACK, AOCS, DATAM, HARNESS, PAYLOAD, POWER, PROP, TCR, THERMAL]

During power bus voltage fluctuations tests, the unit under test shall be initially in a configuration which maximise the interference (ex : unit in ON state).

Units are not required to meet performance parameters under these conditions but must safely survive without any over-stressing or damage and must recover all their nominal operating performance.

*

Reference **SB4-SAT-AD1-P4-REQ-155 b****[FC Applicability:** ANTRACK, AOCS, DATAM, HARNESS, PAYLOAD, POWER, PROP, TCR, THERMAL]

Low speed power fluctuation (integration and hardware verification).

The test shall be performed when the bus voltage starts from 0V to nominal voltage (100V) with $20\text{V/ms} < dV/dt < 10\text{ V/s}$ (see figure below). During such event, the bus voltage shall be within hatched areas.

The unit input current shall be recorded and included in test report.

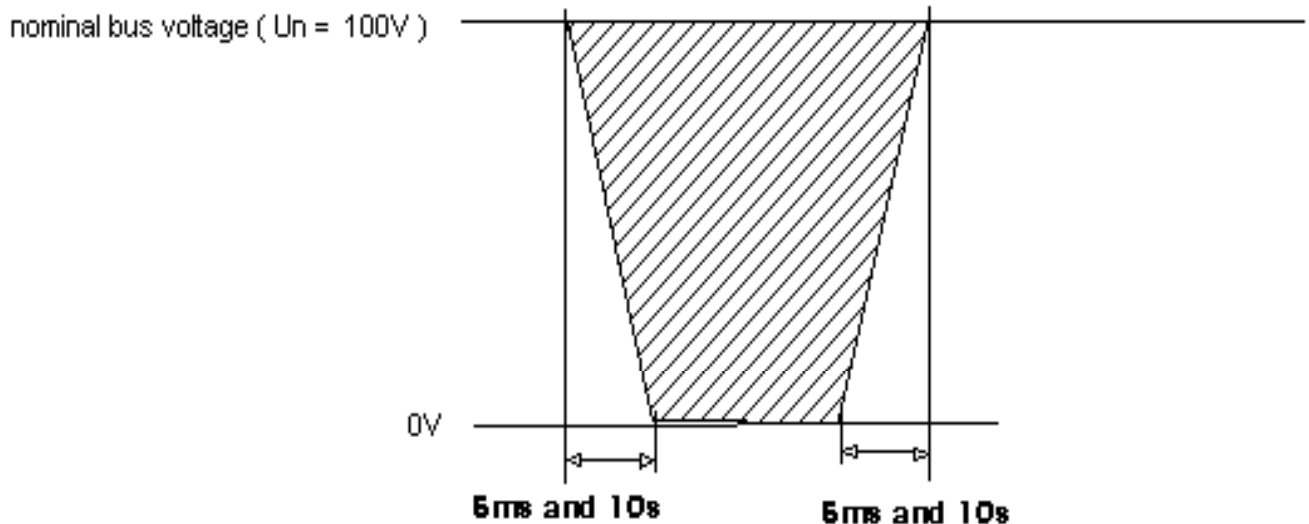


Figure 7: Low speed power bus fluctuation (low dV/dt)

*

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5.6 Mean power demand

Reference **SB4-SAT-AD1-P4-REQ-161 b**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, PAYLOAD, POWER, PROP, TCR, THERMAL]

The mean power demand shall be measured in voltage nominal conditions (see chapter "Power bus nominal voltage") during a period of 5 minutes

*

5.7 Peak power demand

Reference **SB4-SAT-AD1-P4-REQ-162 b**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, PAYLOAD, POWER, PROP, TCR, THERMAL]

The long peak power demand shall be measured in voltage nominal conditions (see chapter "Power bus nominal voltage") at worst functional case of equipment (wheel spin up, telecomand generation, etc)

*

5.8 Load current limitation

Reference **SB4-SAT-AD1-P4-REQ-164 b**

[FC Applicability: ANTRACK, AOCS, DATAM, HARNESS, PAYLOAD, POWER, PROP, TCR, THERMAL]

The maximum current drawn by the unit from the supply lines in case of failure, shall be limited to 1.5 times the current peak value corresponding to the long peak power demand (except during the unit ON/OFF sequence)

*

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6. SIGNAL LINE INTERFACE REQUIREMENTS

Reference **SB4-SAT-AD1-P4-REQ-442**

[FC Applicability: ALL CF (hardware)]

Signal interface shall use a return by wire concept.

*

6.1 Conventions

- Time duration : The time duration is defined at 50% of the measured full amplitude.

- Signal rise and fall times : The rise and fall times of a signal are defined as the time between 10% and 90% of the measured voltage swing.

- Measurements : Measurements are made at the unit (or harness) connector level.

6.2 Command interface

6.2.1 Low Level and High Level Commands (LLC & HLC)

HLC and LLC commands are generated through matrix row and column drivers. One row pulled up to a positive voltage and one column pulled down to the secondary 0v in order to command only the device at the node of the activated row and column.

The command signal is a differential voltage pulse distributed to the user for :

- relay driving or general logic control application with low level commands
- payload waveguide relay driving with high level commands

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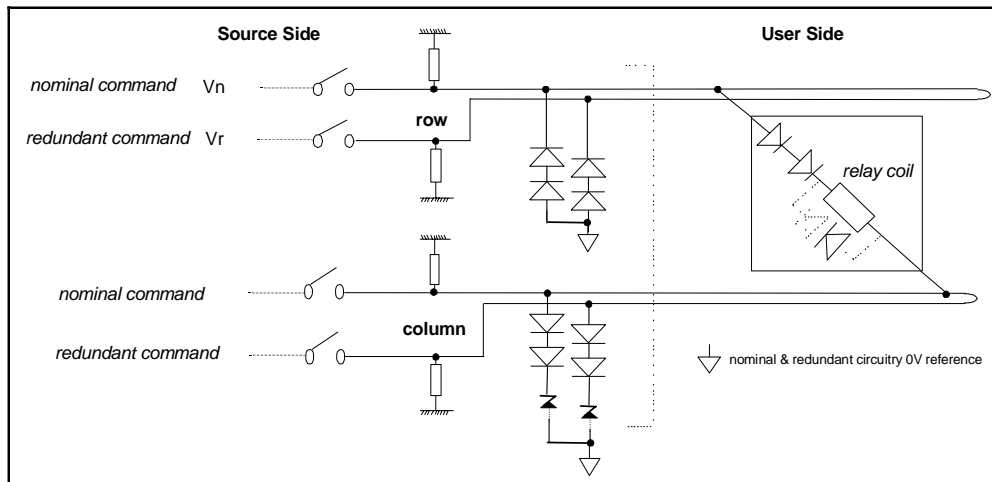
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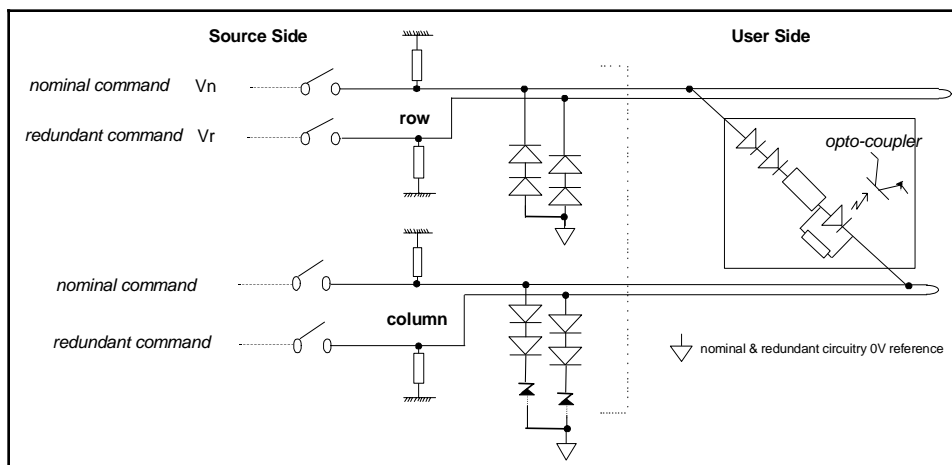
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6.2.1.1 Matrix command schematics

Relay interface



Opto coupler interface



6.2.1.2 Source side requirements

Reference **SB4-SAT-AD1-P4-REQ-182 b**

[FC Applicability: DATAM]

The command lines (rows and columns) shall be double insulated inside the equipment (except external side of I/O connectors) and no failure propagation shall occur between rows, between columns or between row and column.

*

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Reference **SB4-SAT-AD1-P4-REQ-184 a**

[FC Applicability: DATAM]

matrix command (LLC and HLC) outputs shall be protected by a current limiting device

*

Reference **SB4-SAT-AD1-P4-REQ-191 b**

[FC Applicability: DATAM]

For matrix MAP, the pulse duration shall be programmed between 15ms to 1s.

*

Reference **SB4-SAT-AD1-P4-REQ-621**

[FC Applicability: DATAM]

For Short LLC, TI shall be between 3ms and 7ms ($T_d < 40\text{ms}$).

*

Reference **SB4-SAT-AD1-P4-REQ-622**

[FC Applicability: DATAM]

For Long HLC, TI shall be between 110 ms and 210ms ($T_d > 530\text{ms}$).

*

Reference **SB4-SAT-AD1-P4-REQ-192 a**

[FC Applicability: DATAM]

row and column switches shall be closed after the pulse during the demagnetisation of the relay coil.

*

Reference **SB4-SAT-AD1-P4-REQ-193 a**

[FC Applicability: DATAM]

only one command shall be activated at the same time ; simultaneously commands are not allowed.

*

Reference **SB4-SAT-AD1-P4-REQ-194 a**

[FC Applicability: DATAM]

Only one row and one column shall be activated per command and per matrix

*

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6.2.1.3 User side requirements

Reference **SB4-SAT-AD1-P4-REQ-195 a**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

all telecommand users shall provide two diodes in series with the commanded device at any matrix node.

*

Reference **SB4-SAT-AD1-P4-REQ-196 c**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

For user interface with relay coil, two serial free wheel diodes shall be implemented in parallel with the relay coil at user side.

When the time constant of relay (L/R) is inferior to 1ms for LLC or 5ms for HLC, the diodes could be non implemented in the receiver interface.

*

Reference **SB4-SAT-AD1-P4-REQ-637**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

L/R time constant of the relay/RF switch shall be lower than 15 ms

*

Reference **SB4-SAT-AD1-P4-REQ-201 b**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

The user shall not impose any potential or grounding reference on any row or column.

*

6.2.1.3.1 Failures management

Reference **SB4-SAT-AD1-P4-REQ-202 b**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

The user interface design shall permit the unit power on/off without damage when the electrical interfaces are not fully connected.

*

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Reference **SB4-SAT-AD1-P4-REQ-235 b**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Unpowered equipments shall not be damaged and degraded in their performances when command signals are applied.

*

Reference **SB4-SAT-AD1-P4-REQ-236 b**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Each input shall be sufficiently decoupled (fault propagation) from each input/ output :

- normal condition (powered equipment, without failure)
- unpowered equipment
- unpowered equipment and with any one failure.

*

Reference **SB4-SAT-AD1-P4-REQ-237 b**

[FC Applicability: DATAM]

Each command source failure shall not cause the loss of more than 1 command.

*

Reference **SB4-SAT-AD1-P4-REQ-630**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Any short circuit of one row (+ TC at user side) or (-exclusive) one column (- TC at user side) to the structure shall not cause the loss of any TC.

*

6.2.1.4 Command signal characteristics

6.2.1.4.1 Command signal waveform

Signal duration (Td): time between crossing points of rise and fall time to 50% of the full amplitude

Signal rise/fall time (Tr ; Tf): maximum between 10% and 90% of the nominal voltage swing

Delay between 2 signals: time between the voltage crossing point at 50% of the full amplitude level

Closed time Tc: Command duration with switch closed

Free wheeling time: Duration between end of pulse and switch opening

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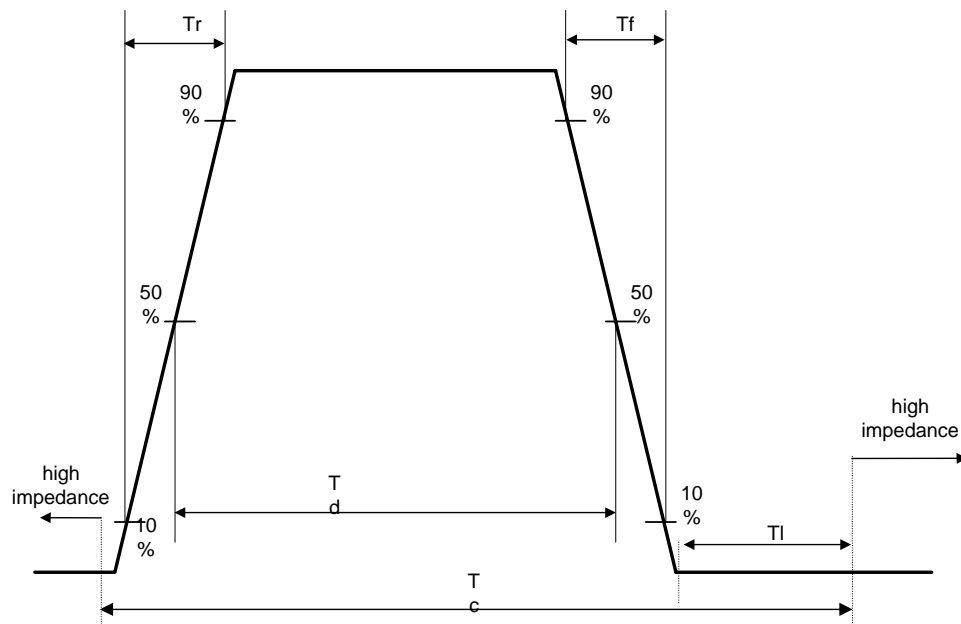


Figure 8: Matrix command signal waveform

6.2.1.4.2 LLC electrical parameters

Reference **SB4-SAT-AD1-P4-REQ-238 c**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

The LLC commands shall comply with these LLC electrical characteristics :

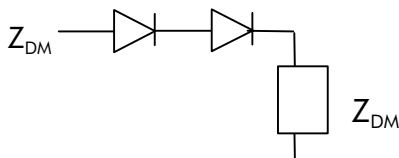
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Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
A	TYPE			
Req-1	Output type	Differential		for matrix drivers organisation
Req-2	Input type		Differential	
B	VOLTAGE			
Req-1	DM low « 0 » voltage	-29V / +4V	-29V / +4V	User shall also comply with Req-H1
Req-2	DM high « 1 » voltage	26 V (+3V / -2V)	26 V (+3V / -5V)	
Req-3	Threshold		$11V \leq V_T \leq 19V$	
Req-4	CM Permanent Fault Voltage Emission	Not allowed	Not allowed	DM = 0
Req-5	DM Permanent Fault Voltage	Not allowed	Not allowed	
Req-6	DM Transient Fault Voltage Emission	-63 V/1 s +33V/80ms	$\pm 2V / 25 \text{ ms}$	
Req-7	DM Transient Fault Voltage Tolerance	-63 V/1 s +33V/80ms	-63 V/1 s +33V/80ms	
C	CURRENT			
Req-1	Driving capability	> 180 mA		
Req-2	Load current		$2,2 \text{ mA} \leq \text{load} \leq 180 \text{ mA}$	Considering the whole DM high level voltage range
Req-3	Overcurrent	$\leq 400 \text{ mA}$		
Req-4	short circuit between 2 outputs	Withstand		
D	IMPEDANCE (Differential impedance excluding the two serial diodes (see figure NOTE 1))			
Req-1	Impedance under DM low voltage		$R \leq 9k\Omega$	
Req-2	Impedance during free wheeling time (TI)	$< 10\Omega$		Excluding diodes inside matrix source

NOTE 1

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Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
E	TIME			
Req-1	Rise Time (Tr)	$50 \mu s \leq Tr \leq 500 \mu s$		Matrix output loaded by a user impedance in accordance with Code C and D.
Req-2	Fall Time (Tf)	$1 \mu s \leq Tf \leq 600 \mu s$		Matrix output loaded by a user impedance in accordance with Code C and D.
Req-3	« On » duration (Td)	$40 \text{ ms} \leq Td \leq 50 \text{ ms}$		
Req-4	Closed duration (TI)	$20 \text{ ms} \leq TI \leq 30 \text{ ms}$		Matrix requirement
Req-5	Spurious Command		$Td \leq 0,1 \text{ ms}$	Td = time duration
F	MATRIX COMMAND GROUNDING AND ISOLATION ⁽²⁾			
Req-1	Between matrix ground and Chassis: R equivalent	$113 \text{ K}\Omega < R < 2 \text{ M}\Omega$	$> 10 \text{ M}\Omega$	
Req-2	between one row or one column and Chassis: Equivalent Capacitance (In // R equivalent)	$C_{CM} < 1 \text{ nF}$	$C_{CM} < 500 \text{ pF}^{(3)}$	⁽³⁾ Around 10 KHz
Req-3	Between matrix ground and Chassis: C equivalent (In // R equivalent)	$C_{CM} < 34 \text{ nF}^{(3)}$ (for SMU and PFDIU) $C_{CM} < 50 \text{ nF}^{(3)}$ (for PLDIU)		⁽³⁾ Around 10 KHz
Req-4	between row / column lines and relay or opto-coupler at user side		galvanic isolation	use of relay coil or opto-coupler at user side
H	SPECIFIC REQUIREMENT			
Req-1	Transient low "0" voltage	N/A	The input LLC shall not be activated with the following setup hereafter ⁽⁴⁾	U=29V with tr 50 to 500 μs

⁽²⁾ Primary and users secondary grounds shall be considered connected to chassis for measurements

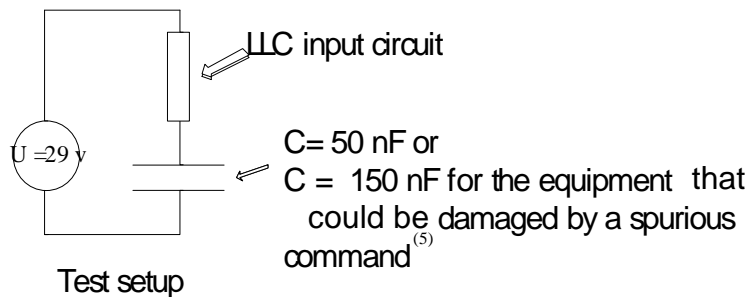
Note: CM: Common mode / DM: Differential Mode

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Test setup⁽⁴⁾



⁽⁵⁾ 150 nF is only applicable to Payload units.

Table 7: LLC electrical characteristics

*

Reference **SB4-SAT-AD1-P4-REQ-587**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

For LLC a single return shall be allowed for a maximum of 4 LLC commands.

*

Reference **SB4-SAT-AD1-P4-REQ-588**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Each return shall be electrical insulated from other return.

*

6.2.1.4.3 HLC electrical parameters

Reference **SB4-SAT-AD1-P4-REQ-239 c**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

The HLC commands shall comply with these HLC electrical characteristics :

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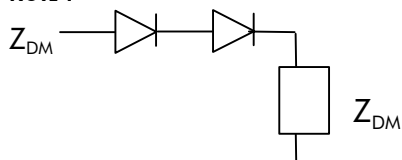
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Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
A	TYPE			
Req-1	Output type	Differential		for matrix drivers organisation
Req-2	Input type		Differential	
B	VOLTAGE			
Req-1	DM low « 0 » voltage	-29 V / +4V	-29 V / +4V	User shall also comply with Req-H1
Req-2	DM high « 1 » voltage	26 V (+3V / - 3V)	26 V (+3V/- 5.5V)	
Req-3	Threshold		$11V \leq V_T \leq 20,5V$	
Req-4	CM Permanent Fault Voltage Emission	Not allowed	Not allowed	DM=0
Req-5	DM Transient Fault Voltage Emission	-63 V / 1s +33V/1s	$\pm 2 V / 125 ms$	
Req-6	DM Transient Fault Voltage Tolerance	-63 V / 1s +33V/1s	-63 V / 1s +33V/1s	
C	CURRENT			
Req-1	Driving capability	> 500 mA		
Req-2	Load current		$22 mA \leq load \leq 500 mA$	Considering the whole DM high level voltage range
Req-3	Overcurrent	$\leq 1 A$		
D	IMPEDANCE (Differential impedance excluding the two serial diodes (see figure NOTE 1))			
Req-1	Impedance under DM low voltage		$R \leq 9k\Omega$	
Req-2	Impedance during free wheeling time (TI)	$< 10\Omega$		Excluding diodes inside matrix source

NOTE 1



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Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
E	TIME			
Req-1	Rise Time (Tr)	$50 \mu s \leq Tr \leq 500 \mu s$		Matrix output loaded by a user impedance in accordance with Code C and D.
Req-2	Fall Time (Tf)	$1 \mu s \leq Tf \leq 600 \mu s$		Matrix output loaded by a user impedance in accordance with Code C and D.
Req-3	« On » duration (Td)	$500ms \leq Td \leq 530ms$		
Req-4	Closed duration (TI)	$110ms \leq TI \leq 140ms$		Matrix requirement
Req-5	Spurious Command		$Td \leq 0,1 \text{ ms}$	Td = time duration
F	MATRIX COMMAND GROUNDING AND ISOLATION ⁽²⁾			
Req-1	Between matrix ground and Chassis: R equivalent	$113 \text{ K}\Omega < R < 2 \text{ M}\Omega$	$> 10 \text{ M}\Omega$	
Req-2	between one row or one column and Chassis: Equivalent Capacitance (In // R equivalent)	$C_{CM} < 1nF$	$C_{CM} < 500 \text{ pF}^{(3)}$	⁽³⁾ Around 10 KHz
Req-3	Between matrix ground and Chassis: C equivalent (In // R equivalent)	$C_{CM} < 50 \text{ nF}^{(3)}$ (for PLDIU) ⁽¹⁾		⁽³⁾ Around 10 KHz
Req-4	between row / column lines and relay or opto-coupler at user side		galvanic isolation	use of relay coil or opto-coupler at user side
H	SPECIFIC REQUIREMENT			
Req-1	Transient low "0" voltage	N/A	The input LLC shall not be activated with the following setup hereafter ⁽⁴⁾	$U = 29V$ with tr 50 to $500 \mu s$

⁽²⁾ Primary and users secondary grounds shall be considered connected to chassis for measurements

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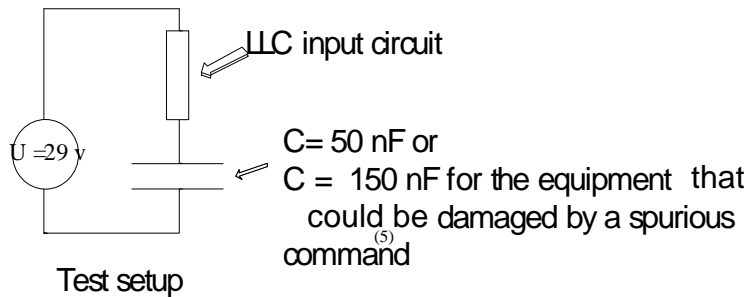
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Note: CM: Common mode / DM: Differential Mode

Test setup⁽⁴⁾



⁽⁵⁾ 150 nF is only applicable to Payload units.

Table 8: HLC electrical characteristics

*

Reference **SB4-SAT-AD1-P4-REQ-589**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Each return shall be electrical insulated from others returns.

*

Reference **SB4-SAT-AD1-P4-REQ-590**

[FC Applicability: ANTRACK, AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

For HLC a single return shall be allowed for a maximum of 4 HLC commands.

*

6.2.2 SBDL Electrical Characteristics

Reference **SB4-SAT-AD1-P4-REQ-626**

[FC Applicability: AOCS, DATAM, TCR]

The following electrical characteristics shall be applied to a "point to point" connection. The cross strap of two redundant transmitters (MASTER) inside the unit (the same Pcb) is allowed.

*

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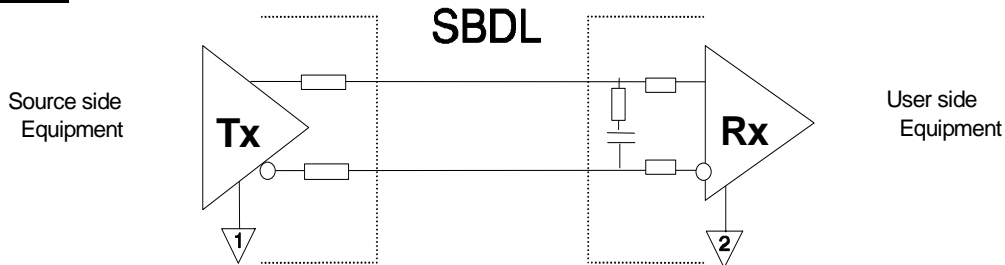
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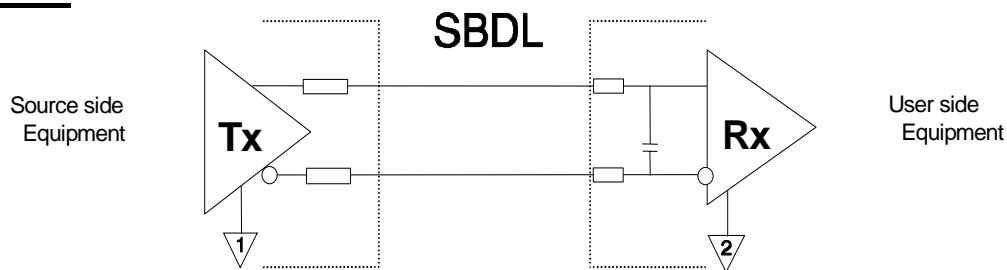
(AD01-P4)

SBDL electrical interface is according to one of these schematics (Option1 and Option2):

OPTION 1



OPTION 2



Reference **SB4-SAT-AD1-P4-REQ-241 b**

[FC Applicability: AOCS, DATAM, TCR]

SBDL serial link differential signals shall be identified as "non-inverted" and "inverted line".

*

Reference **SB4-SAT-AD1-P4-REQ-559**

[FC Applicability: AOCS, DATAM, TCR]

The status of the signal shall be defined as true (logical « 1 ») when the non-inverted line has a positive voltage level w.r.t. the inverted line, i.e. when the non inverted line is at a high voltage level and the inverted line is at a low voltage level.

*

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Reference **SB4-SAT-AD1-P4-REQ-560**

[FC Applicability: AOCS, DATAM, TCR]

The status of the signal shall be defined as false (logical « 0 ») when the non-inverted line has a negative voltage with respect to the inverted line, i.e. when the non-inverted line is at a low level and the inverted line is at a high level.

*

Reference **SB4-SAT-AD1-P4-REQ-627**

[FC Applicability: AOCS, DATAM, TCR]

ML16 clock and address receiver internal state shall not change in case of:

- logical "1" state transition to OFF bus state transition
- OFF bus state transition to logical "1" state.

*

Reference **SB4-SAT-AD1-P4-REQ-243 c**

[FC Applicability: AOCS, DATAM, TCR]

The SBDL interfaces shall comply with the following characteristics:

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Code	PARAMETERS	SOURCE SIDE (transmitter)	USER SIDE (receiver)	COMMENT
A	TYPE			
Req-1	Output type	Differential driver or balanced driver		Differential driver required for ML16 drivers
Req-2	Input type		Differential	
B	VOLTAGE			
Req-1	Low level output voltage (VOL)	0V to 0.5V		D-Req4 (common mode)
Req-2	High level output voltage (VOH)	4 V to 5.5V		D-Req4 (common mode)
Req-3	Low level differential output voltage (logical 0)	-5.5 V to -3.5 V	See (1)	D-Req5
Req-4	High level differential output voltage (logical 1)	3.5 V to 5.5 V	See (1)	D-Req5
Req-5	Logical « 0 » differential threshold		-1V min	
Req-6	Logical « 1 » differential threshold		+1V max	
Req-7	CM Permanent Fault Voltage Emission	-0.5V to +7V		
Req-8	CM Permanent Fault Voltage Emission		-0.5V to +7V	through 2K Ω
Req-9	Overvoltage Tolerance (CM)	-7V to +12V		through 2K Ω
Req-10	Overvoltage Tolerance (CM)		-7V to +12V	
C	CURRENT			
Req-1	Current capability	20mA min. 100mA max.		Differential short circuit
D	IMPEDANCE			
Req-1	Power on differential Impedance	120 $\Omega \pm 10\%$		Serial resistor required
Req-2	Power off differential Impedance	4 K Ω min.		
Req-3	AC differential Impedance		120 Ω in series with 100 pF to 1nF max.	Option 1
Req-4	AC differential Impedance		2 x 2.2 K Ω min with 10 pF min. in parallel	Option 2 (Max. capacitor value is limited by propagation time)
Req-5	DC in line series resistor		2.2 K Ω min.	the value is related to each receiver input
Req-6	DC differential Impedance		10 K Ω min.	

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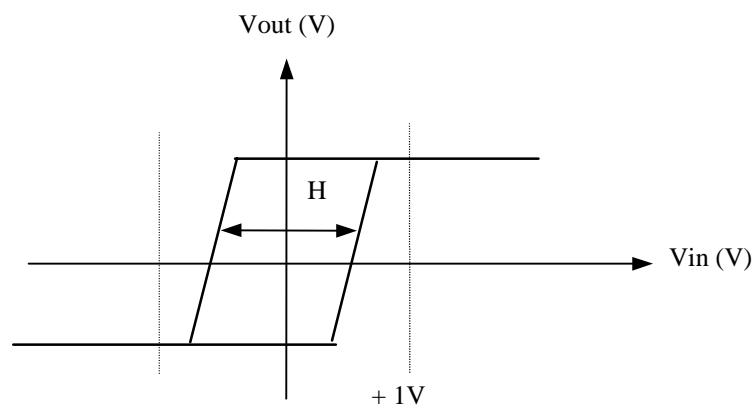
(AD01-P4)

Code	PARAMETERS	SOURCE SIDE (transmitter)	USER SIDE (receiver)	COMMENT
E	TIME			
Req-1	Rise Time (Tr)	$10 \text{ ns} \leq Tr \leq 100 \text{ ns}$		Measured on 120Ω with 50pF in parallel. Only applicable to ML16/DS16
Req-2	Fall Time (Tf)	$10 \text{ ns} \leq Tf \leq 100 \text{ ns}$		Measured on 120Ω with 50pF in parallel Only applicable to ML16/DS16
F	GROUNDING AND ISOLATION			
Req-1	from Secondary Ground (0Vs)	Circuit is referenced to 0Vs	Circuit is referenced to 0Vs	
Req-2	from Primary Ground	Isolated ($> 1\text{M}\Omega // 50\text{nF}$)	Isolated ($> 1\text{M}\Omega // 50\text{nF}$)	
Req-3	from chassis	Connected	Connected	

Table 9: SBDL characteristics

(1) Two solutions are acceptable for the receiver :

*use a classical differential receiver with the following characteristics



- The hysteresis H has to be greater than 0.8V

- The high level threshold has to be under 1V and the low level threshold has to be above -1V (differential measure).

* use the differential line receiver **HS-26C(T)32MS** specially designed for such applications.

*

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6.2.3 Memory Load Command (ML16)

6.2.3.1 Command Definition

The purpose of the memory load command (or 16-bit serial load command) interface is to transfer a 16-bit data word, in serial form, from a Master toward a Slave.

The interface consists of clock, address and data signals and use SBDL interface. The three signals are sent by the Master (Source side) to the Slave (User side).

The following notation is used:

- ML16_ADDRESS: ML16 address signal
- CLOCK: ML16 and DS16 common clock signal
- ML16_DATA: ML16 data signal

Reference **SB4-SAT-AD1-P4-REQ-548**

[FC Applicability: AOCS, DATAM]

Outside the data transfer period, ML Address & ML/DS Clock shall be in logical « 1 » state.

*

Reference **SB4-SAT-AD1-P4-REQ-550**

[FC Applicability: AOCS, DATAM]

One dedicated address line shall be provided to each ML16 user.

*

Reference **SB4-SAT-AD1-P4-REQ-551**

[FC Applicability: AOCS, DATAM]

One clock signal shall be provided to each user, for telecommand and telemetry.

*

Reference **SB4-SAT-AD1-P4-REQ-552**

[FC Applicability: AOCS, DATAM]

The data shall be valid only when the address line is active (level "0").

*

Reference **SB4-SAT-AD1-P4-REQ-553**

[FC Applicability: AOCS, DATAM]

For each data transfer, 16 clock pulses shall be generated on the clock line.

*

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Reference **SB4-SAT-AD1-P4-REQ-240 b**

[FC Applicability: AOCS, DATAM]

The Master shall shift the data on the rising edge.

*

Reference **SB4-SAT-AD1-P4-REQ-628**

[FC Applicability: AOCS, DATAM]

The Slave shall acquire the data on the falling edge.

*

Reference **SB4-SAT-AD1-P4-REQ-554**

[FC Applicability: AOCS, DATAM]

One data line shall be provided to each ML16 user.

*

Reference **SB4-SAT-AD1-P4-REQ-555**

[FC Applicability: AOCS, DATAM]

The data shall be a 16-bit word code.

*

Reference **SB4-SAT-AD1-P4-REQ-557**

[FC Applicability: AOCS, DATAM]

The data word shall be clocked out with the MSB first (bit 0)

*

Reference **SB4-SAT-AD1-P4-REQ-242 b**

[FC Applicability: AOCS, DATAM]

The ML16 commands shall comply with the SBDL electrical characteristics (See chapter "SBDL Electrical Characteristics")

*

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6.2.3.2 Memory Load Command timing

Reference **SB4-SAT-AD1-P4-REQ-561**

[FC Applicability: AOCS, DATAM]

The Memory Load Command shall respect the following timing:

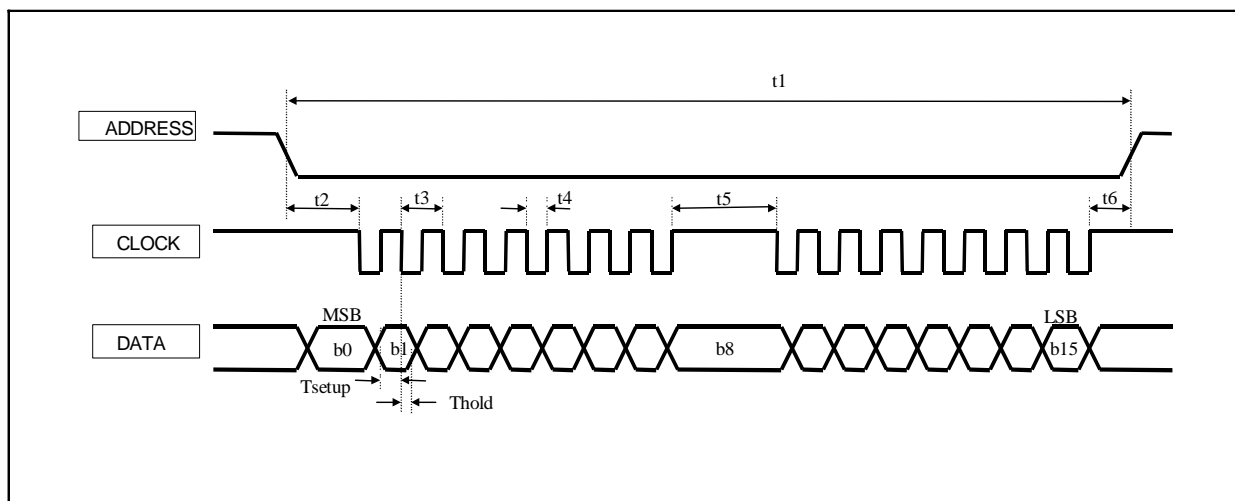


Figure 9: Memory load command signal waveform diagram

TIMING			
		MASTER	SLAVE
t	Reference time	$t=0,954\mu s \pm 5\%$	$t=0,954\mu s \pm 5\%$
t1	Address active state duration	125t max.	125t max.
t2	Address to clock delay	$28t \pm t$	27t min.
t3	Clock period	$4t \pm 0.1t$	$4t \pm 0.1t$
t4	Active to inactive edge of clock delay (Half Clock period)	$2t \pm 0.3t$	$2t \pm 0.5t$
t5	Middle frame gap	1.8t min. 36t max.	1.5t min. 37t max.
t6	Clock rising to end of address	1.8t min.	1.5t min.
Tcc	Command to command delay	3.8t min.	3.5t min.
Tsetup	Data valid setup time to clock falling edge	1.5t min.	0.5t min.
Thold	Clock falling edge to data change	1.5t min.	0.5t min.

Table 10: Memory load command timing

*

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Reference **SB4-SAT-AD1-P4-REQ-604**

[FC Applicability: AOCS, DATAM]

All equipment sequencing constraints differing from the following table shall be approved by the Prime and indicated in the equipment IDS.

		Master	Slave
Command to acquisition delay	Tca	3.8t min	3.5t min
Acquisition to command delay	Tac	3.8t min	3.5t min

*

6.3 Telemetry interface

6.3.1 Telemetry channel types

The telemetry channel types are :

- a. Analog Channel (AN)
- b. Digital Bi Level Channels (DB)
- c. Digital relay channels (DR)
- d. Digital Serial Channel 16-bit (DS16)
- e. Thermistors Power Supply and Conditioning (TH)

6.3.2 Analog channels

6.3.2.1 Analog channels definition

For ADSP users the analog TM is coded in 12 bits.

For unit including BBC/RUBI device, the analog TM is coded in 10 bits.

The system accuracy of the analog channels is better than ± 1 % of full scale.

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6.3.2.2 Analog channels accuracy

Reference **SB4-SAT-AD1-P4-REQ-244 b**

[FC Applicability: AOCS, DATAM, POWER]

The accuracy of the analog channel signal conditioning in the source shall be as specified in the corresponding subsystem specification but shall be limited to ± 0.5 % of full scale.

*

Reference **SB4-SAT-AD1-P4-REQ-613**

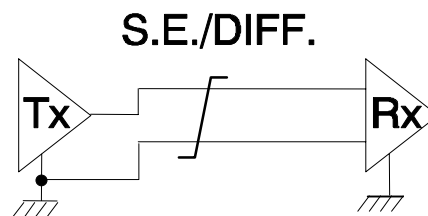
[FC Applicability: AOCS, DATAM, POWER]

The overall A/D conversion accuracy including sampling error, quantization error plus offset shall be less than ± 0.5 % of full scale.

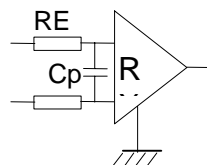
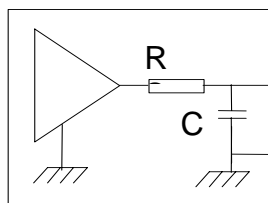
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6.3.2.3 Analog channels characteristics

- Standard analog channel:



- Parameter definition:



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Reference **SB4-SAT-AD1-P4-REQ-250 c**

[FC Applicability: AOCS, DATAM, POWER]

The analog telemetry shall comply with these analog electrical characteristics:

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
A	TYPE			
Req-1	Output type	Single ended		
Req-2	Input type		Differential	
B	VOLTAGE			
Req-1	Range	0 V / 5.12V		
Req-2	Fault Voltage Emission	± 15 V	± 15 V	
Req-4	Fault Voltage Tolerance	± 17 V	± 17 V	
C	CURRENT			
Req-1	Over-current	≤ 15 mA		permanent
D	IMPEDANCE			
Req-1	impedance ON	$R_s \leq 5 \text{ K}\Omega$ in parallel with $100 \text{ nF} \leq C \leq 1 \text{ }\mu\text{F}$ ($R_S \times C \geq 0,1 \text{ ms}$)	$\geq 1 \text{ M}\Omega$	
Req-2	impedance OFF	$R_P \leq 100 \text{ k}\Omega$ (2)	$\geq 1 \text{ M}\Omega$	
Req-3	Receiver input Capacity		100 pF Max	500 pF for harness
Req-4	DC in line series resistor		$R_e \geq 3 \text{ K}\Omega$	value related to each receiver input
Req-5	Receiver filter Capacity		$C_p \geq 10 \text{ nF}$	
E	GROUNDING AND ISOLATION			
Req-1	from secondary ground (0Vs)	Connected	$\geq 1 \text{ M}\Omega$	

Table 11: Analogic telemetry characteristics

(2) Rp is the impedance between positive output and the ground when the unit (source side) is OFF.

*

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6.3.3 Digital Bi-level channel

6.3.3.1 Digital Bi-Level channel definition

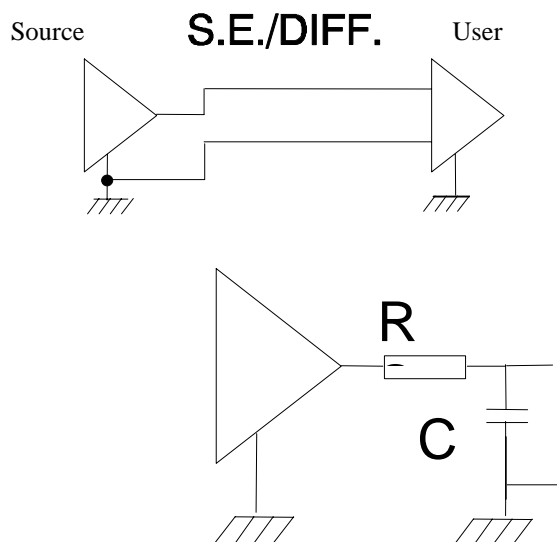
Reference **SB4-SAT-AD1-P4-REQ-562**

[FC Applicability: AOCS, DATAM]

The digital bi-level information shall be presented by the source in the form of a voltage that can assume only two distinct values, an on-level («ONE» level) and an off level («ZERO» level).

*

6.3.3.2 Digital Bi-Level channel characteristics



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Reference **SB4-SAT-AD1-P4-REQ-260 c**

[FC Applicability: AOCS, DATAM]

The digital bi-level telemetry shall comply with these digital bi-level electrical characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE	COMMENT
A	TYPE			
Req-1	Output type	Single ended		
Req-2	Input type		Differential	
Req-3	Transfer	DC COUPLER	DC COUPLER	
B	VOLTAGE			
Req-1	Low level output voltage (discrete "0")	0V to 0.5V		
Req-2	High level output voltage (discrete "1")	+3.5V to +10V		
Req-3	Fault Voltage Emission	± 15 V	± 15 V	
Req-4	Fault Voltage Tolerance	± 17 V	± 17 V	
C	CURRENT			
Req-1	Over-current	≤ 10 mA		permanent
D	IMPEDANCE			
Req-1	impedance ON	$R_s \leq 5 \text{ K}\Omega$ in parallel with $100 \text{ nF} \leq C \leq 1 \text{ }\mu\text{F}$ ($R_S \times C \geq 0,1 \text{ ms}$)	$\geq 220 \text{ k}\Omega$	
Req-2	impedance OFF	$R_P \leq 100 \text{ k}\Omega$ (2)	$\geq 1 \text{ M}\Omega$	
Req-3	Capacitance		100 pF max	500 pF for harness
E	GROUNDING AND ISOLATION			
Req-1	from secondary ground (0Vs)	connected	isolated ($\geq 1 \text{ M}\Omega$)	

Table 12: Digital bilevel telemetry characteristics

(2) Rp is the impedance between positive output and the ground when the unit (source side) is OFF.

*

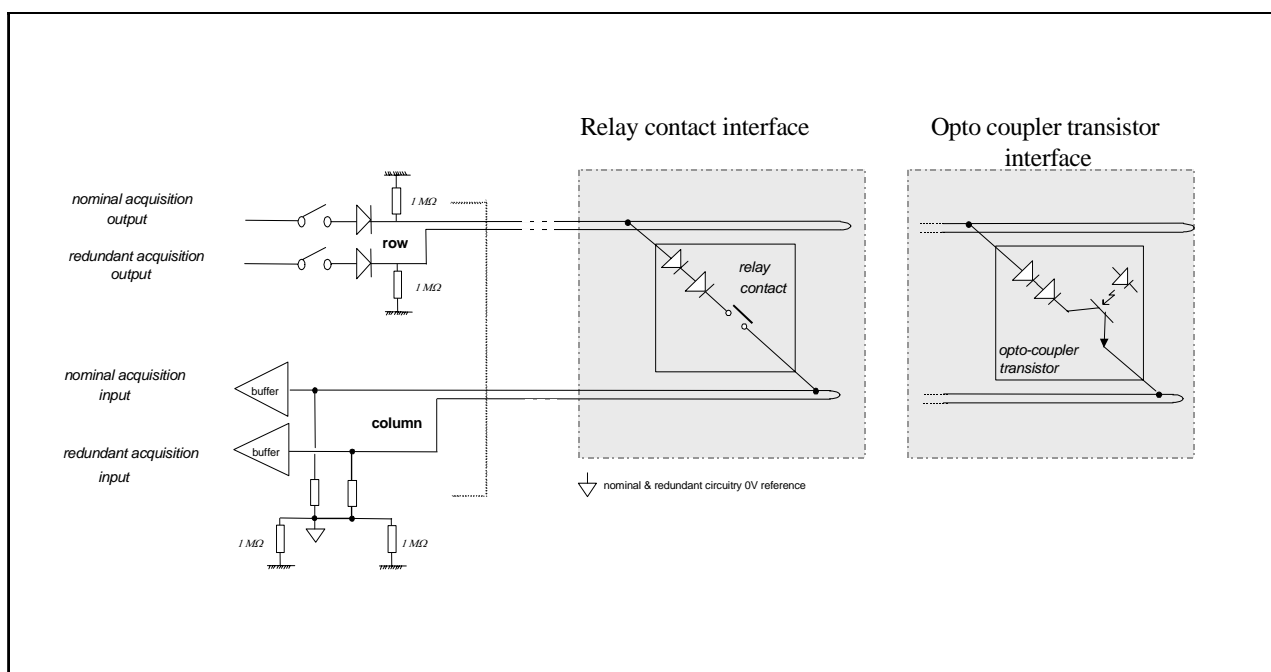
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6.3.4 Digital switch closure channel telemetry

The Digital relay acquisition also called DR shall be used to transmit a relay or a switch status signal.

6.3.4.1 Matrix switch closure acquisition definition

The matrix switch closure acquisitions are performed through a matrix organisation. One row is pulled up to a positive voltage and the switch closure status is acquired on the column.



6.3.4.1.1 Source side requirements

Source side is related to the switch closure location

Reference **SB4-SAT-AD1-P4-REQ-266 b**

[FC Applicability: AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

All source shall provide two diodes in series with the switch closure device.

*

Reference **SB4-SAT-AD1-P4-REQ-267 a**

[FC Applicability: AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Each row and column line shall be insulated from the mechanical ground inside the source equipment

*

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Reference **SB4-SAT-AD1-P4-REQ-268 a**

[FC Applicability: AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

The source equipment shall provide a galvanic isolation between the switch closure (contact or opto-coupler transistor) lines and the source electrical circuitry

*

Reference **SB4-SAT-AD1-P4-REQ-269 b**

[FC Applicability: AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

The source equipment shall not impose any potential or grounding reference on any row or column.

*

Reference **SB4-SAT-AD1-P4-REQ-563**

[FC Applicability: AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Closed contact shall correspond to the TM "Zero" level with the unit powered or active

*

Reference **SB4-SAT-AD1-P4-REQ-564**

[FC Applicability: AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

Open contact shall correspond to the TM "One" level with the unit unpowered or inactive

*

6.3.4.1.2 Receiver (or user) side requirements

Receiver side correspond at one hand to the switch closure polarisation outputs and at the other hand to the switch closure acquisition input.

Reference **SB4-SAT-AD1-P4-REQ-272 b**

[FC Applicability: DATAM]

Each node of the matrix switch closures shall be polarised by a nominal or a redundant separated interrogation command circuits.

*

Reference **SB4-SAT-AD1-P4-REQ-565**

[FC Applicability: DATAM]

Each set of switch closure status shall be selected by the nominal or the redundant acquisition input circuits

*

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Reference **SB4-SAT-AD1-P4-REQ-274 b**

[FC Applicability: DATAM]

The command lines (rows and columns) shall be double insulated inside the equipment (except external side of I/O connectors) and no failure propagation shall occur between rows, between columns or between row and column.

*

Reference **SB4-SAT-AD1-P4-REQ-275 b**

[FC Applicability: DATAM]

In case of failure, the concerned row output or the concerned column acquisition input shall be in a high impedance state.

*

Reference **SB4-SAT-AD1-P4-REQ-276 a**

[FC Applicability: DATAM]

The polarisation outputs of the matrix switch closure shall be protected by a current limiting device

*

Reference **SB4-SAT-AD1-P4-REQ-281 a**

[FC Applicability: DATAM]

The matrix acquisition pulse duration shall be at least 20 ms .

*

Reference **SB4-SAT-AD1-P4-REQ-566**

[FC Applicability: DATAM]

At least one serial diode shall be inserted on the positive output (row line output).

*

Reference **SB4-SAT-AD1-P4-REQ-282 a**

[FC Applicability: DATAM]

Only one row shall be selected per interrogation.

*

Reference **SB4-SAT-AD1-P4-REQ-283 b**

[FC Applicability: DATAM]

The matrix acquisition input interfaces shall not overload the source during normal operation (16 status (column lines, worst case) could be acquired simultaneously).

*

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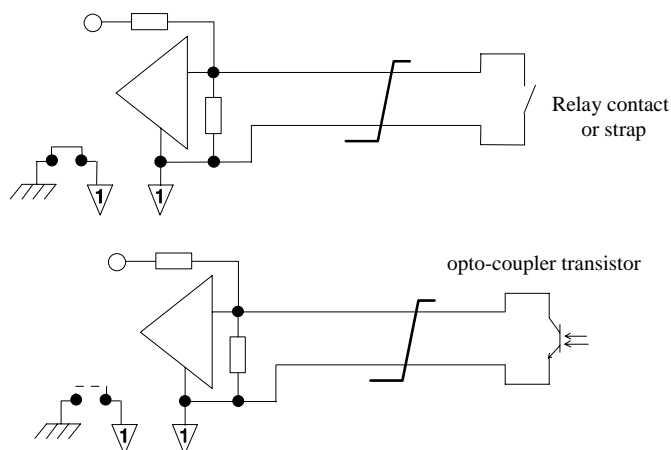
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6.3.4.2 Single ended switch closure acquisition definition

Direct switch closure acquisition shall be performed via a dedicated circuits referenced to the secondary 0V.

Digital relay channel telemetry schematics (Relay and opto-coupler transistor):



6.3.4.2.1 Source side requirements

Source side is related to the switch closure location.

Reference **SB4-SAT-AD1-P4-REQ-301 α**

[FC Applicability: DATAM, PROP]

Digital switch closure channels shall be completely isolated from any other return inside the source equipment

*

Reference **SB4-SAT-AD1-P4-REQ-302 α**

[FC Applicability: DATAM, PROP]

The source equipment shall provide a galvanic isolation between the switch closure lines and the source electrical circuitry

*

Reference **SB4-SAT-AD1-P4-REQ-303 α**

[FC Applicability: DATAM, PROP]

Separated returns for nominal and redundant channels shall be provided.

*

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Reference **SB4-SAT-AD1-P4-REQ-567**

[FC Applicability: DATAM, PROP]

Closed contact shall correspond to the TM "Zero" level with the unit powered or active

*

Reference **SB4-SAT-AD1-P4-REQ-568**

[FC Applicability: DATAM, PROP]

Open contact shall correspond to the TM "One" level with the unit unpowered or inactive

*

6.3.4.2.2 Receiver (or user) side requirements

Receiver side correspond to the switch closure acquisition inputs

Reference **SB4-SAT-AD1-P4-REQ-304 b**

[FC Applicability: DATAM, PROP]

Digital relay shall be referenced to the secondary ground inside the user equipment

*

6.3.4.3 Digital relay channel telemetry characteristics

Reference **SB4-SAT-AD1-P4-REQ-308 c**

[FC Applicability: AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

For matrix organisation, the digital relay telemetry shall comply with these digital relay electrical characteristics :

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Code	PARAMETERS	SOURCE SIDE DR	USER SIDE PCB	COMMENT
A	TYPE			
Req-1	Output type	differential		
Req-2	Input type		differential	for matrix organisation
B	VOLTAGE			
Req-1	Row min. voltage	N/A	9V	
Req-2	DM fault voltage emission	Not allowed	± 17 V	
Req-3	DM fault voltage tolerance	-17 V	N/A	permanent, ON or OFF
Req-4	DM fault voltage tolerance	± 17 V	N/A	permanent OFF only
Req-5	CM fault voltage emission	Not allowed	± 17 V	
Req-6	Drop voltage («ON state »)	$\leq 3,7$ V at 1mA		- relay : 2 diodes + 1 relay contact - opto : 2 diodes+1 transistor junction
Req-7	CM Fault Voltage Tolerance	± 17 V	± 17 V	DM = 0
C	CURRENT			
Req-1	Contact capability 'ON'	$I \geq 1$ mA	$0,5\text{mA} < I < 5\text{mA}$	Permanent, closed contact
Req-2	Contact capability 'OFF' (leakage)	$< 200\mu\text{A}$ @ 17V		Permanent, open contact
Req-3	Fault Current emission	N/A	$< 100\text{mA}$	

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Code	PARAMETERS	SOURCE SIDE DR	USER SIDE PCB	COMMENT
E	<i>MATRIX DR GROUNDING AND ISOLATION</i> ⁽¹⁾			
Req-1	between row / column lines and Chassis	$\geq 1 \text{ M}\Omega$ // $< 50 \text{ pF}$ for switch** $< 500 \text{ pF}$ for all the other equipment**	$113 \text{ K}\Omega < R < 10 \text{ M}\Omega$ // $// < 25 \text{ pF}$	** Only stray capacitance, no physical capacitance shall be added. Note: For Repeater Subsystem only the equivalent capacitance for one MAP equivalent matrix (contribution of all units connected) shall be lower than 33nF.
Req-2	Between matrix ground and Chassis		$113 \text{ K}\Omega < R < 10 \text{ M}\Omega$ // $10\text{nF} < C_{\text{CM}} < 50\text{nF}$ for PLDIU or $10\text{nF} < C_{\text{CM}} < 34\text{nF}$ for PFDIU	
Req-3	Between switch closure lines and the electrical circuitry	galvanic isolation		use of relay contact or opto-coupler transistor at source side

⁽¹⁾ Primary and users secondary grounds shall be considered connected to chassis for measurements

Table 13: Digital relay telemetry characteristics (For matrix acquisition)

*

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Reference **SB4-SAT-AD1-P4-REQ-632****[FC Applicability:** AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

For single ended acquisition, the digital relay telemetry shall comply with these digital relay electrical characteristics :

Code	PARAMETERS	SOURCE SIDE DR	USER SIDE PCB	COMMENT
A	TYPE			
Req-1	Output type	differential		
Req-2	Input type		Single ended	for single ended acquisition
B	VOLTAGE			
Req-1	DM fault voltage emission	Not allowed	± 16 V	
Req-2	DM fault voltage tolerance	± 16 V	N/A	permanent OFF only
Req-3	Drop voltage («ON state ») for DR ABM / MBSV / Umbilical	≤ 4 V / 400mA / 50ms		Only for ABM / MBSV / Umbilical
	Drop voltage («ON state ») for DR BSV/ SMU / PYPGP	$\leq 0,5$ V / 10mA		Only for BSV/ SMU / PYPGP
	Drop voltage («ON state ») for DR TOM/ BAPTA / SADM	≤ 1 V / < 1mA		Only for TOM/ BAPTA / SADM
C	CURRENT			
Req-1	Contact capability 'OFF' (leakage)	<100 μ A @ 5V		Permanent, open contact
Req-2	Fault Current emission	N/A	<100mA	

Code	PARAMETERS	SOURCE SIDE DR	USER SIDE PCB	COMMENT
E	SINGLE COMMAND GROUNDING AND ISOLATION			
Req-1	From Primary or Secondary Ground	Galvanic isolation		Not applicable to optical switches (BAPTA/SADM)
Req-2	Chassis	Isolated (≥ 1 M Ω)		Not applicable to optical switches (BAPTA/SADM)

Table 14: Digital relay telemetry characteristics (Single ended acquisition)

*

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Reference **SB4-SAT-AD1-P4-REQ-591**

[FC Applicability: AOCS, DATAM, PAYLOAD, POWER, PROP, TCR]

For an equipment all digital relay telemetry return shall be insulated from all other digital relay telemetry return and from grounding

*

6.3.5 Digital serial channels : DS16

6.3.5.1 Telemetry definition

The function of this interface is to transfer in a serial form a 16-bit data word from the Slave to the Master.

The interface consists in clock, sample and data signals, and it uses SBDL interface.

Clock and Sample signals are provided by the Master. Data signal is provided by the Slave.

The following notation is used:

- DS16_SAMPLE: DS16 sample signal
- CLOCK: ML16 and DS16 common clock signal
- DS16_DATA: DS16 data signal

The interface consists of clock, sample and data signals shall use SBDL interface.

Reference **SB4-SAT-AD1-P4-REQ-570**

[FC Applicability: AOCS, DATAM]

Outside the data transfer period, DS Sample & ML/DS Clock shall be in logical « 1 » state.

*

Reference **SB4-SAT-AD1-P4-REQ-571**

[FC Applicability: AOCS, DATAM]

The data transfer shall be valid only when sample line is active (level "0").

*

Reference **SB4-SAT-AD1-P4-REQ-572**

[FC Applicability: AOCS, DATAM]

One dedicated sampling signal line shall be provided to each DS16 user.

*

Reference **SB4-SAT-AD1-P4-REQ-573**

[FC Applicability: AOCS, DATAM]

One clock signal shall be provided to each user, for telecommand and telemetry.

*

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Reference **SB4-SAT-AD1-P4-REQ-575**

[FC Applicability: AOCS, DATAM]

For each data word transfer, 16 clock pulses shall be generated on the clock line.

*

Reference **SB4-SAT-AD1-P4-REQ-309 b**

[FC Applicability: AOCS, DATAM]

The Slave shall shift the data on the falling edge.

*

Reference **SB4-SAT-AD1-P4-REQ-629**

[FC Applicability: AOCS, DATAM]

The Master shall acquire the data on the falling edge.

*

Reference **SB4-SAT-AD1-P4-REQ-576**

[FC Applicability: AOCS, DATAM]

Each DS16 Slave shall provide one data line to its corresponding Master.

*

Reference **SB4-SAT-AD1-P4-REQ-578**

[FC Applicability: AOCS, DATAM]

The data shall be clocked out with the MSB first (bit 0).

*

6.3.5.2 Digital serial Electrical characteristics

Reference **SB4-SAT-AD1-P4-REQ-313 b**

[FC Applicability: AOCS, DATAM]

The digital serial telemetry shall comply with the SBDL electrical characteristics (See chapter:"SBDL Electrical Characteristics")

*

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6.3.5.3 Digital serial telemetry timing

Reference **SB4-SAT-AD1-P4-REQ-580**

[FC Applicability: AOCS, DATAM]

The Digital Serial Telemetry shall respect the following timing:

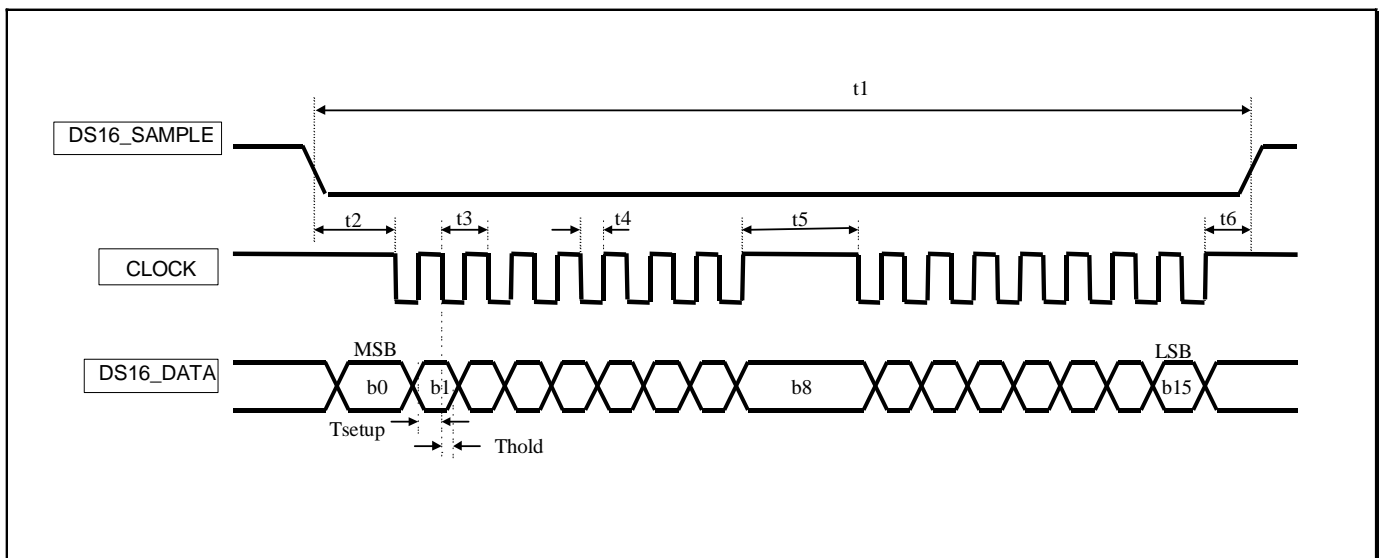


Figure 10: Digital Serial 16-Bit Telemetry Signal Waveform Diagram

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TIMING			
		MASTER	SLAVE
t	Reference time	$t=0,954\mu s \pm 5\%$	$t=0,954\mu s \pm 5\%$
t1	Sample active state duration	125t max.	125t max.
t2	Sample to clock delay	$28t \pm t$	26.5t min.
t3	Clock period	$4t \pm 0.1t$	$4t \pm 0.1t$
t4	Active to inactive edge of clock delay (Half Clock period)	$2t \pm 0.3t$	$2t \pm 0.5t$
t5	Middle frame gap	1.8t min 36t max	1.5t min 37t max
t6	inactive edge clock to transfer end Clock rising to end of sample	1.8t min	1.5t min
Taa	Acquisition to acquisition delay	3.8t min	3.5t min
Tsetup	Data valid setup time to clock falling edge	1.5t min	2.8t min
Thold	Clock falling edge to data change	0t min	0t min

Table 15: Digital serial telemetry timing

*

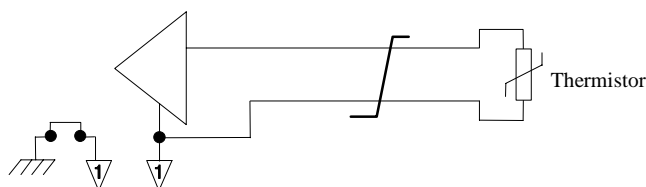
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6.3.6 thermistors power supply and conditioning (TH)



6.3.6.1 Thermistors type

Reference **SB4-SAT-AD1-P4-REQ-636**

[FC Applicability: AIT, ANTRACK, AOCs, DATAM, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

Thermistor type shall be chosen according to the following table:

DESIGNATION	TYPE	Temperature range	Corresponding R range
FENWAL or equivalent	526-31BS13 or equivalent	- 60 °C to + 160 °C	1342 KΩ to 0.302 KΩ
BETATHERM or equivalent	G15K4D425 or equivalent	- 60 °C to + 160 °C	1342 KΩ to 0.302 KΩ
GULTON or Victory Engineering or equivalent	34 TD 25	- 55 °C to + 125 °C	408,34 KΩ to 0.1317 KΩ or 385.5 KΩ to 0.137 KΩ
ROSEMOUNT	118 MF	- 200 °C to + 260 °C	0.34 KΩ to 3.97 KΩ
ROSEMOUNT	118 MF	- 50 °C to + 400 °C	1.5 KΩ to 5 KΩ
Thruster thermistor	PT200	- 200 °C to + 520 °C	37.04 to 575.23Ω

Table 16: Thermistors type

*

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6.3.6.1.1 Type: FENWAL or equivalent

The 25°C value is 15000 Ohms

Temperature	Résistance ohm	Résistance Tolerance $\pm\%$	Temperature	Résistance ohm	Résistance Tolerance $\pm\%$
-60	1342000	10,00	55	4923	1,03
-55	957000	9,01	60	4160	1,03
-50	690500	8,07	65	3531	1,04
-45	503700	7,17	70	3009	1,05
-40	371300	6,31	75	2576	1,04
-35	276200	5,48	80	2213	1,03
-30	207500	4,71	85	1908	1,04
-25	157200	4,02	90	1652	1,05
-20	120100	3,35	95	1434	1,03
-15	92500	2,72	100	1250	1,02
-10	71940	2,11	105	1094	1,02
-5	56310	1,54	110	959,4	1,02
0	44420	1,00	115	844,3	1,03
5	35300	1,00	120	745,3	1,03
10	28230	1,01	125	659,8	1,02
15	22730	1,03	130	585,9	1,02
20	18410	1,84	135	521,7	1,02
25	15000	1,02	140	465,5	1,02
30	12300	1,02	145	416,7	1,02
35	10130	1,03	150	373,6	1,01
40	8397	1,03	155	335,7	1,01
45	6995	1,03	160	302,4	1,00
50	5855	1,03			

Table 17: FENWAL thermistors characteristics

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6.3.6.1.2 Type: BETATHERM or equivalent

The 25°C value is 15000 Ohms

Temperature	Résistance ohm	Résistance Tolerance ±%
-60	1342000	10,00
-40	371300	6,30
-20	120100	3,35
0	44420	1,00
25	15000	1,01
50	5855	1,03
70	3009	1,05
100	1250	1,02
125	659,8	2,00
140	465,5	3,00
160	302,4	4,00

Table 18: BETATHERM thermistors characteristics

6.3.6.1.3 Type : Gulton 34 TD 25 or equivalent

The 25°C value is 4000 Ohms

Maximum ratings :

current : 29 mA (recommended nominal maximum operating current : 1 mA)

power : 0.1 W at 25°C

- Old version

Temperature	Résistance K. ohm	Résistance Tolerance ±%	Temperature	Résistance K.ohm	Résistance Tolerance ±%
-55	408,34	3,3	45	1,7362	0,75
-45	197,88	2,8	55	1,1814	0,73
-35	100,81	2,3	65	0,8203	0,67
-25	53,74	2,0	75	0,5805	1,0
-15	29,85	1,6	85	0,4168	0,96
-5	17,21	1,2	95	0,3055	0,91
5	10,269	1,0	105	0,2275	1,16
15	6,321	0,89	115	0,172	1,33
25	4	0,84	125	0,1317	1,53
35	2,608	0,81			

Table 19: GULTON 34TD25 thermistor characteristics (Old Version)

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- New version

Temperature	Résistance K. ohm	Résistance Tolerance $\pm\%$	Temperature	Résistance K.ohm	Résistance Tolerance $\pm\%$
-55	385,48	3,3	45	1,7476	0,75
-45	188,80	2,8	55	1,1944	0,73
-35	97,08	2,3	65	0,8332	0,67
-25	52,16	2,0	75	0,5928	1,0
-15	29,18	1,6	85	0,4288	0,96
-5	16,928	1,2	95	0,3154	0,91
5	10,156	1,0	105	0,23544	1,16
15	6,284	0,89	115	0,17808	1,33
25	4	0,84	125	0,13668	1,53
35	2,6128	0,81			

Table 20: GULTON 34TD25 thermistor characteristics (New Version)

6.3.6.1.4 Type : ROSEMOUNT 118MF Platinum resistance

The 118 MF type are Platinum Thermistors.

The model « 2000 ohms at 0°C » shall be considered.

Maximum ratings :

current : 10 mA (recommended nominal maximum operating current : 1 mA)

power : 0.1 W at 25°C

Temperature	Résistance K. ohm	Résistance Tolerance $\pm\%$	Temperature	Résistance K.ohm	Résistance Tolerance $\pm\%$
-200	343,69	3,4	140	3085,2	2,0
-160	689,2	2,6	180	3386,9	2,0
-120	1026,44	2,3	220	3684,9	2,0
-80	1356,2	2,0	260	3979,2	2,0
-40	1680,2	2,0	300	4269,6	2,0
0	2000	2,0	340	4556,8	2,0
40	2314,7	2,0	380	4812	2,0
80	2625,7	2,0	400	4980	2,0
100	2779,8	2,0			

Table 21: ROSEMOUNT 118MF Platinum thermistor characteristics

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6.3.6.1.5 Thruster thermistor(PT200)

The PT200 type are Platinum Thermistors.

The model « 200 ohms at 0°C » shall be considered.

Maximum ratings :

current : 10mA

power : 0.1W

Temperature(°C)	resistance (ohms)	Resistance tolerance (%)	temperature(°C)	resistance (ohms)	Resistance tolerance (%)
-200	37,04	3,4	80	261,79	2
-180	54,19	2,9	100	277,01	2
-160	71,09	2,6	140	307,17	2
-140	87,75	2,3	180	336,96	2
-120	104,22	2,3	220	366,38	2
-100	120,51	2	260	395,42	2
-80	136,65	2	300	424,1	2
-60	152,66	2	340	452,41	2
-40	168,54	2	380	480,35	2
-20	184,32	2	400	494,18	2
0	200	2	440	521,57	2
20	215,59	2	480	548,59	2
40	231,08	2	520	575,23	2
60	246,48	2			

Table 22: PT200 thermistor characteristics

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6.3.6.2 Thermistors channel telemetry characteristics

Reference **SB4-SAT-AD1-P4-REQ-601**

[FC Applicability: AIT, ANTRACK, AOCS, DATAM, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

Code	PARAMETERS	SOURCE SIDE (TH)	USER SIDE (DHP)	COMMENT
A	TYPE			
Req-1	Output type	differential balanced lines		
Req-2	Input type		Single ended	
B	POWER			
Req-1	Maximum operating power		< 5mW	
C	GROUNDING AND ISOLATION			
Req-1	from secondary ground (0Vs)	isolated ($\geq 10 \text{ M}\Omega$)	grounded	

Table 23: Thermistor telemetry characteristics

*

Reference **SB4-SAT-AD1-P4-REQ-592**

[FC Applicability: AIT, ANTRACK, AOCS, DATAM, MECHANISMS, PAYLOAD, POWER, PROP, TCR, THERMAL, ANTENNA]

For an equipment all thermistor telemetry return shall be insulated from all other thermistor telemetry return.

*

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6.4 UMBILICAL INTERFACE

6.4.1 Umbilical definition

Proper telemetry and telecommand PCM signals shall be routed to the umbilical connector from Command Control sub-system.

These signals are :

- two separate inputs for TC
- two separate outputs for TM

Reference **SB4-SAT-AD1-P4-REQ-593**

[FC Applicability: AIT, DATAM, HARNESS, POWER, PROP]

The current of all umbilical lines which cannot be switched off at the power source (at EGSE level or S/C level), shall be limited to 5mA (short circuit current value), during and after filling operations.

*

Reference **SB4-SAT-AD1-P4-REQ-620**

[FC Applicability: AIT, DATAM, HARNESS, POWER, PROP]

Current through umbilical connectors during lift-off shall be lower than:

- 100 mA, and
- Voltage lower than 85V, and
- Maximum power limitation of 2W.

*

6.4.2 Umbilical TC requirements

Reference **SB4-SAT-AD1-P4-REQ-331 a**

[FC Applicability: AIT, DATAM, HARNESS, POWER, PROP]

The TC umbilical interface shall comply the TC transceivers interface characteristics.

*

6.4.3 Umbilical TM requirements

Reference **SB4-SAT-AD1-P4-REQ-332 b**

[FC Applicability: AIT, DATAM, HARNESS, POWER, PROP]

The umbilical TM interface shall comply the TM video signal

*

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Reference **SB4-SAT-AD1-P4-REQ-323 b**

[FC Applicability: AIT, DATAM, HARNESS, POWER, PROP]

The electrical characteristics of umbilical strap shall be as follows :

Code	PARAMETERS	SOURCE SIDE	USER SIDE (strap)	COMMENT
A	TYPE			
Req-1	Output type	Differential		
Req-2	Input type		Single ended	
B	IMPEDANCE			
Req-1	Impedance open	$\geq 10\text{ M}\Omega$	$\leq 100\text{ k}\Omega$	separated
Req-2	Impedance closed	$\leq 10\text{ }\Omega$	$\leq 100\text{ K}\Omega$	not separated

Table 24:Umbilical Strap Characteristics

*

6.5 SMU / Transceiver interfaces

6.5.1 SMU / Receiver interfaces

Reference **SB4-SAT-AD1-P4-REQ-583**

[FC Applicability: DATAM, TCR]

The interface between receiver and the SMU shall provide (form SBDL signal): Squelch, Clock, Lock Status and Data signals.

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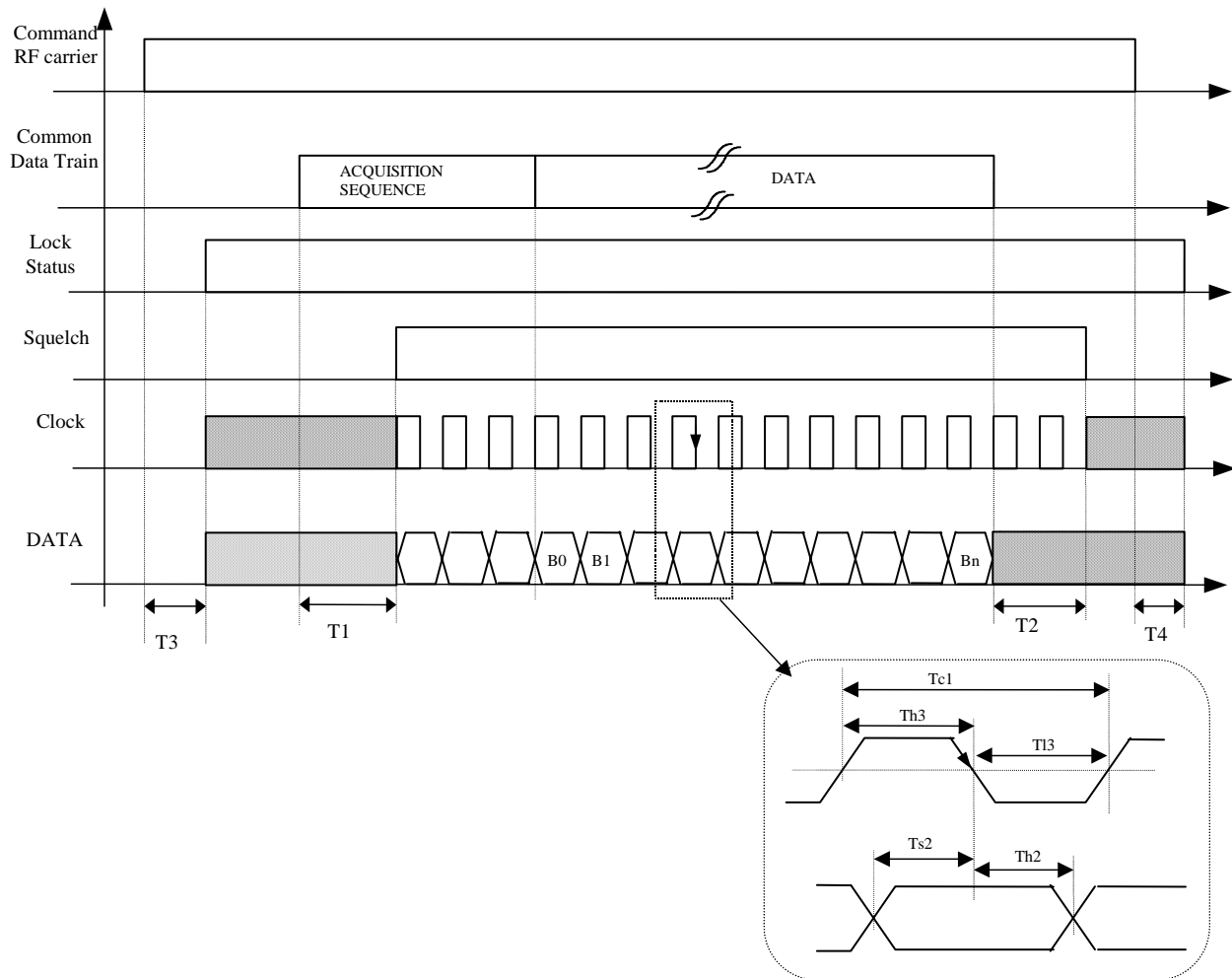


Figure 11: Signals between receiver and SMU.

$T1 : \leq 168 \text{ bits duration}$

$1 \text{ bit duration} \leq T2 \leq 128 \text{ bits duration}$

$T3 \text{ \& } T4 \leq 100\text{ms}$

$Tc1 \text{ (Bit clock period)} = 1 \text{ Bit rate } \pm 5\%$

$Th3 \text{ (TC bit clock high level duration at 50\% edge)} : \geq 60\mu\text{s}$

$Tl3 \text{ (TC bit clock low level duration at 50\% edge)} : \geq 60\mu\text{s}$

$Ts2 \text{ (Set-up time from NRZ DATA bit stable to clock falling edge (sampling edge))} : \geq 10\mu\text{s}$

$Th2 \text{ (Hold time from clock falling edge to NRZ DATA bit change)} : \geq 20\mu\text{s}$

The above described interface is used to transmit from the receiver to the SMU the following signal :
SQUELCH , CLOCK , DATA

*

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Reference **SB4-SAT-AD1-P4-REQ-584**

[FC Applicability: DATAM, TCR]

The receiver bit clock shall be running as soon as Lock Status is 'high'.

*

Reference **SB4-SAT-AD1-P4-REQ-326 b**

[FC Applicability: DATAM, TCR]

Data Validation shall be performed on the falling edge of the clock signal.

*

Reference **SB4-SAT-AD1-P4-REQ-327 a**

[FC Applicability: DATAM, TCR]

The bit clock stability shall be better than +/- 5% as soon as SQUELCH is high and until SQUELCH falls to low.

*

6.5.2 SMU / Transmitter interfaces

Reference **SB4-SAT-AD1-P4-REQ-330 c**

[FC Applicability: DATAM, TCR]

The TM video signals shall comply with the following characteristics :

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Code	PARAMETERS	Transmitter side SMU	Receiver side	COMMENT
A	TYPE			
Req-1	Output type	single ended		
Req-2	Input type		differential	
Req-3	Type of Modulation	BPSK	BPSK	
Req-4	Waveform	Filtered quasi sine wave	Filtered quasi sine wave	
B	VOLTAGE			
Req-1	output AC voltage	$3V \pm 5.7\%$ peak to peak		
Req-2	DC Fault Voltage Emission	$-1V < U < 10V$	$\pm 17V$ in series with $> 2k\Omega$	
Req-3	DC Fault Voltage Tolerance	$\pm 17V$ in series with $> 2k\Omega$	$-1V < U < 10V$	
C	IMPEDANCE			
Req-1	output impedance (1)	$< 100\Omega$ in series with $> 100nF$		
Req-2	input impedance		$> 10k\Omega // < 500pF$	
D	SPECIFIC REQUIREMENT			
Req-1	TM sub-carrier frequency	65536 Hz	65536 Hz	upgrade : 32768Hz
Req-2	TM sub-carrier frequency stability	$\pm 10^{-4}$		
Req-3	TM bit rate	4096 bit/s or 8192 bit/s	4096 bit/s or 8192 bit/s	
Req-4	Phase plot accuracy	$\pm 2^\circ$		Difference between theoretical and real phase
Req-5	group delay variations	$< 1\mu s$ peak to peak		
Req-6	Amplitude distortion	< 1 dB peak to peak		
Req-7	signal to noise ratio	65 dBHz		

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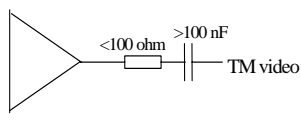
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Code	PARAMETERS	Transmitter side SMU	Receiver side	COMMENT
Req-8	Spurious and Harmonics	<ul style="list-style-type: none"> • <-20dBc : 0<f<220kHz • <-60dBc : f>220kHz 32768Hz +/-8kHz 65536 Hz +/- 8kHz [15kHz ;30kHz] 100kHz +/-1kHz 	N/A N/A	With respect to TM sub carrier levels TM signal bandwidth TM signal bandwidth Ranging signals bandwidth Ranging signals bandwidth
Req-9	phase step response accuracy	± 5% (2)		
E	FAIL SAFE PROTECTION			
Req-1	protection	short circuit proof		
F	GROUNDING AND ISOLATION			
Req-1	From secondary ground 0Vs	Grounded	Galvanic isolation	
Req-2	From primary ground	Isolation ≥ 1MΩ	Isolation ≥ 1MΩ	
Req-3	From chassis	Grounded	Isolation ≥ 1MΩ	

(1)



(2) At all times, for more than 25% of a sub-carrier period after a phase reversal, the phase of the modulated sub-carrier shall be within ±5% of a perfect signal.

Table 25: TM Video Signal Characteristics.

*

6.5.3 SMU / Ciphering

Reference **SB4-SAT-AD1-P4-REQ-635**

[FC Applicability: DATAM]

The SMU digital TM output channel shall provide a 3 signals interface composed of:

- TM_VAL-FRAME: indicates output data is valid
- TM_DATA: serial data stream
- TM_OUT-CLOCK: output synchronised clock

*

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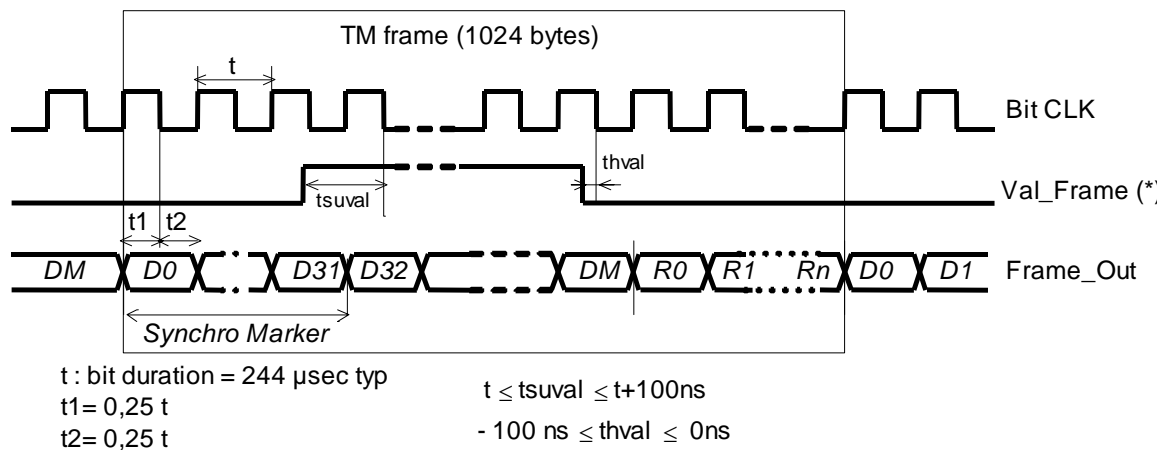
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Reference **SB4-SAT-AD1-P4-REQ-634**

[FC Applicability: DATAM]

The SMU digital TM output signals shall be compliant with chronograms given hereafter :

The SMU digital TM output signals shall be compliant with chronograms given hereafter :



(*) At user's interface, Val_Frame signal shall be half period shifted in order to be synchronised with data.

The Val_Frame signal shall be activated on the last bit of the TM Synchro Marker and shall be deactivated on the last bit of the Trailer Frame (DM).

Table 26: SMU digital TM output characteristics.

*

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(AD01-P4)

6.6 Alarm signal

6.6.1 Alarm signal characteristics

Reference **SB4-SAT-AD1-P4-REQ-334 d**

[FC Applicability: AOCS, DATAM, PROP]

The Alarm signal interface shall comply the SBDL electrical characteristics for: STARTRACKER, IRES, AOCSP, PROP .

*

Reference **SB4-SAT-AD1-P4-REQ-335 b**

[FC Applicability: AOCS, DATAM, PROP]

Requirements **B Req-7** to **B Req-1**, from Table 9: SBDL Characteristics (SB4-SAT-AD1-P4-REQ-243), are not applicable to SBDL alarm signals. The fault voltage emission and tolerance shall be $\pm 7V$.

*

Reference **SB4-SAT-AD1-P4-REQ-585**

[FC Applicability: AOCS, DATAM, PROP]

Alarm signals shall be processed by the SMU.

*

6.7 Synchronisation signals

The SMU provides three synchronisation signal:

- 1Hz: Distributed to PROP Pcb.
- 10Hz: Distributed to PROP Pcb, AOCSP Pcb and STR.
- 1000Hz: Distributed to PROP.

Each signal is redunded.

The 1 Hz signal period accuracy is better than $1s \pm 1\mu s$ by period.

10Hz, 1Hz clock rising transition is synchronous to 1000 Hz rising clock transitions.

Reference **SB4-SAT-AD1-P4-REQ-343 c**

[FC Applicability: AOCS, DATAM, PROP]

The synchronisation signals shall use the RS485 standard.

*

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Requirements

(AD01-P4)

Reference **SB4-SAT-AD1-P4-REQ-344 b**

[FC Applicability: AOCS, DATAM, PROP]

Any failure on the Nominal or (-exclusive) Redundant source signals shall not affect the operational capability of the user unit.

*

Reference **SB4-SAT-AD1-P4-REQ-345 c**

[FC Applicability: AOCS, DATAM, PROP]

The electrical characteristics are defined in the Chapter "SBDL electrical characteristics". Requirements **B Req-7** to **B Req-10**, and **F** (Req-1 and Req-2) from **Table 9** (SB4-SAT-AD1-P4-REQ-243) are not applicable to synchronisation signals.

*

Reference **SB4-SAT-AD1-P4-REQ-612**

[FC Applicability: AOCS, DATAM, PROP]

The fault voltage emission and tolerance shall be $\pm 7V$.

*

Reference **SB4-SAT-AD1-P4-REQ-348 b**

[FC Applicability: AOCS, DATAM, PROP]

The rise and fall time shall be : $100\text{ ns} < t < 500\text{ ns}$.

*

SUBSYSTEM AND UNITS REQUIREMENTS

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Requirements

(AD01-P4)

6.8 Propulsion interfaces

Pull-in voltage is the voltage required to open the valve and maintain it in its last commanded position.

Holding voltage is the voltage required to maintain opened valve.

Drop-out voltage is the voltage required at which valve resume its initial position.

6.8.1 ABM valves

Reference **SB4-SAT-AD1-P4-REQ-356 c**

[FC Applicability: DATAM, PROP]

The ABM valve interface shall comply with the following characteristics :

Code	PARAMETERS	USER SIDE ABM	COMMENT
A	TYPE		
Req-1	Input type	differential 2 coil in series	
B	VOLTAGE		
Req-1	Pull-in Voltage	$\leq 40 \text{ V}$	For two coils in series
Req-2	Drop-out Voltage	$\geq 3 \text{ V}$	For two coils in series
Req-3	Holding Voltage	$\leq 15 \text{ V}$	For two coils in series
Req-4	Fault voltage tolerance	54V	2 coil in series
D	TIME		
Req-1	Opening response time	$\leq 30\text{ms}$	At 21°C, 21 V
Req-2	Closing response time	$\leq 30\text{ms}$	
	IMPEDANCE		
Req-1	Coil Inductance	$\leq 900\text{mH}$	at 21°C
Req-2	Coil Resistance	$16,6 \Omega < R < 28.7 \Omega$	including temperature range
F	GROUNDING AND ISOLATION		
Req-1	Insulation resistance to from chassis	$> 100 \text{ M}\Omega$	

Table 27: ABM Interface Characteristics

*

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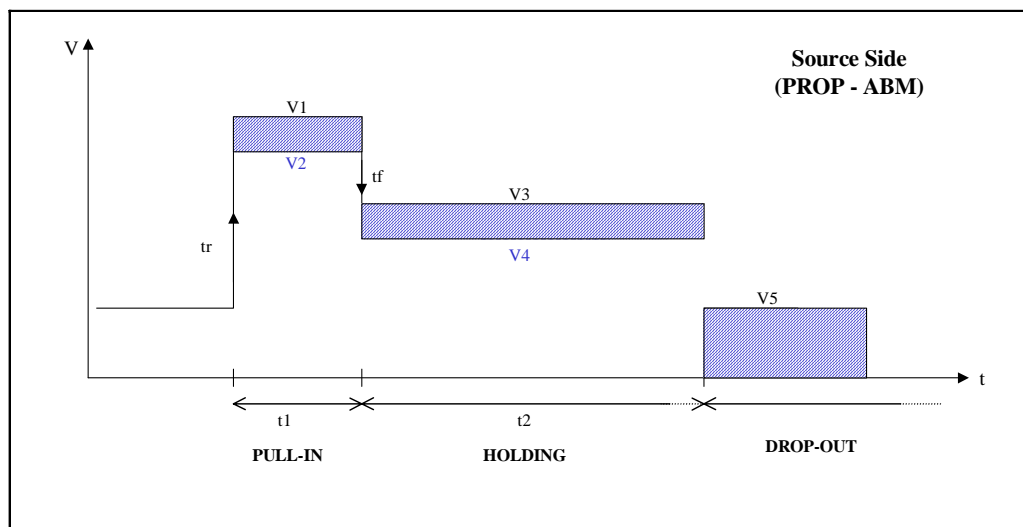
Requirements

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Reference **SB4-SAT-AD1-P4-REQ-594****[FC Applicability:** DATAM, PROP]

The PROP interface (source side) shall comply with the following characteristics:

Code	PARAMETERS	SOURCE SIDE PROP	COMMENT
A	TYPE		
Req-1	Output type	Single ended	
B	VOLTAGE		
Req-1	Pull-in Voltage (V1 & V2))	$46V < V < 53V$	V1 & V2: Refer to figure below
Req-2	Holding Voltage (V3 & V4)	$20V < V < 53V$	V3 & V4: Refer to figure below
Req-3	Drop-out Voltage (V5)	$< 1V$	V5: Refer to figure below
Req-4	Fault voltage emission	$< 53V$	
D	TIME		
Req-1	Pull in pulse duration (t1)	100ms -25ms/+5ms	At 80% of max. pull in voltage t1: Refer to figure below
Req-2	Holding pulse duration (t2)	$\geq 1 \text{ min.}$	t2: Refer to figure below
F	GROUNDING AND ISOLATION		
Req-1	Insulation resistance to from chassis	$> 1 \text{ M}\Omega$ under 50V max.	

**Table 28: PROP-ABM Interface Characteristics**

*

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Requirements

(AD01-P4)

6.8.2 Thruster Bi-stable valves

The bi-stable commands functioning are equivalent to command matrix functioning.

Electrical characteristics are different .

Pull-out voltage is the minimum voltage required to close the valve and maintain it in its last commanded position.

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Reference **SB4-SAT-AD1-P4-REQ-357 d**

[FC Applicability: DATAM, PROP]

The Bistable valve interface shall comply with the following characteristics :

Code	PARAMETERS	SOURCE SIDE (PROP)	USER SIDE Bi-stable Valve	COMMENT
A	TYPE			
Req-1	Output type	Single ended		
Req-2	Input type		differential	bistable
B	VOLTAGE			
Req-1	Pull-in Voltage	33,5 V < V < 42 V	≤ 32V	
Req-2	Pull-out Voltage	33,5 V < V < 42 V	≤ 32V	
Req-3	Fault voltage emission	55V (55ms)		
Req-4	Fault voltage tolerance		55V (55ms)	
D	TIME			
Req-1	Opening/closing response time		<15ms	50V at 21°C
Req-2	Voltage Pulse duration	55±5ms		@50% of max pulse amplitude
Req-3	Rise/fall time	< 5ms		
E	IMPEDANCE			
Req-1	Coil Inductance		≤ 1 H	at 21°C
Req-2	Coil Resistance		260 Ω < R < 485 Ω	including temperature range
F	GROUNDING AND ISOLATION			
Req-1	Insulation resistance to from chassis		> 100 MΩ	at 20°C

Table 29: Bi-Stable Valve characteristics

*

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Requirements

(AD01-P4)

6.8.3 PPS Bi-stable valves

Reference **SB4-SAT-AD1-P4-REQ-358 c**

[FC Applicability: DATAM, PROP]

The PPS valve interface shall comply with the following characteristics :

Code	PARAMETERS	SOURCE SIDE (PROP)	USER SIDE	COMMENT
A	TYPE			
Req-1	Output type	Single ended		
Req-2	Input type		Differential	bistable
B	VOLTAGE			
Req-1	Operating Voltage Range	$31V < V_n < 51V$	30V to 51V	
Req-2	Fault voltage Tolerance		55V	
Req-3	Fault voltage Emission	<55		
C	POWER			
Req-1	Power consumption		42W	50V & 21°C
Req-2	Current		0.82A	
D	TIME			
Req-1	Opening/closing response time	>50ms	<50ms	50V & 21°C
E	IMPEDANCE			
Req-1	Coil Inductance		$\leq 250mH$	1kHz
Req-2	Coil Resistance		$47\Omega < R < 75\Omega$	including temperature range
F	GROUNDING AND ISOLATION			
Req-1	Insulation resistance to from chassis		100 M Ω	500VDC

Table 30: PPS Valve characteristics

*

SUBSYSTEM AND UNITS REQUIREMENTS

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Requirements

(AD01-P4)

6.8.4 Thruster Mono-Stable Valves

Reference **SB4-SAT-AD1-P4-REQ-359 b**

[FC Applicability: DATAM, PROP]

The mono-stable valve command shall be pulse type, with a 1 ms resolution on pulse duration and on pulse start.

The mon-stable command shall operate simultaneously up to 8 valves continuously.

*

Reference **SB4-SAT-AD1-P4-REQ-360 a**

[FC Applicability: DATAM, PROP]

Each command generated by the function shall be read back to generate a mono-stables status .

*

Reference **SB4-SAT-AD1-P4-REQ-361 a**

[FC Applicability: DATAM, PROP]

The On time of the mono-stables shall last from 1 ms to hours with repetition frequency of 33Hz.

*

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Requirements

(AD01-P4)

Reference **SB4-SAT-AD1-P4-REQ-362 d****[FC Applicability:** DATAM, PROP]

The Mono-stable valve interface shall comply with the following characteristics :

Code	PARAMETERS	SOURCE SIDE (PROP)	USER SIDE	COMMENT
A	TYPE			
Req-1	Output type	single ended		
Req-2	Input type		differential	monostables
B	VOLTAGE			
Req-1	Pull-in Voltage	$36\text{ V} < V < 42\text{ V}$	$\leq 25\text{V}$	
Req-2	Drop-out Voltage	$< 1\text{V}$	$\geq 2\text{V}$	
Req-3	Fault voltage emission	55V (50ms)		
Req-4	Fault voltage tolerance		55V (30s)	
D	TIME			
Req-1	Opening/closing response time		$< 2.8\text{ ms}$	50V at 45°C
Req-2	Voltage Rise time + switch ON delay	$< 150\mu\text{s}$		On 190 Ω MSV load
Req-3	Voltage Fall time + switch OFF delay	$< 300\mu\text{s}$		On 478 Ω MSV load
E	IMPEDANCE			
Req-1	Coil Inductance		$< 1\text{H}$	at 21°C
Req-2	Coil Resistance		$190\ \Omega < R < 478\ \Omega$	including temperature range
F	GROUNDING AND ISOLATION			
Req-1	Insulation resistance to from chassis		$> 100\text{ M}\Omega$	at 20°C

Table 31: Mono-Stable Valves characteristics

*

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Requirements

(AD01-P4)

6.8.5 Pressure Transducer

6.8.5.1 Standard pressure transducer

6.8.5.1.1 Standard pressure transducer supply characteristics

Reference **SB4-SAT-AD1-P4-REQ-363 c**

[FC Applicability: DATAM, PROP]

The standard pressure transducer supply interface shall comply with the following characteristics:

Code	PARAMETERS	SOURCE SIDE (PROP)	USER SIDE (SAPT)	COMMENT
A	TYPE			
Req-1	Output type	single ended		
Req-2	Input type		Differential	
B	VOLTAGE			
Req-1	Operating Voltage Range	26.5 >Vop> 28.5V	26 to 28.5V	
Req-2	Fault voltage emission	<30V		
Req-3	Fault voltage tolerance		≥30V	
C	CURRENT			
Req-1	Inrush Current		200 mA max, 4ms	100 A/s max
D	IMPEDANCE			
Req-1	Input impedance		> 1.4 kΩ	10 m of 26 AWG between PROP and Pressure transducer Input current range: 16 to 20mA
E	GROUNDING AND ISOLATION			
Req-1	Insulation resistance from chassis		> 100 MΩ	50V
F	TIME			
Req-1	Time between Power On application and TM data availability	NA	< 1s	
Req-2	Power OFF step response	NA	< 20s	

Table 32: Standard Pressure Transducer Input Characteristics.

*

SUBSYSTEM AND UNITS REQUIREMENTS

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Requirements

(AD01-P4)

6.8.5.1.2 Standard pressure transducer telemetry characteristics

Reference **SB4-SAT-AD1-P4-REQ-364 c**

[FC Applicability: DATAM, PROP]

The standard pressure transducer telemetry interface shall comply the following characteristics :

Code	PARAMETERS	SOURCE SIDE (SAPT)	USER SIDE (PROP)	COMMENT
A	TYPE			
Req-1	Output type	Differential		
Req-2	Input type		Differential	
B	VOLTAGE			
Req-1	Voltage Range	0 V/ 5V		Output noise : 20mVpp (20MHz bandwidth)
Req-2	Output voltage OFFSET	$\pm 5\text{mV}$		
Req-3	Fault Voltage Emission	$U < 15\text{V}$	$\pm 15\text{ V } \Omega$ ($R_s > 47,5\text{ K}\Omega$)	
Req-4	Fault Voltage Tolerance	$\pm 15\text{ V}$ ($R_s > 47,5\text{ K}\Omega$)	$-1.5\text{V} < U < 15\text{V}$	
C	CURRENT			
Req-1	short circuit current	$< 30\text{mA}$		
D	IMPEDANCE			
Req-1	ON impedance	$< 100\ \Omega$	$\geq 1\text{ M}\Omega$	
Req-2	OFF impedance	$< 20\text{ K}\Omega$	$\geq 1\text{ M}\Omega$	
E	GROUNDING AND ISOLATION			
Req-1	From supply ground	$> 10\text{ M}\Omega$	$\geq 1\text{ M}\Omega$	
Req-2	Chassis	$\geq 10\text{ M}\Omega$	$\geq 1\text{ M}\Omega$	

Table 33: Standard Pressure Transducer Telemetry Characteristics.

*

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6.8.5.2 High Accuracy Pressure Transducer :

6.8.5.2.1 High accuracy pressure transducer supply characteristics

Reference **SB4-SAT-AD1-P4-REQ-365 c**

[FC Applicability: DATAM, PROP]

The high accuracy pressure transducer supply interface shall comply with the following characteristics :

Code	PARAMETERS	SOURCE SIDE (PROP)	USER SIDE	COMMENT
A	TYPE			
Req-1	Input type		Differential	
Req-2	Output type	Single ended		
B	VOLTAGE			
Req-1	Operating Voltage Range	11V +/-5 %	9V < V < 12V	
Req-2	Fault voltage emission	<16V		
Req-3	Fault voltage tolerance		≥ 16V	
C	IMPEDANCE			
Req-1	Input resistance		≥ 800 Ω	
D	GROUNDING AND ISOLATION			
Req-1	Insulation resistance to from chassis		>20MΩ (50V) 100nF	

Table 34: High Accuracy Pressure Transducer Input Characteristics.

*

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Requirements

(AD01-P4)

6.8.5.2.2 High accuracy pressure transducer telemetry characteristics

Reference **SB4-SAT-AD1-P4-REQ-366 b**

[FC Applicability: DATAM, PROP]

The high accuracy pressure transducer telemetry interface shall comply the following characteristics :

Code	PARAMETERS	SOURCE SIDE	USER SIDE (PROP)	COMMENT
A	TYPE			
Req-1	Output type	single ended		square wave AC coupled
Req-2	Input		Differential	
B	VOLTAGE			
Req-1	High level	$4.5\text{ V} < V < 5.5\text{V}$		
Req-2	Low level	$0\text{ V} < V < 0.5\text{V}$		
D	IMPEDANCE			
Req-1	Output Impedance	$< 2\text{ K}\Omega$		
Req-2	Input Impedance		$> 5\text{k}\Omega$	
E	TIME			
Req-1	Pressure frequency range	2 to 50 kHz		
Req-2	Temperature frequency range	2 to 200 kHz		
F	GROUNDING AND ISOLATION			
Req-3	From chassis	$> 20\text{M}\Omega (50\text{V}) //$ 100nF	$\geq 1\text{ M}\Omega //$ $< 50\text{nF}$	

Table 35: High Accuracy Pressure Transducer Telemetry Characteristics.

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6.9 Heaters characteristics

Reference **SB4-SAT-AD1-P4-REQ-602**

[FC Applicability: ANTRACK, DATAM, MECHANISMS, STRUCTURE, THERMAL, ANTENNA]

Code	PARAMETERS	SOURCE SIDE (HEATER)	USER SIDE (DHP)	COMMENT
A	TYPE			
Req-1	Output	Differential		
B	POWER			
Req-1	120W heater Maximum power	120W	120W	Tolerance: +0/-10%
Req-2	80 W heater Maximum power	80W	80W	Tolerance: ± 10%
Req-3	60 W heater Maximum power	60W	60W	Tolerance: ± 10%
Req-4	40 W heater Maximum power	40W	40W	Tolerance: ± 10%
Req-5	30 W heater Maximum power	30W	30W	Tolerance: ± 10%
Req-6	15 W heater Maximum power	15W	15W	Tolerance: ± 10%
Req-7	7 W heater Maximum power	7W	7W	Tolerance: ± 10%
C	IMPEDANCE			
Req-1	Max capacitance	<5nF		
Req-2	Max inductance	5 μH		+7μH Harness : twisted pair:AWG 24 or 26
Req-3	Max resistance	(1)		Up to 200Ω/cm ²
D	GROUNDING AND ISOLATION			
Req-1	from Primary Ground	/	connected	
Req-2	from chassis	> 100 MΩ	≥ 1 MΩ // ≤ 50 nF	

(1) The maximum resistance is defined by the heater power.

Table 36: Heater interface characteristics

*

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6.10 Deployment, Full Step, Sinus Cosinus motors Interfaces

6.10.1 Bi and three phases steppers interface characteristics

6.10.1.1 BAPTA / SADM motor interfaces

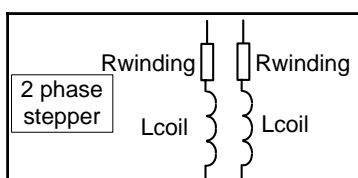
Reference **SB4-SAT-AD1-P4-REQ-368 b**

[FC Applicability: DATAM, POWER]

The BAPTA interfaces shall comply with the following characteristics :

Code	PARAMETERS	BAPTA MOTOR	SADP Pcb	COMMENT
A	CURRENT			
Req-1	Current	$I < 200\text{mA}$	$200\text{mA} \pm 20\text{mA}$	
B	IMPEDANCE			
Req-1	2 phase winding resistance	$60\Omega < R_{\text{winding}} < 115\Omega$		Including temperature range
Req-2	typical 2 phase winding inductance	$L_{\text{coil}} = 200\text{mH} \pm 20\%$		Including temperature range
Req-3	Driver OFF impedance		$> 1\text{K}\Omega$	Only in case of switched current in winding. Not applicable to quasi-static (DC) current source
C	GROUDING AND ISOLATION			
Req-1	Insulation resistance between windings	$> 50\text{ M}\Omega$		Measured under 100 Vmin
Req-2	Insulation resistance : Winding/case	$> 50\text{ M}\Omega$		Measured under 100 Vmin

Table 37: BAPTA interfaces



For information, the 2 phase winding resistance at ambient temperature(25°C) is :

$$88\Omega < R_{\text{winding}} < 91\Omega$$

*

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

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(AD01-P4)

Reference **SB4-SAT-AD1-P4-REQ-607****[FC Applicability:** DATAM, POWER]

The SADM interfaces shall comply with the following characteristics:

Code	PARAMETERS	SADM MOTOR	SADP Pcb	COMMENT
A	CURRENT			
Req-1	Current	$I < 300\text{mA}$	$300\text{mA} \pm 30\text{mA}$	
B	IMPEDANCE			
Req-1	2 phase winding resistance	$26\Omega < R < 77\Omega$		Including temperature range
Req-2	typical 2 phase winding inductance	$L_{\text{coil}} = 170\text{mH} \pm 20\%$		Including temperature range
Req-3	Driver OFF impedance		$> 1\text{K}\Omega$	Only in case of switched current in winding. Not applicable to quasi-static (DC) current source
C	GROUDING AND ISOLATION			
Req-1	Insulation resistance between windings	$> 50 \text{ M}\Omega$		Measured under 100 Vmin
Req-2	Insulation resistance : Winding/structure	$> 50 \text{ M}\Omega$		Measured under 100 Vmin

Table 38: SADM Motor interfaces

*

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

6.10.1.2 Antenna pointing motor interfaces

Reference **SB4-SAT-AD1-P4-REQ-369 b**

[FC Applicability: ANTRACK, DATAM, MECHANISMS, ANTENNA]

The antenna pointing interfaces (motor and Pcb) for a **3 phases rotary actuator** shall comply with the following characteristics :

Code	PARAMETERS	Antenna pointing motor	Motor PCB (FSXP)	COMMENT
A	VOLTAGE			
Req-1	Operating Voltage range	26V \pm 10%	26V \pm 10%	
B	IMPEDANCE			
Req-1	3 phase winding resistance	40 Ω < R < 120 Ω		Including temperature range
Req-2	3 phase winding inductance	L coil=20.4mH \pm 20%		Operating at 20°C
C	CURRENT			
Req-1	Over current protection threshold		> 700 mA	Operating at 20°C
D	GROUDING AND ISOLATION			
Req-1	Insulation resistance between windings	> 50 M Ω		Measured under 200 Vmin
Req-2	Insulation resistance : Winding/case	> 50 M Ω		Measured under 200 Vmin

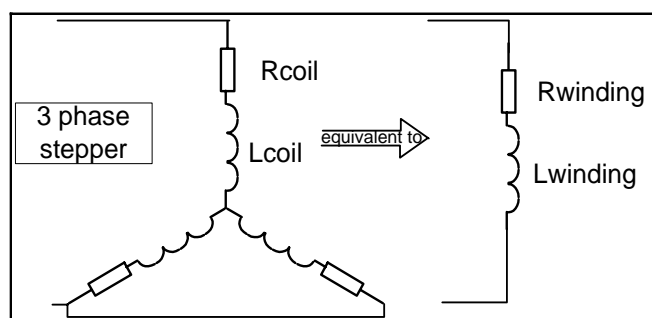


Table 39: Antenna Pointing Motor (3phases RA) and PCB interfaces

*

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

Reference **SB4-SAT-AD1-P4-REQ-625****[FC Applicability:** ANTRACK, DATAM, MECHANISMS, ANTENNA]

The antenna pointing interfaces (motor and Pcb) for a **2 phases rotary actuator** shall comply with the following characteristics :

Code	PARAMETERS	Antenna pointing motor	Motor PCB (FSXP)	COMMENT
A	VOLTAGE			
Req-1	Operating Voltage range	26V \pm 10%	26V \pm 10%	
B	IMPEDANCE			
Req-1	2 phase winding resistance	Rwinding=76 Ω \pm 10%		Operating at 20°C
Req-2	2 phase winding inductance	L coil=150mH \pm 30%		Operating at 20°C
C	CURRENT			
Req-1	Over current protection threshold		> 700 mA	Operating at 20°C
D	GROUDING AND ISOLATION			
Req-1	Insulation resistance between windings	>50 M Ω		Measured under 200 Vmin
Req-2	Insulation resistance : Winding/case	>50 M Ω		Measured under 200 Vmin

Table 40 : Antenna Pointing Motor (2 phases RA) and PCB interfaces

*

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

6.10.1.3 Thruster orientation motor interfaces

Reference **SB4-SAT-AD1-P4-REQ-370 b**

[FC Applicability: DATAM, PROP]

The thruster orientation interfaces (motor and Pcb) shall comply with the following characteristics :

Code	PARAMETERS	Thruster Orientation Motor	Motor PCB (FSXP)	COMMENT
A	VOLTAGE			
Req-1	Operating Voltage range	26V ±10%	26V ±10%	
B	IMPEDANCE			
Req-1	3 phase winding resistance	$60\Omega < R_{winding} < 120\Omega$		Including temperature range
Req-2	3 phase winding inductance	$L_{coil} = 200mH \pm 20\%$		Including temperature range
C	CURRENT			
Req-1	Over current protection threshold		> 700 mA	Operating at 20°C
D	GROUDING AND ISOLATION			
Req-1	Insulation resistance between windings	> 50 MΩ		Measured under 200 Vmin
Req-2	Insulation resistance : Winding/case	> 50 MΩ		Measured under 200 Vmin

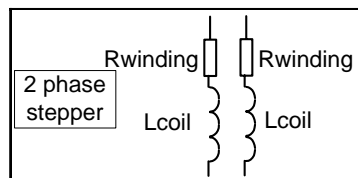


Table 41: Thruster Orientation Motor and PCB interfaces

*

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

6.10.2 Brush motor interface

Two types of Brush Motor can be used. The motor selected shall comply with one of the following requirements (depending on the Motor Pcb)

Reference **SB4-SAT-AD1-P4-REQ-371 b**

[FC Applicability: DATAM, POWER]

The Brush motor interfaces (motor and Pcb (SADP)) shall comply with the following characteristics :

Code	PARAMETERS	BRUSH MOTOR	MOTOR PCB (SADP)	COMMENT
A	VOLTAGE			
Req-1	Operating Voltage: generator mode		<9.6 V	
Req-2	Operating Voltage : motor mode		5.5V < V < 6.9V	
Req-3	Overvoltage Tolerance	9V ± 5%	9V ± 5%	Motor mode
B	CURRENT			
Req-1	Operating Current		220 mA < I < 260 mA	
Req-2	Fault Current Emission	< 275 mA	I < 250 mA	
C	IMPEDANCE			
Req-1	winding resistance	15 Ω ± 5 Ω		Including temperature range
Req-2	winding inductance	1mH < L < 4mH		
D	GROUDING AND ISOLATION			
Req-1	Insulation Impedance : Winding/case	≥ 10 MΩ		
Req-2	Insulation Impedance : Winding/: Winding	≥ 1 MΩ		
Req-3	Capacitance: Winding/case	≤ 10nF		

Table 42: Brush motor and PCB (SADP) interfaces

*

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Requirements

(AD01-P4)

Reference **SB4-SAT-AD1-P4-REQ-609****[FC Applicability: DATAM, POWER]**

The Brush motor interfaces (motor and Pcb (S4DSAP)) shall comply with the following characteristics :

Code	PARAMETERS	BRUSH MOTOR	MOTOR PCB (S4DSAP)	COMMENT
A	VOLTAGE			
Req-1	Over voltage emission		35 V *	* During less than 10 ms
Req-2	Supply voltage		22 V < V < 29 V	
B	CURRENT			
Req-1	Inrush Current	2 A for up to 10 ms		
Req-2	Operating Current		200 mA	
C	IMPEDANCE			
Req-1	Winding resistance	$38\Omega \pm 4\Omega$		At room temperature
Req-2	Winding inductance	$2\text{mH} < L < 3\text{mH}$		
D	GROUDING AND ISOLATION			
Req-1	Insulation Impedance : Winding/case	$\geq 10 \text{ M}\Omega$		
Req-2	Insulation Impedance : Winding/Winding	$\geq 1 \text{ M}\Omega$		
Req-3	Capacitance: Winding/case	$\leq 10\text{nF}$		

Table 43: Brush motor and PCB (S4DSAP) interfaces

*

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

6.10.3 Sensors Interfaces

6.10.3.1 Potentiometers Interfaces

Reference **SB4-SAT-AD1-P4-REQ-372 c**

[FC Applicability: ANTRACK, DATAM, MECHANISMS, POWER]

The potentiometers interfaces shall comply with the following characteristics (except for SADM motors):

Code	PARAMETERS	SOURCE SIDE	USER SIDE (motor pcb)	COMMENT
A	TYPE			
Req-1	Output	Floating		
B	IMPEDANCE			
Req-1	Resistance range	5 k Ω < R < 22 k Ω	> 3M Ω	
C	VOLTAGE			
Req-1	Maximum voltage	20 V	20 V	
D	GROUDING AND ISOLATION			
Req-1	Insulation resistance : leads	> 100M Ω 100V		

Table 44: Coarse and fine potentiometer characteristics

*

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Reference **SB4-SAT-AD1-P4-REQ-608**

[FC Applicability: ANTRACK, DATAM, MECHANISMS, POWER]

The SADM potentiometers interfaces shall comply with following characteristics:

Code	PARAMETERS	SOURCE SIDE	USER SIDE (SADP)	COMMENT
A	TYPE			
Req-1	Output	Floating		
B	IMPEDANCE			
Req-1	Resistance range	90 kΩ < R < 110 kΩ	> 3MΩ	
C	VOLTAGE			
Req-1	Maximum Voltage	20 V	20 V	
D	GROUDING AND ISOLATION			
Req-1	Insulation resistance : leads	> 100MΩ 100V		

Table 45: SADM Coarse potentiometer characteristics

*

6.10.3.2 Micro-switch Interface

DR single ended interface is applicable (See requirement SB4-SAT-AD1-P4-REQ-632)

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- Electrical Design and Interfaces

Requirements

(AD01-P4)

6.10.3.3 Optical switch interface

Reference **SB4-SAT-AD1-P4-REQ-377 c**

[FC Applicability: ANTRACK, DATAM, MECHANISMS, POWER]

The FSMP and SADP Pcb's shall be able to supply and acquire optical switch in compliance with the following characteristics :

<i>Parameter</i>	<i>Value</i>
Redundancy	cold redundancy
Power supply (Vs)	+5V (DC) \pm 5%
Max. Consumption (Vs=5V)	50 mA
Output interface	open collector (Compliant with DR Single ended acquisition: See SB4-SAT-AD1-P4-REQ-632)
Reference duration (tp)	> 5ms
Switching time (td)	< 100ms

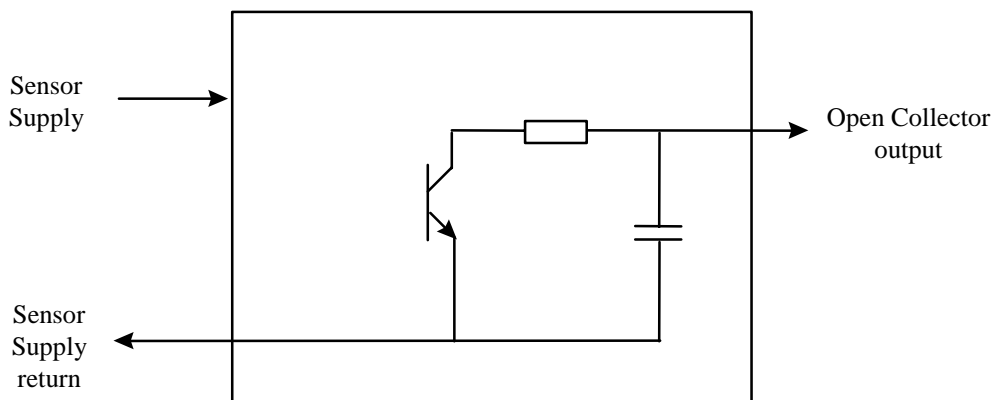


Figure 12: Optical switch electrical interface

*

SUBSYSTEM AND UNITS REQUIREMENTS

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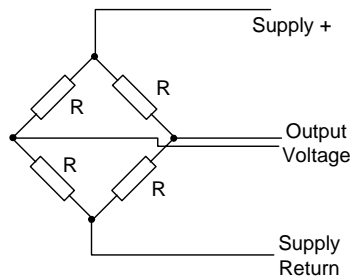
Requirements

(AD01-P4)

6.10.3.4 Strain gauge

Two types of strain gauge exists :

- one type for deployment
- two types for battery



6.10.3.4.1 Deployment strain gauge

Reference **SB4-SAT-AD1-P4-REQ-380 c**

[FC Applicability: ANTRACK, DATAM, MECHANISMS, POWER]

The deployment strain gauge interface shall comply with the following characteristics :

Code	PARAMETERS	SOURCE SIDE (Strain gauge)	Pcb SIDE	COMMENT
A	TYPE			
Req-1	Output	Floating		
B	VOLTAGE			
Req-1	Supply voltage		$13.6 \pm 10\%$	between strain gauge and SDMP : 6m of #26
Req-2	Output voltage (differential mode)	$-30\text{mV} < V_o < +30\text{mV}$		
Req-3	Output voltage (common mode)	$6.8 \pm 10\%$		
C	IMPEDANCE			
Req-1	gauge impedance (R)	700Ω or 350Ω		Wheaston bridge

Table 46: Deployment strain gauge characteristics

*

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Requirements

(AD01-P4)

6.10.3.4.2 Battery NiH2 Strain Gauge

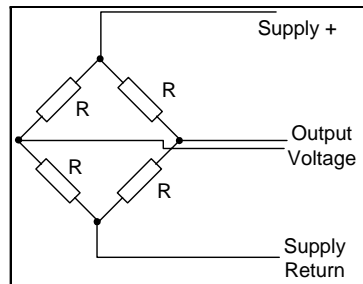


Figure 13: Battery strain gauge type 1

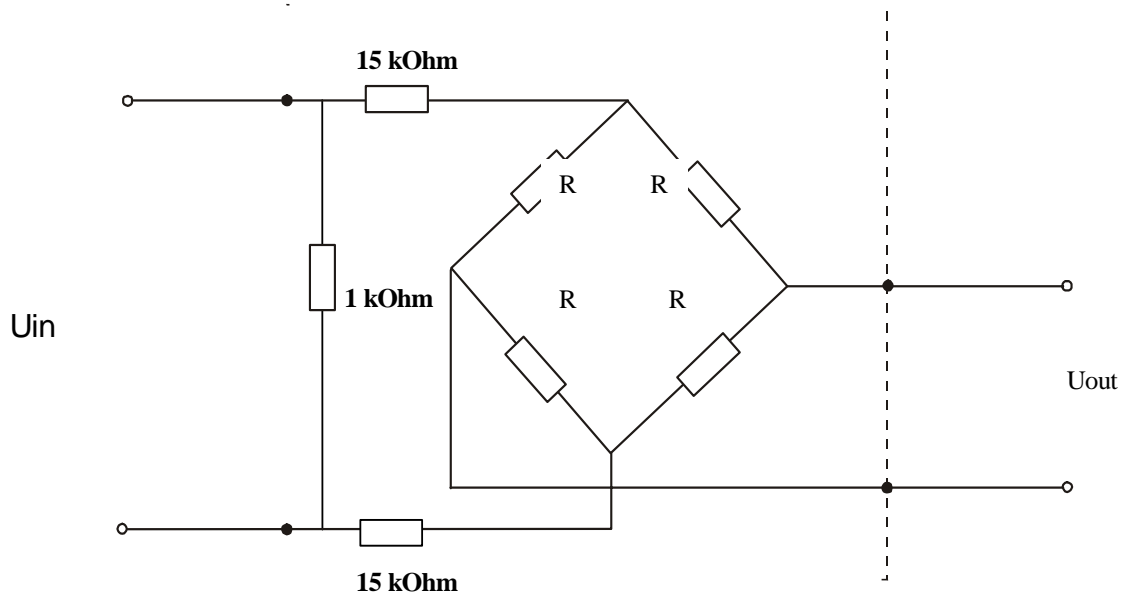


Figure 14: Battery strain gauge type 2

SUBSYSTEM AND UNITS REQUIREMENTS

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Requirements

(AD01-P4)

Reference **SB4-SAT-AD1-P4-REQ-381 b**

[FC Applicability: ANTRACK, DATAM, MECHANISMS, POWER]

The battery strain gauge interface (type1 and type2) shall comply with the following characteristics :

Code	PARAMETERS	Strain Gauge	Pcb SIDE	COMMENT
A	TYPE			
Req-1	Output	floating		
B	VOLTAGE			
Req-1	Supply voltage	10 V+/- 1%	10V, +1%, -0.9%	between strain gauge and BMP : 8m of #26
Req-2	Output voltage	< +30mV		
C	IMPEDANCE			
Req-1	Gauge type1 impedance (R)	350 Ω or 1000 $\Omega \pm 10\%$		Wheaston bridge - See figure Type1 Including Temperature range
Req-2	Gauge type2 impedance (R)	3000 $\Omega < R < 3500 \Omega$		Wheaston bridge - See figure Type2 Including Temperature range

Table 47: Battery strain gauge characteristics

*

6.11 PYRO Interfaces

Reference **SB4-SAT-AD1-P4-REQ-597**

[FC Applicability: ANTRACK, DATAM, HARNESS, MECHANISMS, POWER, PROP, ANTENNA]

All inactive wires in connection with the EED circuits shall be grounded and static discharge resistors of 100 K Ω shall be connected from the wires of the EED to the satellite structure.

*

Reference **SB4-SAT-AD1-P4-REQ-598**

[FC Applicability: ANTRACK, DATAM, HARNESS, MECHANISMS, POWER, PROP, ANTENNA]

Firing circuits between the power source and the EEDs shall be broken in both the positive and return lines at a safe/arm switch.

*

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

Reference **SB4-SAT-AD1-P4-REQ-599****[FC Applicability:** ANTRACK, DATAM, HARNESS, MECHANISMS, POWER, PROP, ANTENNA]

The PYRO interfaces (EED / PYPGP Pcb) shall comply with the following characteristics:

Code	PARAMETERS	SOURCE SIDE (PYPGP)	USER SIDE (Initiator)	COMMENT
A	TYPE			
Req-1	Output	Current source	Differential	
B	CURRENT			
Req-1	Minimum firing current	4.1A	4.1 A	
Req-2	Max no-fire current	<1A	1A-5min	
Req-3	Check out current		10mA	
Req-4	Max firing current	5.2A		during 250ms max
Req-5	Max battery input current in OFF state	<1mA		For one battery input (among 2)
C	IMPEDANCE			
Req-1	Bridge wire resistance		1.05 Ω +/- 0.1 Ω	
Req-2	Line resistance	$\leq 5 \Omega$		Total (harness + EED) resistance between Source and User (Return included)
E	TIME			
Req-1	Firing duration	0.015s < T < 0.1s	15ms min. @4.1A	
F	GROUDING AND ISOLATION			
Req-1	Insulation resistance to the chassis	<1 M Ω	$\geq 1 \text{ M}\Omega$	User side: R between shorted bridge wire and case
G	POWER SOURCE VOLTAGE			
Req-1	Voltage range with Lilon battery	28V < V < 37V	N/A	at PYPGP connector level, with or without firing current and with PYPGP=ON or OFF
Req-2	Voltage range with NiH2 battery, PYPGP=ON (firing or not)	28V < V < 40V	N/A	at PYPGP connector level
Req-3	Voltage range with NiH2 battery, PYPGP=OFF	28V < V < 44V	N/A	at PYPGP connector level

Table 48: PYRO interfaces characteristics

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Reference **SB4-SAT-AD1-P4-REQ-633**

[FC Applicability: ANTRACK, DATAM, HARNESS, MECHANISMS, POWER, PROP, ANTENNA]

The PYRO interfaces shall comply with the following characteristics with by-pass configuration:

Code	PARAMETERS	SOURCE SIDE (PYPGP)	USER SIDE (bypass + LMU)	COMMENT
A	TYPE			
Req-1	Output	Current source	Differential	
B	CURRENT			
Req-1	Minimum firing current	3.5A	3 A*	*considering a 100ms pulse
Req-2	Max no-fire current	<1mA	<1mA	
Req-4	Max firing current	5.2A		during 250ms max
Req-5	Max battery input current in OFF state	<1mA		For one battery input (among 2)
C	IMPEDANCE			
Req-1	Bypass Resistance		< 1 Ω	
Req-2	LMU switch (+ return) resistance		< 1 Ω	
Req-3	Total resistance	$\leq 5 \Omega$		Total (harness +LMU +bypass) resistance between Source and User (Return included)
E	TIME			
Req-1	Firing duration	0.1s < T < 0.25s	0.1s < T* < 0.25s	* with Firing current = 3A
F	GROUDING AND ISOLATION			
Req-1	Insulation resistance to the chassis	<1 M Ω	$\geq 1 \text{ M}\Omega$	
G	POWER SOURCE VOLTAGE			
Req-1	Voltage range with LiIon battery	28V < V < 37V	N/A	at PYPGP connector level, with or without firing current and with PYPGP=ON or OFF
H	OUTPUT VOLTAGE			
Req-1	Maximum dV/dt	<4V/ μ s	N/A	at PYPGP connector level,

Table 49: PYRO interfaces characteristics in by-pass configuration.

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(AD01-P4)

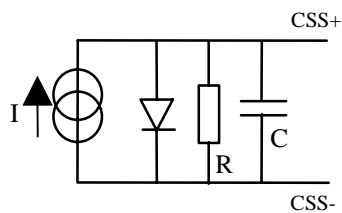
6.12 AOCS Interfaces

6.12.1 Coarse Sun Sensor interface

6.12.1.1 CSS current source

One CSS delivers 4 coarse analog detectors.

Schematic :



Reference **SB4-SAT-AD1-P4-REQ-385 c**

[FC Applicability: AOCS, DATAM]

The CSS current source interfaces (AOCSP/AOCSP_NG) shall be compliant to these characteristics :

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- Electrical Design and Interfaces

Requirements

(AD01-P4)

Code	PARAMETERS	SOURCE SIDE Analog detector	USER SIDE (AOCSP/AOCSP_NG)	COMMENT
A	VOLTAGE			
Req-1	Maximum fault voltage emission		$\pm 5 \text{ V}$	
Req-2	Permanent Fault voltage tolerance	$\pm 5 \text{ V}$		
B	CURRENT			
Req-1	Operating current range	$0 < I < 1 \text{ mA}$		
Req-2	Maximum current	10mA		
Req-3	Permanent current tolerance		10mA	
C	IMPEDANCE			
Req-1	Resistance (R)	$> 10 \text{ K}\Omega$		
Req-2	Capacitance (C)	$5 \text{ nF} \leq C \leq 17 \text{ nF}$		
D	FAILURE MODE			
Req-1	Failure Mode	<ul style="list-style-type: none"> ▪ Short circuit ▪ Open circuit ▪ Short circuit between wire + and structure ▪ Short circuit between wire - and structure 	Fail safe	

Table 50: CSS current source interfaces characteristics

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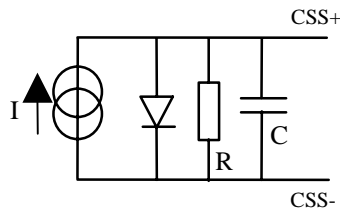
- Electrical Design and Interfaces

Requirements

(AD01-P4)

6.12.1.2 CSS voltage source

Schematic :



Reference **SB4-SAT-AD1-P4-REQ-605**

[FC Applicability: AOCS, DATAM]

The CSS voltage source interfaces (AOCSP_NG) shall be compliant to these characteristics:

Code	PARAMETERS	SOURCE SIDE Analog detector	USER SIDE AOCSP_NG	COMMENT
A	VOLTAGE			
Req-1	Maximum fault voltage emission		$\pm 15 \text{ V}$	
Req-2	Permanent Fault voltage tolerance	$\pm 15 \text{ V}$		
Req-3	Operating voltage range	$0 < V < 100 \text{ mV}$		
Req-4	Maximum voltage including failure	1 V		
Req-5	Permanent failure voltage tolerance		1 V	
B	IMPEDANCE			
Req-1	Source Impedance (R)	$< 10 \Omega$		Differential
Req-2	Load impedance		$> 75 \text{ K}\Omega$	Differential
Req-3	Capacitance (C)	$50 \text{ pF} \leq C \leq 17 \text{ nF}$		
C	FAILURE MODE			
Req-1	Failure Mode	<ul style="list-style-type: none"> ▪ Short circuit ▪ Open circuit ▪ Short circuit between wire + and structure ▪ Short circuit between wire - and structure 	Fail safe	

Table 51: CSS voltage source interfaces characteristics

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SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

6.12.2 Reaction Wheel interface

Each reaction wheel have 3 commands and 4 telemetries :

Commands :

- Torque command and Torque direction (interfaced by AOCSP) : PWM format
- ON/OFF command (2 ON and 2 OFF commands) : Low level Command

Telemetries :

- Tachometer (interfaced by AOCSP) : Frequency format
- Speed direction (interfaced by AOCSP) : Bi-level format
- Motor current (interfaced by AOCSP) : PWM format
- ON/OFF status : Switch closure
- Wheel NOGO (interfaced by AOCSP) : Bi-level format

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(AD01-P4)

Simplified schematic :

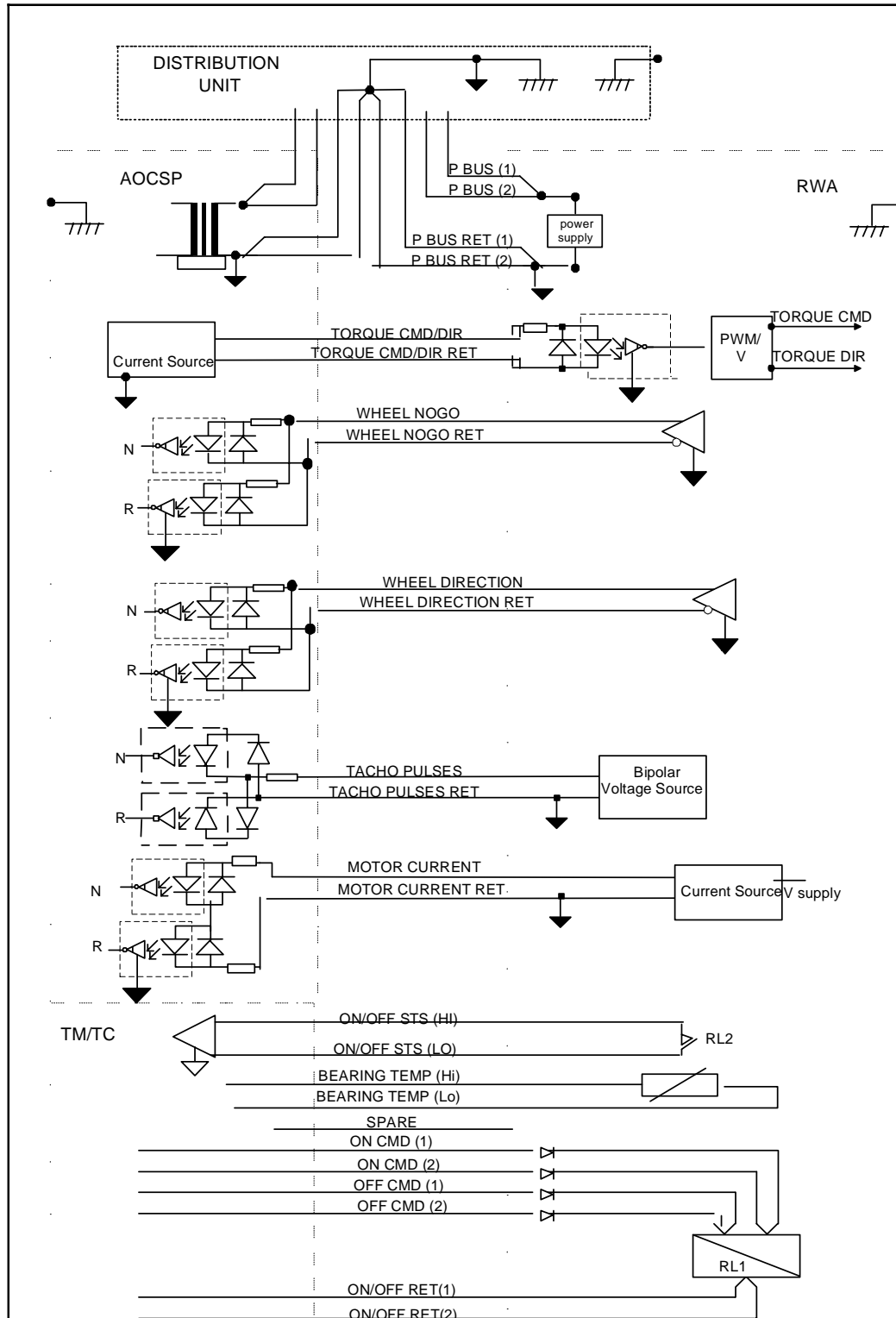


Figure 15: Reaction Wheel interfaces

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Requirements

(AD01-P4)

6.12.2.1 Torque command

The torque command useful range is 10% (= - torque max.) to 90% (= + torque max.).

Reference **SB4-SAT-AD1-P4-REQ-386 c**

[FC Applicability: AOCs, DATAM]

The torque command shall comply with the following table:

Code	PARAMETERS	SOURCE SIDE AOCSP	USER SIDE WHEEL	COMMENT
A	CURRENT			
Req-1	Low level current (discrete "0")	0mA \pm 0.25mA		
Req-2	High level current (discrete "1")	7mA < I _{hl} < 13mA		
B	VOLTAGE			
Req-1	Maximum Voltage drop		<1.9V at 13mA	
Req-2	Maximum differential Voltage	-1.5V < V _{diff} < 15V		
C	FREQUENCY			
Req-1	Operational frequency range	400 Hz \leq f \leq 600 Hz		
D	TIME			
Req-1	Rise/Fall time	<50ns		150 Ω ; 600 pF
E	ISOLATION			
Req-1	from primary ground (0Vp)	connected	isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	
Req-2	chassis		isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	

Table 52: Torque telecommand characteristics

*

SUBSYSTEM AND UNITS REQUIREMENTS

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Requirements

(AD01-P4)

6.12.2.2 Wheel direction and Wheel NOGO Telemetry

Reference **SB4-SAT-AD1-P4-REQ-387 c**

[FC Applicability: AOCS, DATAM]

The torque direction shall comply with these electrical characteristics :

Code	PARAMETERS	SOURCE SIDE WHEEL (1)	USER SIDE AOCSP	COMMENT
A	VOLTAGE			
Req-1	Low level differential voltage	0V to 1.5V		
Req-2	High level differential voltage	3.5V to 5.5V		
Req-3	Max Fault voltage emission	-5V to +5V		
B	CURRENT			
Req-1	Current capacity	>10mA		
Req-2	Load current		<10mA	
C	IMPEDANCE			
Req-1	Series resistor		>700 Ω	
D	ISOLATION			
Req-1	from primary ground (0Vp)	connected	isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	
Req-2	chassis		isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	

Table 53 :Wheel NOGO / direction telemetry characteristics

Signal Logic :

Hi="0" and Lo="1" (NOGO State // negative direction)

Hi="1" and Lo="0" (GO State // positive direction)

The interface definition is set up so that current must flow through the optocoupler in order to establish a GO state (positive direction).

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SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

6.12.2.3 Tachometer telemetry

Reference **SB4-SAT-AD1-P4-REQ-388 b**

[FC Applicability: AOCS, DATAM]

The Tachometer interface shall be compliant with the following table :

Code	PARAMETERS	SOURCE SIDE WHEEL	USER SIDE AOCSP	COMMENT
A	VOLTAGE			
Req-1	Low level voltage	-12V \pm 2V		Current capacity : >15mA
Req-2	High level voltage	+12V \pm 2V		
Req-2	Fault voltage emission	\pm 15V		
B	IMPEDANCE			
Req-1	Load impedance		>400 Ω	
Req-2	Source impedance	< 200 Ω		
C	TIME			
Req-1	Minimum Pulse duration	<10 μ s		
D	FREQUENCY			
Req-1	Operating frequency range		0 Hz \leq f \leq 3200 Hz	The wheel tachometer generates 24 pulses per revolution and the maximum speed is 8000 revolution per minute
E	ISOLATION			
Req-1	from primary ground (0Vp)	connected	isolated \geq 1 M Ω // \leq 50 nF	
Req-2	chassis		isolated \geq 1 M Ω // \leq 50 nF	

Table 54 :Tachometer telemetry characteristics

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SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

6.12.2.4 Motor current telemetry : PWM

The motor current is a PWM signal. 10% modulation corresponds to no current, while 90% modulation corresponds to maximum current.

Reference **SB4-SAT-AD1-P4-REQ-390 c**

[FC Applicability: AOCSP, DATAM]

The motor current AOCSP interface shall be compliant with the following table :

Code	PARAMETERS	SOURCE SIDE WHEEL	USER SIDE AOCSP	COMMENT
A	VOLTAGE			
Req-1	Low level voltage	$0 \pm 1.5V$		
Req-2	High level voltage	$12V \pm 2V$		
B	VOLTAGE			
Req-1	Maximum Voltage drop		$2 * 1.9V$ at 13mA	
C	IMPEDANCE			
Req-1	Load impedance		$> 400 \Omega$	
Req-2	Source impedance	$< 400 \Omega$		
D	FREQUENCY			
Req-1	Nominal frequency	$10 \text{ kHz} \pm 2\text{kHz}$		
E	TIME			
Req-1	Rise/Fall Time	$< 500 \text{ ns}$		$150\Omega ; 600\text{pF}$
F	ISOLATION			
Req-1	from primary ground (0Vp)	connected	isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	
Req-2	chassis		isolated $\geq 1 \text{ M}\Omega // \leq 50 \text{ nF}$	

Table 55 :Motor current characteristics

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SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

6.13 Data Bus interfaces

Two types of Data bus are available on SB4000 :

- OBDH - 485
- 1553

The nominal bus is OBDH - 485.

The use of 1553 bus is limited to AOCS equipments :

- Startracker
- Gyro
- IRES

6.13.1 OBDH - 485

The "Data Bus Network Electrical and Protocol Specification" (SBF 6AV2 AS SP 338) document comprises the requirements to be satisfied by the OBDH-485.
(See chapter "Applicable documents")

6.13.2 1553 BUS INTERFACE

The Bus 1553 Applicable documents comprise the requirements to be satisfied by the bus 1553.
(See chapter "Applicable documents")

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

ANNEX 1: CHANGE TRACEABILITY

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-001 b]	AD-AV4-AD01_Part4-3.1-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-638]		New in	3
[SB4-SAT-AD1-P4-REQ-002 b]	AD-AV4-AD01_Part4-3.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-003 b]	AD-AV4-AD01_Part4-3.2.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-004 b]	AD-AV4-AD01_Part4-3.2.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-005 b]	AD-AV4-AD01_Part4-3.5-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-006 b]	AD-AV4-AD01_Part4-3.6-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-610]		New in	3
[SB4-SAT-AD1-P4-REQ-007 c]	AD-AV4-AD01_Part4-3.8.1.1-001/b	Deleted in	3
[SB4-SAT-AD1-P4-REQ-008 b]	AD-AV4-AD01_Part4-3.8.1.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-544]		New in	3
[SB4-SAT-AD1-P4-REQ-009 b]	AD-AV4-AD01_Part4-3.8.2-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-400]		New in	3
[SB4-SAT-AD1-P4-REQ-010 b]	AD-AV4-AD01_Part4-3.8.2-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-011 b]	AD-AV4-AD01_Part4-3.8.2-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-012 b]	AD-AV4-AD01_Part4-3.8.2-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-013 b]	AD-AV4-AD01_Part4-3.8.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-014 b]	AD-AV4-AD01_Part4-3.8.3-002/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-401]		New in	3
[SB4-SAT-AD1-P4-REQ-015 b]	AD-AV4-AD01_Part4-3.9.1.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-016 c]	AD-AV4-AD01_Part4-3.9.1.2-001/b	Deleted in	3
[SB4-SAT-AD1-P4-REQ-017 b]	AD-AV4-AD01_Part4-3.10-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-018 b]	AD-AV4-AD01_Part4-3.10-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-019 b]	AD-AV4-AD01_Part4-3.11.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-020 b]	AD-AV4-AD01_Part4-3.11.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-021 b]	AD-AV4-AD01_Part4-3.11.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-022 b]	AD-AV4-AD01_Part4-3.12.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-023 b]	AD-AV4-AD01_Part4-3.14.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-024 b]	AD-AV4-AD01_Part4-3.14.2-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-025 b]	AD-AV4-AD01_Part4-3.14.2-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-026 b]	AD-AV4-AD01_Part4-3.14.2-003/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-027 b]	AD-AV4-AD01_Part4-3.14.2-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-028 b]	AD-AV4-AD01_Part4-3.14.2-005/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-029 b]	AD-AV4-AD01_Part4-3.14.2-006/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-030 b]	AD-AV4-AD01_Part4-3.14.2-007/a	Deleted in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-031 b]	AD-AV4-AD01_Part4-3.14.2-008/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-032 b]	AD-AV4-AD01_Part4-3.14.2-009/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-033 b]	AD-AV4-AD01_Part4-3.15.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-034 b]	AD-AV4-AD01_Part4-3.15.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-035 b]	AD-AV4-AD01_Part4-3.15.2-002/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-036 b]	AD-AV4-AD01_Part4-3.15.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-037 b]	AD-AV4-AD01_Part4-4.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-038 b]	AD-AV4-AD01_Part4-4.2-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-039 b]	AD-AV4-AD01_Part4-4.2-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-040 b]	AD-AV4-AD01_Part4-4.2.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-041 b]	AD-AV4-AD01_Part4-4.2.1-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-042 b]	AD-AV4-AD01_Part4-4.2.1-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-043 b]	AD-AV4-AD01_Part4-4.2.1-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-044 b]	AD-AV4-AD01_Part4-4.2.1-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-045 b]	AD-AV4-AD01_Part4-4.2.1-006/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-046 c]	AD-AV4-AD01_Part4-4.2.1-007/b	Deleted in	3
[SB4-SAT-AD1-P4-REQ-048 b]	AD-AV4-AD01_Part4-4.2.1-009/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-049 b]	AD-AV4-AD01_Part4-4.2.1-010/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-050 b]	AD-AV4-AD01_Part4-4.2.1-011/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-051 b]	AD-AV4-AD01_Part4-4.2.1-012/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-052 b]	AD-AV4-AD01_Part4-4.2.1-013/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-053 b]	AD-AV4-AD01_Part4-4.2.1-014/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-054 b]	AD-AV4-AD01_Part4-4.2.1-015/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-055 b]	AD-AV4-AD01_Part4-4.2.1-016/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-056 b]	AD-AV4-AD01_Part4-4.2.1-017/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-057 b]	AD-AV4-AD01_Part4-4.2.1-018/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-058 b]	AD-AV4-AD01_Part4-4.2.1-019/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-059 c]	AD-AV4-AD01_Part4-4.2.1-020/b	Deleted in	3
[SB4-SAT-AD1-P4-REQ-060 b]	AD-AV4-AD01_Part4-4.2.1-021/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-061 b]	AD-AV4-AD01_Part4-4.2.1-022/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-062 b]	AD-AV4-AD01_Part4-4.2.1-023/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-063 b]	AD-AV4-AD01_Part4-4.2.1-024/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-064 b]	AD-AV4-AD01_Part4-4.2.2.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-065 b]	AD-AV4-AD01_Part4-4.2.2.1-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-066 b]	AD-AV4-AD01_Part4-4.2.2.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-067 b]	AD-AV4-AD01_Part4-4.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-068 b]	AD-AV4-AD01_Part4-4.3-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-069 b]	AD-AV4-AD01_Part4-4.3-003/a	Deleted in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-070 b]	AD-AV4-AD01_Part4-4.3.1.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-071 b]	AD-AV4-AD01_Part4-4.3.1.1-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-072 b]	AD-AV4-AD01_Part4-4.3.1.1-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-073 b]	AD-AV4-AD01_Part4-4.3.1.1-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-074 b]	AD-AV4-AD01_Part4-4.3.1.1-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-075 b]	AD-AV4-AD01_Part4-4.3.1.1-006/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-076 b]	AD-AV4-AD01_Part4-4.3.1.1-007/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-077 b]	AD-AV4-AD01_Part4-4.3.1.1-008/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-078 b]	AD-AV4-AD01_Part4-4.3.1.1-009/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-079 b]	AD-AV4-AD01_Part4-4.3.1.1-010/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-080 b]	AD-AV4-AD01_Part4-4.3.1.1-011/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-081 b]	AD-AV4-AD01_Part4-4.3.1.1-012/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-082 b]	AD-AV4-AD01_Part4-4.3.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-083 b]	AD-AV4-AD01_Part4-4.3.2-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-084 b]	AD-AV4-AD01_Part4-4.3.2-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-085 b]	AD-AV4-AD01_Part4-4.3.2-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-086 b]	AD-AV4-AD01_Part4-4.3.2.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-087 b]	AD-AV4-AD01_Part4-4.3.2.1-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-088 b]	AD-AV4-AD01_Part4-4.3.2.1-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-089 b]	AD-AV4-AD01_Part4-4.3.2.1-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-090 b]	AD-AV4-AD01_Part4-4.3.2.1-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-091 b]	AD-AV4-AD01_Part4-4.3.2.1-006/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-092 b]	AD-AV4-AD01_Part4-4.3.2.1-007/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-093 b]	AD-AV4-AD01_Part4-4.3.2.1-008/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-094 b]	AD-AV4-AD01_Part4-4.3.2.1-009/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-095 b]	AD-AV4-AD01_Part4-4.3.2.1-010/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-096 b]	AD-AV4-AD01_Part4-4.3.2.1-011/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-097 b]	AD-AV4-AD01_Part4-4.3.2.1-012/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-098 b]	AD-AV4-AD01_Part4-4.3.2.1-013/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-099 b]	AD-AV4-AD01_Part4-4.3.2.1-014/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-100 b]	AD-AV4-AD01_Part4-4.3.2.1-015/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-101 b]	AD-AV4-AD01_Part4-4.3.2.1-016/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-102 b]	AD-AV4-AD01_Part4-4.3.2.1-017/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-103 b]	AD-AV4-AD01_Part4-4.3.2.1-018/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-104 b]	AD-AV4-AD01_Part4-4.3.2.1-019/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-105 b]	AD-AV4-AD01_Part4-4.3.2.1-020/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-106 b]	AD-AV4-AD01_Part4-4.3.2.1-021/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-107 b]	AD-AV4-AD01_Part4-4.3.2.1-022/a	Deleted in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-108 b]	AD-AV4-AD01_Part4-4.3.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-109 b]	AD-AV4-AD01_Part4-4.4-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-110 b]	AD-AV4-AD01_Part4-4.4-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-111 b]	AD-AV4-AD01_Part4-4.4-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-112 b]	AD-AV4-AD01_Part4-4.4-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-113 b]	AD-AV4-AD01_Part4-4.4-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-114 b]	AD-AV4-AD01_Part4-4.5.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-115 b]	AD-AV4-AD01_Part4-4.5.1-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-116 b]	AD-AV4-AD01_Part4-4.5.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-117 b]	AD-AV4-AD01_Part4-4.5.2-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-118 b]	AD-AV4-AD01_Part4-4.6-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-119 b]	AD-AV4-AD01_Part4-4.6-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-120 b]	AD-AV4-AD01_Part4-4.6-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-121 b]	AD-AV4-AD01_Part4-4.6.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-122 b]	AD-AV4-AD01_Part4-4.6.1-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-123 b]	AD-AV4-AD01_Part4-4.6.1-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-124 b]	AD-AV4-AD01_Part4-4.6.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-125 b]	AD-AV4-AD01_Part4-4.6.2-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-126 b]	AD-AV4-AD01_Part4-4.7-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-127 b]	AD-AV4-AD01_Part4-4.7-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-128 b]	AD-AV4-AD01_Part4-4.8-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-129 c]	AD-AV4-AD01_Part4-4.8-002/b	Deleted in	3
[SB4-SAT-AD1-P4-REQ-406]	SB-AD01.3-4.03-010	New in	3
[SB4-SAT-AD1-P4-REQ-407]	SB-AD01.3-4.03-011	New in	3
[SB4-SAT-AD1-P4-REQ-410]	SB-AD01.3-4.03-014	New in	3
[SB4-SAT-AD1-P4-REQ-411]	SB-AD01.3-4.03-015	New in	3
[SB4-SAT-AD1-P4-REQ-412]	SB-AD01.3-4.02-006	New in	3
[SB4-SAT-AD1-P4-REQ-415]	SB-AD01.3-4.02-011	New in	3
[SB4-SAT-AD1-P4-REQ-417]	SB-AD01.3-4.02-012	New in	3
[SB4-SAT-AD1-P4-REQ-418]	SB-AD01.3-4.02-013	New in	3
[SB4-SAT-AD1-P4-REQ-419]	SB-AD01.3-4.02-013	New in	3
[SB4-SAT-AD1-P4-REQ-611]		New in	3
[SB4-SAT-AD1-P4-REQ-420]	SB-AD01.3-4.02-015	New in	3
[SB4-SAT-AD1-P4-REQ-421]	SB-AD01.3-4.02-015	New in	3
[SB4-SAT-AD1-P4-REQ-425]	SB-AD01.3-4.02-019	New in	3
[SB4-SAT-AD1-P4-REQ-423]	SB-AD01.3-4.02-018	New in	3
[SB4-SAT-AD1-P4-REQ-424]	SB-AD01.3-4.02-018	New in	3
[SB4-SAT-AD1-P4-REQ-426]	SB-AD01.3-4.02-020	New in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-427]	SB-AD01.3-4.02-021	New in	3
[SB4-SAT-AD1-P4-REQ-428]	SB-AD01.3-4.02-021	New in	3
[SB4-SAT-AD1-P4-REQ-429]	SB-AD01.3-4.02-004	New in	3
[SB4-SAT-AD1-P4-REQ-430]	SB-AD01.3-4.02-005	New in	3
[SB4-SAT-AD1-P4-REQ-431]	SB-AD01.3-4.02-022	New in	3
[SB4-SAT-AD1-P4-REQ-433]	SB-AD01.3-4.02-023	New in	3
[SB4-SAT-AD1-P4-REQ-435]	SB-AD01.3-4.02-026	New in	3
[SB4-SAT-AD1-P4-REQ-436]	SB-AD01.3-4.02-027	New in	3
[SB4-SAT-AD1-P4-REQ-631]		New in	3
[SB4-SAT-AD1-P4-REQ-438]	SB-AD01.3-4.02-029	New in	3
[SB4-SAT-AD1-P4-REQ-439]	SB-AD01.3-4.02-030	New in	3
[SB4-SAT-AD1-P4-REQ-440]	SB-AD01.3-4.02-031	New in	3
[SB4-SAT-AD1-P4-REQ-624]	SB-AD01.3-4.02-048	New in	3
[SB4-SAT-AD1-P4-REQ-488]	SB-AD01.3-4.03-046	New in	3
[SB4-SAT-AD1-P4-REQ-454]	SB-AD01.3-4.03-035	New in	3
[SB4-SAT-AD1-P4-REQ-459]	SB-AD01.3-4.03-040	New in	3
[SB4-SAT-AD1-P4-REQ-460]	SB-AD01.3-4.03-041	New in	3
[SB4-SAT-AD1-P4-REQ-449]	SB-AD01.3-4.03-006	New in	3
[SB4-SAT-AD1-P4-REQ-450]	SB-AD01.3-4.03-008	New in	3
[SB4-SAT-AD1-P4-REQ-451]		New in	3
[SB4-SAT-AD1-P4-REQ-456]	SB-AD01.3-4.03-037	New in	3
[SB4-SAT-AD1-P4-REQ-596]		New in	3
[SB4-SAT-AD1-P4-REQ-409]	SB-AD01.3-4.03-013	New in	3
[SB4-SAT-AD1-P4-REQ-461]	SB-AD01.3-4.03-042	New in	3
[SB4-SAT-AD1-P4-REQ-462]	SB-AD01.3-4.03-043	New in	3
[SB4-SAT-AD1-P4-REQ-475]	SB-AD01.3-4.03-019	New in	3
[SB4-SAT-AD1-P4-REQ-476]	SB-AD01.3-4.03-020	New in	3
[SB4-SAT-AD1-P4-REQ-477]	SB-AD01.3-4.03-021	New in	3
[SB4-SAT-AD1-P4-REQ-479]	SB-AD01.3-4.03-023	New in	3
[SB4-SAT-AD1-P4-REQ-481]	SB-AD01.3-4.03-025	New in	3
[SB4-SAT-AD1-P4-REQ-482]	SB-AD01.3-4.03-026	New in	3
[SB4-SAT-AD1-P4-REQ-483]	SB-AD01.3-4.03-027	New in	3
[SB4-SAT-AD1-P4-REQ-484]	SB-AD01.3-4.03-028	New in	3
[SB4-SAT-AD1-P4-REQ-485]	SB-AD01.3-4.03-029	New in	3
[SB4-SAT-AD1-P4-REQ-489]	SB-AD01.3-4.03-047	New in	3
[SB4-SAT-AD1-P4-REQ-492]	SB-AD01.3-4.03-050	New in	3
[SB4-SAT-AD1-P4-REQ-493]	SB-AD01.3-4.03-051	New in	3
[SB4-SAT-AD1-P4-REQ-494]	SB-AD01.3-4.03-052	New in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-495]	SB-AD01.3-4.03-053	New in	3
[SB4-SAT-AD1-P4-REQ-606]		New in	3
[SB4-SAT-AD1-P4-REQ-497]	SB-AD01.3-4.03-056	New in	3
[SB4-SAT-AD1-P4-REQ-582]	SB-AD01.3-4.03-059	New in	3
[SB4-SAT-AD1-P4-REQ-490]	SB-AD01.3-4.03-048	New in	3
[SB4-SAT-AD1-P4-REQ-491]	SB-AD01.3-4.03-049	New in	3
[SB4-SAT-AD1-P4-REQ-498]	SB-AD01.3-4.04-002	New in	3
[SB4-SAT-AD1-P4-REQ-499]	SB-AD01.3-4.04-002	New in	3
[SB4-SAT-AD1-P4-REQ-507]	SB-AD01.3-4.04-007	New in	3
[SB4-SAT-AD1-P4-REQ-508]	SB-AD01.3-4.04-007	New in	3
[SB4-SAT-AD1-P4-REQ-506]	SB-AD01.3-4.04-006	New in	3
[SB4-SAT-AD1-P4-REQ-510]	SB-AD01.3-4.04-015	New in	3
[SB4-SAT-AD1-P4-REQ-614]		New in	3
[SB4-SAT-AD1-P4-REQ-511]	SB-AD01.3-4.04-024	New in	3
[SB4-SAT-AD1-P4-REQ-512]	SB-AD01.3-4.04-025	New in	3
[SB4-SAT-AD1-P4-REQ-615]		New in	3
[SB4-SAT-AD1-P4-REQ-518]	SB-AD01.3-4.04-033	New in	3
[SB4-SAT-AD1-P4-REQ-513]	SB-AD01.3-4.04-015	New in	3
[SB4-SAT-AD1-P4-REQ-515]	SB-AD01.3-4.04-029	New in	3
[SB4-SAT-AD1-P4-REQ-517]		New in	3
[SB4-SAT-AD1-P4-REQ-501]	SB-AD01.3-4.04-005	New in	3
[SB4-SAT-AD1-P4-REQ-502]	SB-AD01.3-4.04-005	New in	3
[SB4-SAT-AD1-P4-REQ-503]	SB-AD01.3-4.04-005	New in	3
[SB4-SAT-AD1-P4-REQ-504]	SB-AD01.3-4.04-005	New in	3
[SB4-SAT-AD1-P4-REQ-505]	SB-AD01.3-4.04-005	New in	3
[SB4-SAT-AD1-P4-REQ-394 b]	AD-AV4-AD01_Part4-6.15.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-395 b]	AD-AV4-AD01_Part4-6.15.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-396 b]	AD-AV4-AD01_Part4-6.16.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-519]	SB-AD01.3-4.05-001	New in	3
[SB4-SAT-AD1-P4-REQ-520]	SB-AD01.3-4.05-002	New in	3
[SB4-SAT-AD1-P4-REQ-521]	SB-AD01.3-4.05-003	New in	3
[SB4-SAT-AD1-P4-REQ-522]	SB-AD01.3-4.05-005	New in	3
[SB4-SAT-AD1-P4-REQ-523]	SB-AD01.3-4.05-005	New in	3
[SB4-SAT-AD1-P4-REQ-524]		New in	3
[SB4-SAT-AD1-P4-REQ-525]	SB-AD01.3-4.05-007	New in	3
[SB4-SAT-AD1-P4-REQ-526]	SB-AD01.3-4.05-008	New in	3
[SB4-SAT-AD1-P4-REQ-539]	SB-AD01.3-4.05-044	New in	3
[SB4-SAT-AD1-P4-REQ-540]	SB-AD01.3-4.05-045	New in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-541]	SB-AD01.3-4.05-047	New in	3
[SB4-SAT-AD1-P4-REQ-509]	SB-AD01.3-4.04-009	New in	3
[SB4-SAT-AD1-P4-REQ-514]	SB-AD01.3-4.04-028	New in	3
[SB4-SAT-AD1-P4-REQ-623]		New in	3
[SB4-SAT-AD1-P4-REQ-639]	SB-AD01.3-4.04-019	New in	3
[SB4-SAT-AD1-P4-REQ-619]		New in	3
[SB4-SAT-AD1-P4-REQ-537]	SB-AD01.3-4.05-041	New in	3
[SB4-SAT-AD1-P4-REQ-538]	SB-AD01.3-4.05-042	New in	3
[SB4-SAT-AD1-P4-REQ-528]	SB-AD01.3-4.05-017	New in	3
[SB4-SAT-AD1-P4-REQ-529]	SB-AD01.3-4.05-018	New in	3
[SB4-SAT-AD1-P4-REQ-600]	SB-AD01.3-4.05-033	New in	3
[SB4-SAT-AD1-P4-REQ-640]		New in	3
[SB4-SAT-AD1-P4-REQ-641]	SB-AD01.3-4.05-034	New in	3
[SB4-SAT-AD1-P4-REQ-533]	SB-AD01.3-4.05-027	New in	3
[SB4-SAT-AD1-P4-REQ-534]	SB-AD01.3-4.05-028	New in	3
[SB4-SAT-AD1-P4-REQ-535]	SB-AD01.3-4.05-031	New in	3
[SB4-SAT-AD1-P4-REQ-545]		New in	3
[SB4-SAT-AD1-P4-REQ-532]	SB-AD01.3-4.05-026	New in	3
[SB4-SAT-AD1-P4-REQ-542]	SB-AD01.3-4.05-053	New in	3
[SB4-SAT-AD1-P4-REQ-205 b]	AD-AV4-AD01_Part4-6.1.6.1.2-011/a	Modified in, Moved in	3
[SB4-SAT-AD1-P4-REQ-206 b]	AD-AV4-AD01_Part4-6.1.6.1.2-012/a	Modified in, Moved in	3
[SB4-SAT-AD1-P4-REQ-208 b]	AD-AV4-AD01_Part4-6.1.6.1.4-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-209 c]	AD-AV4-AD01_Part4-6.1.6.1.4-002/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-536]	SB-AD01.3-4.05-036	New in	3
[SB4-SAT-AD1-P4-REQ-543]	SB-AD01.3-4.05-054	New in	3
[SB4-SAT-AD1-P4-REQ-130 b]	AD-AV4-AD01_Part4-5.1.1.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-132 c]	AD-AV4-AD01_Part4-5.1.2.1-001/b	Deleted in	3
[SB4-SAT-AD1-P4-REQ-133 c]	AD-AV4-AD01_Part4-5.1.2.2-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-134 b]	AD-AV4-AD01_Part4-5.1.3-001/aAD-AV4-AD01_Part4-5.1.3-001/a :	Modified in	3
[SB4-SAT-AD1-P4-REQ-135 c]	AD-AV4-AD01_Part4-5.1.3-002/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-138 c]	AD-AV4-AD01_Part4-5.1.4-003/b	Deleted in	3
[SB4-SAT-AD1-P4-REQ-145 b]	AD-AV4-AD01_Part4-5.1.5-007/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-140 b]	AD-AV4-AD01_Part4-5.1.5-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-616]		New in	3
[SB4-SAT-AD1-P4-REQ-464]	SB-AD01.3-4.05-039	New in	3
[SB4-SAT-AD1-P4-REQ-617]		New in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-618]		New in	3
[SB4-SAT-AD1-P4-REQ-465]		New in	3
[SB4-SAT-AD1-P4-REQ-141 b]	AD-AV4-AD01_Part4-5.1.5-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-142 b]	AD-AV4-AD01_Part4-5.1.5-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-143 b]	AD-AV4-AD01_Part4-5.1.5-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-144 b]	AD-AV4-AD01_Part4-5.1.5-006/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-146 c]	AD-AV4-AD01_Part4-5.1.5-008/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-147 b]	AD-AV4-AD01_Part4-5.1.5-009/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-148 c]	AD-AV4-AD01_Part4-5.1.5-010/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-149 c]	AD-AV4-AD01_Part4-5.1.5-011/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-603]		New in	3
[SB4-SAT-AD1-P4-REQ-150 b]	AD-AV4-AD01_Part4-5.2.1-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-151 b]	AD-AV4-AD01_Part4-5.2.1-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-152 b]	AD-AV4-AD01_Part4-5.2.1-003/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-153 b]	AD-AV4-AD01_Part4-5.2.1-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-154 b]	AD-AV4-AD01_Part4-5.2.1-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-155 b]	AD-AV4-AD01_Part4-5.2.1-006/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-156 b]	AD-AV4-AD01_Part4-5.2.1-007/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-157 b]	AD-AV4-AD01_Part4-5.2.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-158 b]	AD-AV4-AD01_Part4-5.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-159 b]	AD-AV4-AD01_Part4-5.4-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-160 b]	AD-AV4-AD01_Part4-5.4-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-161 b]	AD-AV4-AD01_Part4-5.5-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-162 b]	AD-AV4-AD01_Part4-5.6.1-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-163 b]	AD-AV4-AD01_Part4-5.6.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-164 b]	AD-AV4-AD01_Part4-5.7-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-165 b]	AD-AV4-AD01_Part4-5.7-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-166 b]	AD-AV4-AD01_Part4-5.7-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-167 b]	AD-AV4-AD01_Part4-5.7-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-168 b]	AD-AV4-AD01_Part4-5.8.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-169 b]	AD-AV4-AD01_Part4-5.8.1-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-171 b]	AD-AV4-AD01_Part4-5.8.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-172 b]	AD-AV4-AD01_Part4-5.8.3-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-442]	SB-AD01.3-4.02-033	New in	3
[SB4-SAT-AD1-P4-REQ-173 b]	AD-AV4-AD01_Part4-6.1.2.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-174 b]	AD-AV4-AD01_Part4-6.1.2.1-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-175 b]	AD-AV4-AD01_Part4-6.1.2.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-176 b]	AD-AV4-AD01_Part4-6.1.2.3-002/a	Deleted in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-177 b]	AD-AV4-AD01_Part4-6.1.4-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-178 b]	AD-AV4-AD01_Part4-6.1.5-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-210 b]	AD-AV4-AD01_Part4-6.1.6.1.4-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-211 b]	AD-AV4-AD01_Part4-6.1.6.1.4-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-212 b]	AD-AV4-AD01_Part4-6.1.6.1.4-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-213 b]	AD-AV4-AD01_Part4-6.1.6.1.4-006/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-214 b]	AD-AV4-AD01_Part4-6.1.6.1.4-007/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-215 b]	AD-AV4-AD01_Part4-6.1.6.1.4-008/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-216 b]	AD-AV4-AD01_Part4-6.1.6.1.4-009/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-217 b]	AD-AV4-AD01_Part4-6.1.6.1.4-010/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-218 b]	AD-AV4-AD01_Part4-6.1.6.1.4-011/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-219 b]	AD-AV4-AD01_Part4-6.1.6.1.4-012/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-220 c]	AD-AV4-AD01_Part4-6.1.6.1.4-013/b	Deleted in	3
[SB4-SAT-AD1-P4-REQ-179 b]	AD-AV4-AD01_Part4-6.1.6.1.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-180 b]	AD-AV4-AD01_Part4-6.1.6.1.1-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-181 b]	AD-AV4-AD01_Part4-6.1.6.1.1-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-182 b]	AD-AV4-AD01_Part4-6.1.6.1.1-004/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-183 b]	AD-AV4-AD01_Part4-6.1.6.1.1-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-185 b]	AD-AV4-AD01_Part4-6.1.6.1.1-007/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-186 b]	AD-AV4-AD01_Part4-6.1.6.1.1-008/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-187 b]	AD-AV4-AD01_Part4-6.1.6.1.1-009/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-188 b]	AD-AV4-AD01_Part4-6.1.6.1.1-010/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-189 b]	AD-AV4-AD01_Part4-6.1.6.1.1-011/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-190 b]	AD-AV4-AD01_Part4-6.1.6.1.1-012/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-191 b]	AD-AV4-AD01_Part4-6.1.6.1.1-013/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-621]		New in	3
[SB4-SAT-AD1-P4-REQ-622]		New in	3
[SB4-SAT-AD1-P4-REQ-196 c]	AD-AV4-AD01_Part4-6.1.6.1.2-002/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-637]		New in	3
[SB4-SAT-AD1-P4-REQ-197 b]	AD-AV4-AD01_Part4-6.1.6.1.2-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-198 b]	AD-AV4-AD01_Part4-6.1.6.1.2-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-199 b]	AD-AV4-AD01_Part4-6.1.6.1.2-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-200 b]	AD-AV4-AD01_Part4-6.1.6.1.2-006/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-201 b]	AD-AV4-AD01_Part4-6.1.6.1.2-007/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-203 b]	AD-AV4-AD01_Part4-6.1.6.1.2-009/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-204 b]	AD-AV4-AD01_Part4-6.1.6.1.2-010/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-207 b]	AD-AV4-AD01_Part4-6.1.6.1.2-013/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-221 b]	AD-AV4-AD01_Part4-6.1.6.2.1-001/a	Deleted in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-222 b]	AD-AV4-AD01_Part4-6.1.6.2.1-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-223 b]	AD-AV4-AD01_Part4-6.1.6.2.1-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-224 b]	AD-AV4-AD01_Part4-6.1.6.2.1-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-225 b]	AD-AV4-AD01_Part4-6.1.6.2.1-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-226 b]	AD-AV4-AD01_Part4-6.1.6.2.2-001/a:	Deleted in	3
[SB4-SAT-AD1-P4-REQ-227 b]	AD-AV4-AD01_Part4-6.1.6.2.2-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-228 b]	AD-AV4-AD01_Part4-6.1.6.2.2-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-229 b]	AD-AV4-AD01_Part4-6.1.6.2.2-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-230 b]	AD-AV4-AD01_Part4-6.1.6.2.2-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-231 b]	AD-AV4-AD01_Part4-6.1.6.2.2-006/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-232 b]	AD-AV4-AD01_Part4-6.1.6.2.2-007/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-202 b]	AD-AV4-AD01_Part4-6.1.6.1.2-008/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-235 b]	AD-AV4-AD01_Part4-6.1.6.3-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-236 b]	AD-AV4-AD01_Part4-6.1.6.3-002/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-237 b]	AD-AV4-AD01_Part4-6.1.6.3-003/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-630]		New in	3
[SB4-SAT-AD1-P4-REQ-233 b]	AD-AV4-AD01_Part4-6.1.6.2.5-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-234 b]	AD-AV4-AD01_Part4-6.1.6.2.5-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-238 c]	AD-AV4-AD01_Part4-6.1.6.4.2-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-587]		New in	3
[SB4-SAT-AD1-P4-REQ-588]		New in	3
[SB4-SAT-AD1-P4-REQ-239 c]	AD-AV4-AD01_Part4-6.1.6.4.3-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-589]		New in	3
[SB4-SAT-AD1-P4-REQ-590]		New in	3
[SB4-SAT-AD1-P4-REQ-626]		New in	3
[SB4-SAT-AD1-P4-REQ-241 b]	AD-AV4-AD01_Part4-6.1.7.4-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-559]		New in	3
[SB4-SAT-AD1-P4-REQ-560]		New in	3
[SB4-SAT-AD1-P4-REQ-627]		New in	3
[SB4-SAT-AD1-P4-REQ-243 c]	AD-AV4- AD01_Part4-6.1.8-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-548]		New in	3
[SB4-SAT-AD1-P4-REQ-550]		New in	3
[SB4-SAT-AD1-P4-REQ-551]		New in	3
[SB4-SAT-AD1-P4-REQ-552]		New in	3
[SB4-SAT-AD1-P4-REQ-553]		New in	3
[SB4-SAT-AD1-P4-REQ-240 b]	AD-AV4-AD01_Part4-6.1.7.1-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-628]		New in	3
[SB4-SAT-AD1-P4-REQ-554]		New in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-555]		New in	3
[SB4-SAT-AD1-P4-REQ-557]		New in	3
[SB4-SAT-AD1-P4-REQ-242 b]	AD-AV4-AD01_Part4-6.1.7.4-002/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-561]		New in	3
[SB4-SAT-AD1-P4-REQ-604]		New in	3
[SB4-SAT-AD1-P4-REQ-244 b]	AD-AV4-AD01_Part4-6.2.3.3-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-613]		New in	3
[SB4-SAT-AD1-P4-REQ-245 b]	AD-AV4-AD01_Part4-6.2.3.4-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-246 c]	AD-AV4-AD01_Part4-6.2.3.5-001/b	Deleted in	3
[SB4-SAT-AD1-P4-REQ-247 b]	AD-AV4-AD01_Part4-6.2.3.5-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-248 c]	AD-AV4-AD01_Part4-6.2.3.6-001/b	Deleted in	3
[SB4-SAT-AD1-P4-REQ-250 c]	AD-AV4-AD01_Part4-6.2.3.8-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-251 b]	AD-AV4-AD01_Part4-6.2.3.9.1.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-252 b]	AD-AV4-AD01_Part4-6.2.3.9.1.3-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-253 b]	AD-AV4-AD01_Part4-6.2.3.9.2.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-254 b]	AD-AV4-AD01_Part4-6.2.3.9.3.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-255 b]	AD-AV4-AD01_Part4-6.2.3.9.3.4-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-562]		New in	3
[SB4-SAT-AD1-P4-REQ-256 b]	AD-AV4-AD01_Part4-6.2.4.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-257 b]	AD-AV4-AD01_Part4-6.2.4.3-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-259 b]	AD-AV4-AD01_Part4-6.2.4.4-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-258 b]	AD-AV4-AD01_Part4-6.2.4.4-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-260 c]	AD-AV4-AD01_Part4-6.2.4.6-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-261 b]	AD-AV4-AD01_Part4-6.2.4.7.1.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-262 b]	AD-AV4-AD01_Part4-6.2.4.7.1.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-263 b]	AD-AV4-AD01_Part4-6.2.4.7.2.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-264 b]	AD-AV4-AD01_Part4-6.2.4.7.3.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-265 b]	AD-AV4-AD01_Part4-6.2.5.1.1-001/aAD-AV4-AD01_Part4-6.2.5.1.1-001/a :	Deleted in	3
[SB4-SAT-AD1-P4-REQ-266 b]	AD-AV4-AD01_Part4-6.2.5.3.1-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-269 b]	AD-AV4-AD01_Part4-6.2.5.3.1-004/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-270 b]	AD-AV4-AD01_Part4-6.2.5.3.1-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-563]		New in	3
[SB4-SAT-AD1-P4-REQ-564]		New in	3
[SB4-SAT-AD1-P4-REQ-271 b]	AD-AV4-AD01_Part4-6.2.5.3.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-272 b]	AD-AV4-AD01_Part4-6.2.5.3.2-002/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-565]	AD-AV4-AD01_Part4-6.2.5.3.2-002/a	New in	3
[SB4-SAT-AD1-P4-REQ-273 b]	AD-AV4-AD01_Part4-6.2.5.3.2-003/a	Deleted in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-274 b]	AD-AV4-AD01_Part4-6.2.5.3.2-004/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-275 b]	AD-AV4-AD01_Part4-6.2.5.3.2-005/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-277 b]	AD-AV4-AD01_Part4-6.2.5.3.2-007/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-278 b]	AD-AV4-AD01_Part4-6.2.5.3.2-008/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-279 b]	AD-AV4-AD01_Part4-6.2.5.3.2-009/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-280 b]	AD-AV4-AD01_Part4-6.2.5.3.2-010/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-566]		New in	3
[SB4-SAT-AD1-P4-REQ-283 b]	AD-AV4-AD01_Part4-6.2.5.3.2-013/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-284 c]	AD-AV4-AD01_Part4-6.2.5.3.2-014/b	Deleted in	3
[SB4-SAT-AD1-P4-REQ-286 b]	AD-AV4-AD01_Part4-6.2.5.3.4-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-287 b]	AD-AV4-AD01_Part4-6.2.5.3.4-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-288 b]	AD-AV4-AD01_Part4-6.2.5.3.4-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-289 b]	AD-AV4-AD01_Part4-6.2.5.3.4-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-290 b]	AD-AV4-AD01_Part4-6.2.5.3.4-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-291 b]	AD-AV4-AD01_Part4-6.2.5.3.4-006/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-292 b]	AD-AV4-AD01_Part4-6.2.5.3.4-007/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-293 b]	AD-AV4-AD01_Part4-6.2.5.3.4-008/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-294 b]	AD-AV4-AD01_Part4-6.2.5.3.4-009/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-295 b]	AD-AV4-AD01_Part4-6.2.5.3.4-010/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-296 b]	AD-AV4-AD01_Part4-6.2.5.3.4-011/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-297 c]	AD-AV4-AD01_Part4-6.2.5.3.4-012/b	Deleted in	3
[SB4-SAT-AD1-P4-REQ-298 b]	AD-AV4-AD01_Part4-6.2.5.4-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-299 b]	AD-AV4-AD01_Part4-6.2.5.4-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-300 b]	AD-AV4-AD01_Part4-6.2.5.4-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-567]		New in	3
[SB4-SAT-AD1-P4-REQ-568]		New in	3
[SB4-SAT-AD1-P4-REQ-304 b]	AD-AV4-AD01_Part4-6.2.5.4.2-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-305 b]	AD-AV4-AD01_Part4-6.2.5.4.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-306 b]	AD-AV4-AD01_Part4-6.2.5.4.3-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-307 b]	AD-AV4-AD01_Part4-6.2.5.4.4-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-308 c]	AD-AV4-AD01_Part4-6.2.5.5-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-632]		New in	3
[SB4-SAT-AD1-P4-REQ-591]		New in	3
[SB4-SAT-AD1-P4-REQ-570]		New in	3
[SB4-SAT-AD1-P4-REQ-571]		New in	3
[SB4-SAT-AD1-P4-REQ-572]		New in	3
[SB4-SAT-AD1-P4-REQ-573]		New in	3
[SB4-SAT-AD1-P4-REQ-575]		New in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-309 b]	AD-AV4-AD01_Part4-6.2.6.1-001/aAD-AV4-AD01_Part4-6.2.6.1-001/a :	Modified in	3
[SB4-SAT-AD1-P4-REQ-629]		New in	3
[SB4-SAT-AD1-P4-REQ-576]		New in	3
[SB4-SAT-AD1-P4-REQ-578]		New in	3
[SB4-SAT-AD1-P4-REQ-310 b]	AD-AV4-AD01_Part4-6.2.6.1-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-311 b]	AD-AV4-AD01_Part4-6.2.6.4-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-312 b]	AD-AV4-AD01_Part4-6.2.6.5-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-313 b]	AD-AV4-AD01_Part4-6.2.6.5-002/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-580]		New in	3
[SB4-SAT-AD1-P4-REQ-314 b]	AD-AV4-AD01_Part4-6.2.6.6.1.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-315 b]	AD-AV4-AD01_Part4-6.2.6.6.1.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-316 b]	AD-AV4-AD01_Part4-6.2.6.6.2.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-317 b]	AD-AV4-AD01_Part4-6.2.6.6.3.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-636]		New in	3
[SB4-SAT-AD1-P4-REQ-318 b]	AD-AV4-AD01_Part4-6.2.7.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-319 b]	AD-AV4-AD01_Part4-6.2.7.2-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-601]		New in	3
[SB4-SAT-AD1-P4-REQ-592]		New in	3
[SB4-SAT-AD1-P4-REQ-593]		New in	3
[SB4-SAT-AD1-P4-REQ-620]		New in	3
[SB4-SAT-AD1-P4-REQ-323 b]	AD-AV4-AD01_Part4-6.3-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-324 b]	AD-AV4-AD01_Part4-6.4.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-583]		Modified in	3
[SB4-SAT-AD1-P4-REQ-584]		New in	3
[SB4-SAT-AD1-P4-REQ-326 b]	AD-AV4-AD01_Part4-6.4.1-003/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-328 b]	AD-AV4-AD01_Part4-6.4.1-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-329 b]	AD-AV4-AD01_Part4-6.4.1-006/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-330 c]	AD-AV4-AD01_Part4-6.4.2-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-635]		New in	3
[SB4-SAT-AD1-P4-REQ-634]		New in	3
[SB4-SAT-AD1-P4-REQ-333 b]	AD-AV4-AD01_Part4-6.6.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-334 d]	AD-AV4-AD01_Part4-6.6.2-001/c	Modified in	3
[SB4-SAT-AD1-P4-REQ-335 b]	AD-AV4-AD01_Part4-6.6.2-002/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-585]		New in	3
[SB4-SAT-AD1-P4-REQ-336 b]	AD-AV4-AD01_Part4-6.6.3.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-337 b]	AD-AV4-AD01_Part4-6.6.3.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-338 b]	AD-AV4-AD01_Part4-6.6.4.1-001/a	Deleted in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-339 b]	AD-AV4-AD01_Part4-6.6.4.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-340 b]	AD-AV4-AD01_Part4-6.6.5.1.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-341 b]	AD-AV4-AD01_Part4-6.6.5.1.4-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-342 b]	AD-AV4-AD01_Part4-6.6.5.2.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-343 c]	AD-AV4-AD01_Part4-6.7-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-344 b]	AD-AV4-AD01_Part4-6.7-002/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-345 c]	AD-AV4-AD01_Part4-6.7-003/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-612]		New in	3
[SB4-SAT-AD1-P4-REQ-346 b]	AD-AV4-AD01_Part4-6.7-004/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-347 b]	AD-AV4-AD01_Part4-6.7-005/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-356 c]	AD-AV4-AD01_Part4-6.9.2-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-594]		New in	3
[SB4-SAT-AD1-P4-REQ-357 d]	AD-AV4-AD01_Part4-6.9.3.1.1-001/c	Modified in	3
[SB4-SAT-AD1-P4-REQ-358 c]	AD-AV4-AD01_Part4-6.9.3.1.2-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-359 b]	AD-AV4-AD01_Part4-6.9.4-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-362 d]	AD-AV4-AD01_Part4-6.9.4.1.1-001/c	Modified in	3
[SB4-SAT-AD1-P4-REQ-367 b]	AD-AV4-AD01_Part4-6.9.6-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-363 c]	AD-AV4-AD01_Part4-6.9.5.1.1-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-364 c]	AD-AV4-AD01_Part4-6.9.5.1.2-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-365 c]	AD-AV4-AD01_Part4-6.9.5.2.1-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-366 b]	AD-AV4-AD01_Part4-6.9.5.2.2-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-602]		New in	3
[SB4-SAT-AD1-P4-REQ-368 b]	AD-AV4-AD01_Part4-6.11.1.1.1-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-607]		New in	3
[SB4-SAT-AD1-P4-REQ-369 b]	AD-AV4-AD01_Part4-6.11.1.1.2-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-625]		New in	3
[SB4-SAT-AD1-P4-REQ-370 b]	AD-AV4-AD01_Part4-6.11.1.1.3-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-371 b]	AD-AV4-AD01_Part4-6.11.1.2-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-372 c]	AD-AV4-AD01_Part4-6.11.2.1-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-608]		New in	3
[SB4-SAT-AD1-P4-REQ-373 b]	AD-AV4-AD01_Part4-6.11.2.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-374 b]	AD-AV4-AD01_Part4-6.11.2.2-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-375 b]	AD-AV4-AD01_Part4-6.11.2.3-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-376 b]	AD-AV4-AD01_Part4-6.11.2.3-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-377 c]	AD-AV4-AD01_Part4-6.11.2.4-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-378 b]	AD-AV4-AD01_Part4-6.11.2.4-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-379 b]	AD-AV4-AD01_Part4-6.11.2.4-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-380 c]	AD-AV4-AD01_Part4-6.11.2.5.1-001/b	Modified in	3

SUBSYSTEM AND UNITS REQUIREMENTS

- Electrical Design and Interfaces

Requirements

(AD01-P4)

PUID	PUID in AD01-P4 issue 2.2 and AD01-P3 issue 3.0	Change Status	Doc Issue
[SB4-SAT-AD1-P4-REQ-381 b]	AD-AV4-Ad01_Part4-6.11.2.5.2-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-382 b]	AD-AV4-AD01_Part4-6.12.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-383 b]	AD-AV4-AD01_Part4-6.12.1-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-384 b]	AD-AV4-AD01_Part4-6.12.1-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-597]	SB-AD01.3-4.02-036	New in	3
[SB4-SAT-AD1-P4-REQ-598]	SB-AD01.3-4.02-037	New in	3
[SB4-SAT-AD1-P4-REQ-599]		New in	3
[SB4-SAT-AD1-P4-REQ-633]		New in	3
[SB4-SAT-AD1-P4-REQ-385 c]	AD-AV4-AD01_Part4-6.13.1-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-605]		New in	3
[SB4-SAT-AD1-P4-REQ-386 c]	AD-AV4-AD01_Part4-6.13.2.1-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-387 c]	AD-AV4-AD01_Part4-6.13.2.2-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-388 b]	AD-AV4-AD01_Part4-6.13.2.3-001/a	Modified in	3
[SB4-SAT-AD1-P4-REQ-389 b]	AD-AV4-AD01_Part4-6.13.2.3-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-390 c]	AD-AV4-AD01_Part4-6.13.2.4-001/b	Modified in	3
[SB4-SAT-AD1-P4-REQ-391 b]	AD-AV4-AD01_Part4-6.14-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-392 b]	AD-AV4-AD01_Part4-6.14-002/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-393 b]	AD-AV4-AD01_Part4-6.14-003/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-397 b]	AD-AV4-AD01_Part4-6.17.1-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-398 b]	AD-AV4-AD01_Part4-6.17.2-001/a	Deleted in	3
[SB4-SAT-AD1-P4-REQ-399 c]	AD-AV4-AD01_Part4-6.17.2-002/b	Deleted in	3

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