V TOP
FALL & TRI (I / IV) SEMESTER 2019-20 - ADD / DROP

17BCE2399 - BRIJGOPAL BHARADWAJ - BCE - Computer Science and Engineering - BTECH 10-Jul-2019 10:16:08

Note :

This part will enable after selecting the Course Registration Option given below.

- Home
- View Registered Course(s)
- Modify Slot(s)
- Delete Registered Course(s)
- Curriculum Credits View

	Credits	Courses
Maximum	27	-
Minimum	16	-
Registered	25	7

Sign out

REGISTERED COURSE(S)

Registered Course(s)

Group	Course Code	Course Title	Course Type	L T P J	Credit	Course Category	Course Option	Class No.	Slot	Venue	Faculty	Status
General (Semester)	CSE3009	Internet of Things	Embedded Theory	3 0 0 0	3	Programme Elective	Regular	VL2019201001441	F1+TF1	SJT710	ARUNKUMAR T - SCOPE	Registered and Approved
General (Semester)	CSE3009	Internet of Things	Embedded Project	0 0 0 4	1	Programme Elective	Regular	VL2019201001442	F1+TF1	NIL	ARUNKUMAR T - SCOPE	Registered and Approved
General (Semester)	CSE3024	Web Mining	Embedded Theory	3 0 0 0	3	Programme Elective	Regular	VL2019201005591	F2+TF2	SJT508	ANURADHA J - SCOPE	Registered and Approved
General (Semester)	CSE3024	Web Mining	Embedded Lab	0 0 2 0	1	Programme Elective	Regular	VL2019201005877	L9+L10	SJT516	ANURADHA J - SCOPE	Registered and Approved
General (Semester)	CSE4001	Parallel and Distributed Computing	Embedded Theory	2 0 0 0	2	Programme Core	Regular	VL2019201001357	C1	SJT707	SAIRABANU J - SCOPE	Registered and Approved
General (Semester)	CSE4001	Parallel and Distributed Computing	Embedded Lab	0 0 2 0	1	Programme Core	Regular	VL2019201001473	L47+L48	SJT417	SAIRABANU J - SCOPE	Registered and Approved
General (Semester)	CSE4001	Parallel and Distributed Computing	Embedded Project	0 0 0 4	1	Programme Core	Regular	VL2019201001474	L47+L48	NIL	SAIRABANU J - SCOPE	Registered and Approved
General (Semester)	CSE4003	Cyber Security	Embedded Theory	3 0 0 0	3	Programme Elective	Regular	VL2019201006712	A2+TA2	SJT102	PRAMOD KUMAR MAURYA - SCOPE	Registered and Approved
General (Semester)	CSE4003	Cyber Security	Embedded Project	0 0 0 4	1	Programme Elective	Regular	VL2019201006713	A2+TA2	NIL	PRAMOD KUMAR MAURYA - SCOPE	Registered and Approved
General (Semester)	CSE4019	Image Processing	Embedded Theory	3 0 0 0	3	Programme Elective	Regular	VL2019201005526	E2+TE2	SJT505	SURESHKUMAR N - SCOPE	Registered and Approved
General (Semester)	CSE4019	Image Processing	Embedded Project	0 0 0 4	1	Programme Elective	Regular	VL2019201005527	E2+TE2	NIL	SURESHKUMAR N - SCOPE	Registered and Approved
General (Semester)	MAT3004	Applied Linear Algebra	Theory Only	3 2 0 0	4	Programme Core	Regular	VL2019201000511	C2+TC2+TCC2+V5	SJT508	RAGHAVENDAR K - SAS	Registered and Approved
General (Semester)	STS3201	Programming Skills for Employment	Soft Skill	0 0 0 0	1	University Core (GENERAL Basket)	Regular	VL2019201000195	D1+TD1	SJT201	FACE (APT) - SSL	Registered and Approved

Time Table

Registered Slots / Hours are highlighted with green color.

If there is no green highlight it indicates that there are no Registered List Slots / Hours.

Theory	Start	08:00	09:00	10:00	11:00	12:00	-	Lunch	14:00	15:00	16:00	17:00	18:00	18:50	19:01
	End	08:50	09:50	10:50	11:50	12:50	-	Lunch	14:50	15:50	16:50	17:50	18:50	19:00	19:50
Lab	Start	08:00	08:46	10:00	10:46	11:31	12:16	Lunch	14:00	14:46	16:00	16:46	17:31	18:16	-
	End	08:45	09:30	10:45	11:30	12:15	13:00	Lunch	14:45	15:30	16:45	17:30	18:15	19:00	-
MON	Theory	A1	F1-CSE3009-ETH-SJT710	D1-STS3201-SS-SJT201	TB1	TG1	-	Lunch	A2-CSE4003-ETH-SJT102	F2-CSE3024-ETH-SJT508	D2	TB2	TG2	-	V3
	Lab	L1	L2	L3	L4	L5	L6	Lunch	L31	L32	L33	L34	L35	L36	-
TUE	Theory	B1	G1	E1	TC1	TAA1	-	Lunch	B2	G2	E2-CSE4019-ETH-SJT505	TC2-MAT3004-TH-SJT508	TAA2	-	V4
	Lab	L7	L8	L9-CSE3024-ELA-SJT516	L10-CSE3024-ELA-SJT516	L11	L12	Lunch	L37	L38	L39	L40	L41	L42	-
WED	Theory	C1-CSE4001-ETH-SJT707	A1	F1-CSE3009-ETH-SJT710	V1	V2	-	Lunch	C2-MAT3004-TH-SJT508	A2-CSE4003-ETH-SJT102	F2-CSE3024-ETH-SJT508	TD2	TBB2	-	V5-MAT3004-TH-SJT508
	Lab	L13	L14	L15	L16	-	-	Lunch	L43	L44	L45	L46	L47-CSE4001-ELA-SJT417	L48-CSE4001-ELA-SJT417	-
THU	Theory	D1-STS3201-SS-SJT201	B1	G1	TE1	TCC1	-	Lunch	D2	B2	G2	TE2-CSE4019-ETH-SJT505	TCC2-MAT3004-TH-SJT508	-	V6
	Lab	L19	L20	L21	L22	L23	L24	Lunch	L49	L50	L51	L52	L53	L54	-
FRI	Theory	E1	C1-CSE4001-ETH-SJT707	TA1	TF1-CSE3009-ETH-SJT710	TD1-STS3201-SS-SJT201	-	Lunch	E2-CSE4019-ETH-SJT505	C2-MAT3004-TH-SJT508	TA2-CSE4003-ETH-SJT102	TF2-CSE3024-ETH-SJT508	TDD2	-	V7
	Lab	L25	L26	L27	L28	L29	L30	Lunch	L55	L56	L57	L58	L59	L60	-
SAT	Theory	V8	X11	X12	Y11	Y12	-	Lunch	X21	Z21	Y21	W21	W22	-	V9
	Lab	L71	L72	L73	L74	L75	L76	Lunch	L77	L78	L79	L80	L81	L82	-
SUN	Theory	V10	Y11	Y12	X11	X12	-	Lunch	Y21	Z21	X21	W21	W22	-	V11
	Lab	L83	L84	L85	L86	L87	L88	Lunch	L89	L90	L91	L92	L93	L94	-

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