ELECTRONICS ENGINEERING SOCIETY

UDYAM'25

I-CHIP

PS-1

PROBLEM STATEMENT: MASTER DMA CONTROLLER IMPLEMENTATION

INTRODUCTION

IN MODERN VLSI SYSTEMS, EFFICIENT DATA TRANSFER MECHANISMS ARE CRUCIAL TO MINIMIZE PROCESSOR OVERHEAD AND MAXIMIZE SYSTEM PERFORMANCE. DIRECT MEMORY ACCESS (DMA) IS ONE SUCH TECHNIQUE THAT ALLOWS DATA TRANSFER BETWEEN MEMORY REGIONS WITHOUT PROCESSOR INTERVENTION.

IN THIS CHALLENGE, PARTICIPANTS WILL DESIGN A MASTER DMA CONTROLLER, WHICH WILL INTERACT WITH A WORD-ADDRESSABLE SLAVE MEMORY USING THE AXI-LITE PROTOCOL. THE DMA CONTROLLER WILL READ A BLOCK OF DATA FROM A SOURCE ADDRESS, TEMPORARILY STORE IT IN A SYNCHRONOUS FIFO BUFFER, AND THEN WRITE THE DATA BACK TO A DESTINATION ADDRESS. THE TESTBENCH AND SLAVE MEMORY WILL BE PROVIDED BY THE ORGANIZERS TO EVALUATE THE DESIGN.

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TASK DESCRIPTION

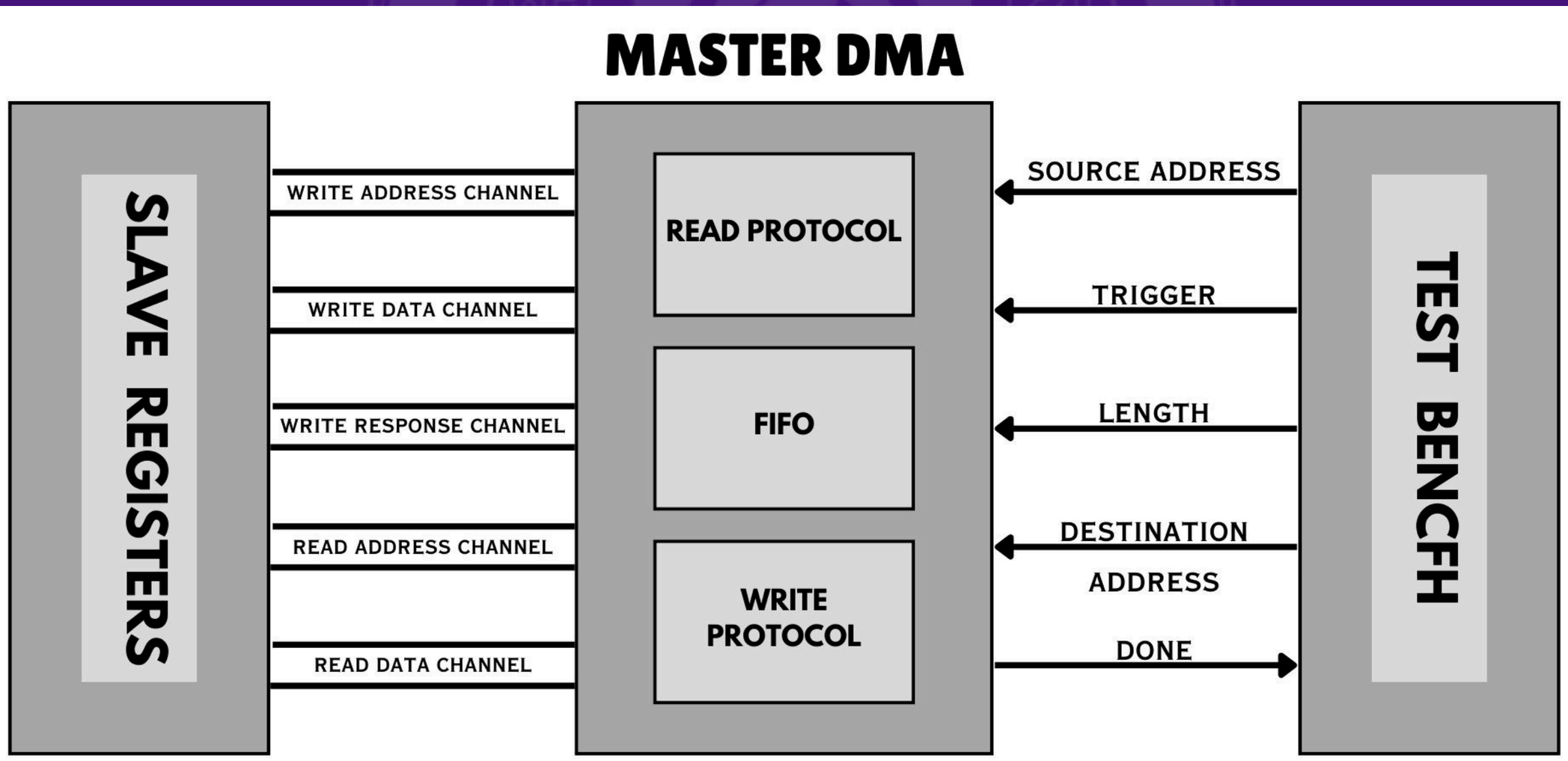
THE MASTER DMA CONTROLLER IS A HARDWARE MODULE DESIGNED TO PERFORM AUTONOMOUS DATA TRANSFER BETWEEN MEMORY LOCATIONS USING THE AXI-LITE PROTOCOL, WITHOUT DIRECT PROCESSOR INTERVENTION. IT ENABLES EFFICIENT MOVEMENT OF DATA WHILE ENSURING PROPER SYNCHRONIZATION WITH MEMORY THROUGH A HANDSHAKING MECHANISM.

THE DESIGN FEATURES TWO PRIMARY OPERATIONS: READ AND WRITE, EXECUTED THROUGH INDEPENDENT STATE MACHINES. UPON INITIATION, THE DMA MUST CORRECTLY FETCH DATA FROM A WORD-ADDRESSABLE SLAVE MEMORY AND TEMPORARILY STORE IT IN AN INTERNAL FIFO BUFFER BEFORE WRITING IT TO THE DESTINATION ADDRESS. THE MEMORY ADDRESSING FOLLOWS A WORD-ALIGNED STRUCTURE, MEANING THAT THE SOURCE ADDRESS, DESTINATION ADDRESS, AND TRANSFER LENGTH MUST ALWAYS BE MULTIPLES OF 4 BYTES.

THE WRITE OPERATION STARTS IN PARALLEL AS SOON AS THERE IS DATA AVAILABLE IN THE FIFO. THE MASTER DMA RETRIEVES DATA FROM THE FIFO AND WRITES IT SEQUENTIALLY TO THE DESTINATION ADDRESS IN MEMORY. THE DESIGN ENSURES THAT READ AND WRITE OPERATIONS ARE EFFICIENTLY HANDLED THROUGH SEPARATE STATE MACHINES, AND PROPER HANDSHAKING IS MAINTAINED USING AXI-LITE PROTOCOL SIGNALS. THE TRANSFER IS CONSIDERED COMPLETE WHEN ALL WORDS HAVE BEEN SUCCESSFULLY WRITTEN, AT WHICH POINT THE DONE SIGNAL IS ASSERTED.

PARTICIPANTS ARE ENCOURAGED TO DESIGN THEIR TESTBENCH AND SLAVE REGISTER MODULE TO VERIFY THE FUNCTIONALITY OF THEIR DMA CONTROLLER. HOWEVER, FINAL EVALUATION WILL BE CONDUCTED USING A DIFFERENT TESTBENCH AND SLAVE MEMORY, PROVIDED BY THE CONTEST ORGANIZERS. THE TESTBENCH AND SLAVE REGISTERS WILL ADHERE TO THE SAME AXI-LITE INTERFACE SPECIFICATIONS AS DEFINED IN THE PROBLEM STATEMENT.

BLOCK DIAGRAM



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FUNCTIONAL REQUIREMENTS

1. AXI-LITE TRANSACTIONS

- THE MASTER DMA SHOULD USE AXI PROTOCOL AND COMMUNICATE WITH THE WORD-ADDRESSABLE SLAVE MEMORY.
- THE SLAVE MEMORY SUPPORTS WORD-BASED ADDRESSING (I.E, EACH MEMORY LOCATION STORES A 32-BIT WORD).
- THE MASTER DMA SHOULD CORRECTLY IMPLEMENT AXI READ AND WRITE TRANSACTIONS .

2. FIFO BUFFER

- A 16-DEPTH, 32-BIT WIDTH SYNCHRONOUS FIFO SHOULD BE IMPLEMENTED INSIDE THE MASTER DMA.
- THE FIFO WILL TEMPORARILY STORE DATA DURING THE READ-WRITE PROCESS.
- FIFO SIGNALS MUST BE PROPERLY CONTROLLED (FIFO_FULL, FIFO_EMPTY, FIFO_RD_EN, FIFO_WR_EN).

INPUTS & OUTPUTS OF MASTER DMA

Signal Name	Direction	Width	Description
clk	Input	1-bit	System clock signal
reset	Input	1-bit	Active-high reset
trigger	Input	1-bit	Triggers DMA operation
length	Input	5-bit	Number of words to transfer
source_address	Input	32-bit	Start address of source memory
destination_address	Input	32-bit	Start address of destination memory
done	Output	1-bit	DMA transfer completion signal
ARADDR	Output	32-bit	AXI Read Address

ARVALID	Output	1-bit	AXI Read Address Valid
ARREADY	Input	1-bit	AXI Read Address Ready
RDATA	Input	32-bit	AXI Read Data
RVALID	Input	1-bit	AXI Read Data Valid
RREADY	Output	1-bit	AXI Read Ready
AWADDR	Output	32-bit	AXI Write Address
AWVALID	Output	1-bit	AXI Write Address Valid
AWREADY	Input	1-bit	AXI Write Address Ready
WDATA	Output	32-bit	AXI Write Data
WVALID	Output	1-bit	AXI Write Data Valid
WREADY	Input	1-bit	AXI Write Ready
BVALID	Input	1-bit	AXI Write Response Valid
BREADY	Output	1-bit	AXI Write Response Ready

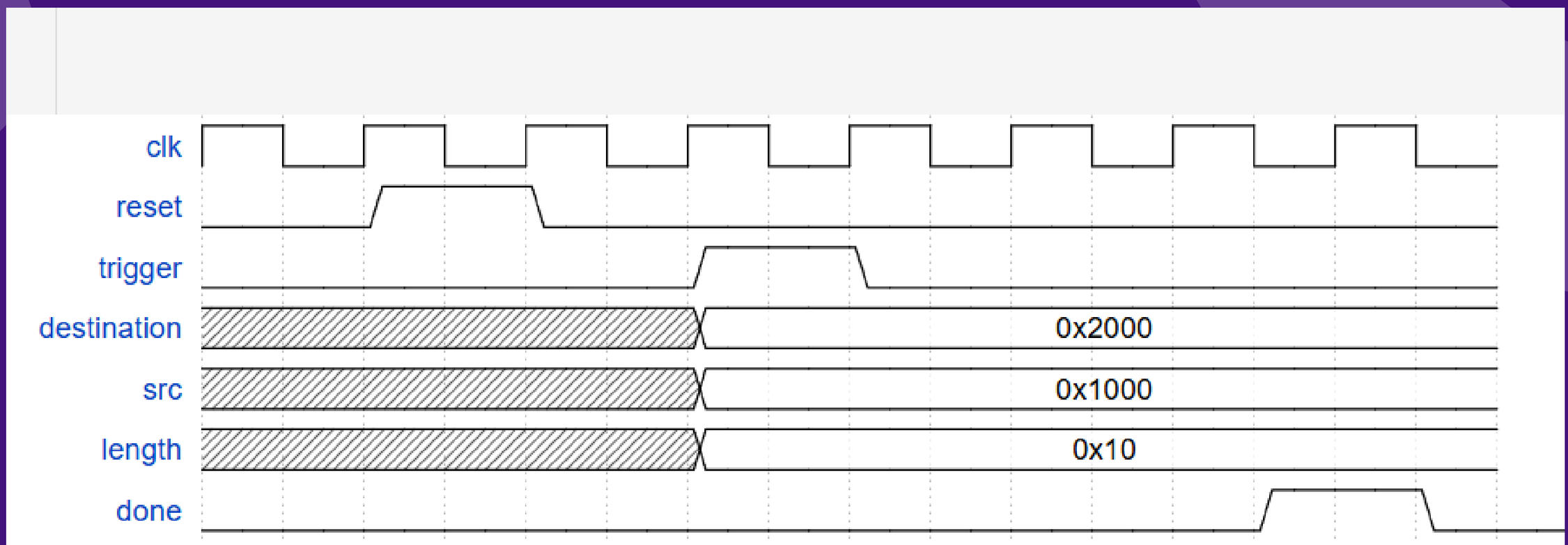
MEMORY DATA EXAMPLE

FOR LENGTH = 16, THE MASTER DMA WILL TRANSFER 4 WORDS (16 BYTES) FROM THE SOURCE MEMORY (0X1000) TO THE DESTINATION MEMORY (0X2000).

BEFORE DMA TRANSFER
SOURCE MEMORY (DATA TO BE READ)
0X1000 : AABBCCDD
0X1004 : 11223344
0X1008 : 55667788
0X100C : 99AABBCC

DESTINATION MEMORY (BEFORE WRITING)
0X2000 : 00000000
0X2004 : 00000000
0X2008 : 00000000
0X200C : 00000000

AFTER DMA TRANSFER
DESTINATION MEMORY (AFTER WRITING)
0X2000 : AABBCCDD
0X2004 : 11223344
0X2008 : 55667788
0X200C : 99AABBCC



TEAM COMPOSITION & SUBMISSION

- TEAM SIZE: 2 MEMBERS
- SUBMISSION DEADLINE: 5TH MARCH
- DELIVERABLES:
  - VIVADO PROJECT CONTAINING THE VERILOG IMPLEMENTATION OF THE MASTER DMA.
  - DOCUMENTATION EXPLAINING THE DESIGN CHOICES, STATE MACHINE LOGIC, FIFO USAGE, AND AXI-LITE HANDSHAKING METHODOLOGY.