Introduction to Microcircuits
Lab 6: SeriesParallel MOS Networks and MOS Current Dividers

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1 Experiment 1: Transistor Matching

We characterized each of the transistors on the ALD1106 chip by measuring the channel current as a function of gate voltage. Using an EKV, the transistors' I_s, κ, and V_{T0} values were extracted. They are as follows:

NMOS	I_s	V_{T0}	κ
NMOS 1	$1.8808 * 10^{-6}$ (A)	0.5786 (V)	0.7149
NMOS 2	$1.9038 * 10^{-6}$ (A)	0.5767 (V)	0.7104
NMOS 3	$1.9164 * 10^{-6}$ (A)	0.5798 (V)	0.7085
NMOS 4	$1.9168 * 10^{-6}$ (A)	0.5795 (V)	0.7087

The current-voltage characteristics of each transistor, along with their EKV fits, are shown in figure 1 below. As seen in the graph, the transistors match each other extremely well. Their EKV fits are so close as to be on top of each other.

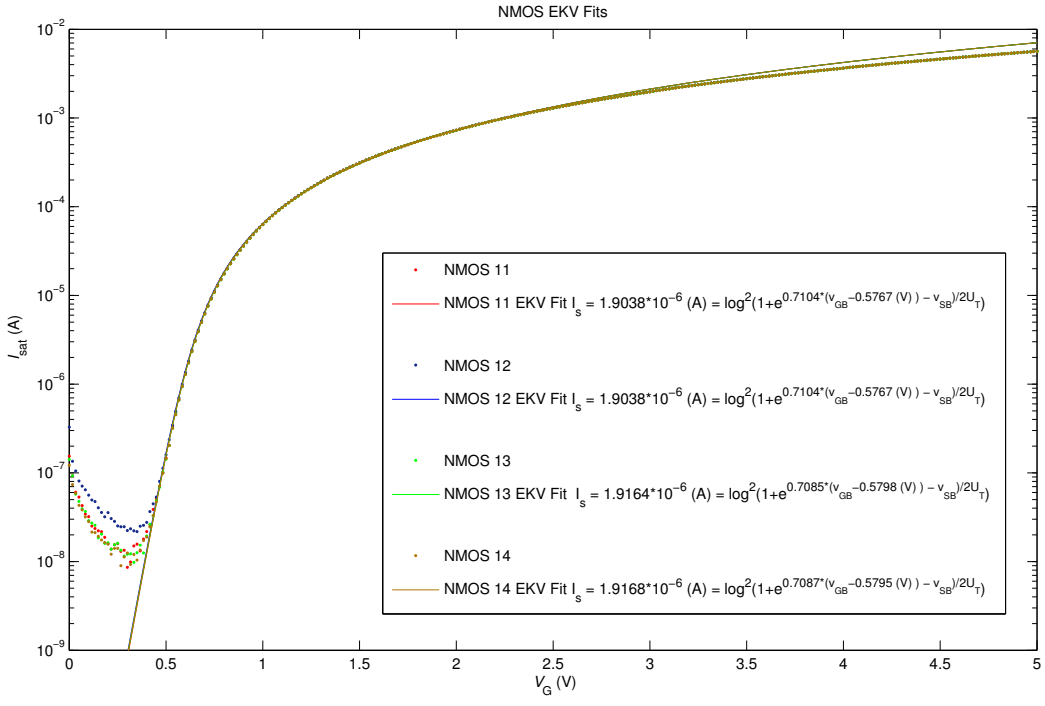

Figure 1: The current voltage (gate) for each of the four NMOS transistors, along with their EKV fits.

We then measured how well each of these four transistors matched each other by calculating the percent

difference between their measured channel currents and the mean channel current. The results are shown in figure 2 below:

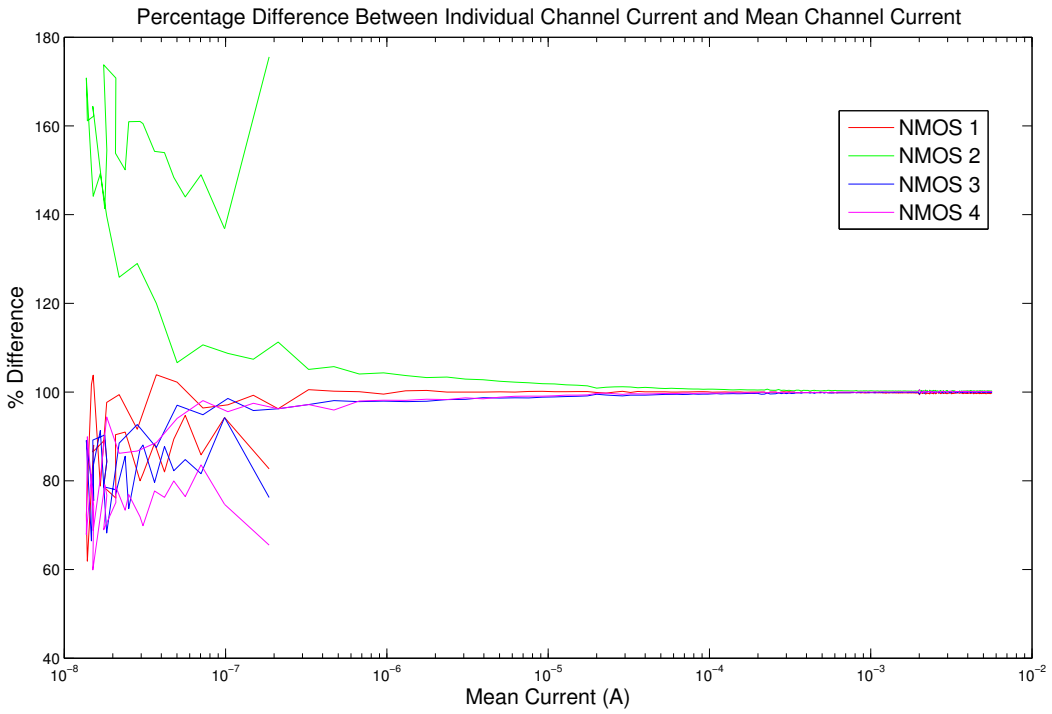

Figure 2: The percent difference of each NMOS channel current plotted against the mean channel current.

As shown in the graph above, the transistors match eachother extremely well, with differences of 180% or less. Some transistors match each other better than others; our second mosfet seems to match the other three less well. The graph also suggests that the transistors match each other better in strong inversion than they do in weak inversion. The difference between their individual currents and the mean current seems to decrease as the mean current increases.

2 Experiment 2: MOS Transistors in Series and Parallel

Next, we measured channel current as a function of gate voltage for three simple circuit setups; the first, with just one nMOS transistor; the second, with two transistors in parallel, and third, with the same two transistors in series. Each circuit setup was tested with both $V_{DS} = 10\text{mV}$ and $V_{DS} = V_{dd}(5V)$. We expected the parallel configuration to yield twice the amount of current as the single transistor, and the series configuration to yield half the amount. The results are shown in figures 3 and 4 below:

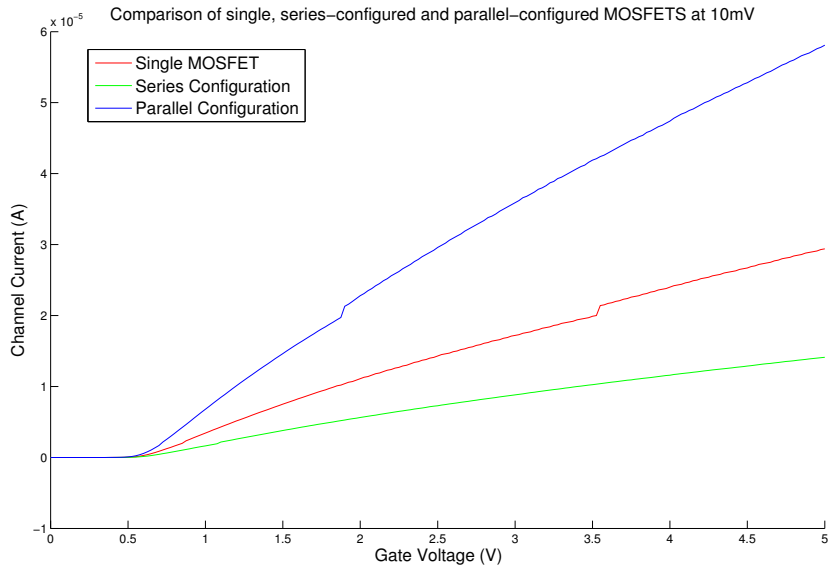

Figure 3: The comparison of parallel, series, and individual mosfet configurations at 10mV.

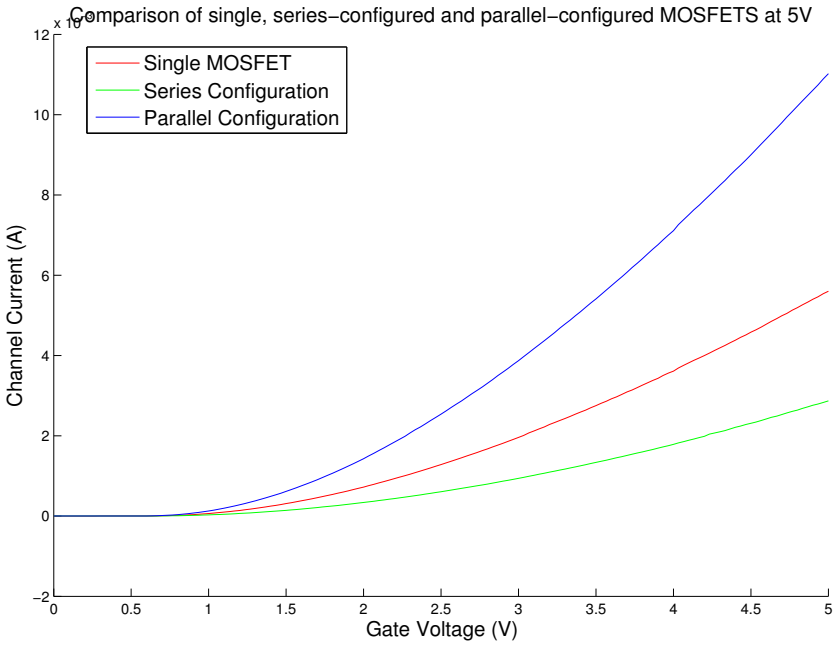

Figure 4: The comparison of parallel, series, and individual mosfet configurations at 5V.

As we expected, we measured twice the amount of current of a single MOSFET in the parallel configuration, and half the individual-configuration current in a series configuration.

We also compared the ratio of the series and parallel configurations and the single transistor, in figures 5 and 6.

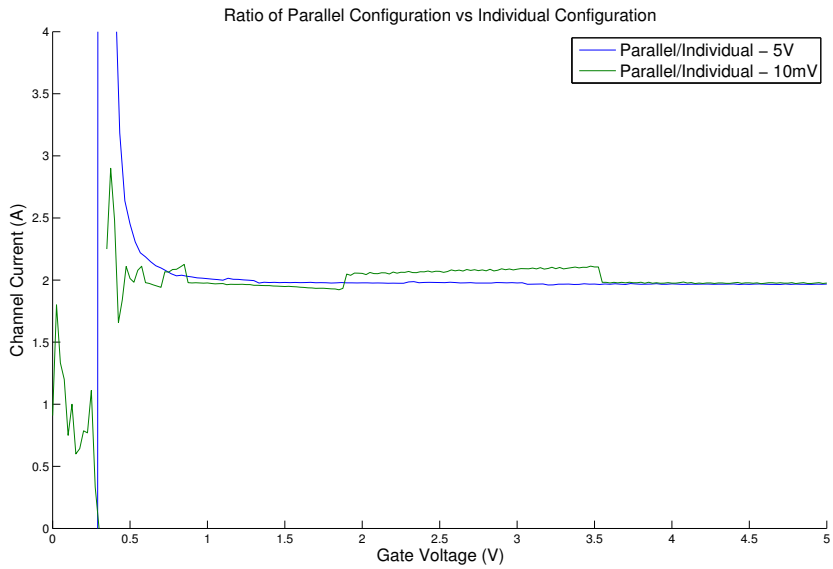

Figure 5: The percent difference of each NMOS channel current plotted against the mean channel current.

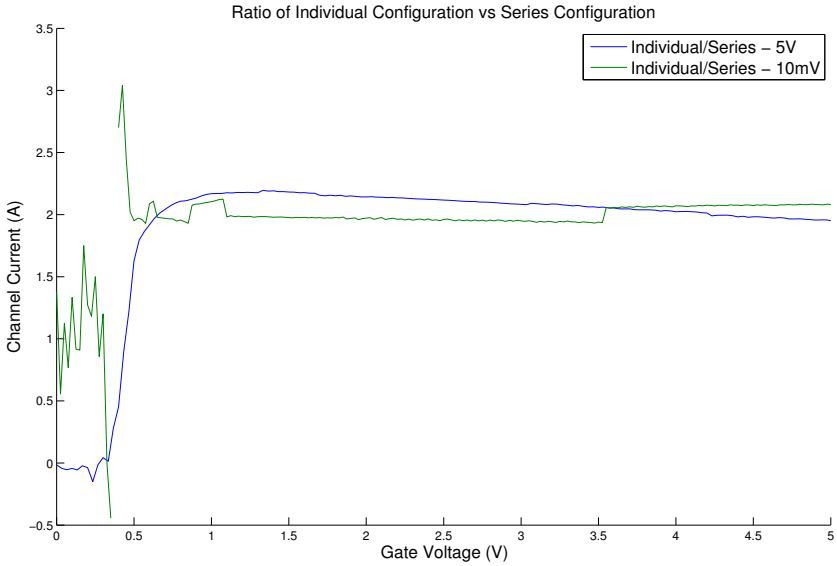

Figure 6: The percent difference of each NMOS channel current plotted against the mean channel current.

Again, the parallel configuration yielded twice the individual configuration current, giving a parallel/individual ratio of 2. The series configuration yielded half the individual configuration amount, giving an individual/series ratio of 2 as well. The equivalencies work fairly well, but there is some variation in the exact ratio value as the gate voltage is swept. Certain regions are more accurate than others; the weak inversion region ($V_G < .5V$) does not hold well to the ratio, while the strong inversion region ($V_G > 1V$) is much more accurate for the series configration, and is accurate up until approximately $2V$ in the parallel configuration.

3 Experiment 3: MOS Current Dividers

Next, we constructed two different two-way current dividers with small integer divider ratios, using series/-parallel configurations, and measured output current as a function of input current. We used integer ratios of 1/3, by using an individual MOSFET in one branch (branch 1) and two MOSFETS in parallel in the other (branch 2). Theoretically, we can expect the divider ratios of these current dividers to be one third, as per the equation:

$$\frac{I_1}{I_{in}} = \frac{S_1}{S_1 + S_2}$$

where S is the strength factor of the MOSFET, and knowing that a single MOSFET has a strength factor of 1, while two MOSFETs in parallel have a strength factor of 2 and two MOSFETs in series have a strength factor of $\frac{1}{2}$. We then compared the measured and theoretical currents in figures 7 and 8 below:

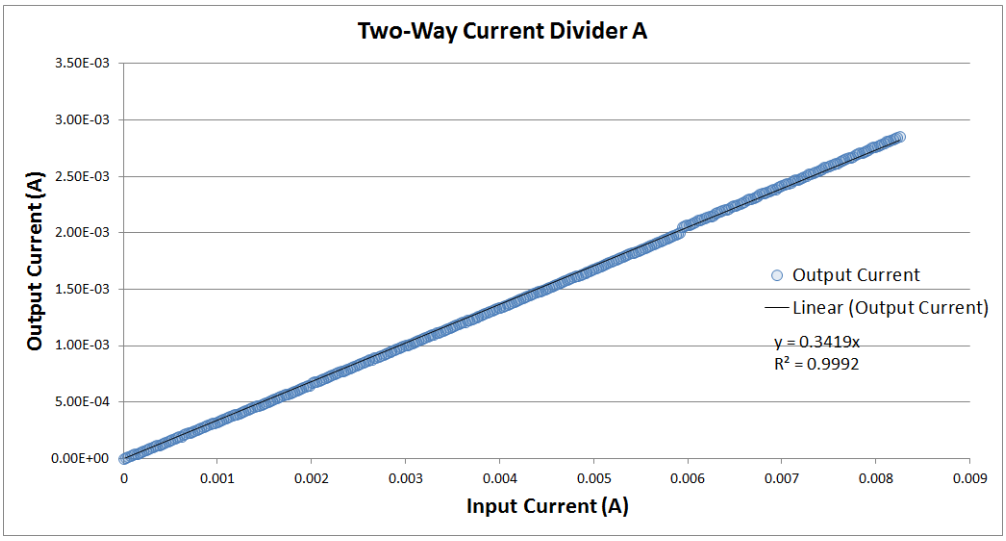

Figure 7: The input/output current characteristic of current divider A.

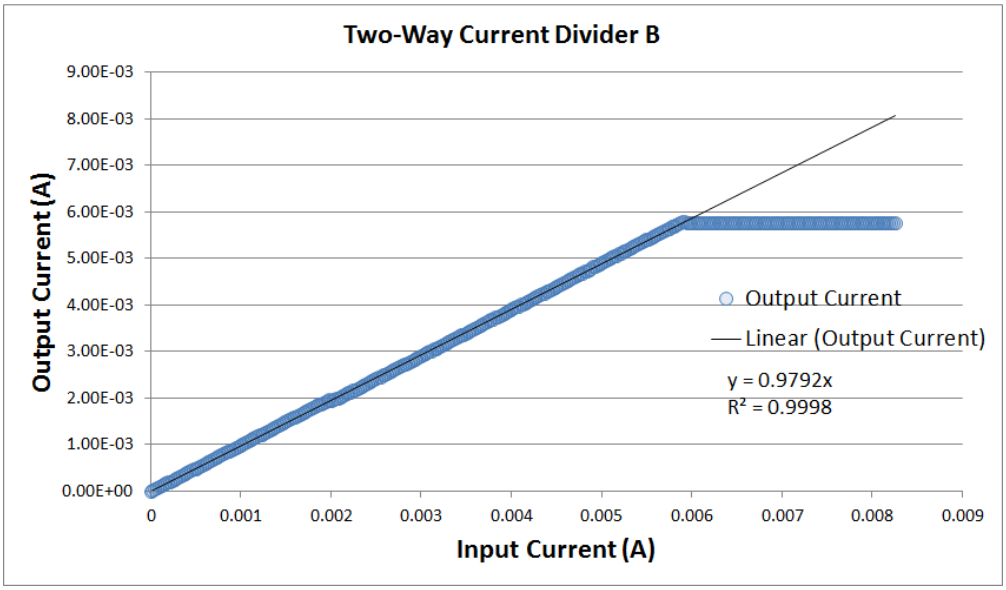

Figure 8: The input/output current characteristic of current divider B.

The graph above for current divider A shows a fit with slope of approximately 0.34, which matches our expectations from the equation above.

The graph for current divider B does not follow our predicted behavior, with a slope of approximately one. This may be due to an error in the circuit or during measurement.

4 Discussion

In this lab, we experimented with transistor matching, series and parallel combinations of MOSFETs, and two-way current dividers. We verified that all four transistors on a single ALD1106 array were extremely closely matched. We then used these transistors to construct series and parallel combinations, and verified that two MOSFETs in parallel would behave as a single MOSFET with double the strength ratio, while two MOSFETs in series would behave as a single MOSFET with half. Using this knowledge, we constructed a current divider, and verified that the divider ratio would match $\frac{I_1}{I_{in}} = \frac{S_1}{S_1+S_2}$.