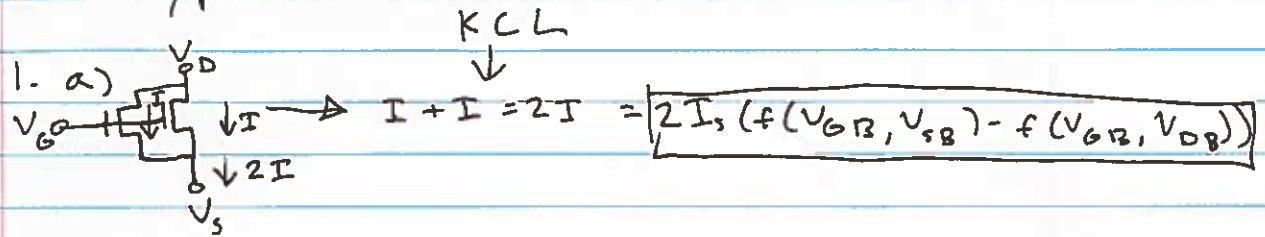


Series / parallel MOS networks



b)
$$I_{final} = I_S(f(V_G, V_S) - f(V_G, (V_D - V_S)/2))$$

$$= I_S(f(V_G, (V_D - V_S)/2) - f(V_G, V_D))$$

$f(V_G, V_S) - f(V_G, V_D) = 2f(V_G, (V_D - V_S)/2)$
 I don't know how to explain ~~this~~ with these equations, but it's very clear that ~~a~~ a nMOSFET w/ $V_S = A$ and $V_D = B$ will have 2x the current through it than an nMOSFET w/ $V_S = \frac{1}{2}A$ and $V_D = B$ or $V_S = A$ and $V_D = \frac{1}{2}B$.

2. a) $I_{in} = I_1 + I_2$ and $I_{in} = I_1 + I_2$

b) if $V_1 = V_2$

$$\frac{I_1}{I_{in}} = \frac{1}{2} \quad \frac{I_2}{I_{in}} = \frac{1}{2}$$

c) if $V_1 \neq V_2$, $I_1 \neq I_2$ in saturation

b/c $I_S = \frac{2\mu C_{ox} V_T^2}{K} \left(\frac{W}{L}\right)$ so $I_S \propto \frac{W}{L}$

and $I_{sat} \propto I_S$ so $I_{sat} \propto \frac{W}{L}$

$I > I_{sat}$ d) The max is $I_{sat,1} + I_{sat,2}$. If this limit is exceeded, the current will try to draw from the substrate and the device will get hot and explode in a terrible fire of death.

