



from breaking down
the ladder, we see
that if $I_1 = I$, $I_{total} = 2I$
and $I_2 = \frac{1}{2} I$
 $I_3 = \frac{1}{4} I$
 $I_4 = \frac{1}{8} I$
 $I_5 = \frac{1}{16} I$

I think the relationship holds
only for SI (maybe MI too)
b/c in exp 2 the ratio
for WI ~~was not~~ was not
the expected ratio.

For the parallel
configuration, ~~again~~ the
ratio did not reach $\frac{1}{2}$.

$$\frac{I_{\text{single nMOS}}}{I_{\text{parallel nMOS}}}$$

extending the ladder
too much results in ~~too~~
~~small~~ $V_{DS} \rightarrow$ too small
and $V_{GS} \rightarrow$ too small to maintain
the ratio. For ~~small~~ V_{GS}
only hold V_G so high, so
 V_{GS} is a limiting factor
on the ladder extension.