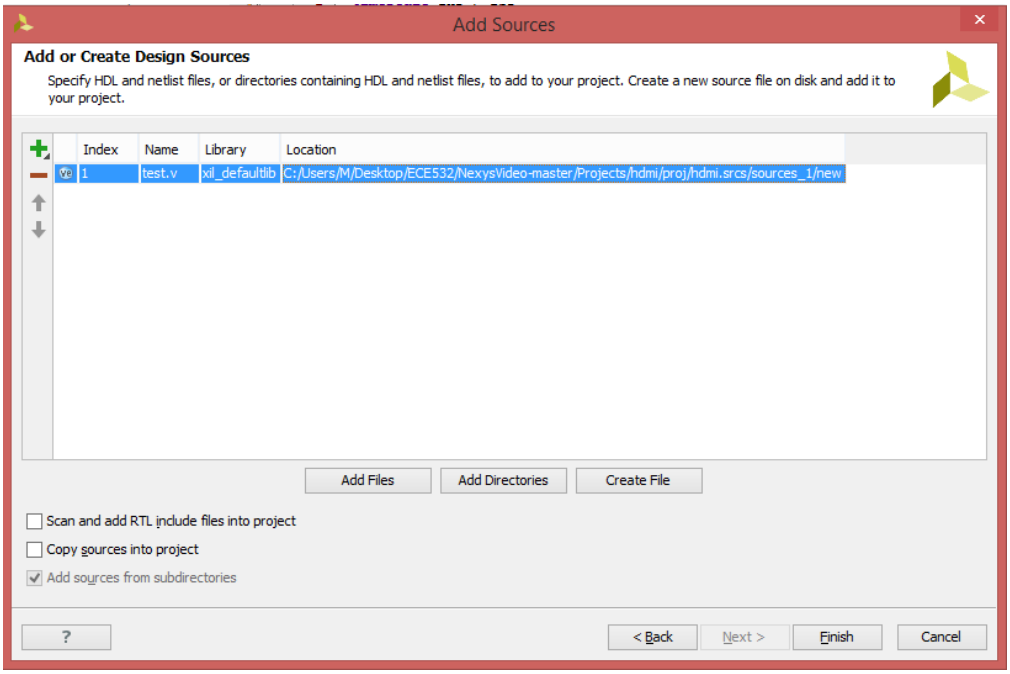
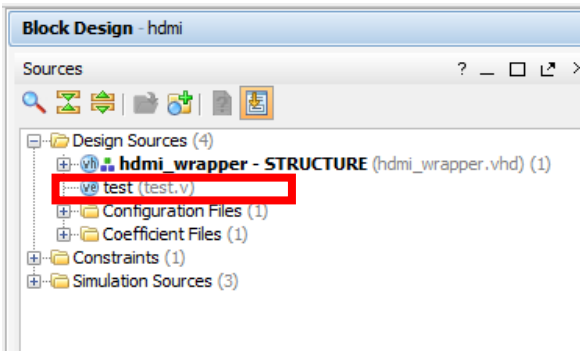
## Adding Verilog Files as Separate Blocks

Sometimes, you want to use logic without interfacing with the AXI signals. To add a custom Verilog file into the block diagram, follow the below steps:

- Create a blank Verilog file, i.e. test.v
- Add it to the project through File > Add Sources (Alt + A)
- Select “Add or create design sources”
- Select “Add files” and browse for your file




- Next, navigate to your block diagram. You should see your new Verilog file in the hierarchy, under “Design Sources”




- Right-click the file and “Add Module to Block Design”. You should now see it in the diagram and can place it as desired.