Gebze Technical University

Computer Engineering Departman

CSE 436 Digital Integrated Circuit

Homework #3

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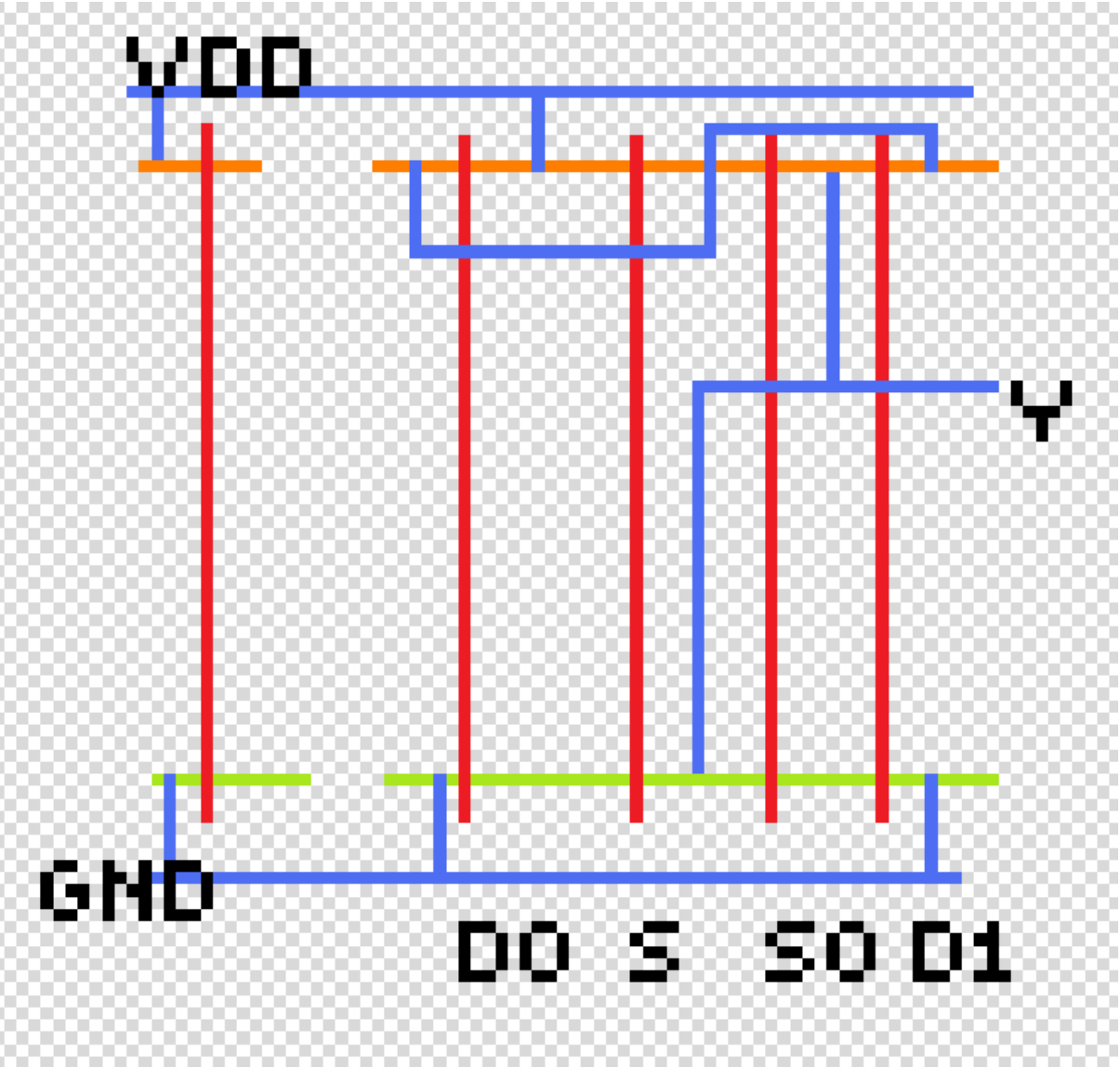
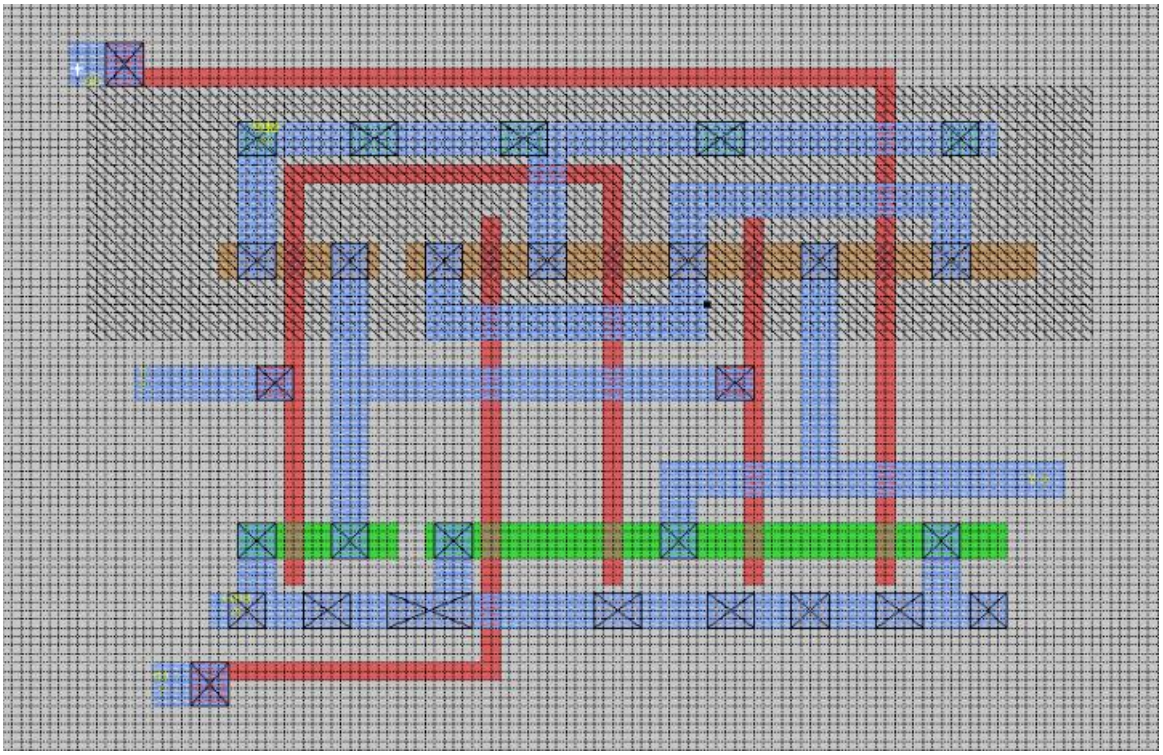
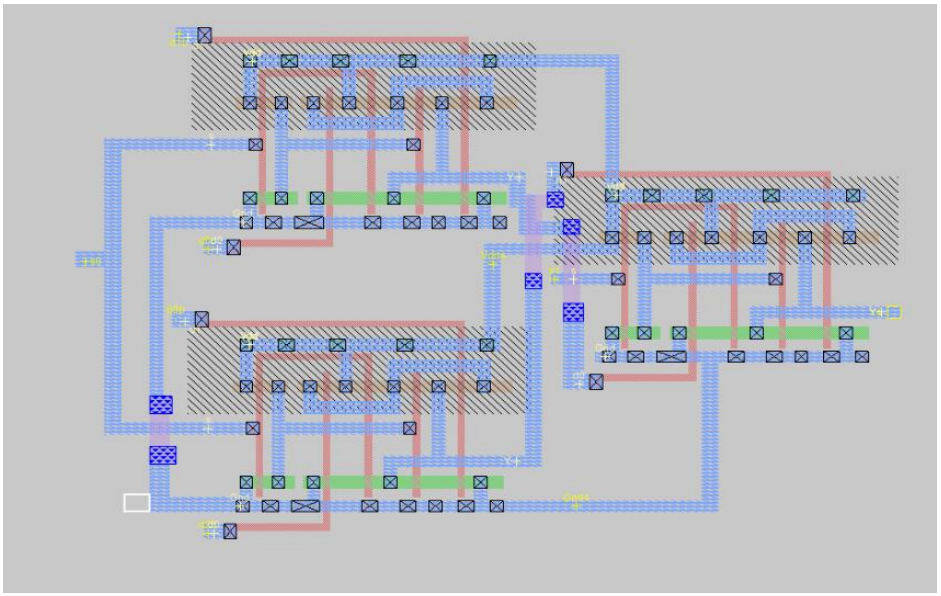
❖ Below is the 2x1 stick diagram design.



❖ Below is the 2x1 mux magic design.



❖ Below is the 4x1 mux magic design.

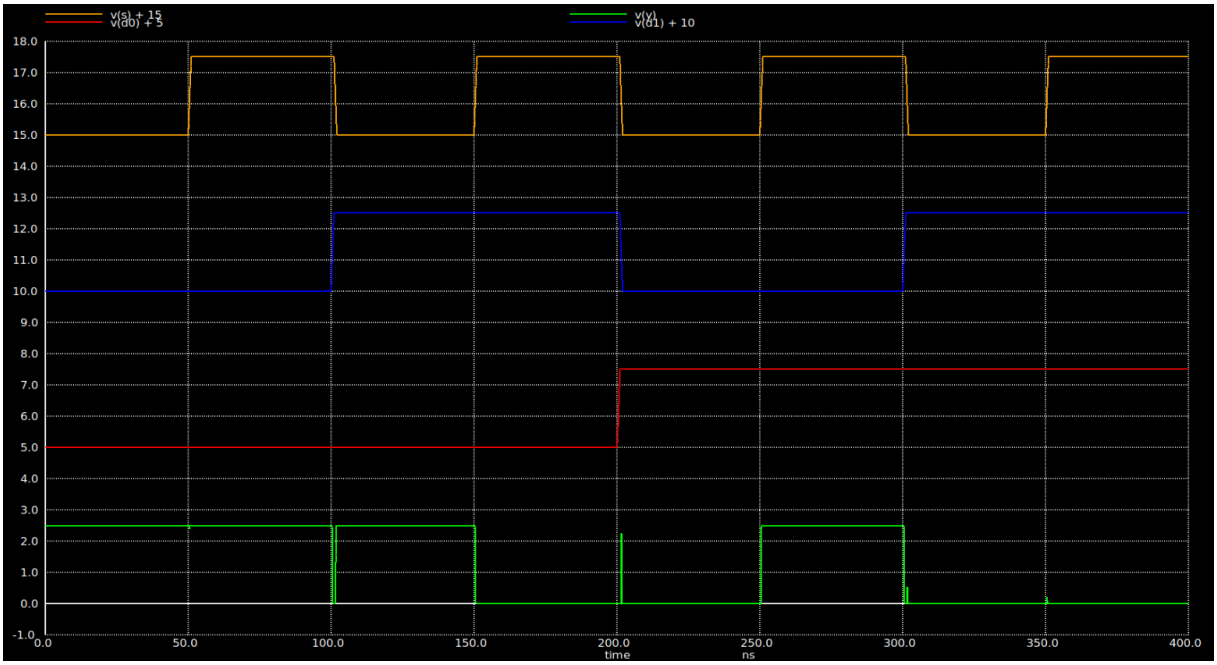


2x1 Mux Text Case

S = orange Y = Green

D0 = red D1 = Blue

All expected results for the 2x1 multiplexer have turned out correctly.

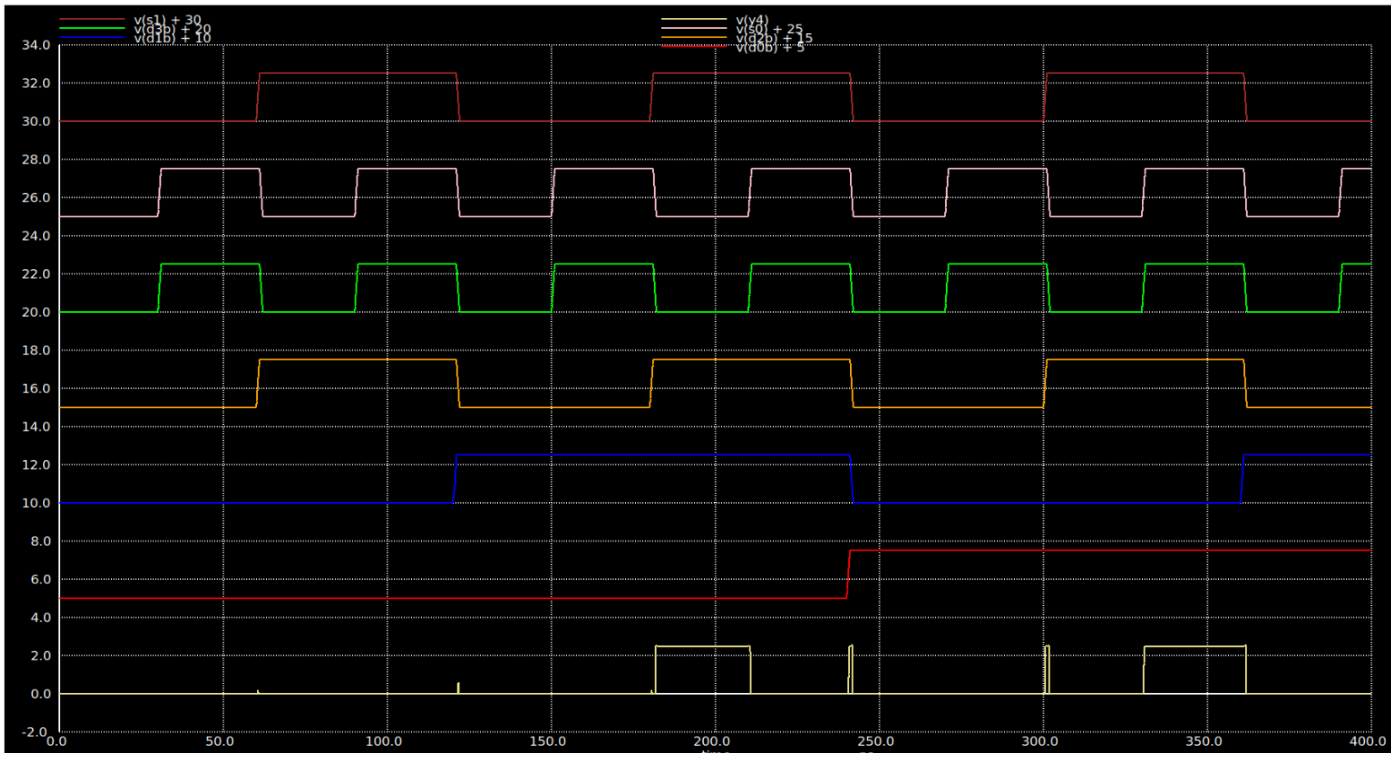


Spice File

```
57  VDD Vdd 0 2.5
58
59  VD0 d0 0 PULSE(0 2.5V 200ns 0 0 200ns 400ns)
60  VD1 d1 0 PULSE(0 2.5V 100ns 0 0 100ns 200ns)
61  VS s 0 0 PULSE(0 2.5V 50ns 0 0 50ns 100ns)
62
63
64  .OPTIONS TEMP=25 reltol=1e-6
65  .tran 1NS 400NS
66
67  .control
68  run
69
70  plot V(d0) + 5 V(d1) + 10 V(s) + 15 V(Y)
71
72  .endc
73  .end
```

❖ There was an error in the combination for the 4x1 multiplexer; **the expected results couldn't be obtained**. Below are the combined forms of the 2x1 multiplexers and the test results.

S1 = Dark Red S0 = purple d3b = green d2b = orange d1 = blue d0 = red y = yellow



Spice File

```
144
145   VDD Vdd4 0 2.5
146
147   VGND Gnd4 0 0
148
149   VD0 d0b 0 PULSE(0 2.5V 240ns 0 0 240ns 480ns)
150   VD1 d1b 0 PULSE(0 2.5V 120ns 0 0 120ns 240ns)
151   VD2 d2b 0 PULSE(0 2.5V 60ns 0 0 60ns 120ns)
152   VD3 d3b 0 PULSE(0 2.5V 30ns 0 0 30ns 60ns)
153   VS1 s1 0 0 PULSE(0 2.5V 60ns 0 0 60ns 120ns)
154   VS0 s0 0 0 PULSE(0 2.5V 30ns 0 0 30ns 60ns)
155
156
157   .OPTIONS TEMP=25 reltol=1e-6
158   .tran 1NS 400NS
159
160   .control
161   run
162
163   plot V(d0b) + 5 V(d1b) + 10 V(d2b) + 15 V(d3b) + 20 V(s0) + 25 V(s1) + 30 V(Y4)
164
165   .endc
166   .end
```