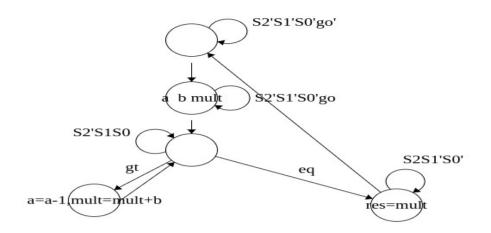
Logic And Circuit Project 2



Truth Table FSM

N2	N1	N0	eq	gt	run	S2	S 1	S0	go
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	1	1	1
0	0	0	1	0	1	0	1	1	1
0	1	1	0	1	0	0	1	1	0
0	1	1	0	1	1	0	1	1	0
0	1	1	1	0	0	1	0	0	0
0	1	1	1	0	1	1	0	0	0
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	1	0	0	0	0
1	0	0	1	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0
1	0	0	1	1	0	0	0	0	0
1	0	0	1	1	1	0	0	0	0

Boolean Expressions

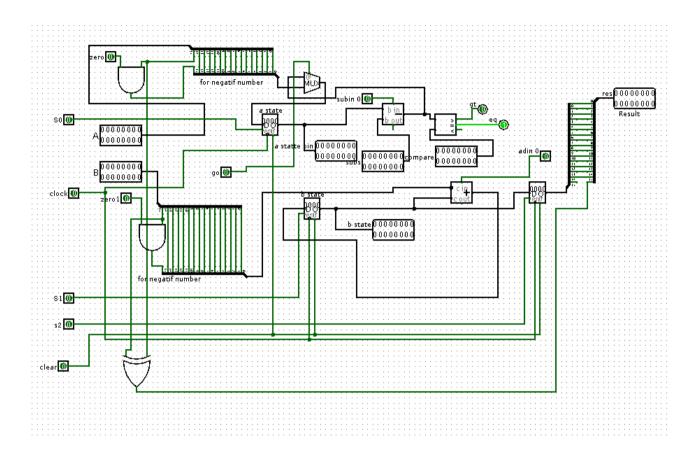
S2: 'N2'N0 gt + N0'gt

S1:'N2'N0 run +'N2 gt

S0:'N2'N0 run +'N2 gt

go:'N2'N0 run

DATAPATH



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