TMS320x2833x, 2823x DSC External Interface (XINTF)

Reference Guide

Literature Number: SPRU949C
September 2007–Revised May 2009

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Read This First

This document describes the external interface (XINTF) used in the F2833x or F2823x device. The XINTF is a nonmultiplexed asynchronous bus.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h or with a leading 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the related devices and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

Data Manual and Errata—

SPRS439— TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 Digital Signal Controllers (DSCs) Data Manual contains the pinout, signal descriptions, as well as electrical and timing specifications for the F2833x/2823x devices.

SPRZ272— TMS320F28335, F28334, F28332, TMS320F28235, F28234, F28232 Digital Signal Controllers (DSCs) Silicon Errata describes the advisories and usage notes for different versions of silicon.

CPU User's Guides—

SPRU430 —TMS320C28x CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). It also describes emulation features available on these DSPs.

SPRUEO2 —TMS320C28x Floating Point Unit and Instruction Set Reference Guide describes the floating-point unit and includes the instructions for the FPU.

Peripheral Guides—

SPRU566 —TMS320x28xx, 28xxx DSP Peripheral Reference Guide describes the peripheral reference guides of the 28x digital signal processors (DSPs).

SPRUFB0 —TMS320x2833x, 2823x System Control and Interrupts Reference Guide describes the various interrupts and system control features of the 2833x and 2823x digital signal controllers (DSCs).

SPRU812 —TMS320x2833x, 2823x Analog-to-Digital Converter (ADC) Reference Guide describes how to configure and use the on-chip ADC module, which is a 12-bit pipelined ADC.

SPRU949 —TMS320x2833x, 2823x DSC External Interface (XINTF) Reference Guide describes the XINTF, which is a nonmultiplexed asynchronous bus, as it is used on the 2833x and 2823x devices.

SPRU963 —TMS320x2833x, 2823x Boot ROM Reference Guide describes the purpose and features of the bootloader (factory-programmed boot-loading software) and provides examples of code. It also describes other contents of the device on-chip boot ROM and identifies where all of the information is located within that memory.

SPRUFB7 —TMS320x2833x, 2823x Multichannel Buffered Serial Port (McBSP) Reference Guide describes the McBSP available on the 2833x and 2823x devices. The McBSPs allow direct interface between a DSP and other devices in a system.

SPRUFB8 —TMS320x2833x, 2823x Direct Memory Access (DMA) Module Reference Guide describes the DMA on the 2833x and 2823x devices.

SPRUG04 —TMS320x2833x, 2823x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide describes the main areas of the enhanced pulse width modulator that include digital motor control, switch mode power supply control, UPS (uninterruptible power supplies), and other forms of power conversion.

SPRUG02 —TMS320x2833x, 2823x High-Resolution Pulse Width Modulator (HRPWM) Reference Guide describes the operation of the high-resolution extension to the pulse width modulator (HRPWM).

SPRUFG4 —TMS320x2833x, 2823x Enhanced Capture (eCAP) Module Reference Guide describes the enhanced capture module. It includes the module description and registers.

SPRUG05 —TMS320x2833x, 2823x Enhanced Quadrature Encoder Pulse (eQEP) Module Reference Guide describes the eQEP module, which is used for interfacing with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine in high-performance motion and position control systems. It includes the module description and registers.

SPRUEU1 —TMS320x2833x, 2823x Enhanced Controller Area Network (eCAN) Reference Guide describes the eCAN that uses established protocol to communicate serially with other controllers in electrically noisy environments.

SPRUFZ5 —TMS320x2833x, 2823x Serial Communications Interface (SCI) Reference Guide describes the SCI, which is a two-wire asynchronous serial port, commonly known as a UART. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format.

SPRUEU3 —TMS320x2833x, 2823x DSC Serial Peripheral Interface (SPI) Reference Guide describes the SPI - a high-speed synchronous serial input/output (I/O) port - that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmed bit-transfer rate.

SPRUG03 — TMS320x2833x, 2823x Inter-Integrated Circuit (I2C) Module Reference Guide describes the features and operation of the inter-integrated circuit (I2C) module.

Tools Guides—

SPRU513 —TMS320C28x Assembly Language Tools v5.0.0 User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

SPRU514 —TMS320C28x Optimizing C/C++ Compiler v5.0.0 User's Guide describes the TMS320C28x™ C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

SPRU608 — TMS320C28x Instruction Set Simulator Technical Overview describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x™ core.

SPRU625 —TMS320C28x DSP/BIOS 5.32 Application Programming Interface (API) Reference Guide describes development using DSP/BIOS.

TMS320x2833x, 2823x DSC External Interface (XINTF)

The external interface (XINTF) is a nonmultiplexed asynchronous bus, similar to the TMS320x281x external interface.

This guide is applicable for the XINTF found on the TMS320x2833x family of processors. This includes all Flash-based and RAM-based devices within the 2833x family.

1 Functional Description

The XINTF is mapped into three fixed memory-mapped zones as defined in Figure 1.

Each of the 28x XINTF zones has a chip-select signal that is toggled when an access is made to that particular zone. On some devices the chip-select signals for two zones may be internally ANDed together to form a single shared chip select. In this manner, the same memory is connected to both zones or external decode logic can be used to separate the two.

Each of the three zones can also be programmed with a specified number of wait states, strobe signal set-up and hold timing. The number of wait states, set-up and hold timing is separately specified for a read access and a write access. In addition, each zone can be programmed for extending wait states externally using the XREADY signal or not. The programmable wait-state, chip-select and programmable strobe timing enables glueless interface to external memories and peripherals.

You specify the set-up/hold and access wait states for each XINTF zone by configuring the associated XTIMINGx registers. The access timing is based on an internal clock called XTIMCLK. XTIMCLK can be set to the same rate as the SYSCLKOUT or to one-half of SYSCLKOUT. The rate of XTIMCLK applies to all of the XINTF zones. XINTF bus cycles begin on the rising edge of XCLKOUT and all timings and events are generated with respect to the rising edge of XTIMCLK.

1.1 Differences from the TMS320x281x XINTF

The XINTF described in this document is functionally very similar to the TMS320x281x XINTF. The main differences are:

- **Data Bus Width:**
  Each XINTF zone can be configured individually to use a 16-bit or 32-bit data bus. Using the 32-bit mode improves performance since 32 bits of data can be read or written in a single access. The data bus width does not change the size of the XINTF zones or memory reach. In 32-bit mode, the lowest address line XA0 becomes a 2nd write enable. The 281x XINTF is limited to a 16-bit data bus.
- **Address Bus Reach:**
  The address reach has been extended to 20 address lines. Zone 6 and Zone 7 both use the full address reach of 1M x 16 words each. The 281x address reach is 512k x 16 words.
- **Direct Memory Access (DMA):**
  All three XINTF zones are connected to the on-chip DMA module. The DMA can be used to copy code and data to or from the XINTF while the CPU is processing other data. The 281x devices do not include a DMA.

- **XINTF Clock Enable:**
  The XINTF clock (XTIMCLK) is disabled by default to save power. XTIMCLK can be enabled by writing a 1 to bit 12 of the PCLKCR3 register. PCLKCR3 is documented in the device-specific system control and interrupts user's guide. For the F2833x devices, it is *TMS320F2833x System Control and Interrupts Reference Guide* (literature number SPRUFB0). Turning off XTIMCLK does not turn off XCLKOUT. There is a separate control to turn off XCLKOUT. On the 281x, XTIMCLK is always enabled.
- **XINTF Pin MUXing:**
  Many of the XINTF pins are MUXed with general purpose I/O. The GPIO mux registers must be configured for XINTF operation before you can use the XINTF. On the 281x, the XINTF has dedicated pins.
- **Number of Zones and Chip Select Signals:**
  The number of XINTF zones has been reduced to 3: Zone 0, Zone 6 and Zone 7. Each of these zones has a dedicated chip select signal. Zone 0 is still read-followed-by write protected as described in Section 1.4. On the 2812 devices, some zone chip-select signals are shared between zones. Zone 0 and Zone 1 share XZCS0AND1 and Zone 6 and Zone 7 share XZCS6AND7.
- **Zone 7 Memory Mapping:**
  Zone 7 is always mapped. On the 281x devices the MPNMC input signal determines if Zone 7 is mapped. Zone 6 and 7 do not share any locations. On 281x, Zone 7 is mirrored within Zone 6.
- **Zone Memory Map Locations:**
  Zone 0 starts at address 0x4000 and is 4K x 16. On 281x Zone 0 starts at address 0x2000 and is 8K x 16. Zone 6 and 7 are both 1M x 16 and start at 0x100000 and 0x200000 respectively. On 281x these two zones are 512K x 16 and 16K x 16.
- **EALLOW protection:**
  The XINTF registers are now EALLOW protected. On 281x, the XINTF registers were not EALLOW protected.

For timing information always refer to the latest data manual for your particular device.

1.2 Differences from the TMS320x2834x XINTF

The XINTF described in this document is functionally very similar to the TMS320x2833x/2823x XINTF. The main differences are:

- **XA0 and $\overline{\text{WE1}}$**
  For the F2833x/F2823x devices, XA0 and $\overline{\text{WE1}}$ share a single pin; however, for the C2834x device, they are separate pins.
- **XBANK Cycle Selection**
  You must choose the number of delay cycles based on the ratio of XTIMCLK and XCLKOUT. Refer to Section 5. C2834x device do not have this requirement.

For timing information always refer to the latest data manual for your particular device.

1.3 Accessing XINTF Zones

An XINTF zone is a region in the 28x memory map that is directly connected to the external interface. Figure 1 shows zone locations. The memory or peripheral attached to a zone can be accessed directly with the CPU or Code Composer Studio.

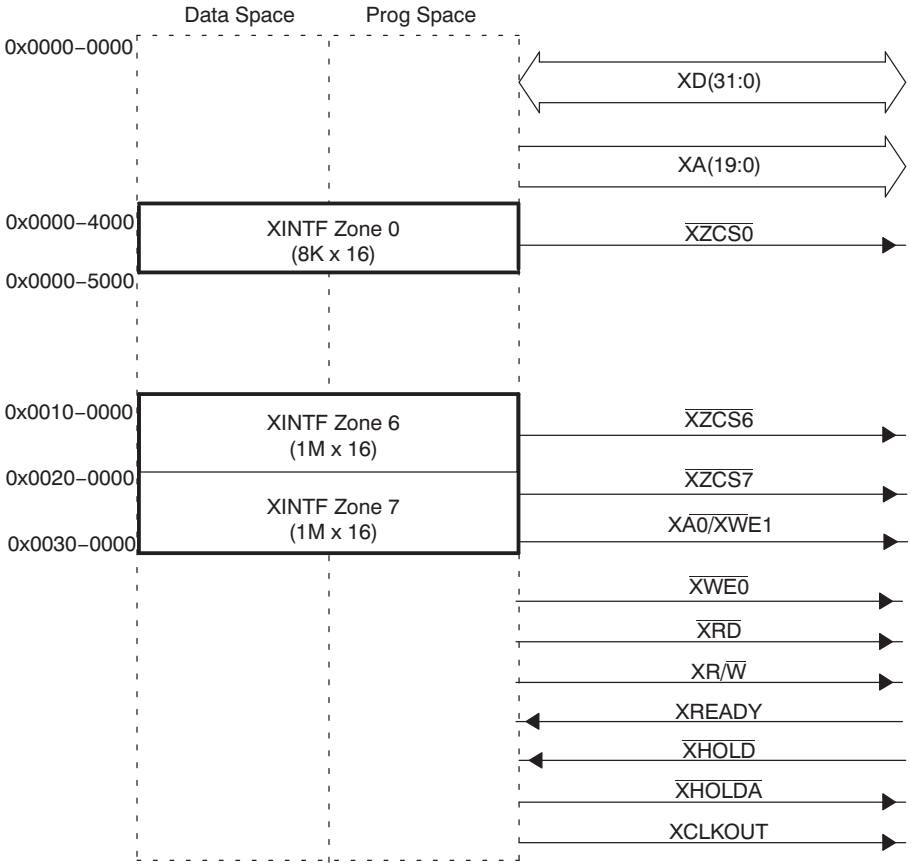
Each XINTF zone can be individually configured with unique read and write access timing and each has an associated zone chip-select signal. This chip-select signal is pulled low so that an access to that zone is currently taking place. On 2833x, 2823x devices, all zone chip select signals are independent.

The external address bus, XA, is 20 bits wide and is shared by all of the zones. What external addresses are generated depends on which zones are being accessed, as follow:

- Zone 0 uses external addresses 0x00000 - 0x00FFF. That is, an access to the first location in Zone 0 will issue external addresses 0x00000 along with chip select 0 ($\overline{\text{XZCS0}}$). An access to the last location in the zone will issue address 0x00FFF with $\overline{\text{XZCS0}}$.

- Zone 6 and 7 both use external addresses 0x00000 - 0xFFFFF. Depending on which zone is accessed, the appropriate zone chip select signal ($\overline{XZCS6}$ or $\overline{XZCS7}$) will also go low.

Figure 1. External Interface Block Diagram



A Each zone can be programmed with different wait states, setup and hold timings. A dedicated zone chip select ($\overline{XZCS}$) signal toggles when an access to a particular zone is performed. These features enable glueless connection to many external memories and peripherals.

B Zones 1 – 5 are reserved for future expansion.

C When the XINTF clock is enabled in PCLKCR3, all zones are enabled.

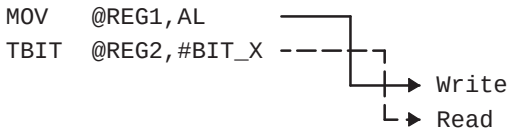
1.4 Write-Followed-by-Read Pipeline Protection

In the 28x CPU pipeline, the read phase of an operation occurs before the write phase. Due to this ordering, a write followed by a read access can actually occur in the opposite order: read followed by write.

For example, the following lines of code perform a write to one location followed by a read from another. Due to the 28x CPU pipeline, the read operation will be issued before the write as shown:

```
MOV   @REG1,AL
TBIT  @REG2,#BIT_X  ---> Read
                    ---> Write
```

On 28x devices, regions of memory where peripheral registers are common are protected from this order reversal by hardware. These regions of memory are said to be read-followed-by-write pipeline protected. XINTF Zone 0 is by default read-followed-by-write pipeline protected. Write and read accesses to Zone 0 are executed in the same order that they are written. For example, a write followed by a read is executed in the same order it was written as shown below:



The 28x CPU automatically protects writes followed by reads to the same memory location. The protection mechanism described above is for cases where the address is not the same, but within a given region of protected memory. In this case, the order of execution is preserved by the CPU automatically inserting enough NOP cycles for the write to complete before the read occurs.

This execution ordering becomes a concern only when peripherals are mapped to the XINTF. A write to one register may update status bits in another register. In this case, the write to the first register must finish before the read to the second register takes place. If the write and read operations are performed in the natural pipeline order, the wrong status may be read since the write would happen after the read. This reversal is not a concern when memory is mapped to the XINTF. Thus, Zone 0 would not typically be used to access memory but instead would be used only to access external peripherals.

If other zones are used to access peripherals that require write-followed-by-read instruction order to be preserved the following solutions can be used:

- Add up to 3 NOP assembly instructions between a write and read instructions. Fewer than three can be used if the code is analyzed and it is found that the pipeline stalls for other reasons.
- Move other instructions before the read to make sure that the write and read are at least three CPU cycles apart.
- Use the -mv compiler option to automatically insert NOP assembly instructions between write and read accesses. This option should be used with caution because this out-of-order execution is a concern only when accessing peripherals mapped to XINTF and not normal memory accesses.

2 XINTF Configuration Overview

This section is an overview of the XINTF parameters that can be configured to fit particular system requirements. The exact configuration used depends on the operating frequency of the 28x, switching characteristics of the XINTF, and the timing requirements of the external devices. Detailed information on each of these parameters is given in the following sections.

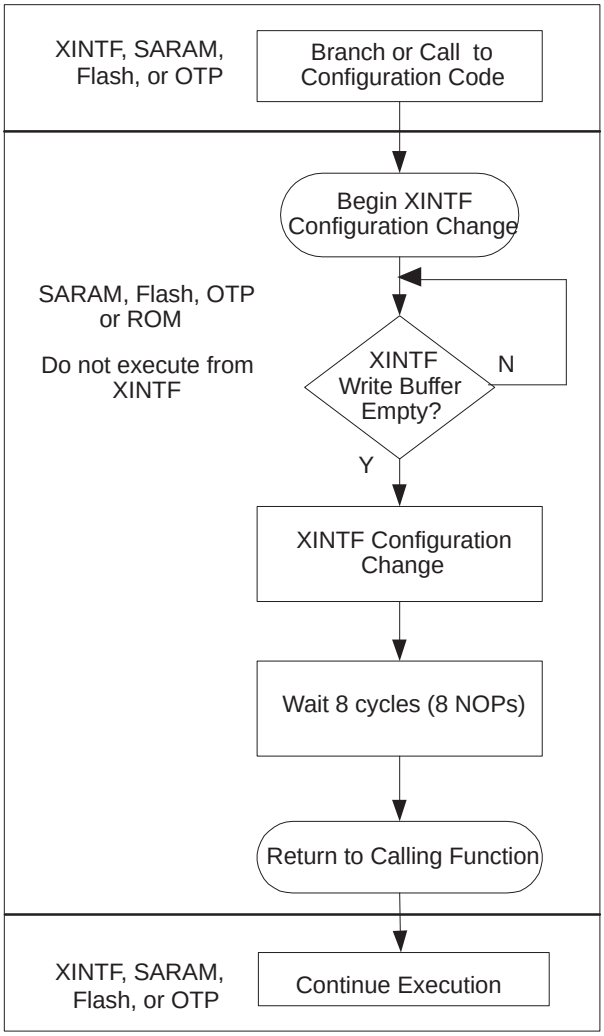
Because a change to the XINTF configuration parameters will cause a change to the access timing, code that configures these parameters should not execute from the XINTF itself.

2.1 Procedure to Change the XINTF Configuration and Timing Registers

During an XINTF configuration or timing change no accesses to the XINTF can be in progress. This includes instructions still in the CPU pipeline, write accesses in the XINTF write buffer, data reads or writes, instruction pre-fetch operations and DMA accesses. To be sure that no access takes place during the configuration follow these steps:

1. Make sure that the DMA is not accessing the XINTF.
2. Follow the procedure shown in Figure 2 to safely modify the XTIMING0/6/7, XBANK, or XINTCNF2 registers.

Figure 2. Access Flow Diagram



Branch or call is required to properly flush the CPU pipeline before the configuration change.

The function that changes the configuration cannot execute from the XINTF.

The XINTF write buffer must be empty before the configuration change.

The stack must not be in external memory.

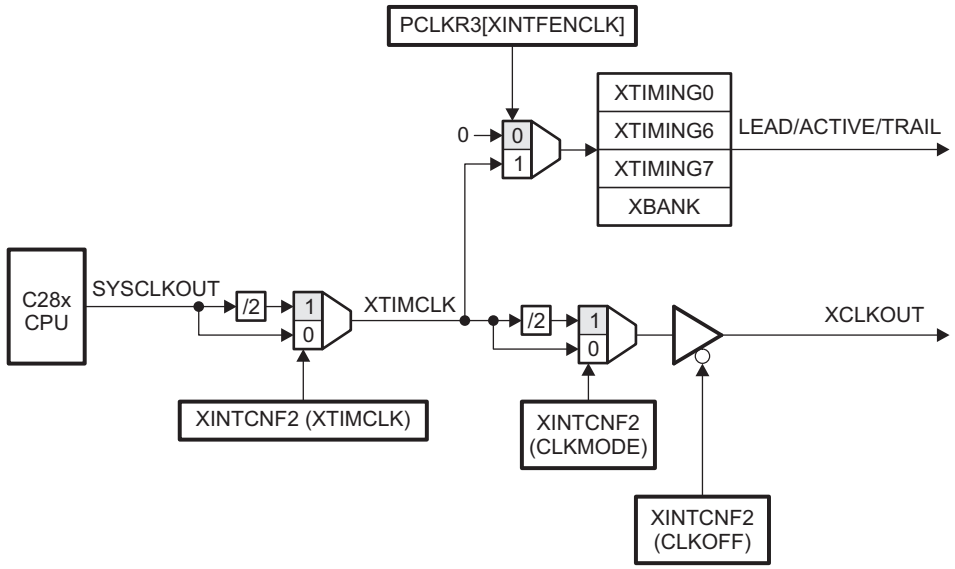
Write instructions to XTIMING0/6/7, XBANK, or XINTCNF2

Wait eight cycles to let the write instructions propogate through the CPU pipeline. This must be done before the return-from-function call is made.

2.2 XINTF Clocking

There are two clocks used by the XINTF module: XTIMCLK and XCLKOUT. Figure 3 shows the relationship between these two clocks and the CPU clock, SYSCLKOUT.

Figure 3. Relationship Between XTIMCLK and SYSCLKOUT



All accesses to all of the XINTF zones are based on the frequency of the internal XINTF clock, XTIMCLK. When configuring the XINTF, you must choose the ratio for the internal XINTF clock, XTIMCLK, with respect to SYSCLKOUT. XTIMCLK can be configured to be either equal or one half of SYSCLKOUT by writing to the XTIMCLK bit in the XINTFCNF2 register. By default XTIMCLK is one-half of SYSCLKOUT.

All XINTF accesses begin on the rising edge of the external clock out, XCLKOUT. In addition, external logic may be clocked off of XCLKOUT. The frequency of XCLKOUT can be configured as a ratio of the internal XINTF clock, XTIMCLK. XCLKOUT can be configured to be either equal or one-half of XTIMCLK by writing to the CLKMODE bit in the XINTFCNF2 register. By default, XCLKOUT is one-half of XTIMCLK, or one-fourth of the CPU clock, SYSCLKOUT.

To reduce system noise, you may choose to not output XCLKOUT on a pin. This is done by writing a 1 to the XINTCNF2[CLKOFF] bit.

2.3 Write Buffer

By default, write access buffering is disabled. In most cases, to improve performance of the XINTF, you should enable write buffering. Up to three writes to the XINTF can be buffered without stalling the CPU. The write buffer depth is configured in the XINTCNF2 register.

2.4 XINTF Access Lead/Active/Trail Wait-State Timing Per Zone

An XINTF zone is a region of memory-mapped addresses that directly access the external interface. The timing of any read or write access to an XINTF zone can be divided into the following three portions: Lead, Active, and Trail. The number of XTIMCLK cycle wait states for each portion of an access can be configured for each XINTF zone in the corresponding zone XTIMING register. Timing for read accesses can be configured separately from timing for write accesses. In addition, to facilitate connections to slow external devices the X2TIMING bit can be used to double the specified lead/active and trail wait states for a particular zone.

During the lead portion, the chip-select signal for the zone being accessed is taken low and the address is placed on the address bus (XA). The total lead period, in XTIMCLK cycles can be configured in the zone's XTIMING register. By default, the lead period is set to the maximum six XTIMCLK cycles for both read and write accesses.

During the active period, the access to the external device is made. For a read access, the read strobe ($\overline{XRD}$) is brought low and data is latched into the DSP. For a write access, the write enable ($\overline{XWE0}$) strobe is brought low and data is placed on the data bus (XD). If the zone is configured to sample the XREADY signal, the external device can control the XREADY signal to further extend the active period beyond the programmed wait states.

The total active period for any access that does not sample XREADY is 1 XTIMCLK cycle plus the number wait states specified in the corresponding XTIMING register. By default, the active wait states are set to the 14 XTIMCLK cycles for both read and write accesses.

The trail period serves as a hold time in which the chip-select signal remains low but the read and write strobes are brought back high. The total trail period, in XTIMCLK cycles can be configured in the zone's XTIMING register. By default the trail period is set to the maximum six XTIMCLK cycles for both read and write accesses.

Based on system requirements, the lead, active and trail wait state values can be configured to best fit the devices connected to a particular XINTF zone. The following should be considered when selecting the timing parameters:

- Minimum wait state requirements as described in Section 4
- The timing characteristics of the XINTF, as described in the device data manual
- The timing requirements of the external device
- Any additional delays between the 28x device and the external device

2.5 XREADY Sampling For Each Zone

By sampling XREADY, the external device can extend the active portion of the access. All of the XINTF zones on a device share the same XREADY input signal but each XINTF zone can individually be configured to either sample or ignore the XREADY signal. In addition, the sampling can be specified as synchronous or asynchronous for each zone.

- Synchronous sampling

  If XREADY is sampled synchronously, then the XREADY signal must meet set-up and hold timing relative to one XTIMCLK edge before the end of the active period. That is, XREADY will be sampled one XTIMCLK cycle before the total lead + active cycles specified for the access.
- Asynchronous sampling

  If XREADY is sampled asynchronously, then the XREADY signal must meet set-up and hold timing relative to three XTIMCLK cycles before the end of the active period. That is, XREADY will be sampled three XTIMCLK cycles before the total lead + active cycles specified for the access.

In both the synchronous and asynchronous case if the XREADY sample is found to be low, the active portion of the cycle is extended by one XTIMCLK cycle and XREADY is sampled again during the next XTIMCLK cycle. This pattern continues until XREADY is sampled high at which time the access will complete normally.

If a zone is configured to sample XREADY, then it is done so for both read and write accesses to that zone. By default each XINTF zone is configured to sample XREADY in the asynchronous mode. When using the XREADY signal, you should consider minimum XINTF wait state requirements as described in Section 4. The minimum requirements are different when sampling XREADY in the synchronous mode vs the asynchronous mode, depending on the following:

- The timing characteristics of the XINTF, as described in the device data sheet.
- The timing requirements of the external device.
- Any additional delays between the 28x device and the external device.

2.6 Bank Switching

When jumping from one XINTF zone to another XINTF zone, a slow device may require extra cycles in order to release the bus in time for another device to gain access. Bank switching allows you to specify a particular zone for which extra cycles will be added for any access that crosses into or out of the specified zone. The zone and number of cycles is configured in the XBANK register. The number of cycles must meet the requirements described in Section 5.

2.7 Zone Data Bus Width

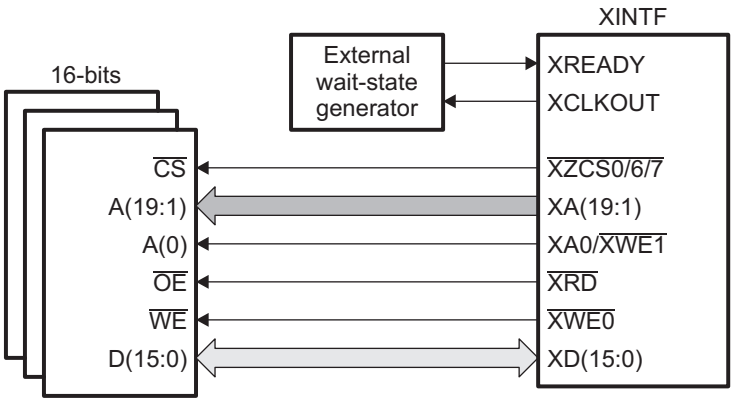
Each XINTF zone can individually be configured for a 16-bit or 32-bit wide data bus. The functionality of the XA0/XWE1 signal changes depending on the configuration. When an XINTF zone is configured for 16-bit mode (XTIMINGx[XSIZE] = 3), then the XA0/XWE1 signal takes on the role of least-significant address line (XA0). In this case, a typical XINTF bus connection looks as shown in Figure 4. The behavior of the XWE0 and XA0/XWE1 signals is summarized in Table 1 and Table 2.

If the width of the three zones (configured by XTIMINGx[XSIZE]) are different from each other, and there is a possibility for back-to-back accesses between two zones of different widths, then at least one delay cycle between the zone accesses should be added using the XBANK configuration discussed in Section 5. For instance, given the zones are configured as follows:

- Zone 0 configured for 16-bit mode (XTIMING0[XSIZE] = 3)
- Zone 6 configured for 32-bit mode (XTIMING6[XSIZE] = 1)
- Zone 7 configured for 32-bit mode (XTIMING7[XSIZE] = 1)

If there is a possibility for back-to-back accesses between Zone 0 and Zone 6 or Zone 0 and Zone 7, then at least one bank switching delay cycle should be added to Zone 0 (i.e. XBANK[BANK] = 0 and XBANK[BCYC] = 1). See Section 5 for configuring XBANK cycles.

Figure 4. Typical 16-bit Data Bus XINTF Connections



When an XINTF zone is configured for 32-bit mode (XTIMINGx[XSIZE] = 1), the XA0/XWE1 signal is the active low write strobe XWE1. XWE1 is used, along with XWE0 for 32-bit bus operation as shown in Figure 5.

Figure 5. Typical 32-bit Data Bus XINTF Connections

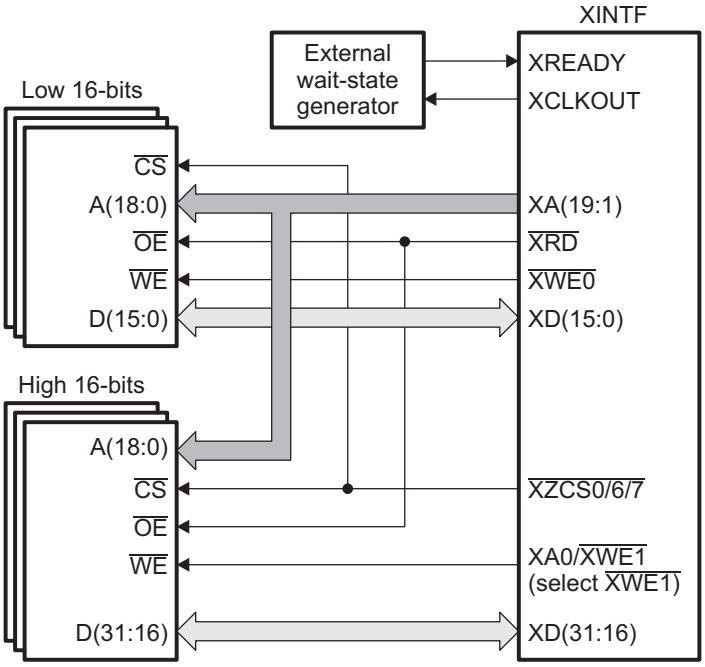


Table 1. 16-bit Mode Behavior

16-bit Mode Write Access	XA0/$\overline{\text{XWE1}}$	$\overline{\text{XWE0}}$
no access	1	1
16-bit value at even address	0	0
16-bit value at odd address	1	0

Table 2. 32-bit Mode Behavior

32-bit Mode Write Access	XA0/$\overline{\text{XWE1}}$	$\overline{\text{XWE0}}$
no access	1	1
16-bit value at even address	1	0
16-bit value at odd address	0	1
32-bit value	0	0

3 External DMA Support (XHOLD, XHOLDA)

The XINTF supports direct memory access (DMA) to its local (off-chip) program and data spaces. This is accomplished with the XHOLD signal input and XHOLDA output. When XHOLD is asserted (low active) a request to the external interface is generated to hold all outputs from the external interface a high impedance state. Upon completion of all outstanding accesses to the external interface, XHOLDA is asserted (low active). XHOLDA signals external devices that the external interface has its outputs in high-impedance state and that another device can control access to external memory or peripherals.

The HOLD Mode bit in XINTCNF2 register enables the automatic generation of a XHOLDA signal and granting access of the external bus, when a valid XHOLD signal is detected. While in HOLD mode, the CPU can continue to execute code from on-chip memory attached to the memory bus. If an attempt is made to access the external interface while XHOLDA is low, a not ready condition is generated, halting the processor. Status bits in the XINTCNF2 register will indicate the state of the XHOLD and XHOLDA signals.

If XHOLD is active, and the CPU attempts a write to the XINTF, the write is not buffered and the CPU will stall. The write buffer is disabled.

The HOLD mode bit in XINTCNF2 register bit will take precedence over the XHOLD input signal. Thus enabling customer code to determine when or not a XHOLD request is to be honored.

The XHOLD input signal is synchronized at the input to the XINTF before any actions are taken. Synchronization is with respect to XTIMCLK.

The HOLDS bit in XINTCNF2 register reflects the current synchronized state of the XHOLD input.

On reset, the HOLD mode bit is enabled, allowing for bootload of external memory using an XHOLD request. If XHOLD signal is active low during reset, the XHOLDA signal is driven low as per normal operation.

During power up, any undefined values in the XHOLD synchronizing latches are ignored and would eventually be flushed out when the clock stabilizes. Hence, synchronizing latches do not need to be reset.

If an XHOLD active low signal is detected, the XHOLDA signal is only driven low after all pending XINTF cycles are completed. Any pending CPU cycles are blocked and the CPU is held in a not-ready state if they are targeted for the XINTF.

Definitions:

Pending XINTF Cycle— Any cycle that is currently in the XINTF FIFO queue.

Pending CPU Cycle—Any cycle that is not in the FIFO queue but is active on the core memory bus.

The XHOLD signal should not be removed until the XHOLDA signal becomes active. Unpredictable results will occur if this rule should be violated.

The state of the XINTF external signals is as follows in HOLD mode:

Signal	HOLD Granted Mode
XA(19:1)	High-impedance
XD(31:0)	High-impedance
XA0/XWE1	High-impedance
XRD, XWE0, XR/W	High-impedance
XZCS0	High-impedance
XZCS6	High-impedance
XZCS7	High-impedance

4 Configuring Lead, Active, and Trail Wait States

XINTF signal timing can be tuned to match specific external device requirements such as setup and hold times for both read and write accesses. The timing parameters can be configured individually for each XINTF zone in the XTIMING registers. Each zone can also be configured to either ignore the XREADY signal or sample it. This allows you to maximize the efficiency of the XINTF based on the memory or peripheral being accessed.

Table 3 shows the relationship between the parameters that can be configured in the XTIMING registers and the duration of the pulse in terms of XTIMCLK cycles, $t_{c(XTIM)}$.

Table 3. Pulse Duration in Terms of XTIMCLK Cycles

		Duration (ns) (1) (2)	
	Description	**X2TIMING = 0**	**X2TIMING = 1**
LR	Lead period, read access	XRDLEAD x $t_{c(xtim)}$	(XRDLEADx2) x $t_{c(xtim)}$
AR	Active period, read access	(XRDACTIVE+WS+1) x $t_{c(xtim)}$	(XRDACTIVEx2+WS+1) x $t_{c(xtim)}$
TR	Trail period, read access	XRDTRAIL x $t_{c(xtim)}$	(XRDTRAILx2) x $t_{c(xtim)}$
LW	Lead period, write access	XWRLEAD x $t_{c(xtim)}$	(XWRLEADx2) x $t_{c(xtim)}$
AW	Active period, write access	(XWRACTIVE+WS+1) x $t_{c(xtim)}$	(XWRACTIVEx2+WS+1) x $t_{c(xtim)}$
TW	Trail period, write access	XWRTRAIL x $t_{c(xtim)}$	(XWRTRAILx2) x $t_{c(xtim)}$

(1) $t_{c(xtim)}$ - Cycle time, XTIMCLK
(2) WS refers to the number of wait states inserted by hardware when using XREADY. If the zone is configured to ignore XREADY (USEREADY= 0) then WS = 0.

Note: Minimum wait-state configurations must be used for each zone's XTIMING register. These wait-state requirements are in addition to any timing requirements as specified by the device to which it is interfaced. For information on requirements for a particular device, see the data sheet for that device.

No internal device hardware is included to detect illegal settings.

4.1 USEREADY = 0

If the XREADY signal is ignored (USEREADY = 0), then the following requirement must be met:

Lead: $LR \geq t_{c(XTIM)}$

$LW \geq t_{c(XTIM)}$

These requirements result in the following XTIMING register configuration restrictions:

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Valid	≥ 1	≥ 0	≥ 0	≥ 1	≥ 0	≥0	0, 1

Examples of valid and invalid timings when not sampling XREADY:

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Invalid[1]	0	0	0	0	0	0	0, 1
Valid	1	0	0	1	0	0	0, 1

(1) No hardware to detect illegal XTIMING configurations

4.2 Synchronous Mode (USEREADY = 1, READYMODE = 0)

If the XREADY signal is sampled in the synchronous mode (USEREADY = 1, READYMODE = 0), then the following requirements must be met:

1 Lead: $LR \geq \times t_{c(XTIM)}$

$LW \geq t_{c(XTIM)}$

2 Active: $AR \geq 2 \times t_{c(XTIM)}$

$AW \geq 2 \times t_{c(XTIM)}$

Note: Restriction does not include external hardware wait states.

These requirements result in the following XTIMING register configuration restrictions:

XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
≥ 1	≥ 1	≥ 0	≥ 1	≥ 1	≥ 0	0, 1[1]

(1) No hardware to detect illegal XTIMING configurations

Examples of valid and invalid timings when using synchronous XREADY:

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Invalid[1]	0	0	0	0	0	0	0, 1
Invalid[1]	1	0	0	1	0	0	0, 1
Valid	1	1	0	1	1	0	0, 1

(1) No hardware to detect illegal XTIMING configurations

4.3 Asynchronous Mode (USEREADY = 1, READYMODE = 1)

If the XREADY signal is sampled in asynchronous mode (USEREADY = 1, READYMODE = 1), then the following requirements must be met:

1 Lead: $LR \geq \times t_{c(XTIM)}$

$LW \geq t_{c(XTIM)}$

2 Active: $AR \geq 2 \times t_{c(XTIM)}$

$AW \geq 2 \times t_{c(XTIM)}$

3 Lead + Active: $LR + AR \geq 4 \times t_{c(XTIM)}$

$LW + AW \geq 4 \times t_{c(XTIM)}$

These requirements result in the following three possible XTIMING register configurations:

Note: Restrictions do not include external hardware wait states.

These requirements result in the following XTIMING register configuration restrictions:

XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
≥ 1	≥ 2	0	≥ 1	≥ 2	0	0, 1

or

XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
≥ 2	≥ 1	0	≥ 2	≥ 1	0	0, 1

Examples of valid and invalid timings when using asynchronous XREADY:

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Invalid[(1)]	0	0	0	0	0	0	0, 1
Invalid[(1)]	1	0	0	1	0	0	0, 1
Invalid[(1)]	1	1	0	1	1	0	0
Valid	1	1	0	1	1	0	1
Valid	1	2	0	1	2	0	0, 1
Valid	2	1	0	2	1	0	0, 1

(1) No hardware to detect illegal XTIMING configurations

Table 4 and Table 5 show the relationship between Lead/Active/Trail values and the XTIMCLK/X2TIMING modes.

Table 4. Relationship Between Lead/Trail Values and the XTIMCLK/X2TIMING Modes

Lead/Trail Value	[XTIMCLK] (1)	X2TIMING (2)	Lead SYSCLKOUT Cycles	Trail SYSCLKOUT Cycles
Formula	0	0	Lead Value * 1	Trail Value * 1
	0	1	Lead Value * 2	Trail Value * 2
	1	0	Lead Value * 2	Trail Value * 2
	1	1	Lead Value * 4	Trail Value * 4
0	X	X	Not a valid value (do not use)	0
1	0	0	1	1
	0	1	2	2
	1	0	2	2
	1	1	4	4
2	0	0	2	2
	0	1	4	4
	1	0	4	4
	1	1	8	8
3	0	0	3	3
	0	1	6	6
	1	0	6	6
	1	1	12	12

(1) XINTCNF2[XTIMCLK] configures the ratio between SYSCLKOUT and XTIMCLK.
(2) X2TIMING is configured per zone in the zone specific XTIMING register.

Table 5. Relationship Between Active Values and the XTIMCLK/X2TIMING Modes

Active Value	XTIMCLK [1]	X2TIMING [2]	Total Active SYSCLKOUT Cycles (includes 1 implied active cycle)
Formula	0	0	Active Value * 1 + 1
	0	1	Active Value * 2 + 1
	1	0	Active Value * 2 + 2
	1	1	Active Value * 4 + 2
0	0	X	1 or Invalid if XREADY used (USEREADY = 1)
	1	X	2 or Invalid if XREADY used (USEREADY = 1)
1	0	0	2
	0	1	3
	1	0	4
	1	1	6
2	0	0	3
	0	1	5
	1	0	6
	1	1	10
3	0	0	4
	0	1	7
	1	0	8
	1	1	14
4	0	0	5
	0	1	9
	1	0	10
	1	1	18
5	0	0	6
	0	1	11
	1	0	12
	1	1	22
6	0	0	7
	0	1	13
	1	0	14
	1	1	26
7	0	0	8
	0	1	15
	1	0	16
	1	1	30

(1) XINTCNF2[XTIMCLK] configures the ratio between SYSCLKOUT and XTIMCLK.
(2) X2TIMING is configured per zone in the zone specific XTIMING register.

5 Configuring XBANK Cycles

When jumping from one XINTF zone to another XINTF zone, a slow device may require extra cycles in order to release the bus in time for another device to gain access. Bank switching allows you to specify a particular zone for which extra cycles will be added for any access that crosses into or out of the specified zone. The zone and number of cycles is configured in the XBANK register.

You must choose the number of delay cycles based on the ratio of XTIMCLK and XCLKOUT. There are three cases:

- **Case 1: XTIMCLK = SYSCLKOUT**
  When XTIMCLK is equal to SYSCLKOUT, there are no restrictions on the selection of XBANK[BCYC].
- **Case 2: XTIMCLK = 1/2 SYSCLKOUT and XCLKOUT = 1/2 XTIMCLK**
  In this case, XBANK[BCYC] must not be 4 or 6. Any other value is valid.
- **Case 3: XTIMCLK = 1/2 SYSCLKOUT and XCLKOUT = XTIMCLK**
- **Case 4: XTIMCLK = 1/4 SYSCLKOUT**
  When delay cycles are inserted between two accesses, there is a zone access before the delay cycles and a zone access after the delay cycles. In order for bank switching to correctly insert the correct number of delay cycles the total access time to the first zone in the sequence must be greater than the number of bank cycles specified. To make sure this happens select XBANK[BCYC] such that it is smaller than the total access to the zone.
  Consider this example: Bank switching is enabled for Zone 7 (XBANK[BANK] = 7) . Delay cycles will be added to any access into or out of Zone 7. This means:
  – If an access to Zone 0 is followed by Zone 7
    The access to Zone 0 must be longer than the number of bank cycles specified.
  – If an access to Zone 1 is followed by Zone 7
    The access to Zone 1must be longer than the number of bank cycles specified.
  – If an access to Zone 7 is followed by Zone 0:
    The access to Zone 7 must be longer than the number of bank cycles specified.
  The lead, active and trail values can be used to make sure the access time is longer than the number of delay cycles. Since XREADY can only extend the access longer, it need not be considered.
  If X2TIMING is 0, then select:
  – XBANK[BCYC] < XWRLEAD + XWRACTIVE + 1 + XWRTRAIL and
  – XBANK[BCYC] < XRDLEAD + XRDACTIVE + 1 + XRDTRAIL
  If X2TIMING = 1, then select:
  – XBANK[BCYC] < XWRLEADx2 + XWRACTIVEx2 + 1 + XWRTRAILx2 and
  – XBANK[BCYC] < XRDLEADx2 + XRDACTIVEx2 + 1 + XRDTRAILx2

Table 6 lists valid XBANK[BCYC] values for different timing configurations. The lead, active and trail values are specified in the zones XTIMING register. When determining the proper XBANK[BCYC] values, use the timing that yields the longest access time. This may be the read or the write timing.

Table 6. Valid XBANK Configurations

Valid XBANK[BCYC]	Total Access Time	XRDLEAD or XWRLEAD	XRDACTIVE or XWRACTIVE	XRDTRAIL or XWRTRAIL	X2TIMING
< 5	1 + (2+1) + 1 = 5	1	2	1	0
< 6	1 + (3+1) + 1 = 6	1	3	1	0
< 7	2 + (3+1) + 1 = 7	2	3	1	0
< 5	1x2 + 0x2 + 1 + 1x2	1	0	1	1
< 5	1x2 + 1x2 + 1 + 0x2	1	1	0	1

6 XINTF Registers

Table 7 shows the XINTF configuration registers. Modification of these registers will affect the timing of XINTF accesses and should be performed only by code running outside of the XINTF.

Table 7. XINTF Configuration and Control Register Mapping

Name	Address	Size (x16)	Description (1)
XTIMING0	0x0000–0B20	2	XINTF Timing Register, Zone 0
XTIMING6 (2)	0x0000–0B2C	2	XINTF Timing Register, Zone 6
XTIMING7	0x0000–0B2E	2	XINTF Timing Register, Zone 7
XINTCNF2 (3)	0x0000–0B34	2	XINTF Configuration Register
XBANK	0x0000–0B38	1	XINTF Bank Control Register
XREVISION	0x0000–0B3A	1	XINTF Revision Register
XRESET	0x0000 083D	1	XINTF Reset Register

(1) All XINTF registers are EALLOW protected.
(2) XTIMING1 - XTIMING5 are reserved for future expansion and are not currently used.
(3) XINTCNF1 is reserved and not currently used.

The individual timing parameters can be programmed into the XTIMING registers described in Figure 6.

6.1 XINTF Timing Registers

Each XINTF zone has one timing register. Changes to this register will affect the timing of that particular zone. Changes to a zone's timing register should be made only by code executing outside of that zone.

Note:

- Minimum wait-state requirements for different modes are shown in Section 2.
- The external device to which the 28x is interfaced may have additional timing constraints. See the vendor documentation for details.
- No logic is included to detect illegal settings.

Figure 6. XTIMING0/6/7 Register

31	22	21	18	17	16
Reserved	X2TIMING	Reserved		XSIZE	
R-0	R/W-1	R-0		R/W-1	

15	14	13	12	11	9	8
READYMODE	USEREADY	XRDLEAD		XRDACTIVE		XRDTRAIL
R/W-1	R/W-1	R/W-1		R/W-1		R/W-1

7	6	5	2	1	0
XRDTRAIL	XWRLEAD	XWRACTIVE		XWRTRAIL	
R/W-1	R/W-1	R/W-1			

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 8. XTIMING0/6/7 Register Field Descriptions

Bit	Field	Value	Description (1)
31:23	Reserved	0	

(1) This register is EALLOW protected.

Table 8. XTIMING0/6/7 Register Field Descriptions (continued)

Bit	Field	Value	Description [(1)]	
22	X2TIMING		This bit specifies the scaling factor of the XRDLEAD, XRDACTIVE, XRDTRAIL, XWRLEAD, XWRACTIVE, and XWRTRAIL values for the zone.	
		0	The values are scaled 1:1	
		1	The values are scaled 2:1 (doubled). This the default mode of operation on power up and reset.	
21:18	Reserved	0		
17:16	XSIZE		These two bits must always be written to as either 0, 1 (32-bit data bus) or 1, 1 (16-bit data bus). Any other combination is reserved and will result in incorrect XINTF behavior.	
		00	Reserved - results in incorrect XINTF behavior	
		01	32-bit interface. In this mode the zone will use all 32 data lines. The XA0/$\overline{WE1}$ signal will behave as $\overline{WE1}$ as described in Section 2.7 .	
		10	Reserved - results in incorrect XINTF behavior	
		11	16-bit interface. In this mode the zone will only use 16 data lines. The XA0/$\overline{WE1}$ signal will behave as XA0. (default at reset)	
15	READYMODE		Sets the XREADY input sampling for the zone as synchronous or asynchronous. This bit is ignored if XREADY is not sampled (USEREADY = 0).	
		0	XREADY input is synchronous for the zone.	
		1	XREADY input is asynchronous for the zone. (default at reset)	
14	USEREADY		Determines if accesses to the zone will sample or ignore the XREADY input signal.	
		0	The XREADY signal is ignored when accesses are made to the zone.	
		1	The XREADY signal can further extend the active portion of an access to the zone past the minimum defined by the XRDACTIVE and XWRACTIVE fields.	
13:12	XRDLEAD		Two-bit field that defines the read cycle lead wait state period, in XTIMCLK cycles. If the X2TIMING bit is set, then the number of wait states are doubled. See Section 4 for minimum requirements in different modes.	
			X2TIMING	**Read Lead Period**
		00	X	Invalid
		01	0	1 XTIMCLK cycle
			1	2 XTIMCLK cycles
		10	0	2 XTIMCLK cycles
			1	4 XTIMCLK cycles
		11	0	3 XTIMCLK cycles
			1	6 XTIMCLK cycles (default)

Table 8. XTIMING0/6/7 Register Field Descriptions (continued)

Bit	Field	Value	Description [(1)]	
11:9	XRDACTIVE		Three-bit field that defines the read cycle active wait state period, in XTIMCLK cycles. The active period is by default 1 XTIMCLK cycle. Therefore, the total active period is (1 + XWRACTIVE) XTIMCLK cycles. If the X2TIMING bit is set, then the number of wait states are doubled. See Section 4 for minimum requirements in different modes.	
			X2TIMING	**Read Active Period Waitstates**
		000	0	0
		001	0	1 XTIMCLK cycle
			1	2 XTIMCLK cycles
		010	0	2 XTIMCLK cycles
			1	4 XTIMCLK cycles
		011	0	3 XTIMCLK cycles
			1	6 XTIMCLK cycles
		100	0	4 XTIMCLK cycles
			1	8 XTIMCLK cycles
		101	0	5 XTIMCLK cycles
			1	10 XTIMCLK cycles
		110	0	6 XTIMCLK cycles
			1	12 XTIMCLK cycles
		111	0	7 XTIMCLK cycles
			1	14 XTIMCLK cycles (default)
8:7	XRDTRAIL		Two-bit field that defines the read cycle trail wait state period, in XTIMCLK cycles. If the X2TIMING bit is set, then the number of wait states are doubled. See Section 4 for minimum requirements in different modes.	
			X2TIMING	**Read Trail Period**
		00	0	0
		01	0	1 XTIMCLK cycle
			1	2 XTIMCLK cycles
		10	0	2 XTIMCLK cycles
			1	4 XTIMCLK cycles
		11	0	3 XTIMCLK cycles
			1	6 XTIMCLK cycles (default)
6:5	XWRLEAD		Two-bit field that defines the write cycle lead wait state period, in XTIMCLK cycles. If the X2TIMING bit is set, then the number of wait states are doubled. See Section 4 for minimum requirements in different modes.	
			X2TIMING	**Write Lead Period**
		00	0	0
		01	0	1 XTIMCLK cycle
			1	2 XTIMCLK cycles
		10	0	2 XTIMCLK cycles
			1	4 XTIMCLK cycles
		11	0	3 XTIMCLK cycles
			1	6 XTIMCLK cycles (default)

Table 8. XTIMING0/6/7 Register Field Descriptions (continued)

Bit	Field	Value	Description [(1)]	
4:2	XWRACTIVE		Three-bit field that defines the write cycle active wait state period, in XTIMCLK cycles. The active period is by default 1 XTIMCLK cycle. Therefore, the total active period is (1 + XWRACTIVE) XTIMCLK cycles. If the X2TIMING bit is set, then the number of wait states are doubled. See Section 4 for minimum requirements in different modes.	
			X2TIMING	**Write Active Period Waitstates**
		000	0	0
		001	0	1 XTIMCLK cycle
			1	2 XTIMCLK cycles
		010	0	2 XTIMCLK cycles
			1	4 XTIMCLK cycles
		011	0	3 XTIMCLK cycles
			1	6 XTIMCLK cycles
		100	0	4 XTIMCLK cycles
			1	8 XTIMCLK cycles
		101	0	5 XTIMCLK cycles
			1	10 XTIMCLK cycles
		110	0	6 XTIMCLK cycles
			1	12 XTIMCLK cycles
		111	0	7 XTIMCLK cycles
			1	14 XTIMCLK cycles (default)
1:0	XWRTRAIL		Two-bit field that defines the write cycle trail wait state period, in XTIMCLK cycles. If the X2TIMING bit is set, then the number of wait states are doubled. See Section 4 for minimum requirements in different modes.	
			X2TIMING	**Write Trail Period**
		00	x	
		01	0	1 XTIMCLK cycle
			1	2 XTIMCLK cycles
		10	0	2 XTIMCLK cycles
			1	4 XTIMCLK cycles
		11	0	3 XTIMCLK cycles
			1	6 XTIMCLK cycles (default)

6.2 XINTF Configuration Register

Figure 7. XINTF Configuration Register (XINTCNF2)

31															19	18			16
Reserved																XTIMCLK			
R-0																R/W-1			

15				12	11	10	9	8
Reserved					HOLDAS	HOLDS	HOLD	Reserved
R-0					R-x	R-y	R-0	R-1

7	6	5	4	3	2	1	0
WLEVEL		Reserved	Reserved	CLKOFF	CLKMODE	WRBUFF	
R-0		R-0	R-1	R/W-0	R/W-1	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset/ x = $\overline{\text{XHOLDA}}$ output; y = $\overline{\text{XHOLD}}$ input

Table 9. XINTF Configuration Register Field Descriptions

Bit	Field	Value	Description [1]
31:19	Reserved		
18:16	XTIMCLK		These bits select the fundamental clock for the timing of lead, active and trail switching operations as defined by the XTIMING and XBANK registers: This setting affects all of the XINTF zones. Changes to the XTIMCLK ratio should be made only by code executing outside of the XINTF. Note: XTIMCLK is disabled by default. It must be enabled in the PCLKCR3 register before the XINTF registers can be written to.
		000	XTIMCLK = SYSCLKOUT/1
		001	XTIMCLK = SYSCLKOUT/2 (default)
		010	Reserved
		100	Reserved
		101	Reserved
		110	Reserved
		111	Reserved
15:12	Reserved		
11	HOLDAS		This bit reflects the current state of the $\overline{\text{XHOLDA}}$ output signal. It can be read by the user to determine if the external interface is currently granting access to an external device.
		0	$\overline{\text{XHOLDA}}$ output signal is low.
		1	$\overline{\text{XHOLDA}}$ output signal is high.
10	HOLDS		This bit reflects the current state of the $\overline{\text{XHOLD}}$ input signal. It can be read by the user to determine if an external device is requesting access to the external bus.
		0	$\overline{\text{XHOLD}}$ input signal is low.
		1	$\overline{\text{XHOLD}}$ input signal is high.

(1) This register is EALLOW protected.

Table 9. XINTF Configuration Register Field Descriptions (continued)

Bit	Field	Value	Description (1)
9	HOLD		This bit grants a request to an external device that drives the $\overline{\text{XHOLD}}$ input signal and the $\overline{\text{XHOLDA}}$ output signal.
			If this bit is set while $\overline{\text{XHOLD}}$ and $\overline{\text{XHOLDA}}$ are both low (external bus accesses granted) then the $\overline{\text{XHOLDA}}$ signal is forced high (at the end of the current cycle) and the external interface is taken out of high-impedance mode.
			On a reset $\overline{\text{XRS}}$, this bit is set to zero. If, on a reset, the $\overline{\text{XHOLD}}$ signal is active low, then the bus and all signal strobes must be in high-impedance state and the $\overline{\text{XHOLDA}}$ signal is also driven active-low.
			When HOLD mode is enabled and $\overline{\text{XHOLDA}}$ is active-low (external bus grant active) then the core can still execute code from internal memory. If an access is made to the external interface, then a not ready signal is generated and the core is stalled until the $\overline{\text{XHOLD}}$ signal is removed.
		0	Automatically grants a request to an external device that is driving both the $\overline{\text{XHOLD}}$ input signal and the $\overline{\text{XHOLDA}}$ output signal low (default)
		1	Does not grant a request to an external device that drives the $\overline{\text{XHOLD}}$ input signal low while the $\overline{\text{XHOLDA}}$ output signal stays high.
8	Reserved		
7:6	WLEVEL		The current number of writes buffered are detectable as follows:
		00	Empty
		01	1 value currently in the write buffer
		10	2 values currently in the write buffer
		11	3 values currently in the write buffer
5:4	Reserved		
3	CLKOFF		Turn XCLKOUT mode off. This is done for power savings and noise reduction. This bit is set to 0 on a reset.
		0	XCLKOUT is enabled. (default)
		1	XCLKOUT is disabled.
2	CLKMODE		XCLKOUT divide by 2 mode. All bus timings, irrespective of which mode is enabled, will start from the rising edge of XCLKOUT. The default mode of operation on power up and reset is /2 mode. Changes to the CLKMODE bit should be made only by code executing outside of the XINTF.
		0	XCLKOUT is equal to XTIMCLK
		1	XCLKOUT is a divide by 2 of XTIMCLK (default)
1:0	WRBUFF		Write Buffer Depth. The write buffer allows the processor to continue execution without waiting for XINTF write accesses to complete. The write buffer depth is selectable as follows:
		00	No write buffering. The CPU will be stalled until the write completes on the XINTF. (default) Note: Default mode on reset ($\overline{\text{XRS}}$).
		01	One write is buffered and the CPU will stall for the second write. The CPU is stalled until the write cycle begins on the XINTF (there could be a read cycle currently active on the XINTF).
		10	Two writes are buffered and the CPU will stall for the third write. The CPU will be stalled until the first write begins its cycle on the XINTF.
		11	Three writes are buffered. The CPU is stalled if a fourth write follows. The CPU will be stalled until the first write begins its cycle on the XINTF.
			Order of execution is preserved, e.g., writes are performed in the order they were accepted. The processor is stalled on XINTF reads until all pending writes are done and the read access completes. If the buffer is full, any pending reads or writes to the buffer will stall the processor.
			The Write Buffer Depth can be changed; however, it is recommended that the write buffer depth be changed only when the buffer is empty (this can be checked by reading the “Write Buffer Level” bits). Writing to these bits when the level is not zero may have unpredictable results.

6.3 XBANK Register

Figure 8. XBANK Register

15	6	5	3	2	0
Reserved		BCYC		BANK	
R-0		R/w-1		R/W-1	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 10. XBANK Register Field Descriptions

Bit	Field	Value	Description [(1)]
15:6	Reserved		
5:3	BCYC		These bits specify the number of XTIMCLK cycles to add between any consecutive access that crosses into or out of the specified zone, be it a read or write, program or data space. The number of XTIMCLK cycles can be 0 to 7. On a reset ($\overline{XRS}$), the value defaults to 7 XTIMCLK cycles (14 SYSCLKOUT cycles).
		000	0 cycle
		001	1 XTIMCLK cycle
		010	2 XTIMCLK cycles
		011	3 XTIMCLK cycles
		100	4 XTIMCLK cycles
		101	5 XTIMCLK cycles
		110	6 XTIMCLK cycles
		111	7 XTIMCLK cycles (default)
2:0	BANK		These bits specify the XINTF zone for which bank switching is enabled, ZONE 0 to ZONE 7. At reset, XINTF Zone 7 is selected.
		000	Zone 0
		001	Reserved
		010	Reserved
		011	Reserved
		100	Reserved
		101	Reserved
		110	Zone 6
		111	Zone 7 (selected at reset by default)

(1) This register is EALLOW protected.

6.4 XREVISION Register

Figure 9. XREVISION Register

15	0
REVISION	
R-0	

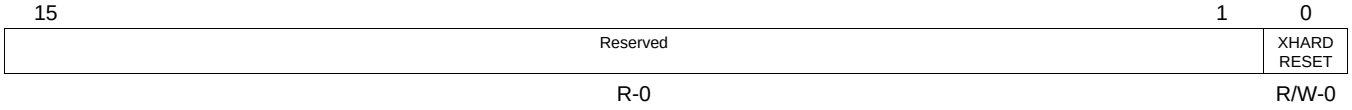
LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 11. XREVISION Register Field Descriptions

Bit	Field	Value	Description
15:0	REVISION		Current XINTF Revision. For internal use/reference. Test purposes only. Subject to change.

6.5 XRESET Register

Figure 10. XRESET Register



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 12. XRESET Register Field Descriptions

Bit	Field	Value	Description [(1)]
31	Reserved		
30	XHARDRESET		A hard reset may be used in cases where the CPU detects the XREADY signal is stuck low during a DMA transfer.
		0	Writing a 0 has no effect. This bit always reads back a 0.
		1	Force an XINTF hard reset. The XTIMING, XBANK, and XINTCNF2 registers will return to their default state and all XINTF signals will go to their inactive state. Any pending access will be lost including data in the write buffer. Any stall condition to DMA will be released.

(1) This register is EALLOW protected.

7 Signal Descriptions

Table 13. XINTF Signal Descriptions

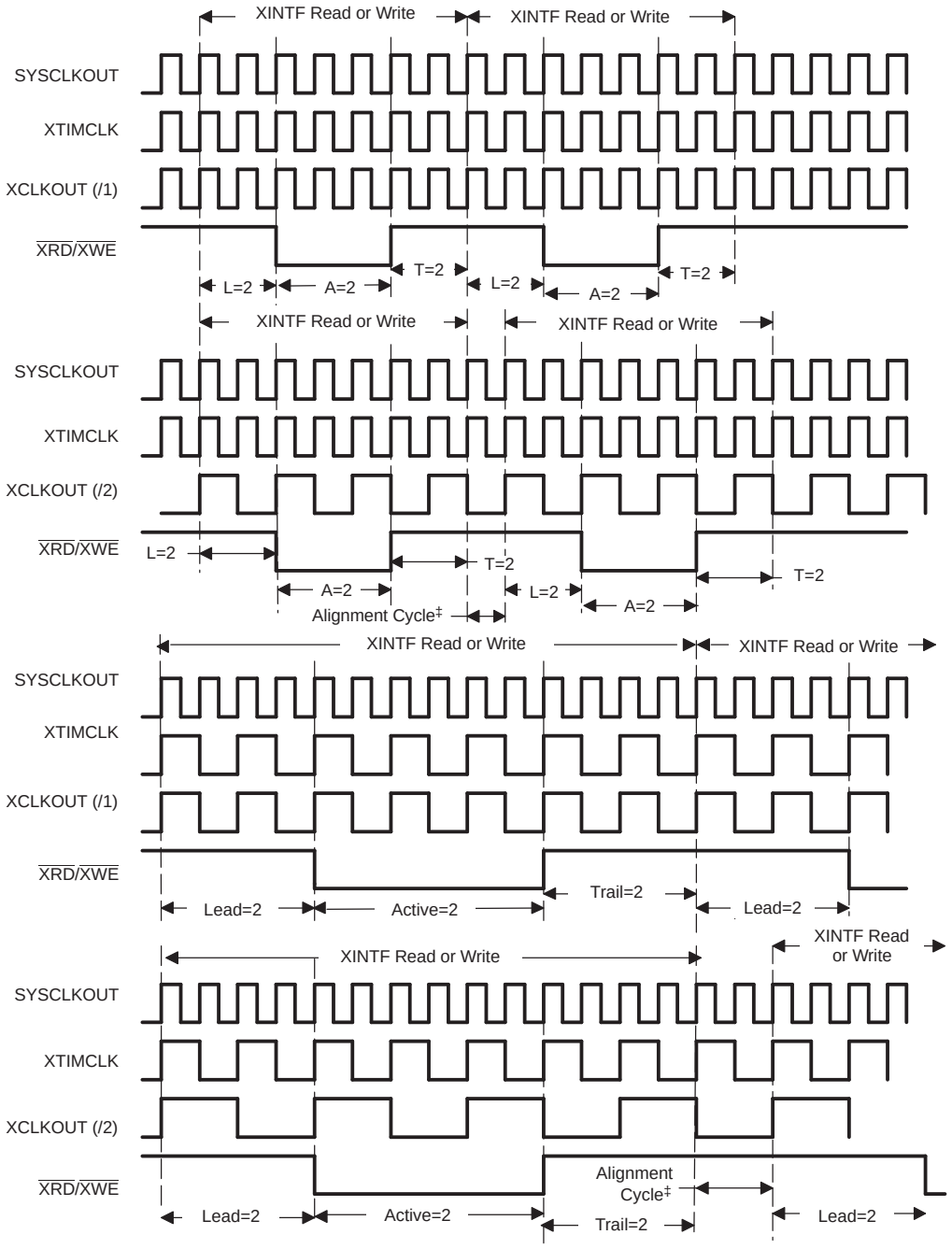
Name	Type	Description
XD(31:0)	I/O/Z	Bidirectional 32-bit data bus. In 16-bit mode only XD(15:0) are used.
XA(31:1)	O/Z	Address bus. The address is placed on the bus on the rising edge of XCLKOUT and held on the bus until the next access. Specific devices may not have all 32 address lines. See the data sheet for a specific device.
XA0/ $\overline{\text{XWE1}}$	O/Z	In 16-bit data mode (see), this signal is the least significant address line (XA0). In 32-bit data mode, this signal is the active low write strobe $\overline{\text{XWE1}}$. $\overline{\text{XWE1}}$ is used, along with $\overline{\text{XWE0}}$, for 32-bit bus operation as shown in Section 2.7.
XCLKOUT	O/Z	Single output clock derived from the XTIMCLK to be used for on-chip and off-chip wait-state generation and as a general-purpose clock source. XCLKOUT is either the same frequency or ½ the frequency of XTIMCLK, as defined by the CLKMODE bit in the XINTCNF2 register. At reset XCLKOUT = XTIMCLK/2 XTIMCLK = SYSCLKOUT/2
$\overline{\text{XWE0}}$	O/Z	Active low write strobe. In 16-bit mode, this signal is driven low on all bus modes and data size types. In 32-bit mode, it is driven as shown in Figure 5. The write strobe waveform is specified, per zone basis, by the Lead, Active, Trail periods in the XTIMINGx registers.
$\overline{\text{XRD}}$	O/Z	Active low read strobe. This signal is driven low on all bus modes and data size types. The read strobe waveform is specified, per zone basis, by the Lead, Active, Trail periods in the XTIMINGx registers. Note: The $\overline{\text{XRD}}$ and $\overline{\text{XWE0}}$ signals are mutually exclusive.
XR/$\overline{\text{W}}$	O/Z	Read-not-write control. When high, this signal indicates a read cycle is active, when low, it indicates a write cycle is active. This signal is normally held high. The XR/$\overline{\text{W}}$ signal performs similar functions to the $\overline{\text{XRD}}$ and $\overline{\text{XWE0}}$ signals. Generally, users opt to use $\overline{\text{XWE0}}$ and $\overline{\text{XWE1}}$ because they are cleaner and easier to use.
$\overline{\text{XZCS0}}$ $\overline{\text{XZCS6}}$ $\overline{\text{XZCS7}}$	O	Zone chip-selects. These signals are active when an access to the addressed zone is performed.
XREADY	I	Indicates peripheral is READY to complete the access when asserted to 1. For each XINTF zone, this can be configured to be a synchronous or an asynchronous input. In synchronous mode, the XINTF interface block requires XREADY to be valid one XTIMCLK clock cycle before the end of the active period. In asynchronous mode, The XINTF interface block samples XREADY three XTIMCLK clock cycles before the end of the active period. XREADY is sampled at the XTIMCLK rate independent of the XCLKOUT mode.
$\overline{\text{XHOLD}}$	I	This signal, when active low, requests the XINTF to release the external bus (place all busses and strobes into high-impedance state). The XINTF releases the bus when any current access is complete and there are no pending accesses on the XINTF. This signal is an asynchronous input and is synchronized by XTIMCLK.
$\overline{\text{XHOLDA}}$	O/Z	This signal is driven active low, when the XINTF has granted an $\overline{\text{XHOLD}}$ request. All XINTF busses and strobe signals will be in a high-impedance state. This signal is released when the $\overline{\text{XHOLD}}$ signal is released. External devices should only drive the external bus when this signal is active low.

8 Waveforms

Figure 11 shows example timing waveforms for various XTIMCLK and XCLKOUT modes assuming X2TIMING = 0 and Lead = 2, Active = 2 and Trail = 2.

Note: The diagrams included in this document are conceptual, cycle-by-cycle representations of the XINTF behavior. They do not take into account any buffer delays and additional setup times that will be found on a physical device. For more exact device-specific timing information for the XINTF, see the data sheet electrical timing specifications for that device.

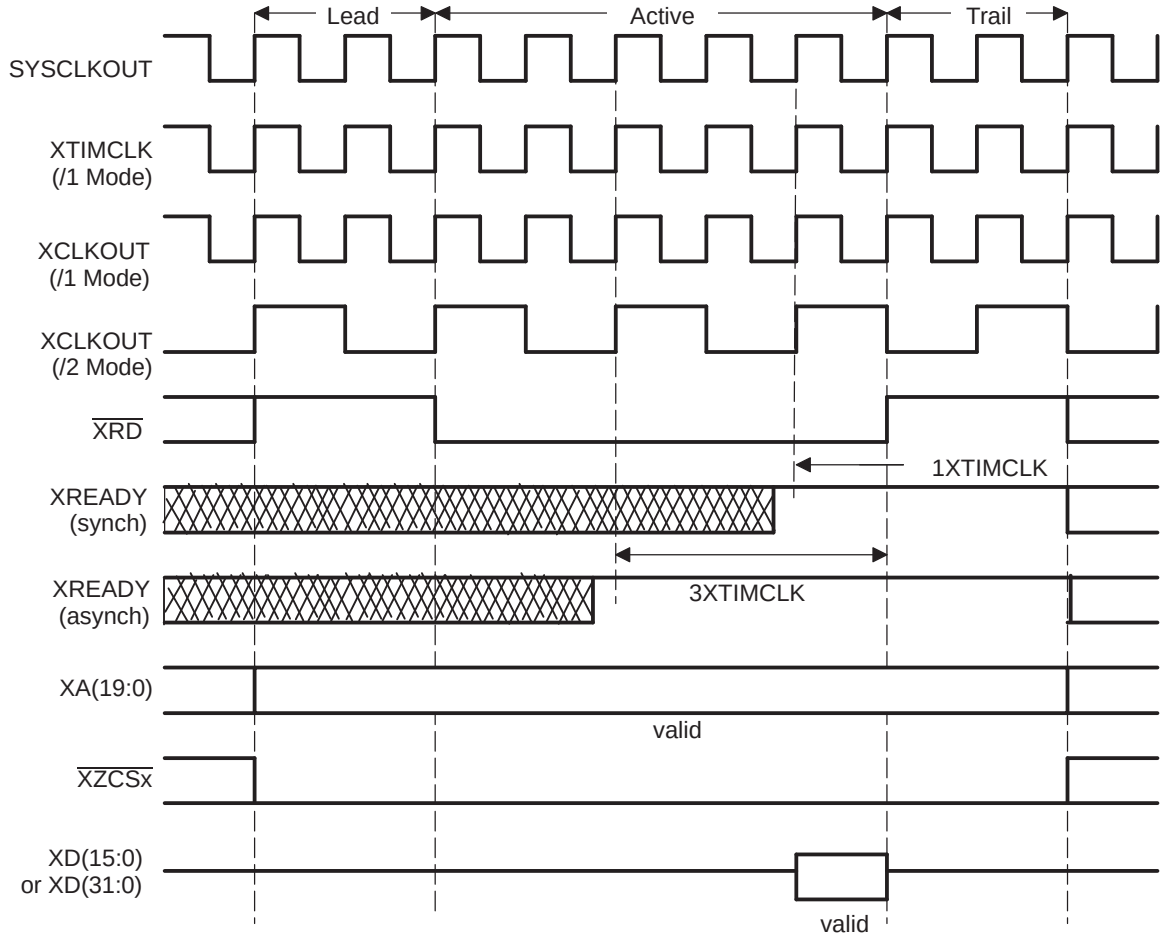
Figure 11. XTIMCLK and XCLKOUT Mode Waveforms



A X2TIMING = 0, XRDLEAD/XWRLEAD = 2, XRDACTIVE/XWRACTIVE = 2, XRDTRAIL/XWRTRAIL = 2

B Alignment cycle. Necessary to make sure all bus cycles start on rising edge of XCLKOUT.

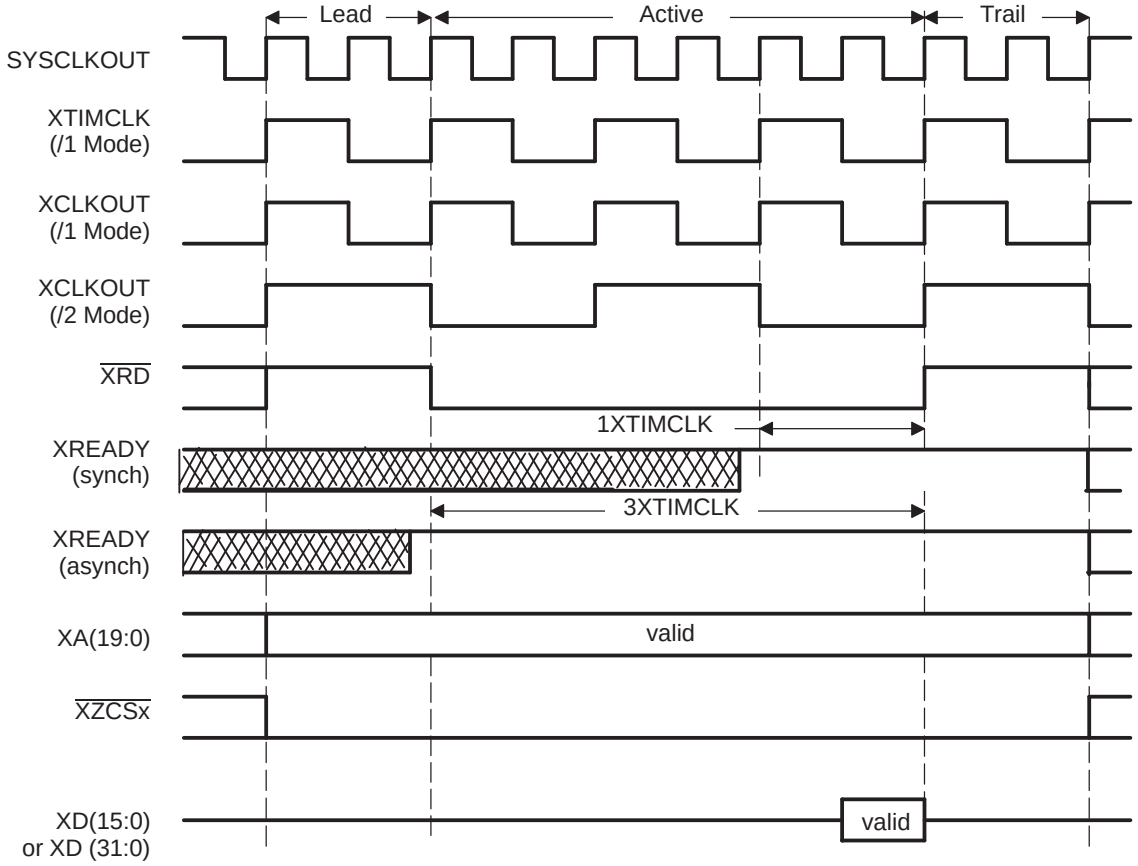
Figure 12. Generic Read Cycle (XTIMCLK = SYSCLKOUT mode)



A XRDLEAD = 2, XRDACTIVE = 4, XRDTRAIL = 2

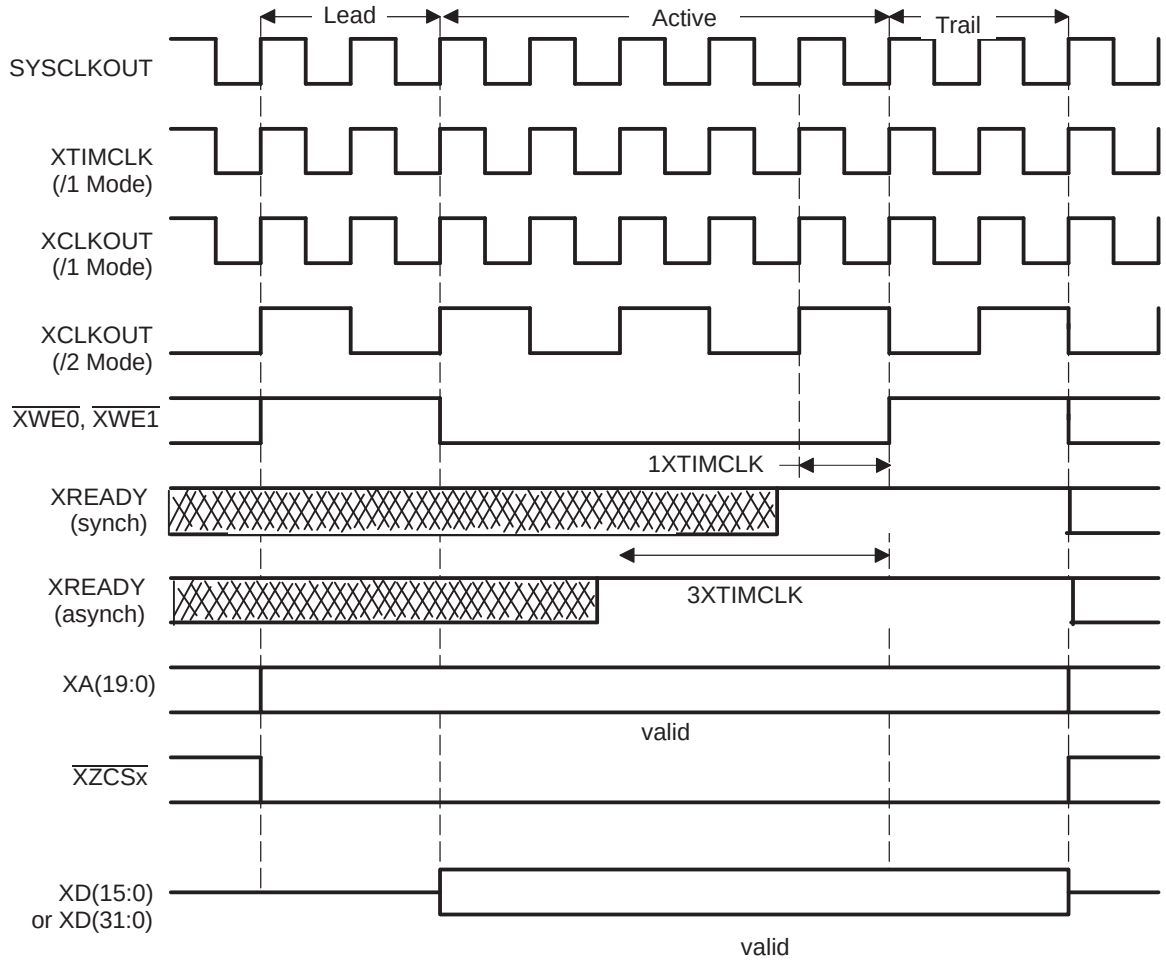
The XREADY signal can be sampled synchronously or asynchronously or ignored by each zone. If it is sampled synchronously, then the XREADY signal MUST meet set-up and hold timing relative to one XTIMCLK edge before the end of the active period. If it is sampled asynchronously, then the XREADY signal MUST meet set-up and hold timing relative to three XTIMCLK edges before the end of the active period. If XREADY is low at the sampling interval, an extra XTIMCLK period is added to the active phase and the XREADY input is sampled again on the next rising edge of XTIMCLK. XCLKOUT has no effect on the sampling interval.

Figure 13. Generic Read Cycle (XTIMCLK = ½ SYSCLKOUT mode)



A XRDLEAD = 1, XRDACTIVE = 3, XRDTRAIL = 1

Figure 14. Generic Write Cycle (XTIMCLK = SYSCLKOUT mode)



A XWRACTIVE = 2, XWRACTIVE = 4, XWRTRAIL = 2

B If the lead and active timing parameters are set low enough, it may not be possible to generate a valid XREADY signal. No hardware is added to detect this.

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