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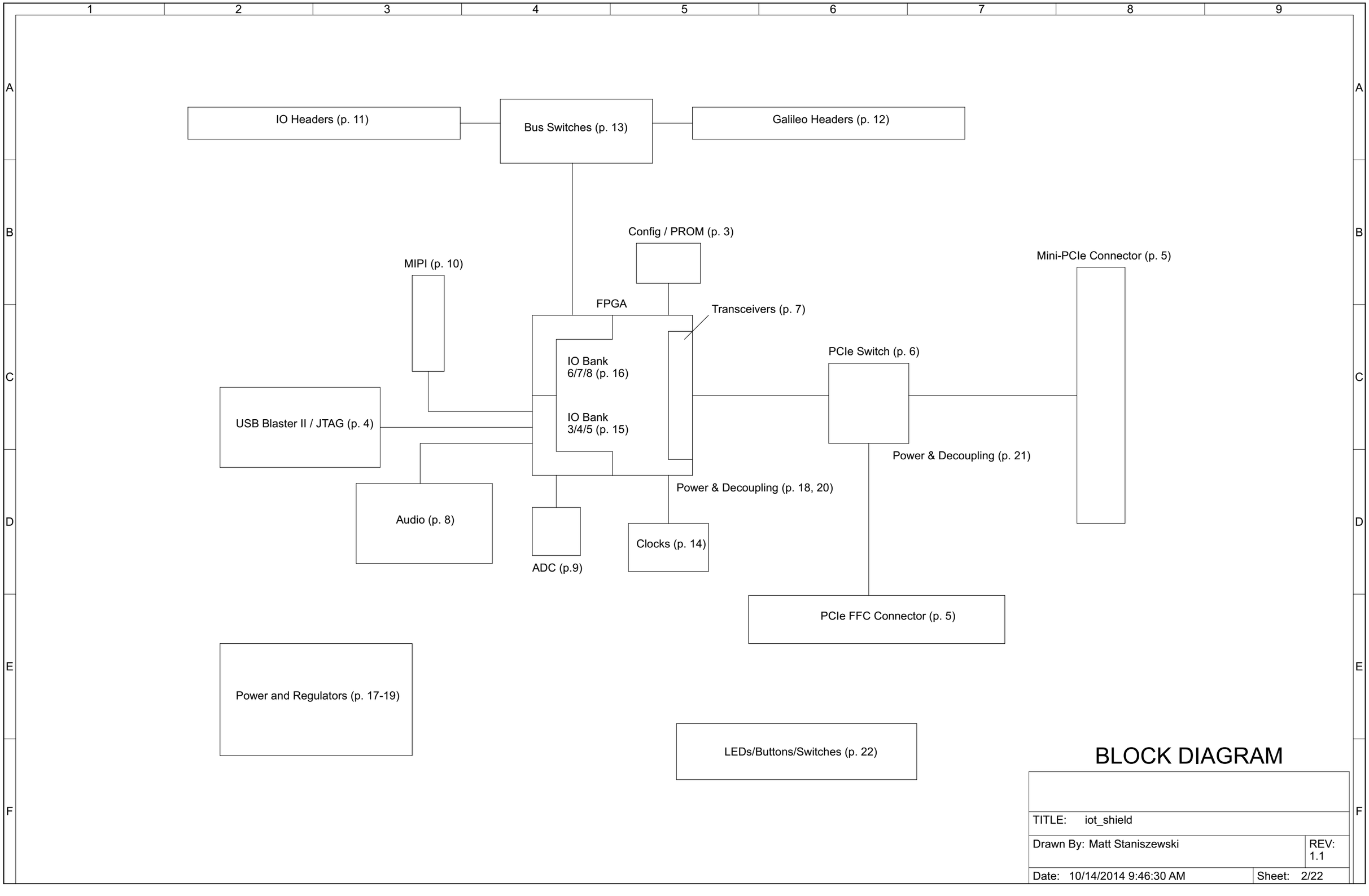


# BLOCK DIAGRAM

| | | |
|---|---|---|
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| Drawn By: Matt Staniszewski | | REV: 1.1 |
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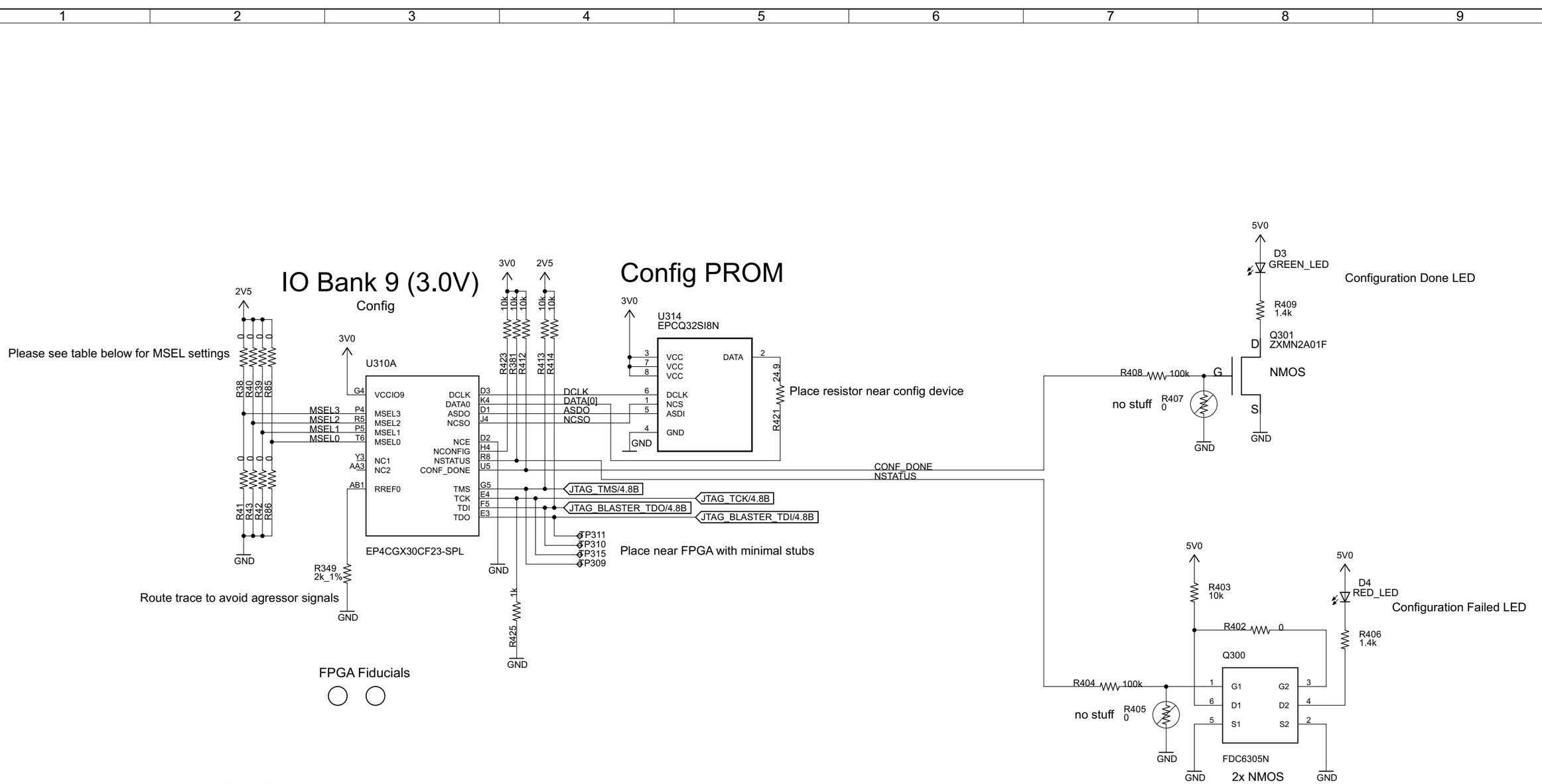


## MSEL Settings

| Function | MSEL3 | | MSEL2 | | MSEL1 | | MSEL0 | |
|---|---|---|---|---|---|---|---|---|
| Resistor | R166 | R164 | R167 | R165 | R170 | R168 | R171 | R169 |
| stuff | X | | | X | X | | X | |
| no stuff | | X | X | | | X | | X |

Current configuration: AS x1 Mode, Fast POR

# FPGA CONFIG / JTAG

| | |
|---|---|
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# Micro USB

J16
10118194-0001LF

Route high-speed USB signals carefully

VBUS_5V
FX2_D_N
FX2_D_P
R130 0
no stuff
SH1 SH2 SH3 SH4 SH5 SH6
CH_GND

U11
ESD
TPD2EUSB30DR
R303 1M
C300 4700pF
10k R131

Y300 24MHz
Crystal
C303 12pF
C302 12pF
C301 0.1uF

Place on USB peninsula for J20

# JTAG Header

J301
CLP-107-02-F-D-K
C_USB_MAX_TCK
C_USB_MAX_TDO
C_USB_MAX_TMS
C_USB_MAX_TDI
R335 1k
R371 1k
R372 1k

# USB Controller

U300
CY7C68013A-56PVXC

FX2_RESETN
FX2_WAKEUP
24M_XTALIN
24M_XTALOUT
USB_CLK
R304 0
FX2_SLRDN
FX2_SLWRN
FX2_SCL
FX2_SDA
R126 2k
R125 2k
R305 20k
C316 0.1uF

PB0/FD0 FX2_PB0
PB1/FD1 FX2_PB1
PB2/FD2 FX2_PB2
PB3/FD3 FX2_PB3
PB4/FD4 FX2_PB4
PB5/FD5 FX2_PB5
PB6/FD6 FX2_PB6
PB7/FD7 FX2_PB7
PD0/FD8 FX2_PD0
PD1/FD9 FX2_PD1
PD2/FD10 FX2_PD2
PD3/FD11 FX2_PD3
PD4/FD12 FX2_PD4
PD5/FD13 FX2_PD5
PD6/FD14 FX2_PD6
PD7/FD15 FX2_PD7
PA0/INT0
PA1/INT1 FX2_PA1
PA2/SLOE FX2_PA2
PA3/WU2 FX2_PA3
PA4/FIFOADR0 FX2_PA4
PA5/FIFOADR1 FX2_PA5
PA6/PKTEND FX2_PA6
PA7/FLAGD/SLCS FX2_PA7
CTL0/FLAGA FX2_FLAGA
CTL1/FLAGB FX2_FLAGB
CTL2/FLAGC FX2_FLAGC

C74 C75 C76 C78 C53 C52 C51 C77 0.1uF

Place near CY7C68013A

FX2_SDA R123 0 MAX_SDA

MAX811SEUS+T
R98 100k FX2_RESETN
C54 0.1uF
Voltage Monitor U10

# CPLD

U5A
EPM570GT100

FX2_PB5 FX2_PB4 FX2_PB3 FX2_FLAGA FX2_PB7 FX2_PB6 FX2_PB2
FX2_FLAGB FX2_FLAGC FX2_SCL FX2_PB1 FX2_PA1 FX2_PA2 USB_DISABLEN
USB_CLK/16.4F FX2_PB0 MAX_SDA FX2_RESETN

IOB1_1 IOB1_2 IOB1_3 IOB1_4 IOB1_5 IOB1_6 IOB1_7 IOB1_8
IOB1_9 IOB1_10 IOB1_11 IOB1_12 IOB1_13 IOB1_14 IOB1_15 IOB1_16
IOB1/GCLK0 IOB1/GCLK1 IOB1/DEV_OE IOB1_DEV_CLRN
IOB1_17 IOB1_18 IOB1_19 IOB1_20 IOB1_21 IOB1_22 IOB1_23 IOB1_24
IOB1_25 IOB1_26 IOB1_27 IOB1_28 IOB1_29 IOB1_30 IOB1_31 IOB1_32
TMS TDI TCK TDO

FX2_PA5 FX2_PA4 FX2_PA3 FX2_SLRDN FX2_SLWRN FX2_PA7 FX2_PA6 JTAG_TCK/3.5C
FX2_PD6 FX2_PD7 FX2_PD4 FX2_PD5
JTAG_BLASTER_TDO/3.4C JTAG_TMS/3.4C JTAG_BLASTER_TDI/3.5C
C_USB_MAX_TMS R129 0 FX2_PD1
C_USB_MAX_TDI R128 0 FX2_PD2
C_USB_MAX_TCK R95 0 FX2_PD0
C_USB_MAX_TDO R127 0 FX2_PD3

R45 1k

CPLD Fiducials

U5B
EPM570GT100

JTAG_TX SC_RX SC_TX JTAG_RX
USB_RESETN/16.3C USB_OEN/16.6B USB_RDN/16.6C USB_WRN/16.6B
R20 0 M570_PCIE_JTAG_EN
FPGA_CPLD_CLK1/16.6B FPGA_CPLD_CLK0/16.6B

IOB2_1 IOB2_2 IOB2_3 IOB2_4 IOB2_5 IOB2_6 IOB2_7 IOB2_8
IOB2_9 IOB2_10 IOB2_11 IOB2_12 IOB2_13 IOB2_14 IOB2_15 IOB2_16
IOB2/GCLK2 IOB2/GCLK3
IOB2_20 IOB2_19 IOB2_18 IOB2_17 IOB2_21 IOB2_22 IOB2_23 IOB2_24
IOB2_25 IOB2_26 IOB2_27 IOB2_28 IOB2_29 IOB2_30 IOB2_31 IOB2_32
IOB2_33 IOB2_34 IOB2_35 IOB2_36 IOB2_37 IOB2_38

USB_DATA0/16.7C USB_DATA1/16.8C USB_DATA2/16.6C USB_DATA3/16.6C USB_DATA4/16.7B USB_DATA5/16.8B USB_DATA6/16.8B USB_DATA7/16.8C
USB_ADDR0/16.7C USB_ADDR1/16.8C USB_FULL/16.6C USB_EMPTY/16.6C USB_SCL/16.7B USB_SDA/16.7B
FPGA_CPLD_IO0/16.7C FPGA_CPLD_IO1/16.8B FPGA_CPLD_IO2/16.8B FPGA_CPLD_IO3/16.7C FPGA_CPLD_IO4/16.8C FPGA_CPLD_IO5/16.7B

R376 R375 R374 R373 1k

U5C
EPM570GT100

GNDINT VCCINT GNDIO VCCIO1 VCCIO2

C320 C334 C333 C332 C321 C335 0.1uF

Place near MAX II

# USB Blaster Status LEDs

U307
MMDT3904-7-F
JTAG_RX R334 200
JTAG_TX R336 200
R302 1.2k
R308 1.2k
D14 GREEN_LED
D13 GREEN_LED

U7
MMDT3904-7-F
SC_RX R338 200
SC_TX R311 200
R300 1.2k
R301 1.2k
D16 GREEN_LED
D15 GREEN_LED

# USB BLASTER II

| | |
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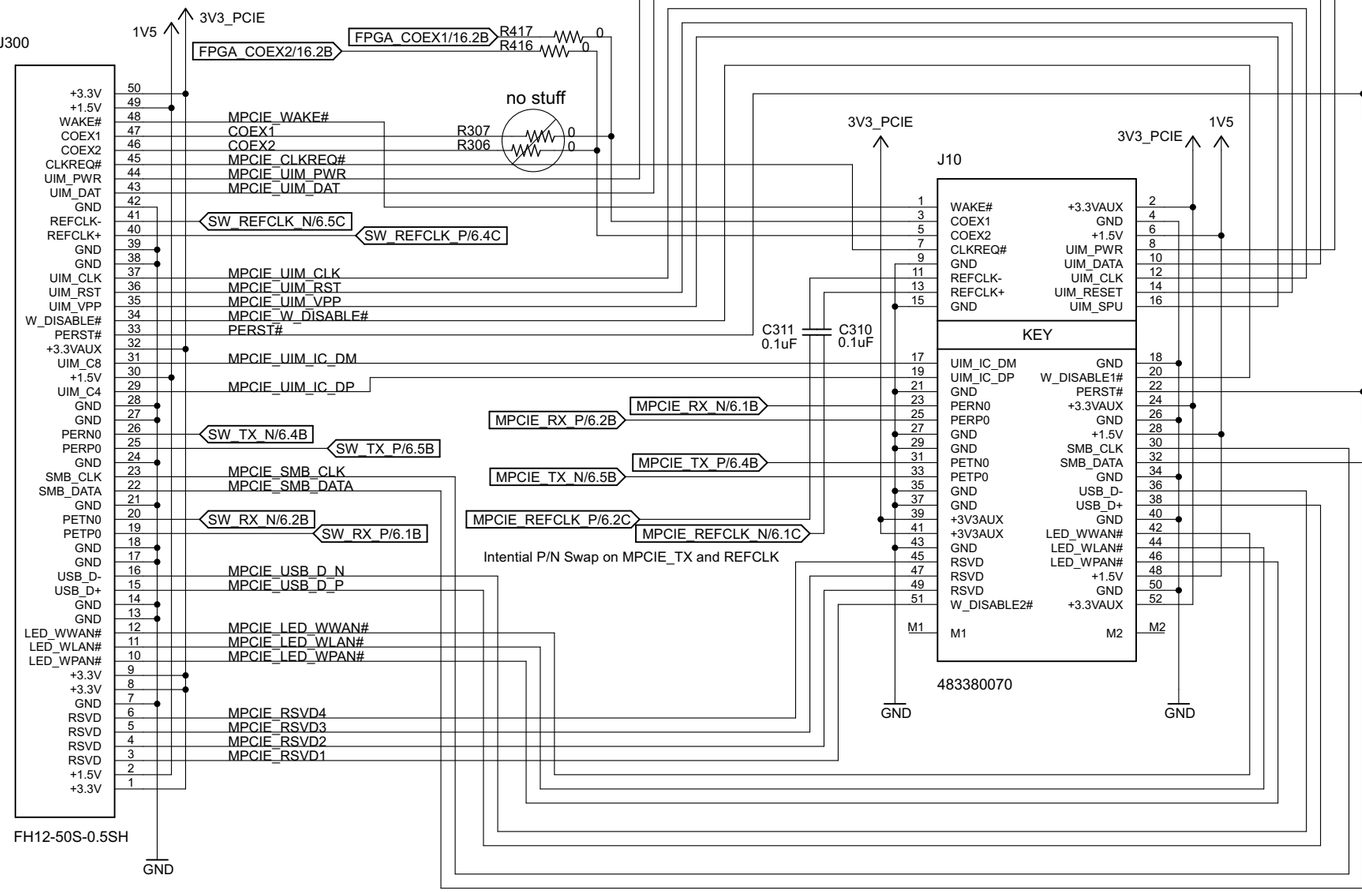
# FFC Connector

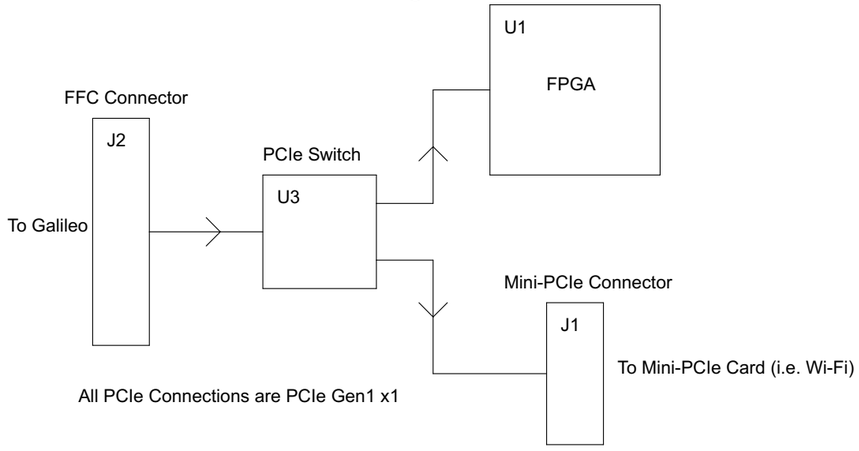



FFC Cable to Galileo

# Mini-PCIe Connector




# PCIe Flow Diagram




# PCIe CONNECTORS

| | |
|---|---|
| TITLE: iot_shield | |
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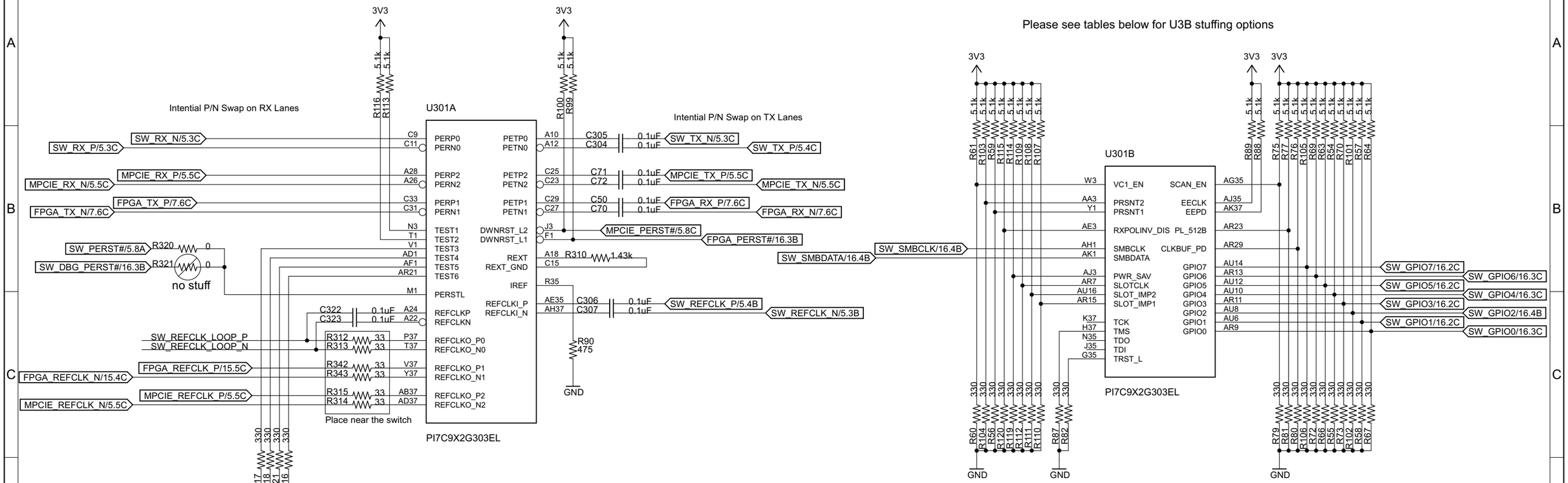


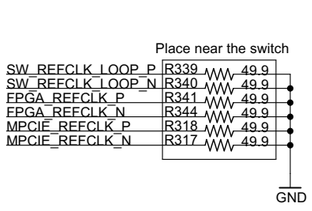


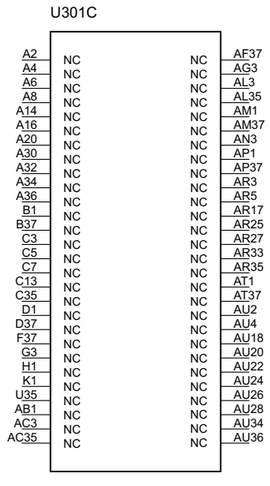


| Function | VC1_EN | | PRSNT2 | | PRSNT1 | | RXPOLINV_DIS | | PWR_SAV | | SLOTCLK | | SLOT_IMP2 | | SLOT_IMP1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Resistor | R47 | R46 | R53 | R48 | R54 | R49 | R55 | R50 | R56 | R51 | R57 | R52 | R58 | R68 | R66 | R69 |
| stuff | | X | | X | | X | | X | X | | X | | X | | X | |
| no stuff | X | | X | | X | | X | | | X | | X | | X | | X |

| Function | SCAN_EN | | PL_512B | | CLKBUF_PD | | GPIO7 | | GPIO6 | | GPIO5 | | GPIO4 | | GPIO3 | | GPIO2 | | GPIO1 | | GPIO0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Resistor | R72 | R73 | R40 | R39 | R59 | R41 | R60 | R42 | R61 | R43 | R62 | R44 | R63 | R45 | R64 | R65 | R74 | R77 | R75 | R78 | R76 | R79 |
| stuff | | X | X | | | X | X | | X | | X | | X | | X | | X | | X | | X | |
| no stuff | X | | | X | X | | | X | | X | | X | | X | | X | | X | | X | | X |

# PCIe SWITCH

| | |
|---|---|
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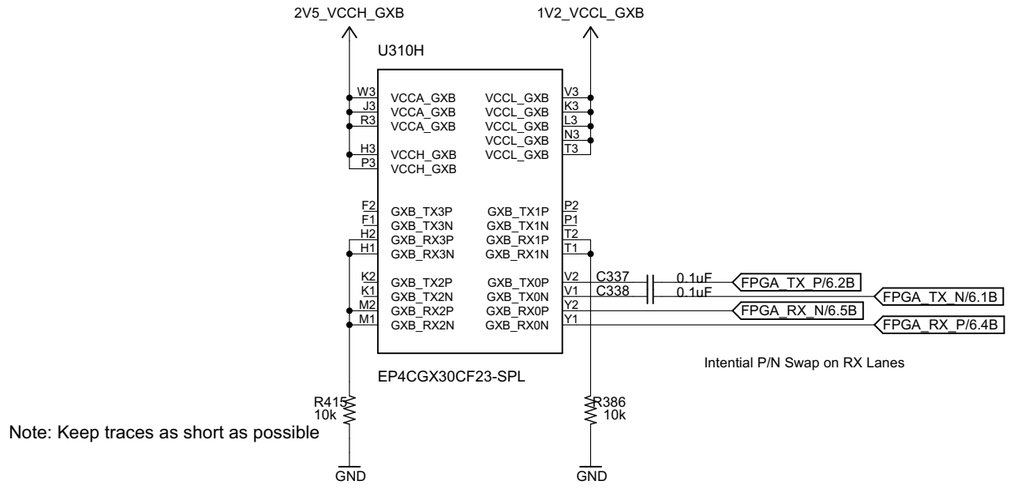


# FPGA PCIe CONNECTIONS

| | | |
|---|---|---|
| | | |
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# Codec

U3

TLV320AIC3100IRHBR

3V3 3V3

R10 2.7k
R11 2.7k
R5 10k

5V0 3V3 1V8

C360 0.1uF
C356 10uF
C26 0.1uF
C27 0.1uF
C358 100uF_1210_6.3V
C357 0.1uF
C359 0.1uF
C362 0.1uF
C361 10uF

GND

CODEC_GPIO1/16.6B
CODEC_DIN/16.6C
CODEC_WCLK/16.6B
CODEC_BCLK/16.6C
CODEC_MCLK/14.6E
CODEC_SDA/16.6C
CODEC_SCL/16.6C
CODEC_RESET#/16.6B

C10 0.1uF

# Speaker Output

L1 MPZ1608S221A
L2 MPZ1608S221A
L3 MPZ1608S221A
L5 MPZ1608S221A

SPKP_R
SPKM_R
SPKP_L
SPKM_L

no stuff R435 0
no stuff R436 0

ED555/4DS
J4

CODEC_DOUT/16.6B

# Headphone Jack

C354 47uF
C355 47uF

HP_L
HP_R
HP_DET

J5
SJ-43516-SMT

R401 2.2k
R400 2.2k
R399 2.2k

0 R14

VOL_MICDET

no stuff 0 R12

# Microphone Jack

C28 0.47uF
C29 0.47uF

J6
MIC1LP
MIC1RP
SJ-43516-SMT

# Volume Control (optional)

3V3
R420 48.7k
R422 3361S-1-503GLF
R424 0
C363 0.22uF
VOL
no stuff

# AUDIO

| | | |
|---|---|---|
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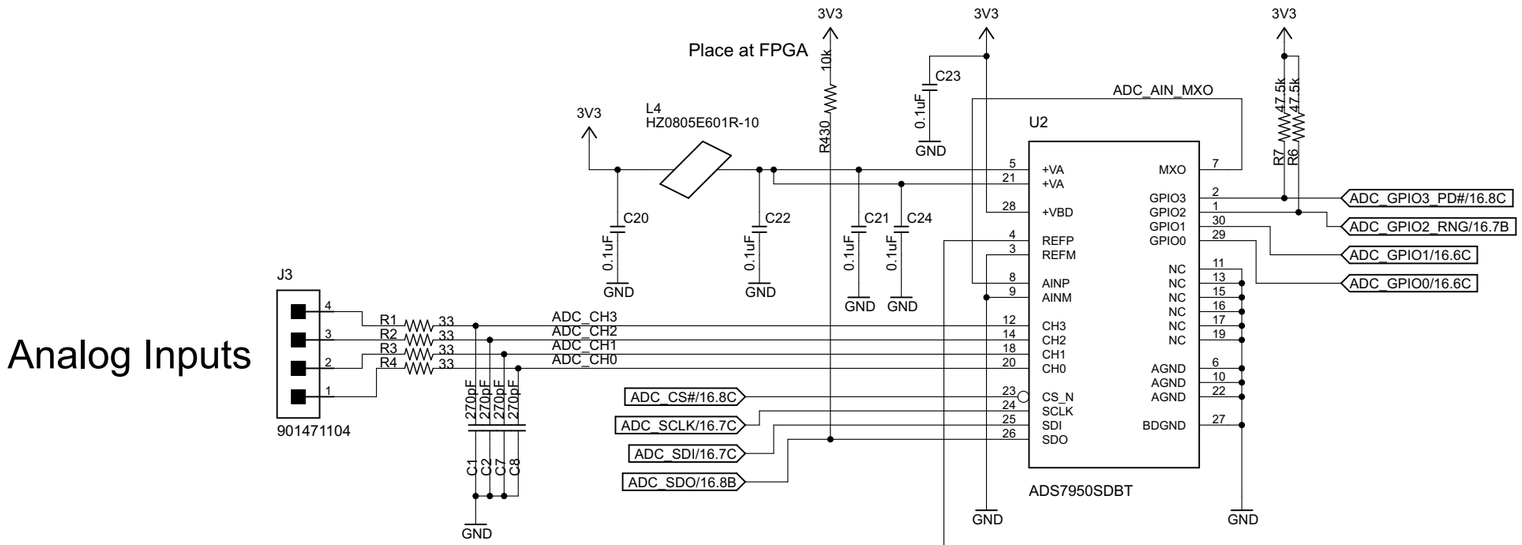
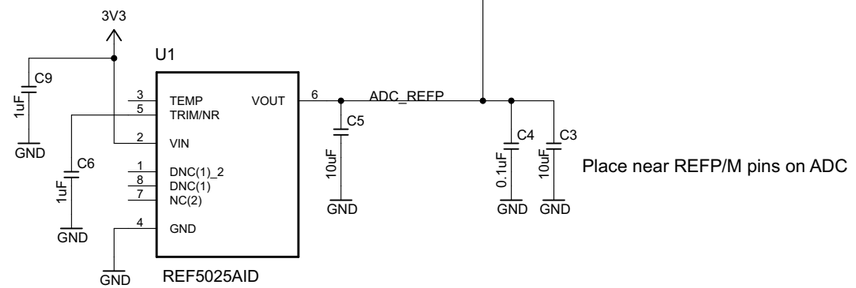
# A/D Converter (ADC)




# 2.5V Reference




# ADC

| | | |
|---|---|---|
| TITLE: iot_shield | | |
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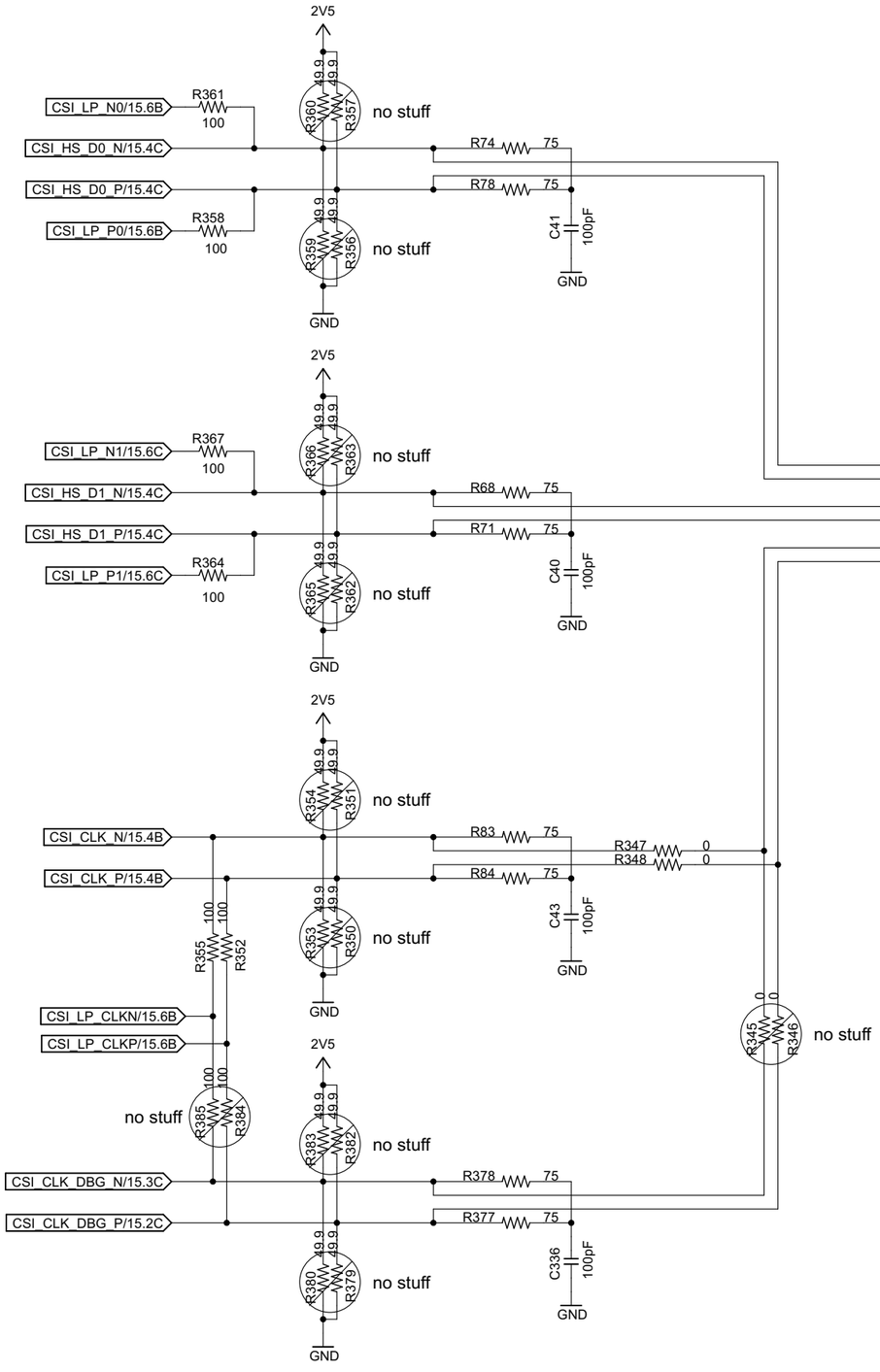
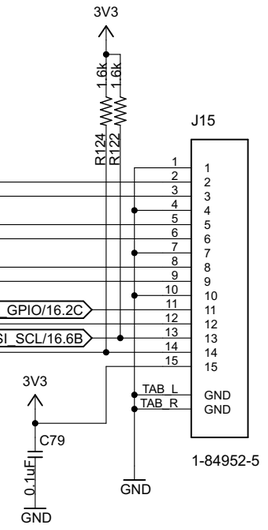
# MIPI CSI-2 Connector




# MIPI

| | |
|---|---|
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| Drawn By: Matt Staniszewski | REV: 1.1 |
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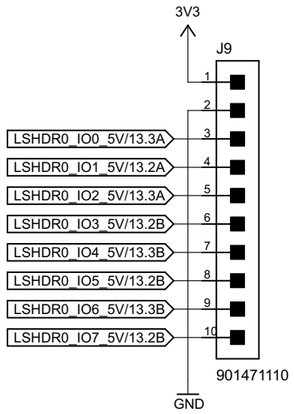
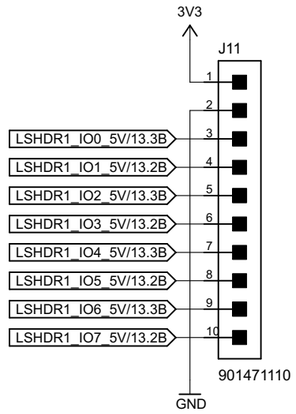
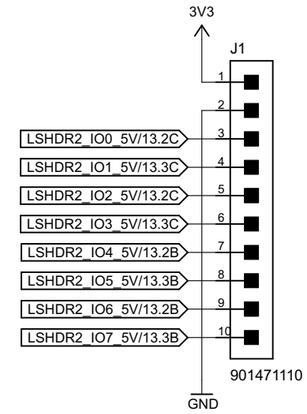
# Low-Speed IO Header 0




# Low-Speed IO Header 1

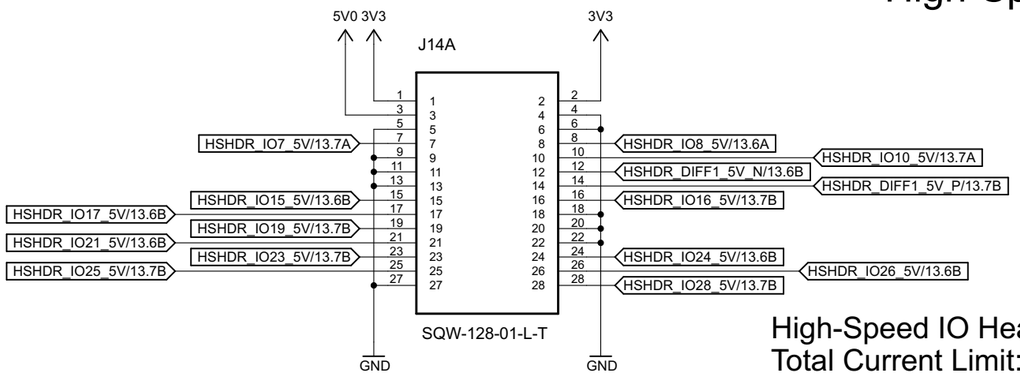


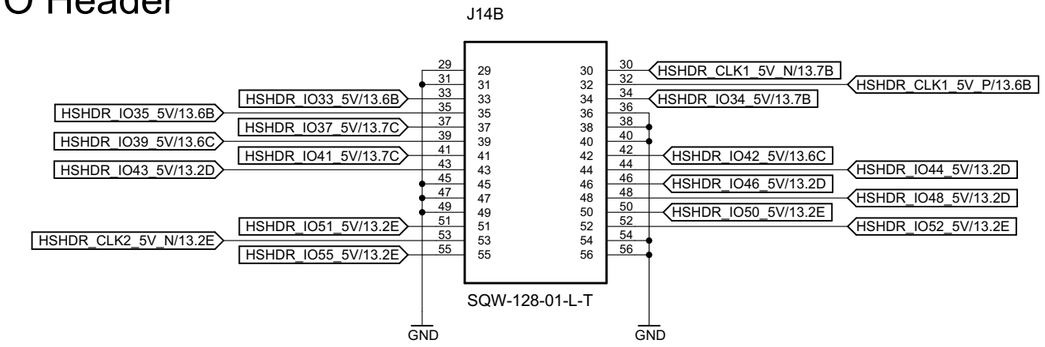

# Low-Speed IO Header 2



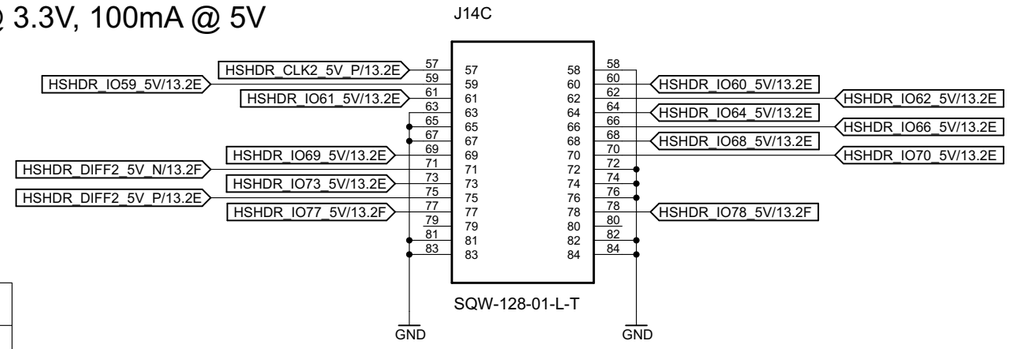

Low-Speed IO Header 0-2
Total Current Limit: 60mA @ 3.3V

# High-Speed IO Header



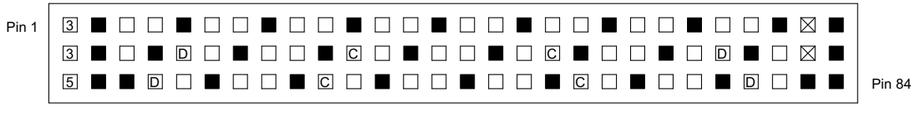

High-Speed IO Header
Total Current Limit: 40mA @ 3.3V, 100mA @ 5V




## Low-Speed IO Header Pinout


Note: Use 5V Header (J8, p. 17) for 5V power

## High-Speed IO Header Pinout




Note: Clock Pins 30 and 32 are FPGA input; Clock Pins 53 and 57 are FPGA output
Note: All differential and clock pairs are 2.5V

## Key

- ☐ Digital IO
- ■ Ground
- 3 3.3V
- 5 5V
- D Differential Pair (+/-)
- C Clock Pair (+/-)
- ☒ No Connect

# IO HEADERS

| | |
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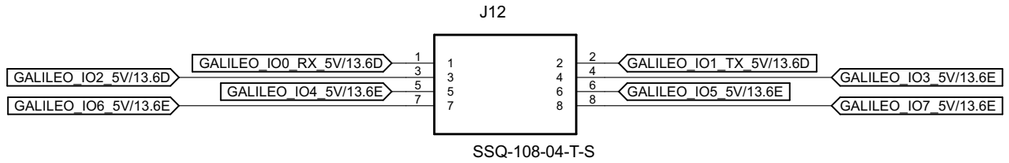
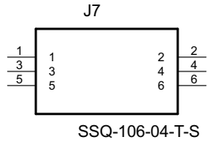
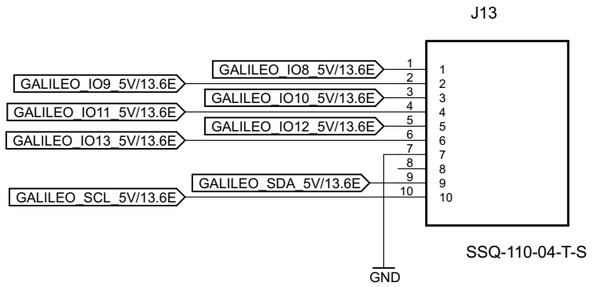
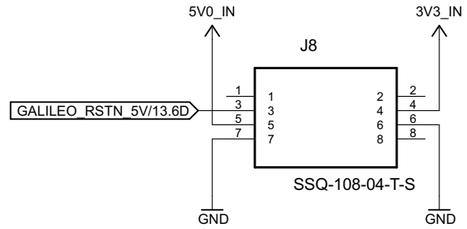
Note: Pin numbers match Galileo schematics



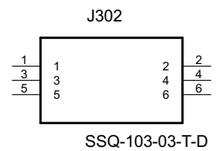




Analog input pins not connected to shield

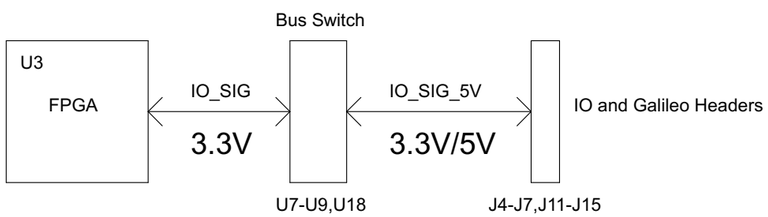



ICSP pins not connected to shield



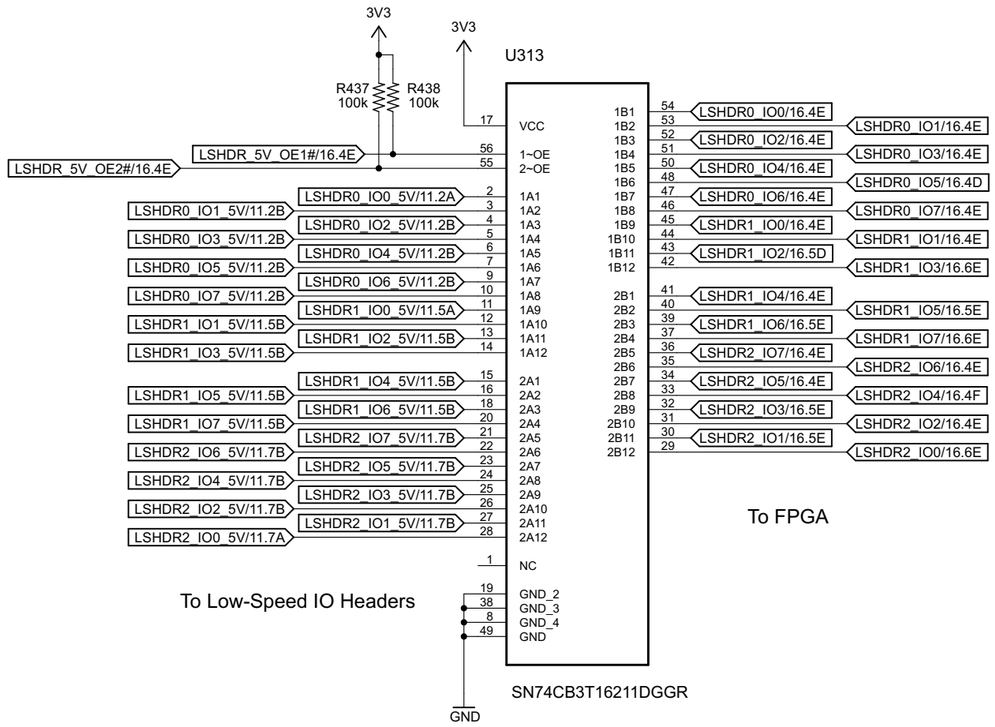

## IO Signal Flow

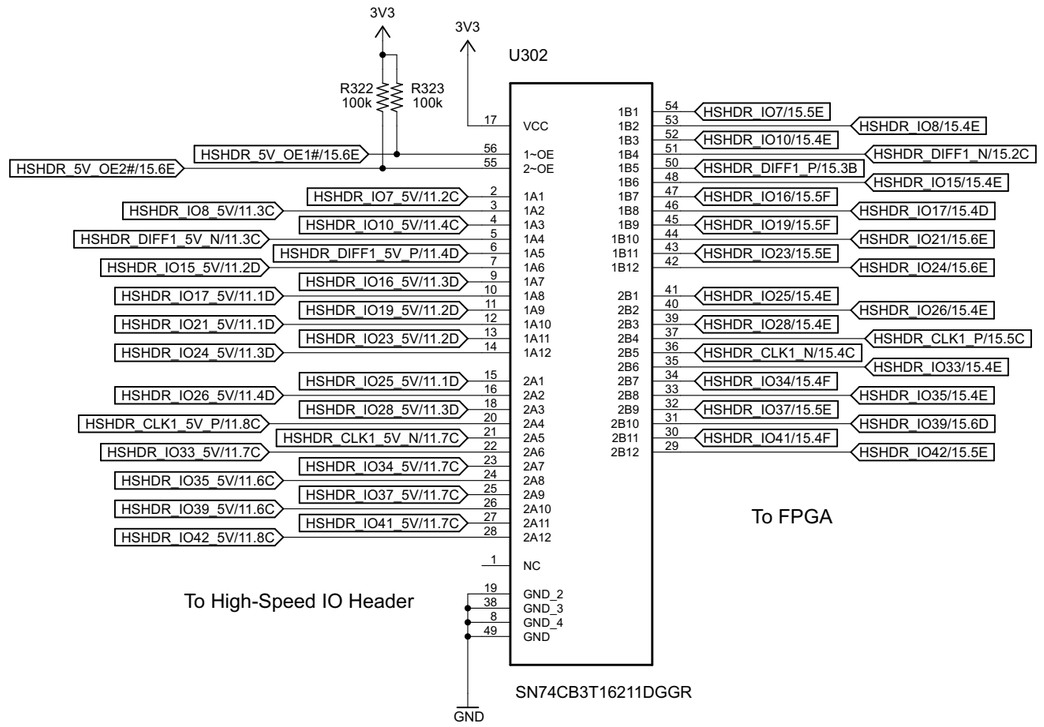


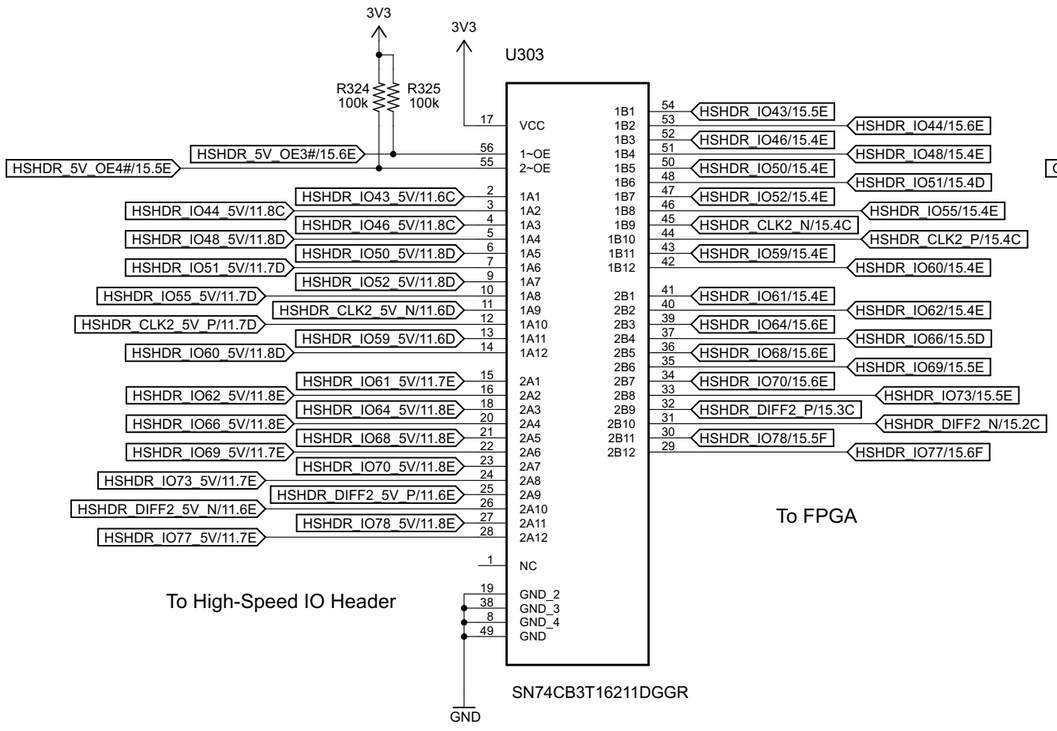

Note: '_5V' are Galileo/IO header signals and are 5V-tolerant.
Signals without '_5V' are 3.3V FPGA IOs (not 5V tolerant).

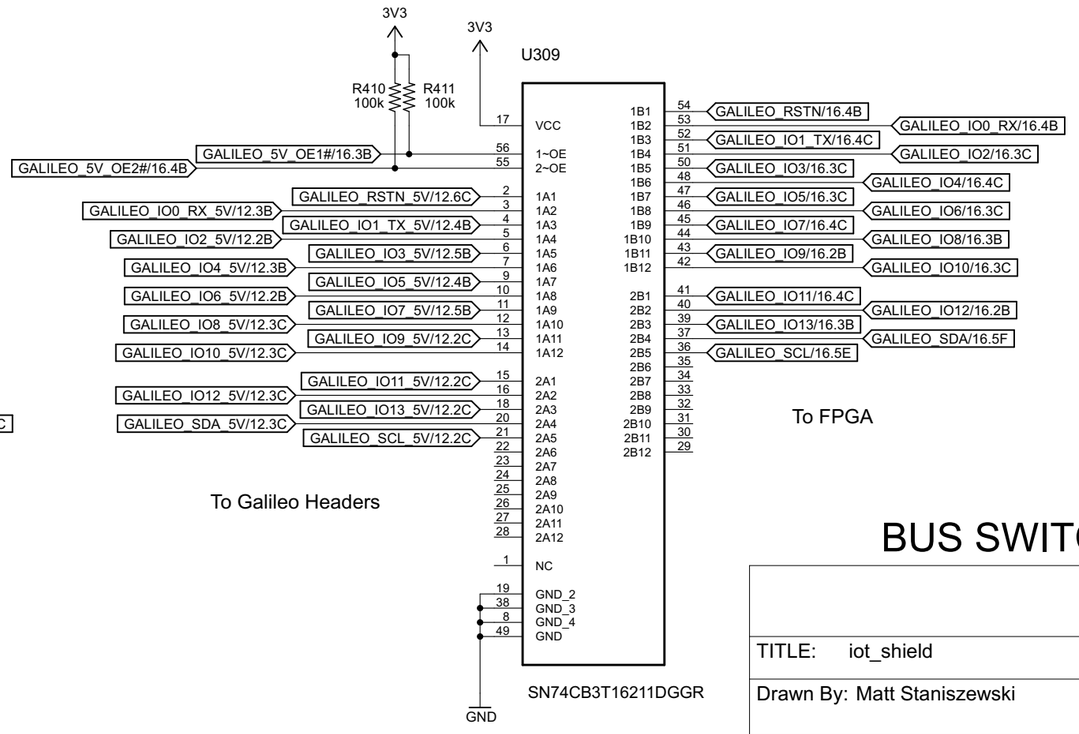
# GALILEO HEADERS

| | | |
|---|---|---|
| TITLE: iot_shield | | |
| Drawn By: Matt Staniszewski | | REV: 1.1 |
| Date: 10/14/2014 9:46:30 AM | Sheet: 12/22 | |



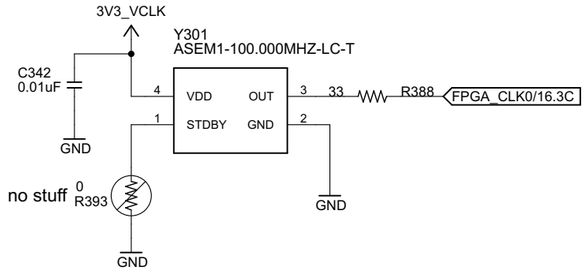



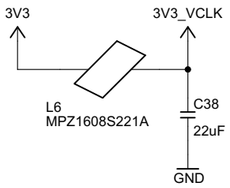

# BUS SWITCHES

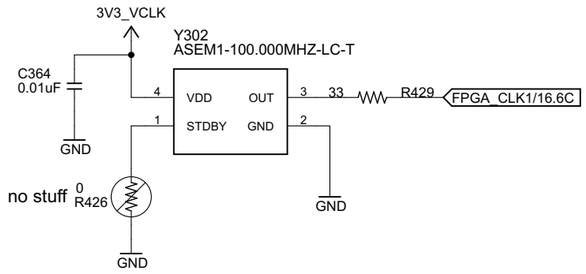
| | | |
|---|---|---|
| TITLE: iot_shield | | |
| Drawn By: Matt Staniszewski | | REV: 1.1 |
| Date: 10/14/2014 9:46:30 AM | Sheet: 13/22 | |

100MHz CMOS Oscillator

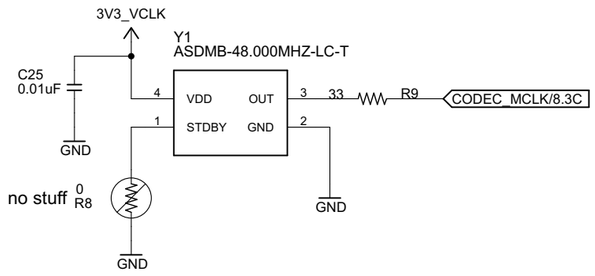



100MHz CMOS Oscillator




48MHz CMOS Oscillator

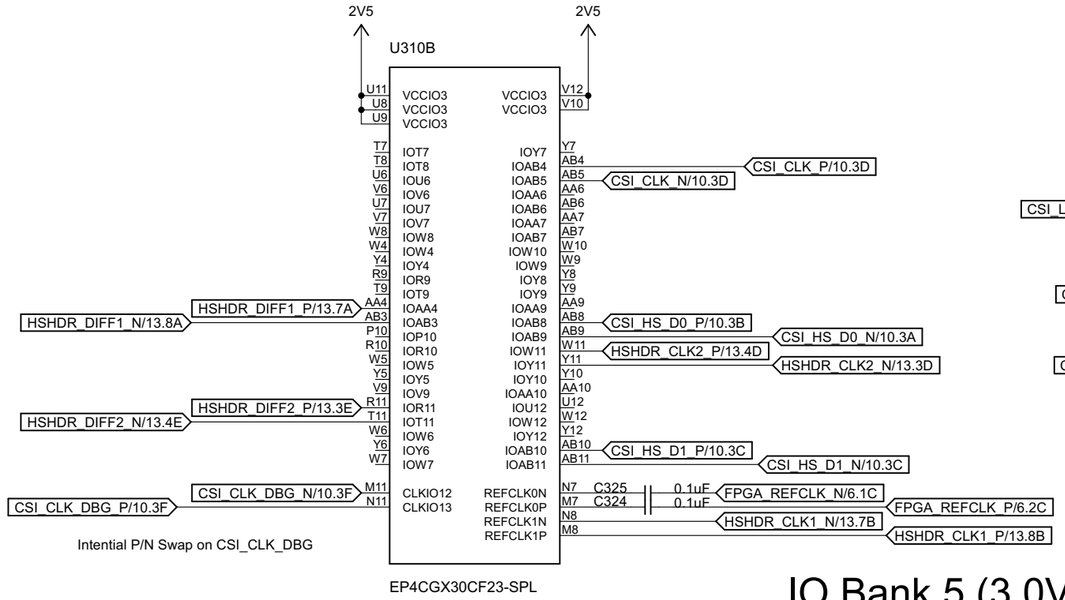



# CLOCKS

| | |
|---|---|
| TITLE: iot_shield | |
| Drawn By: Matt Staniszewski | REV: 1.1 |
| Date: 10/14/2014 9:46:30 AM | Sheet: 14/22 |

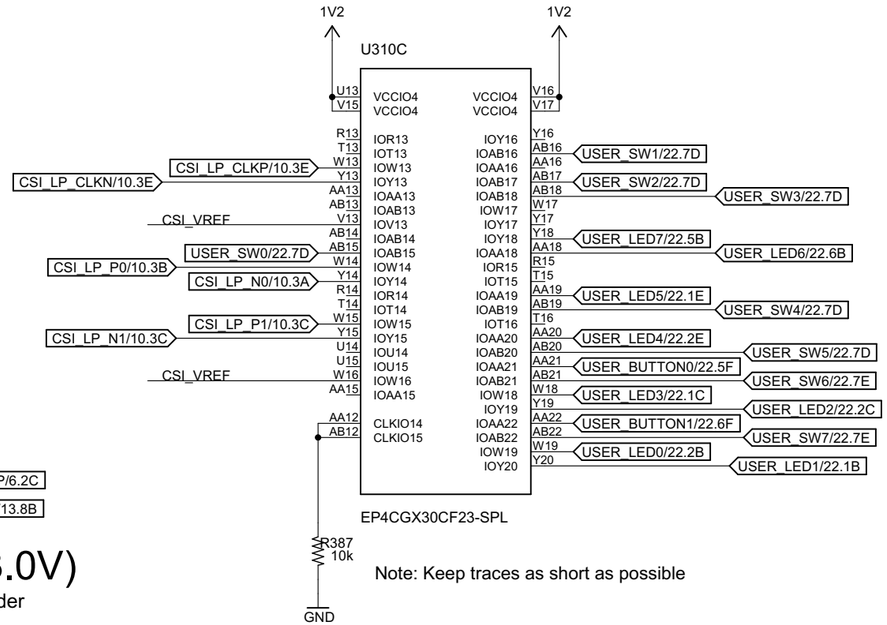
# IO Bank 3 (2.5V)

MIPI/Clock/High-Speed IO Header




# IO Bank 4 (1.2V)

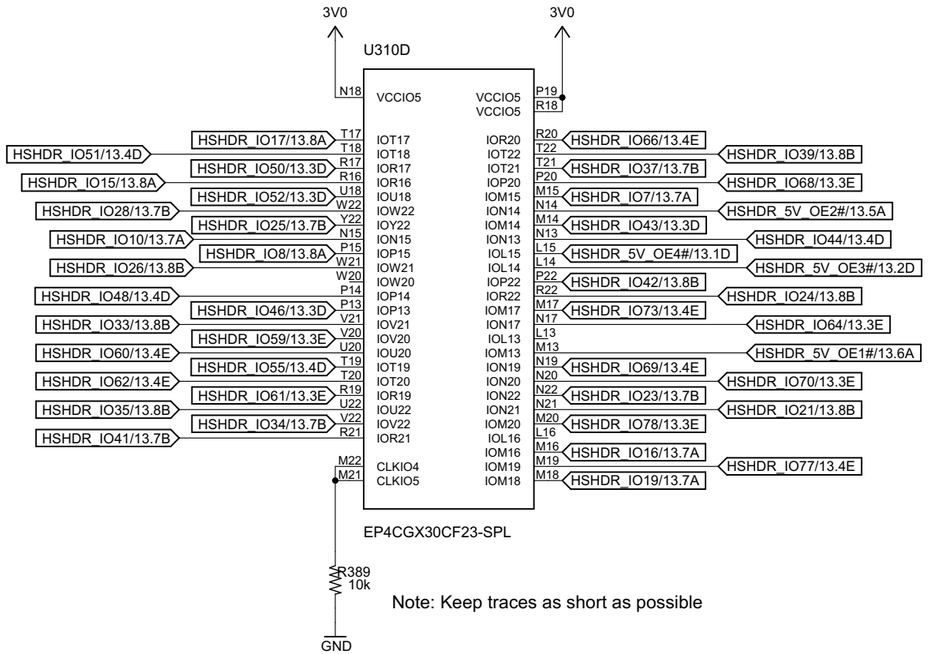
MIPI/LEDs/Buttons/Switches




Note: Keep traces as short as possible

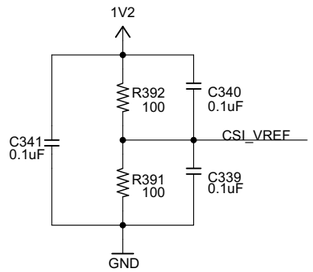
# IO Bank 5 (3.0V)

High-Speed IO Header




Note: 3.0V IO Banks are compatible with 3.3V signaling

Note: Keep traces as short as possible

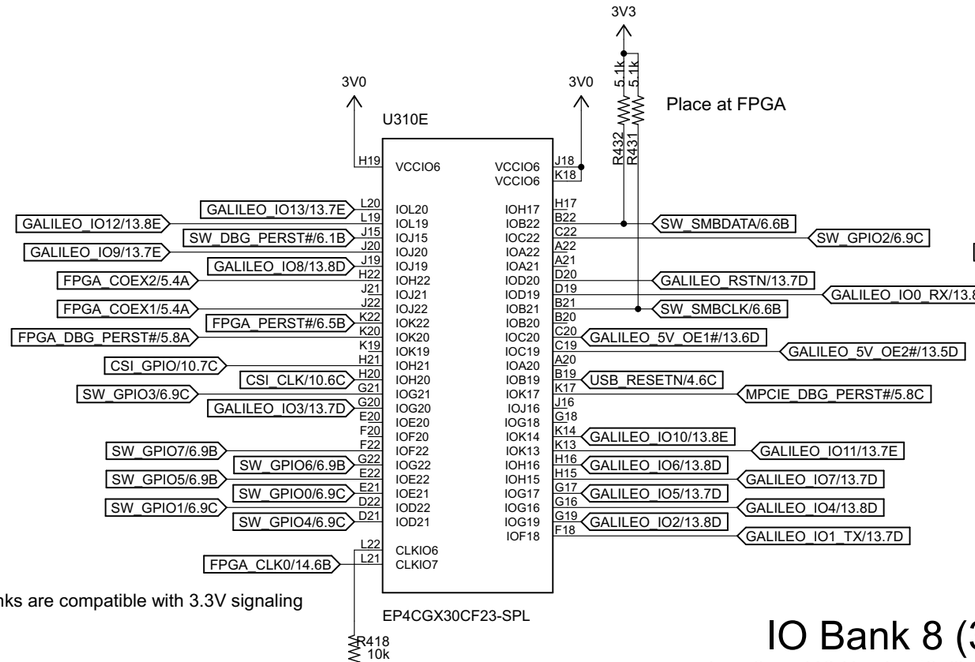



# FPGA IO BANK 3 / 4 / 5

| | | |
|---|---|---|
| TITLE: iot_shield | | |
| Drawn By: Matt Staniszewski | | REV: 1.1 |
| Date: 10/14/2014 9:46:30 AM | Sheet: 15/22 | |

# IO Bank 6 (3.0V)

PCIe/Switch/Galileo IOs/Clock

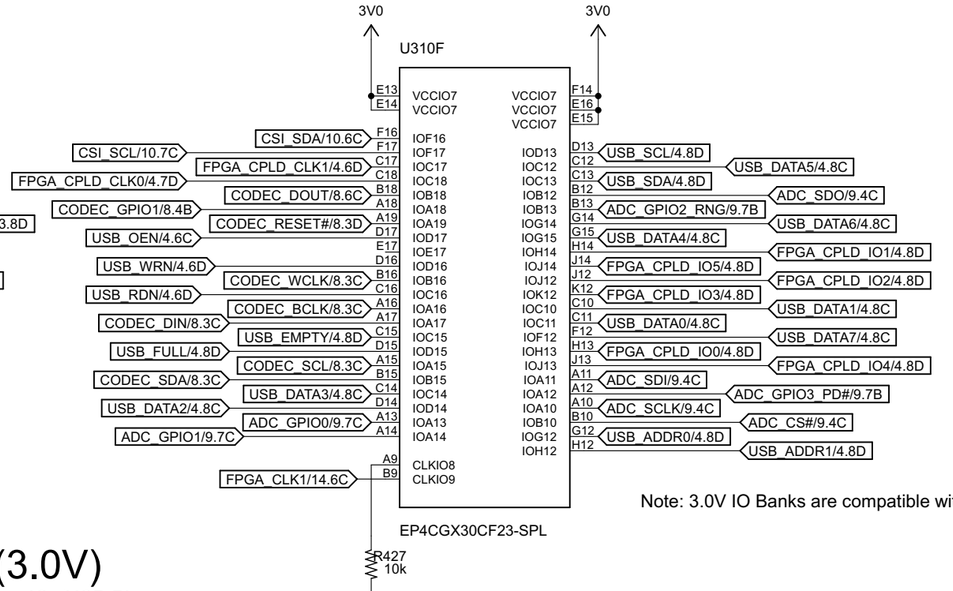



Note: 3.0V IO Banks are compatible with 3.3V signaling

Note: Keep traces as short as possible

# IO Bank 7 (3.0V)

Codec/ADC/Clock/USB Blaster

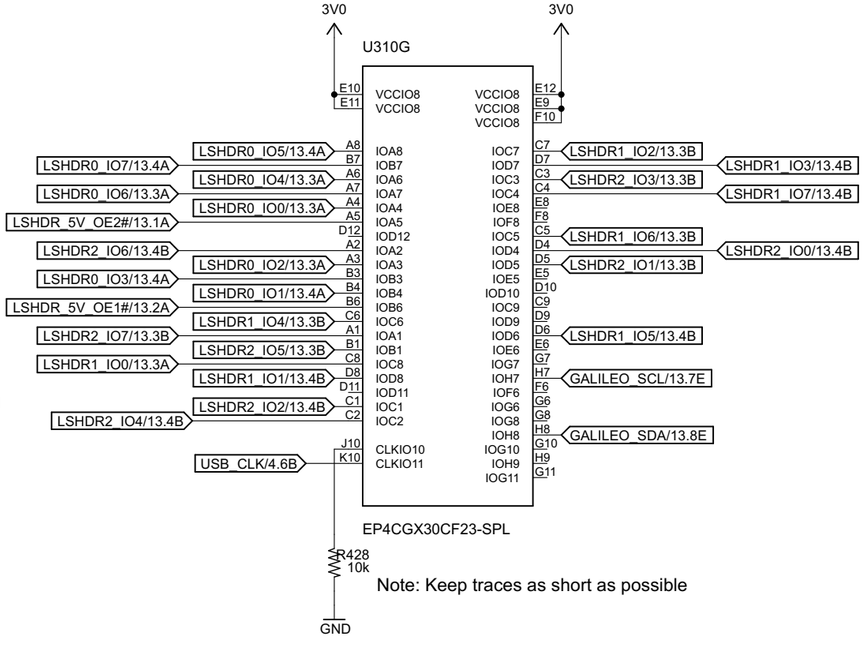



Note: 3.0V IO Banks are compatible with 3.3V signaling

Note: Keep traces as short as possible

# IO Bank 8 (3.0V)

Low-Speed IO Headers/Galileo IOs/USB Blaster



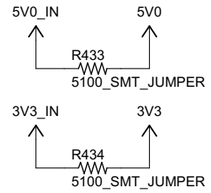

Note: 3.0V IO Banks are compatible with 3.3V signaling

Note: Keep traces as short as possible

# FPGA IO BANK 6 / 7 / 8

| | |
|---|---|
| TITLE: iot_shield | |
| Drawn By: Matt Staniszewski | REV: 1.1 |
| Date: 10/14/2014 9:46:30 AM | Sheet: 16/22 |

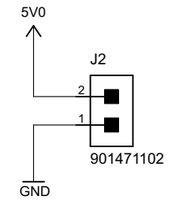
# POWER IN JUMPERS




Metal jumpers; Place at least 75mil apart

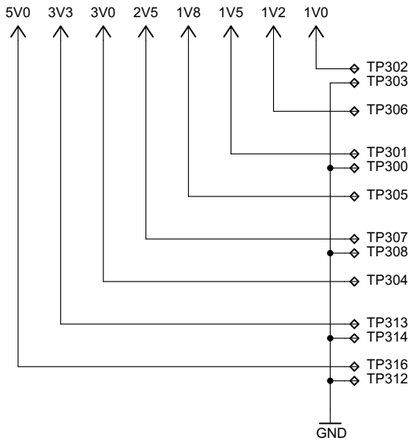
# 5V HEADER

Use 5V Header (J8) to supply 5V power to devices



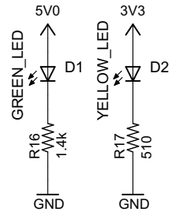

5V Header Total Current Limit: 100mA @ 5V

# POWER PROBE TESTPOINTS

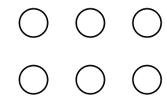



Place ground testpoint next to each rail testpoint
(except where a common ground pad can be shared)

# POWER LEDs




BOARD FIDUCIALS



Note: Shield power limits assume all header current limits are used and a Mini-PCIe Gen1 card (i.e. Wi-Fi) is connected.

It is assumed that additional shields or USB devices are not connected to the Galileo; please use at your own risk.

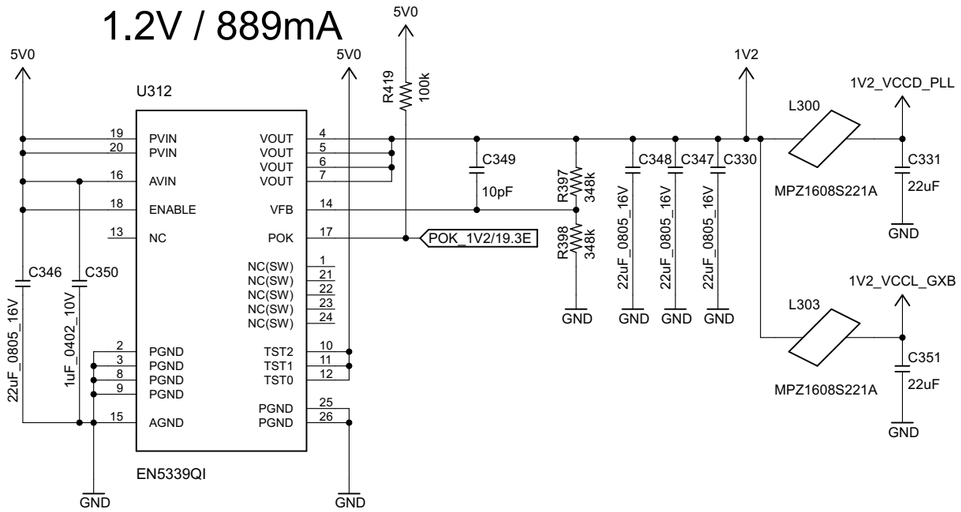
For larger FPGAs (GX50 and above), input power must be supplied externally. Remove R4 and R5 and power the 5V0 and 3V3 voltage rails from a separate source.

# POWER IN

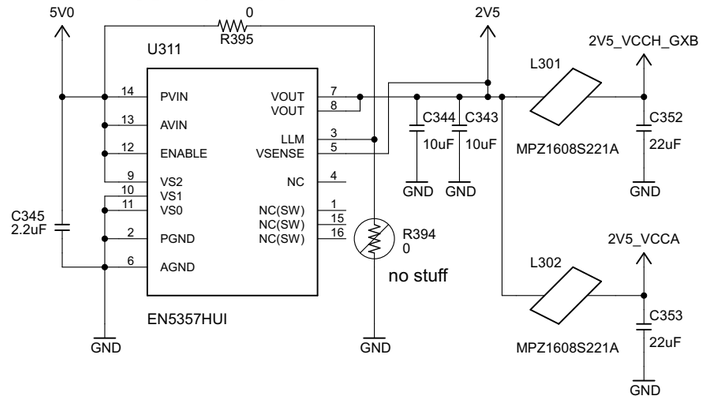
| | | |
|---|---|---|
| TITLE: iot_shield | | |
| Drawn By: Matt Staniszewski | | REV: 1.1 |
| Date: 10/14/2014 9:46:30 AM | Sheet: 17/22 | |

## 1.2V / 889mA

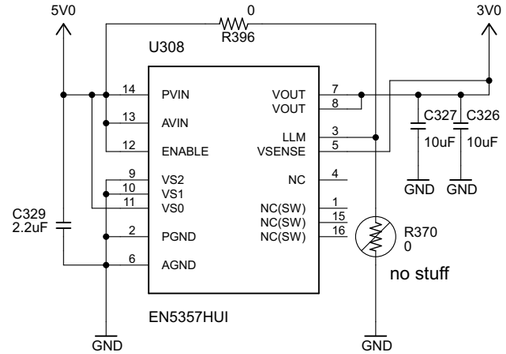
Place C21 as close to AVIN as possible



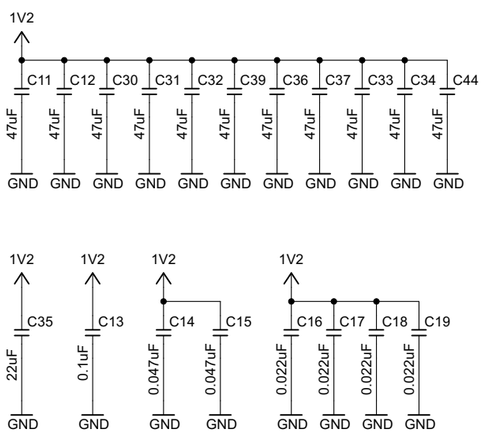

## 2.5V / 133mA




## 3.0V / 7mA



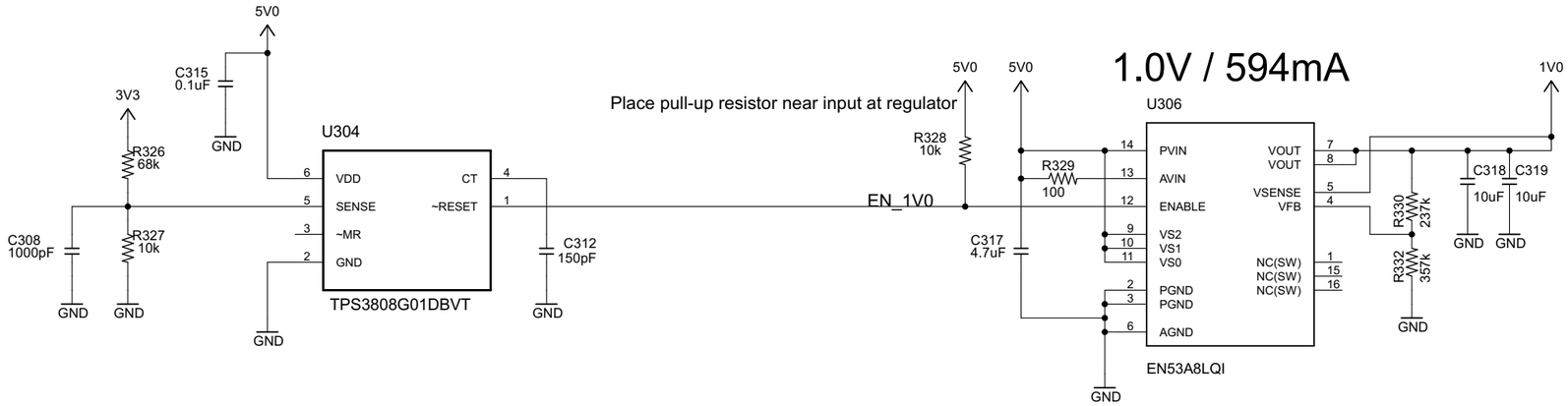

## FPGA Decoupling

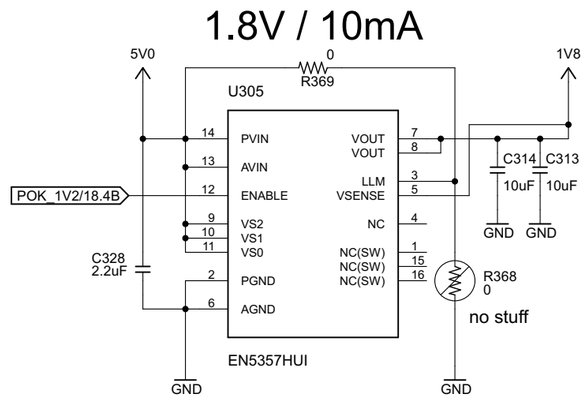



# FPGA VREGS / DECOUPLING

| | |
|---|---|
| TITLE: iot_shield | |
| Drawn By: Matt Staniszewski | REV: 1.1 |
| Date: 10/14/2014 9:46:30 AM | Sheet: 18/22 |

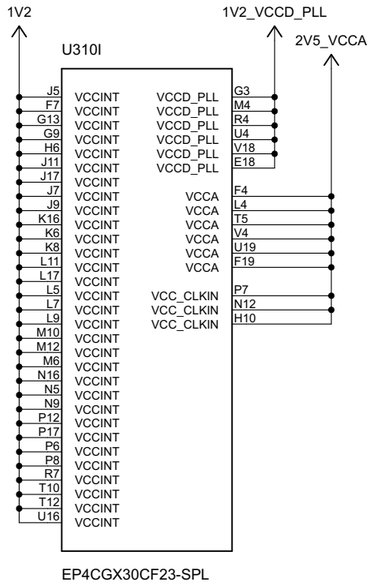
# Supervisor (1.0V POK)

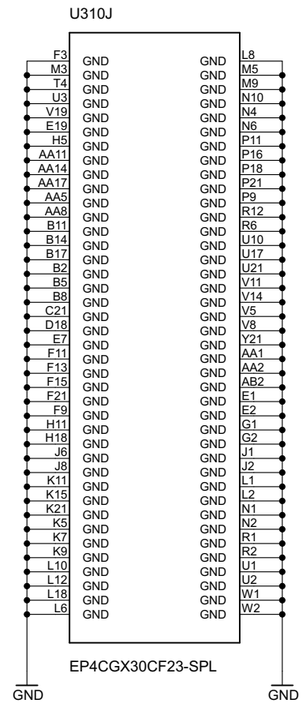



# SYSTEM VREGS

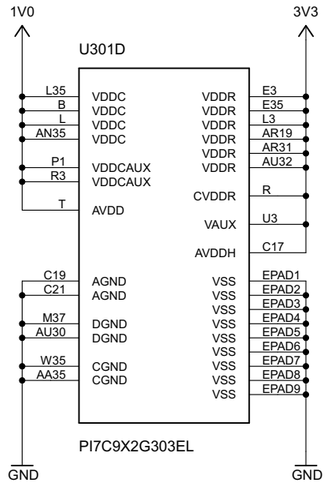
| | |
|---|---|
| TITLE: iot_shield | |
| Drawn By: Matt Staniszewski | REV: 1.1 |
| Date: 10/14/2014 9:46:30 AM | Sheet: 19/22 |

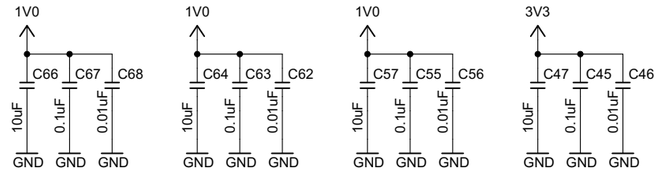


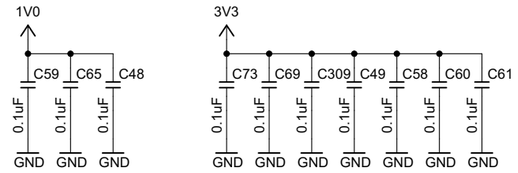

# FPGA PWR / GND

| | |
|---|---|
| TITLE: iot_shield | |
| Drawn By: Matt Staniszewski | REV: 1.1 |
| Date: 10/14/2014 9:46:30 AM | Sheet: 20/22 |




Place groupings at each power pad (T, B, L, R)

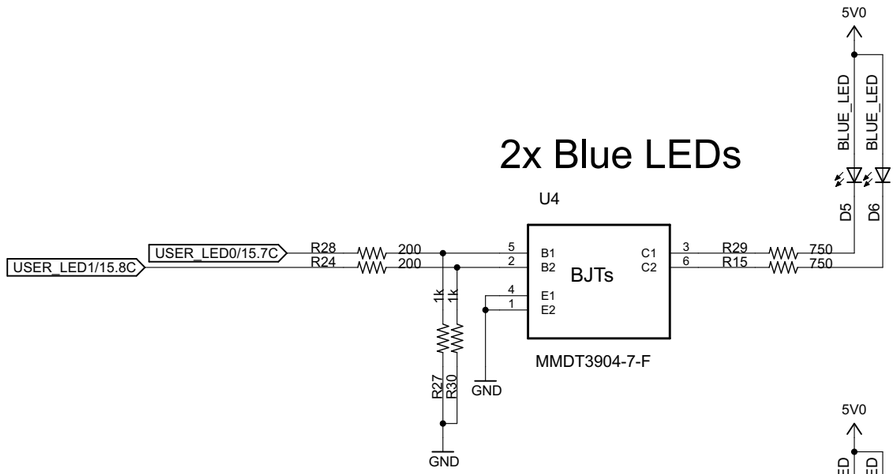



Place common capacitor between near pads with same voltage

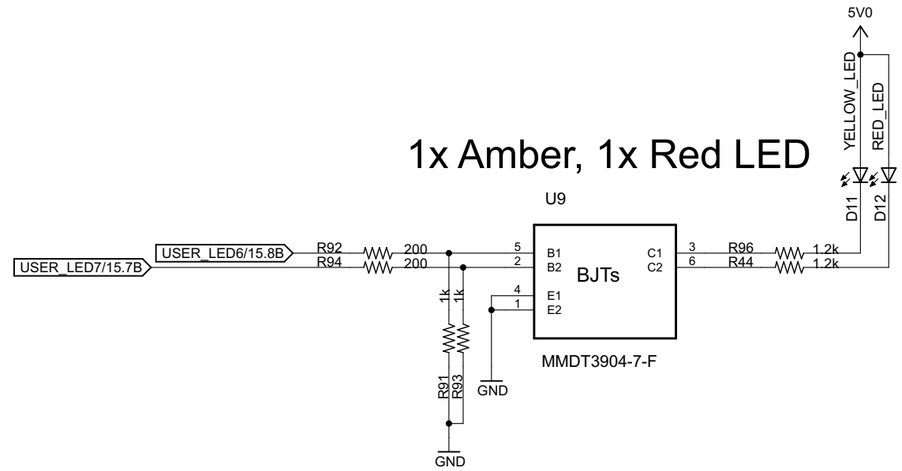
# SW PWR / GND / DECOUPLING

| | |
|---|---|
| TITLE: iot_shield | |
| Drawn By: Matt Staniszewski | REV: 1.1 |
| Date: 10/14/2014 9:46:30 AM | Sheet: 21/22 |

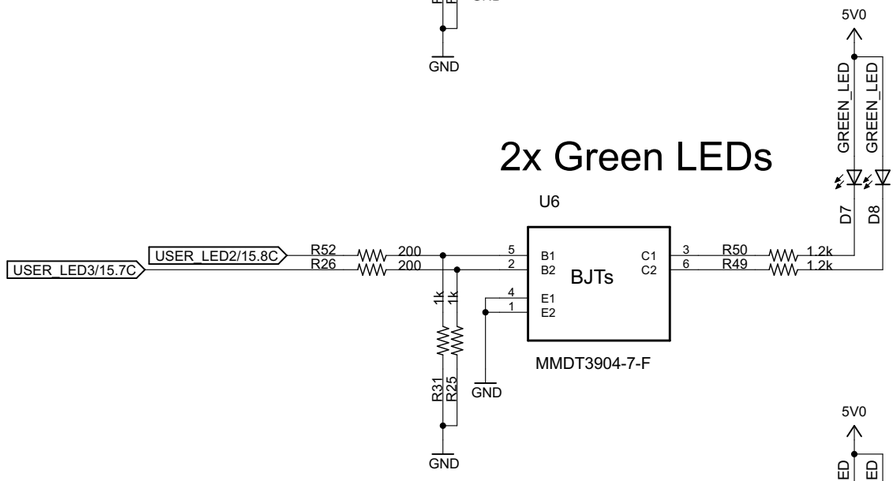
## 2x Blue LEDs



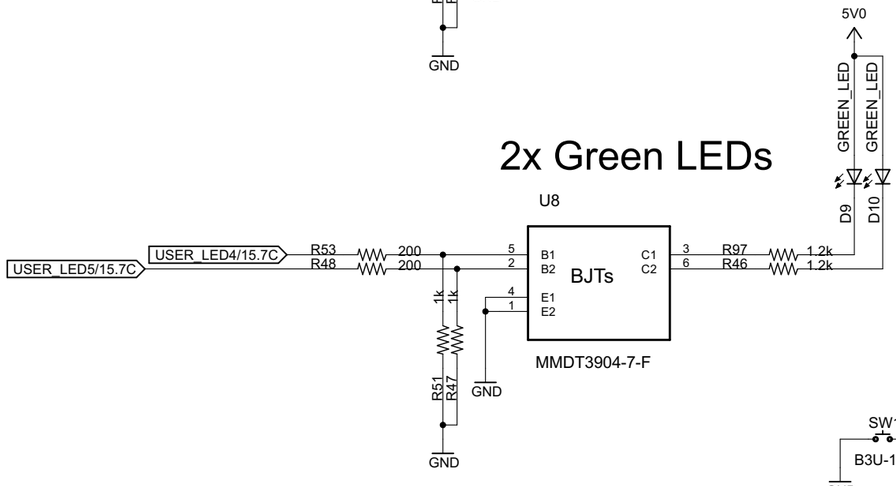

## 1x Amber, 1x Red LED



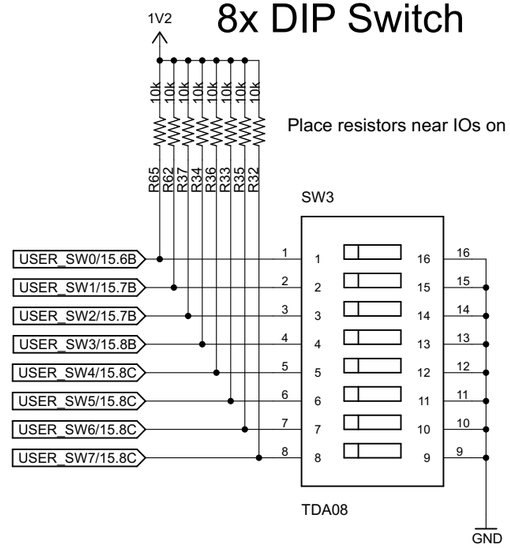

## 2x Green LEDs



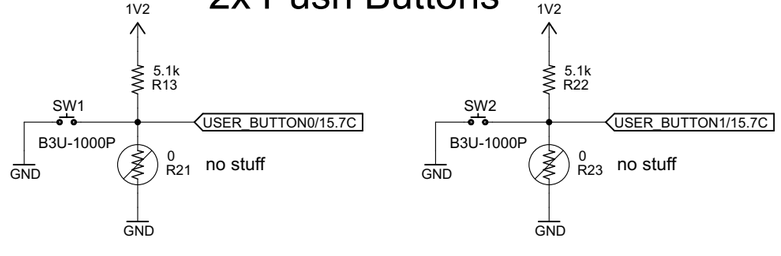

## 2x Green LEDs




## 8x DIP Switch




## 2x Push Buttons




# LEDS / BUTTONS / SWITCHES

| | | |
|---|---|---|
| TITLE: iot_shield | | |
| Drawn By: Matt Staniszewski | | REV: 1.1 |
| Date: 10/14/2014 9:46:30 AM | Sheet: 22/22 | |