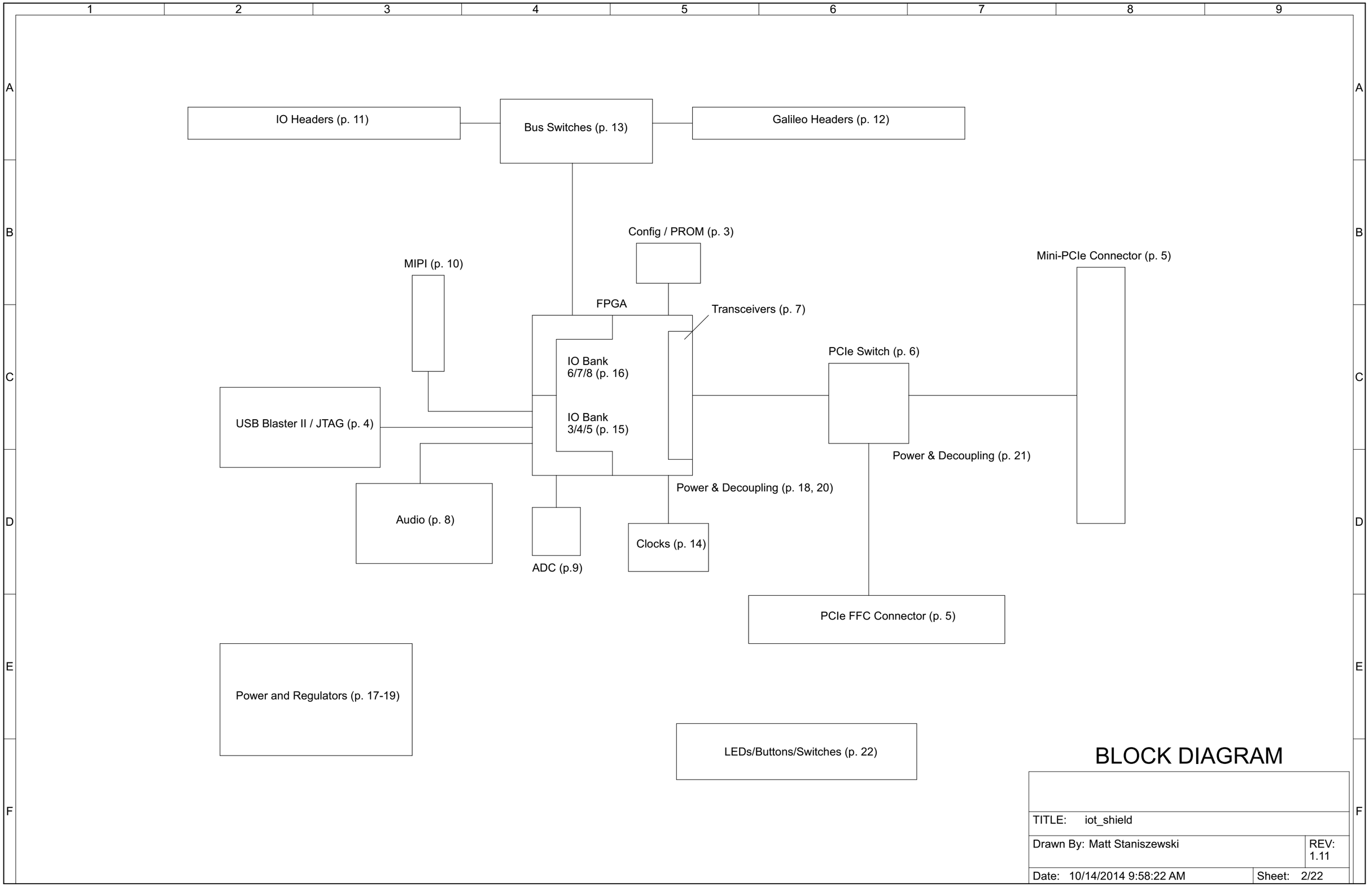
TABLE OF CONTENTS

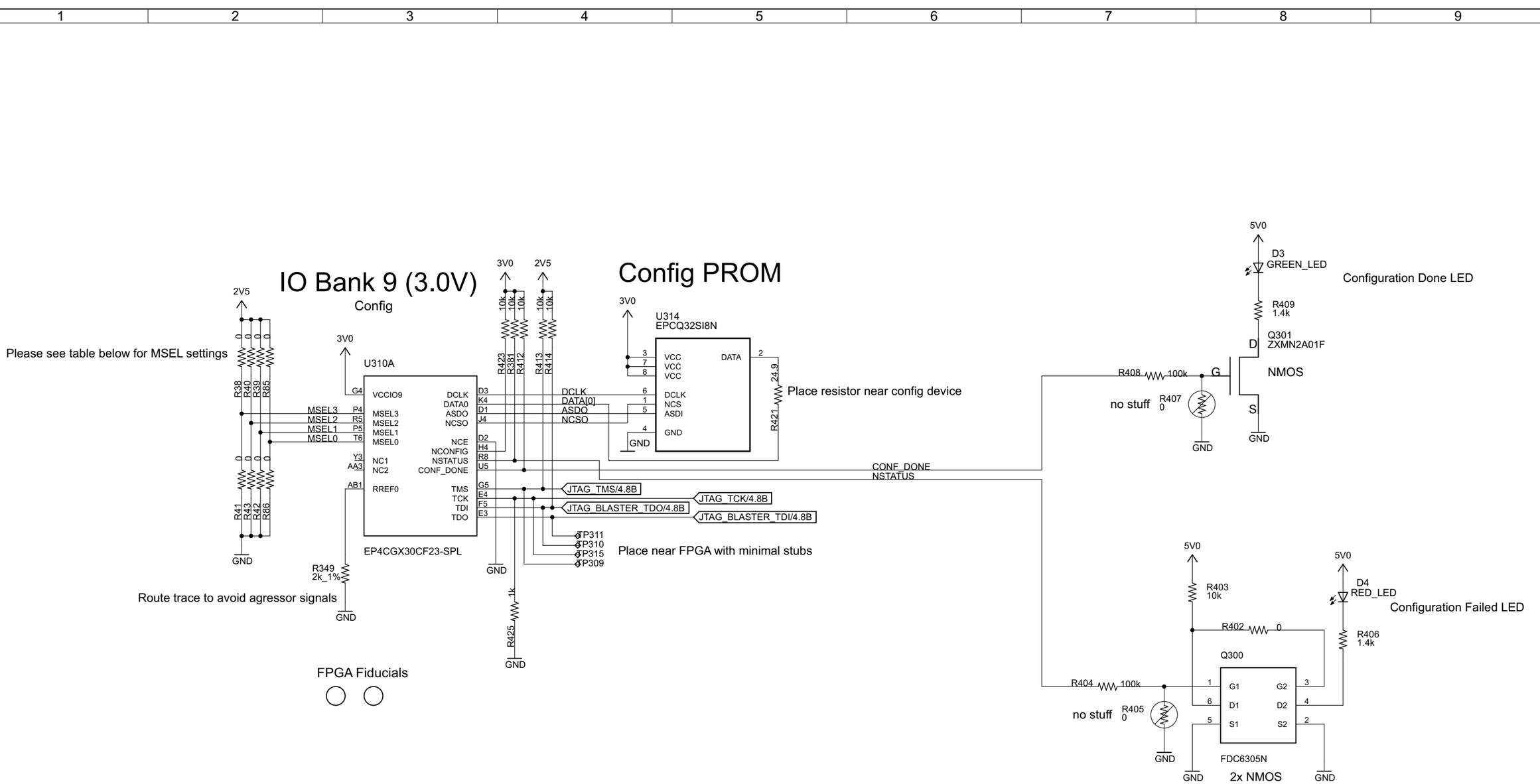
REV 1.11 10/14/2014 9:58:22 AM

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 1/22	



BLOCK DIAGRAM

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 2/22	



MSEL Settings

Function	MSEL3		MSEL2		MSEL1		MSEL0	
Resistor	R166	R164	R167	R165	R170	R168	R171	R169
stuff	X			X	X		X	
no stuff		X	X			X		X

Current configuration: AS x1 Mode, Fast POR

FPGA CONFIG / JTAG

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 3/22

Micro USB

J16
10118194-0001LF

Route high-speed USB signals carefully

VBUS_5V
FX2_D_N
FX2_D_P
R130 0
no stuff
SH1 SH2 SH3 SH4 SH5 SH6
CH_GND

R303 1M
CH_GND C300 4700pF GND

U11
ESD
TPD2EUSB30DR
GND
10k R131

Y300 24MHz
Crystal
C303 12pF
C302 12pF
3V3 C301 0.1uF GND

Place on USB peninsula for J20

JTAG Header

J301
C_USB_MAX_TCK
C_USB_MAX_TDO
C_USB_MAX_TMS
C_USB_MAX_TDI
1k R335
CLP-107-02-F-D-K

FX2_SDA R123 0 MAX_SDA

MAX811SEUS+T
R98 100k FX2_RESETN
GND MR# RESET# VCC
C54 0.1uF
Voltage Monitor U10

USB Controller

U300
2k R126 2k R125
20k R305 C316 0.1uF

FX2_RESETN
FX2_WAKEUP
24M_XTALIN
24M_XTALOUT
FX2_SLRDN
FX2_SLWRN
USB_CLK R304 0
FX2_SCL
FX2_SDA
R371 1k R372 1k

RESET
WAKEUP
XTALIN
XTALOUT
CLKOUT/T1OUT
RDY0/SLRD
RDY1/SLRW
IFCLK/T0OUT
RESEVED
SCL
SDA
DPLUS
DMINUS
AVCC
AVCC
AGND
AGND

PB0/FD0 FX2_PB0
PB1/FD1 FX2_PB1
PB2/FD2 FX2_PB2
PB3/FD3 FX2_PB3
PB4/FD4 FX2_PB4
PB5/FD5 FX2_PB5
PB6/FD6 FX2_PB6
PB7/FD7 FX2_PB7
PD0/FD8 FX2_PD0
PD1/FD9 FX2_PD1
PD2/FD10 FX2_PD2
PD3/FD11 FX2_PD3
PD4/FD12 FX2_PD4
PD5/FD13 FX2_PD5
PD6/FD14 FX2_PD6
PD7/FD15 FX2_PD7
PA0/INT0
PA1/INT1 FX2_PA1
PA2/SLOE FX2_PA2
PA3/WU2 FX2_PA3
PA4/FIFOADR0 FX2_PA4
PA5/FIFOADR1 FX2_PA5
PA6/PKTEND FX2_PA6
PA7/FLAGD/SLCS FX2_PA7
CTL0/FLAGA FX2_FLAGA
CTL1/FLAGB FX2_FLAGB
CTL2/FLAGC FX2_FLAGC

CY7C68013A-56PVXC

C74 C75 C76 C78 C53 C52 C51 C77 0.1uF
Place near CY7C68013A

CPLD

U5A
CPLD Fiducials
R45 1k

FX2_PB5 FX2_PB4 FX2_PB3 FX2_FLAGA FX2_PB7 FX2_PB6 FX2_PB2
FX2_FLAGB FX2_FLAGC FX2_SCL FX2_PB1 FX2_PA1 FX2_PA2 USB_DISABLEN
USB_CLK/16.4F FX2_PB0 MAX_SDA FX2_RESETN

IOB1_1 … IOB1_32

FX2_PA5 FX2_PA4 FX2_PA3 FX2_SLRDN FX2_SLWRN FX2_PA7 FX2_PA6
JTAG_TCK/3.5C
FX2_PD6 FX2_PD7 FX2_PD4 FX2_PD5
JTAG_BLASTER_TDO/3.4C
JTAG_BLASTER_TDI/3.5C
JTAG_TMS/3.4C
C_USB_MAX_TMS R129 0 FX2_PD1
C_USB_MAX_TDI R128 0 FX2_PD2
C_USB_MAX_TCK R95 0 FX2_PD0
C_USB_MAX_TDO R127 0 FX2_PD3

TMS TDI TCK TDO
EPM570GT100

U5B
R376 1k R375 1k R374 1k R373 1k

JTAG_TX SC_RX SC_TX JTAG_RX
USB_RESETN/16.3C
USB_OEN/16.6B
USB_RDN/16.6C
USB_WRN/16.6B
R20 0 M570_PCIE_JTAG_EN
FPGA_CPLD_CLK1/16.6B
FPGA_CPLD_CLK0/16.6B

IOB2_1 … IOB2_38

USB_DATA0/16.7C
USB_DATA1/16.8C
USB_DATA2/16.6C
USB_DATA3/16.6C
USB_DATA4/16.7B
USB_DATA5/16.8B
USB_DATA6/16.8B
USB_DATA7/16.8C
USB_ADDR0/16.7C
USB_ADDR1/16.8C
USB_FULL/16.6C
USB_EMPTY/16.6C
USB_SCL/16.7B
USB_SDA/16.7B
FPGA_CPLD_IO0/16.7C
FPGA_CPLD_IO1/16.8B
FPGA_CPLD_IO2/16.8B
FPGA_CPLD_IO3/16.7C
FPGA_CPLD_IO4/16.8C
FPGA_CPLD_IO5/16.7B

EPM570GT100

USB Blaster Status LEDs

U307
JTAG_RX R334 200
JTAG_TX R336 200
1k 1k
R333 R331
BJTs
MMDT3904-7-F
R302 1.2k
R308 1.2k
D14 GREEN_LED
D13 GREEN_LED

U7
SC_RX R338 200
SC_TX R311 200
1k 1k
R337 R309
BJTs
MMDT3904-7-F
R300 1.2k
R301 1.2k
D16 GREEN_LED
D15 GREEN_LED

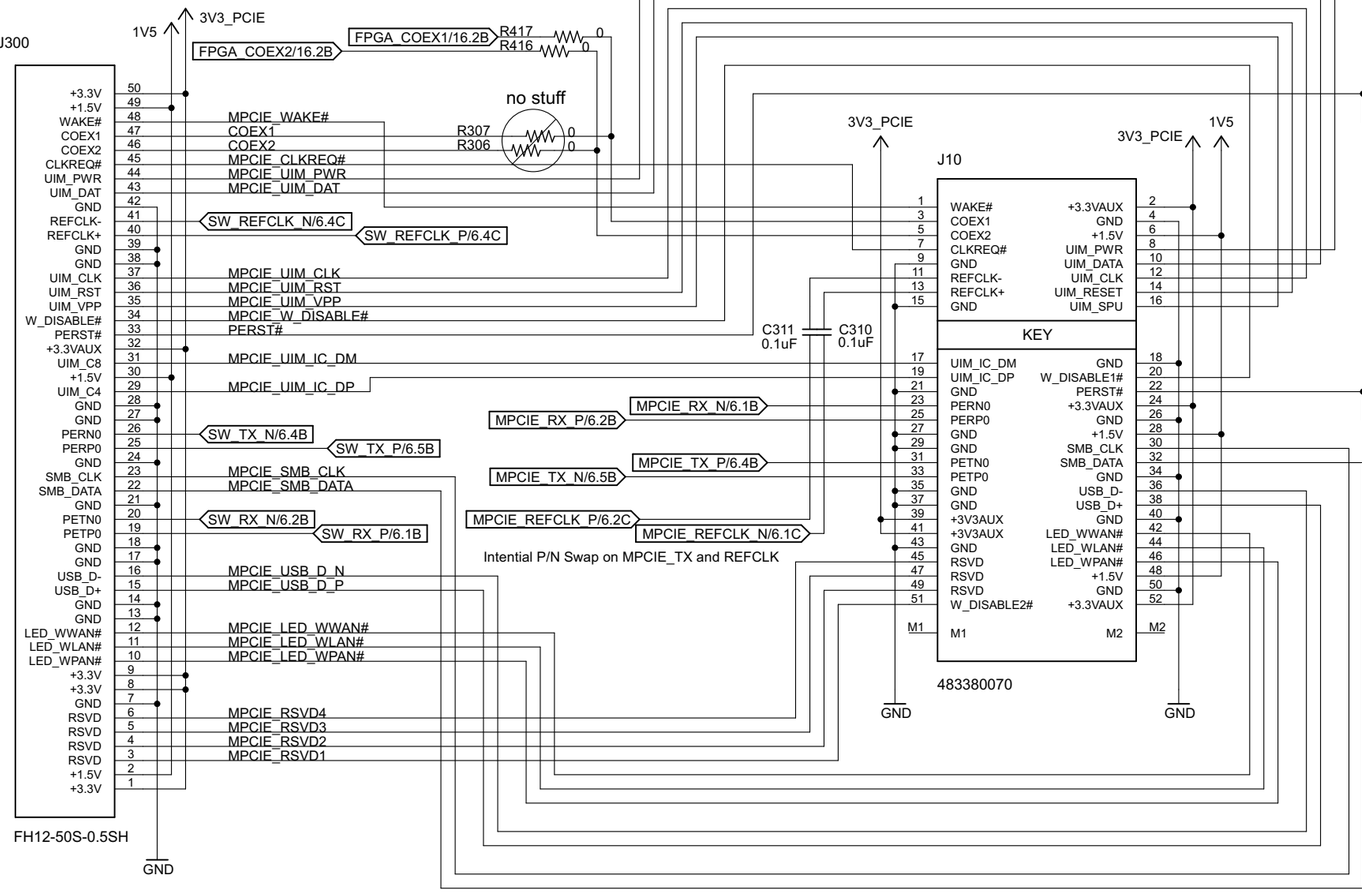
U5C
GNDINT VCCINT
GNDIO VCCIO1
GNDIO VCCIO2
EPM570GT100

C320 C334 0.1uF
C333 C332 C321 C335 0.1uF
Place near MAX II

USB BLASTER II

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 4/22

FFC Connector

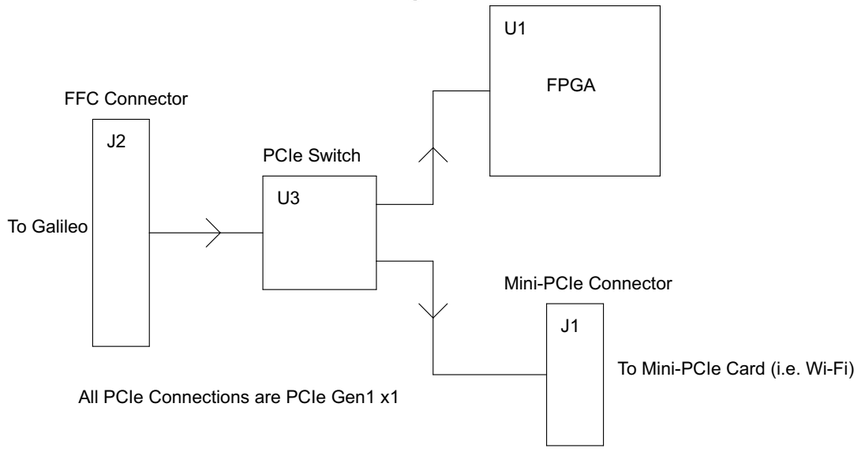


FFC Cable to Galileo

Mini-PCIe Connector

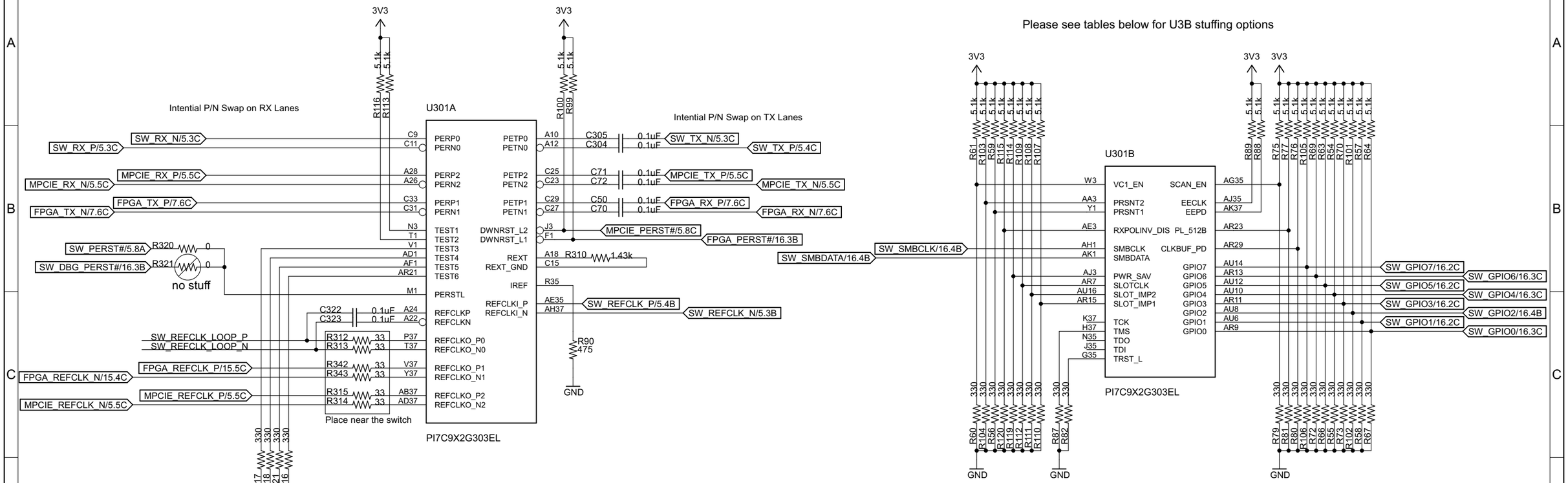
Note: J1 Supports speeds up to Gen1 (2.5Gbps)

PCIe Flow Diagram



PCIe CONNECTORS

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 5/22

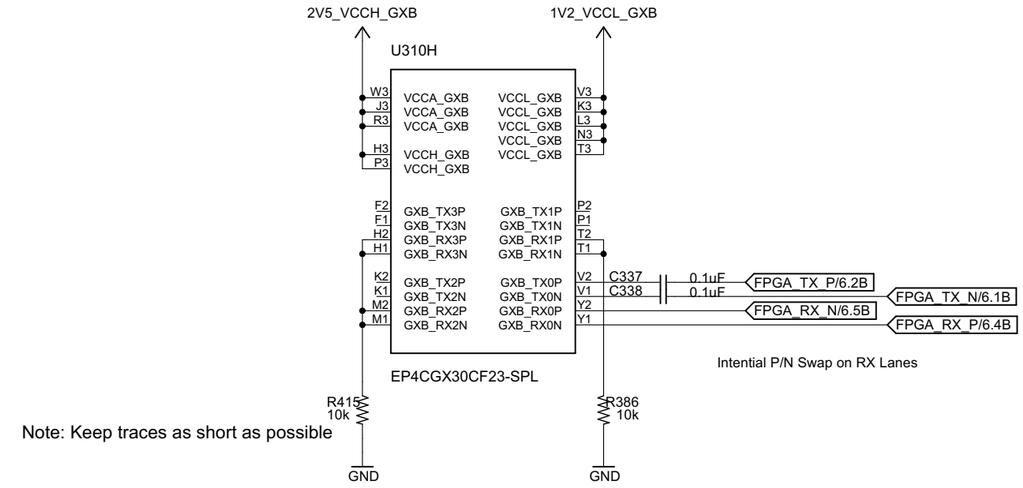


Function	VC1_EN		PRSNT2		PRSNT1		RXPOLINV_DIS		PWR_SAV		SLOTCLK		SLOT_IMP2		SLOT_IMP1	
Resistor	R47	R46	R53	R48	R54	R49	R55	R50	R56	R51	R57	R52	R58	R68	R66	R69
stuff		X		X		X		X	X		X		X		X	
no stuff	X		X		X		X			X		X		X		X

Function	SCAN_EN		PL_512B		CLKBUF_PD		GPIO7		GPIO6		GPIO5		GPIO4		GPIO3		GPIO2		GPIO1		GPIO0	
Resistor	R72	R73	R40	R39	R59	R41	R60	R42	R61	R43	R62	R44	R63	R45	R64	R65	R74	R77	R75	R78	R76	R79
stuff		X	X			X	X		X		X		X		X		X		X		X	
no stuff	X			X	X			X		X		X		X		X		X		X		X

PCIe SWITCH

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 6/22	



FPGA PCIe CONNECTIONS

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 7/22	

Codec

U3

TLV320AIC3100IRHBR

AVDD, IOVDD, DVDD, SPLVDD, SPRVDD, HPVDD, WCLK, BCLK, MCLK, SDA, SCL, GPIO1, DIN, ~RESET, VOL/MICDET, MIC1LP, MIC1LM, MIC1RP, EP, DVSS, SPLVSS, SPRVSS, IOVSS, AVSS, HPVSS, HPL, SPRM, HPR, SPLM, SPRP, DOUT, SPLP, MICBIAS

3V3 3V3

R10 2.7k, R11 2.7k, R5 10k

5V0 3V3 1V8

C360 0.1uF, C356 10uF, C26 0.1uF, C27 0.1uF, C358 100uF_1210_6.3V, C357 0.1uF, C359 0.1uF, C362 0.1uF, C361 10uF — GND

CODEC_GPIO1/16.6B

CODEC_DIN/16.6C

CODEC_WCLK/16.6B

CODEC_BCLK/16.6C

CODEC_MCLK/14.6E

CODEC_SDA/16.6C

CODEC_SCL/16.6C

CODEC_RESET#/16.6B

C10 0.1uF — GND

R401 2.2k, R400 2.2k, R399 2.2k

VOL_MICDET

C28 0.47uF, C29 0.47uF

Speaker Output

L1 MPZ1608S221A — SPKP_R

L2 MPZ1608S221A — SPKM_R

L3 MPZ1608S221A — SPKP_L

L5 MPZ1608S221A — SPKM_L

R435 0 no stuff, R436 0 no stuff

ED555/4DS — J4

CODEC_DOUT/16.6B

Headphone Jack

C354 47uF — HP_L

C355 47uF — HP_R

HP_DET

J5 — SJ-43516-SMT — GND

Microphone Jack

J6 — MIC1LP, MIC1RP — SJ-43516-SMT — GND

0 R14

no stuff 0 R12

Volume Control (optional)

3V3

R420 48.7k

R422 3361S-1-503GLF

R424 0

C363 0.22uF — GND

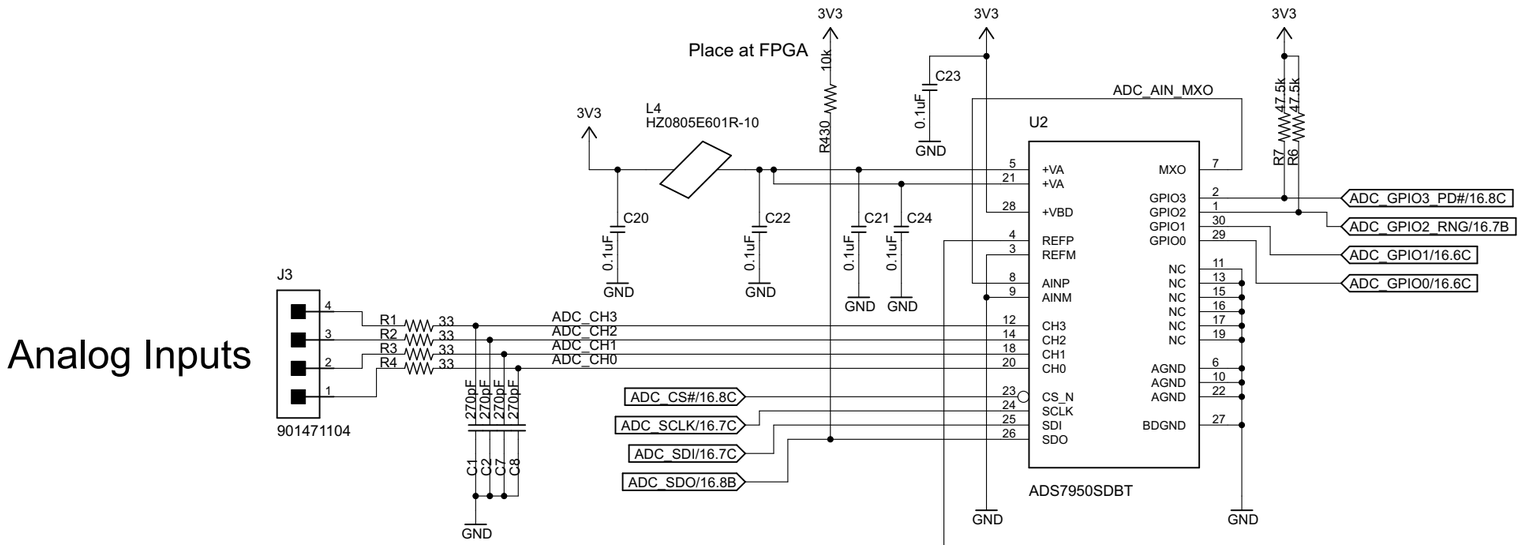
VOL

no stuff

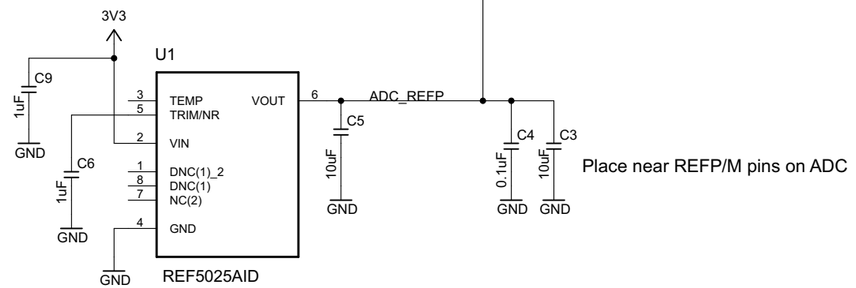
AUDIO

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 8/22

A/D Converter (ADC)



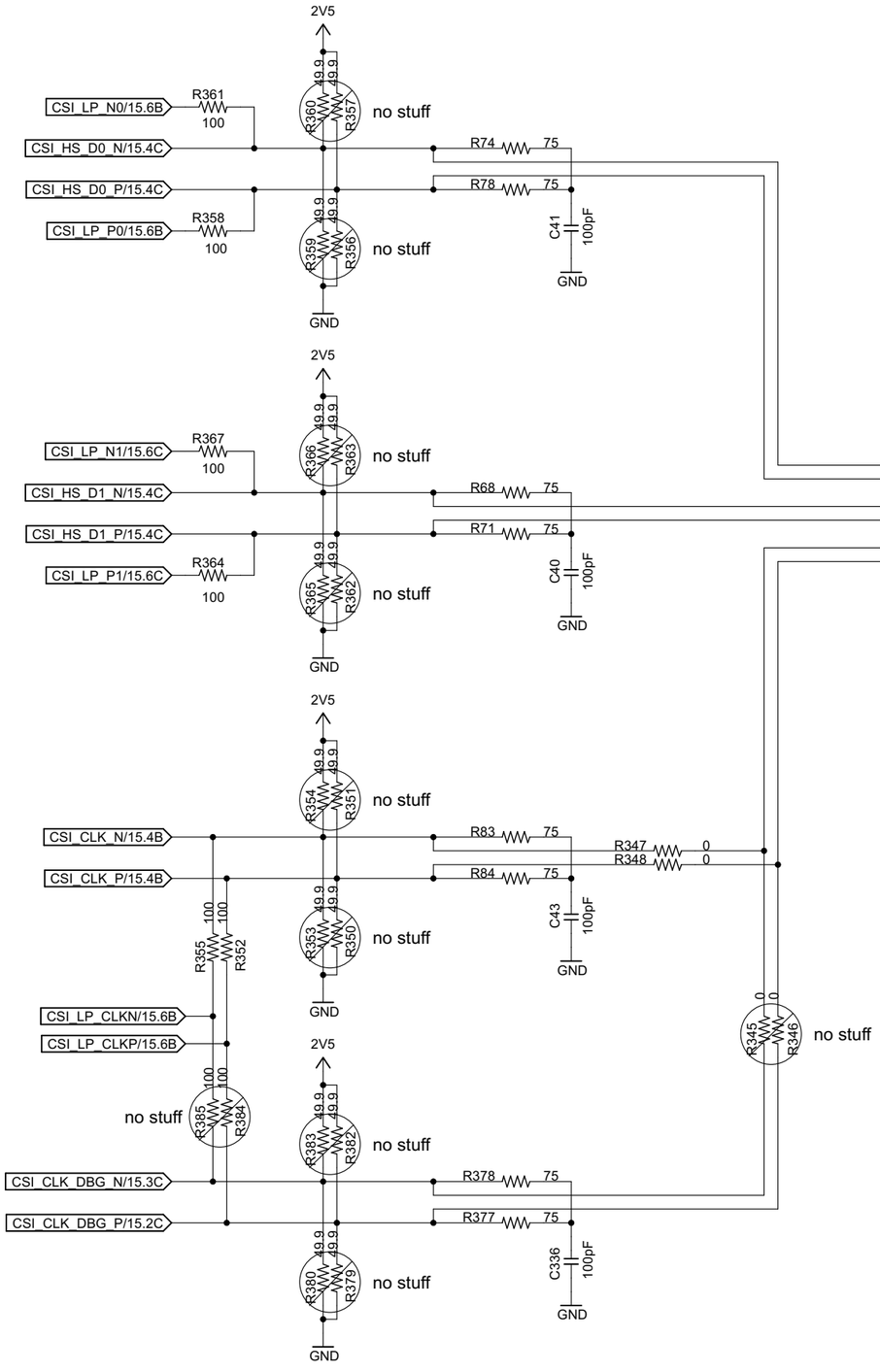
2.5V Reference



ADC

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 9/22	

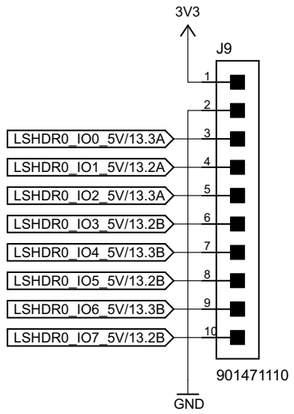
MIPI CSI-2 Connector



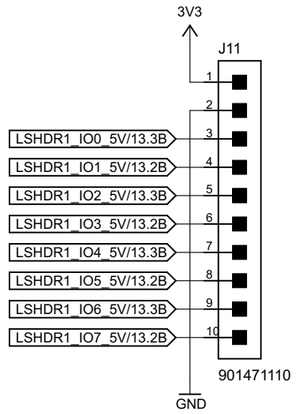
MIPI

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 10/22	

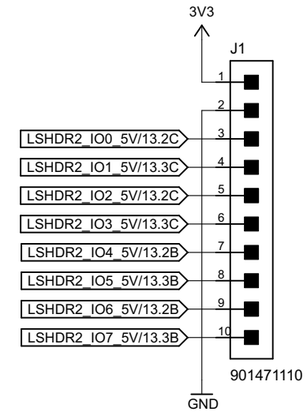
Low-Speed IO Header 0



Low-Speed IO Header 1

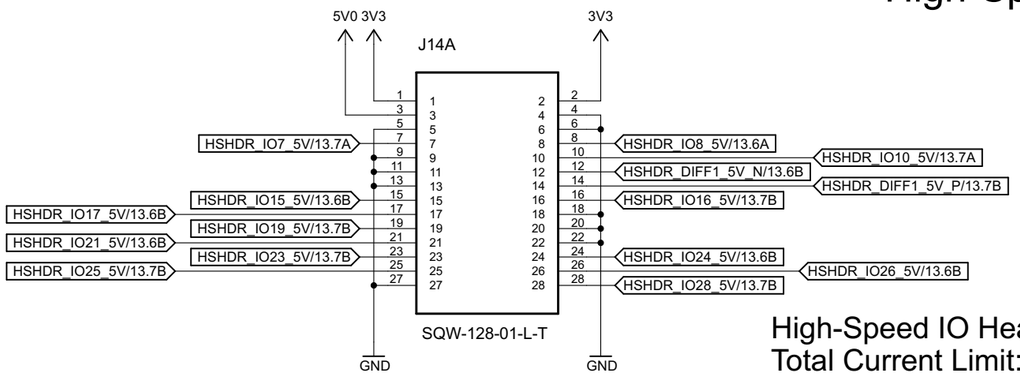


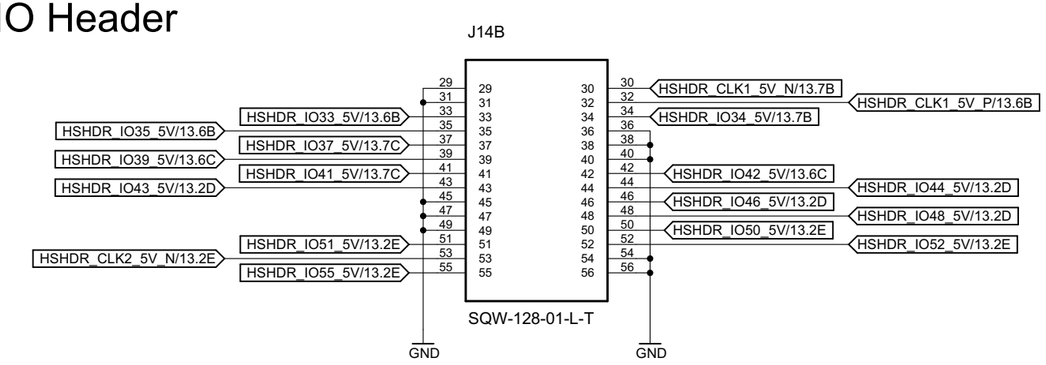
Low-Speed IO Header 2



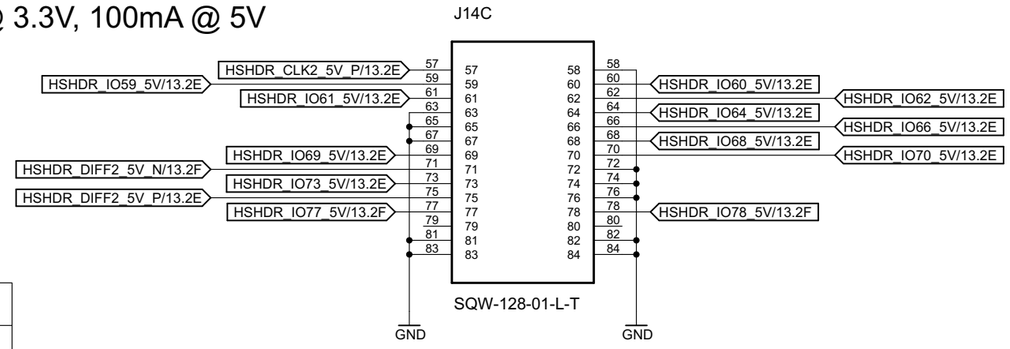
Low-Speed IO Header 0-2
Total Current Limit: 60mA @ 3.3V

High-Speed IO Header





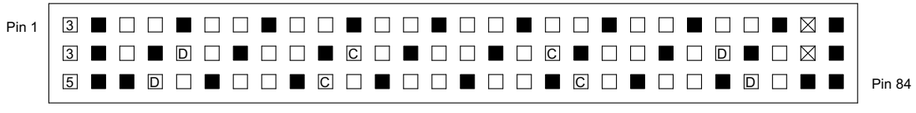
High-Speed IO Header
Total Current Limit: 40mA @ 3.3V, 100mA @ 5V



Low-Speed IO Header Pinout

Note: Use 5V Header (J8, p. 17) for 5V power

High-Speed IO Header Pinout



Note: Clock Pins 30 and 32 are FPGA input; Clock Pins 53 and 57 are FPGA output
Note: All differential and clock pairs are 2.5V

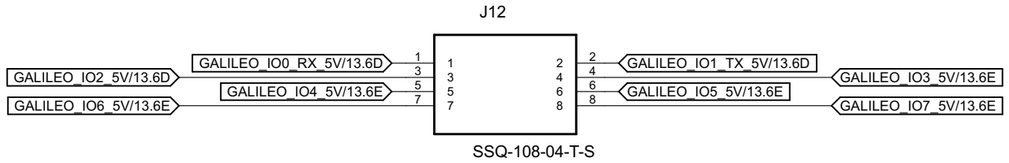
Key

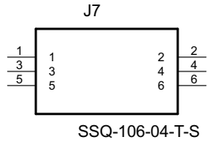
- ☐ Digital IO
- ■ Ground
- 3 3.3V
- 5 5V
- D Differential Pair (+/-)
- C Clock Pair (+/-)
- ☒ No Connect

IO HEADERS

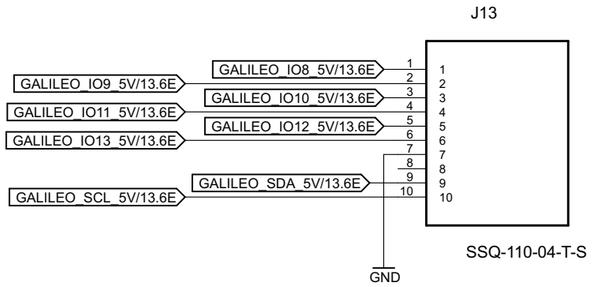
TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 11/22

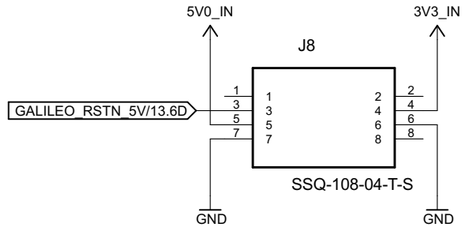
Note: Pin numbers match Galileo schematics



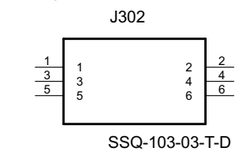


Analog input pins not connected to shield

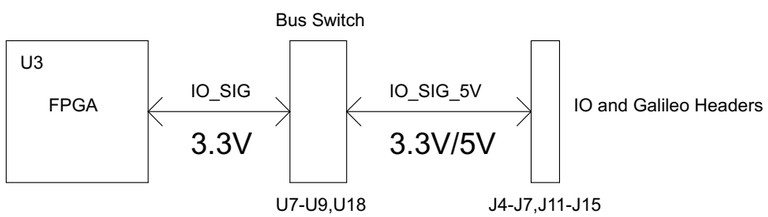




ICSP pins not connected to shield



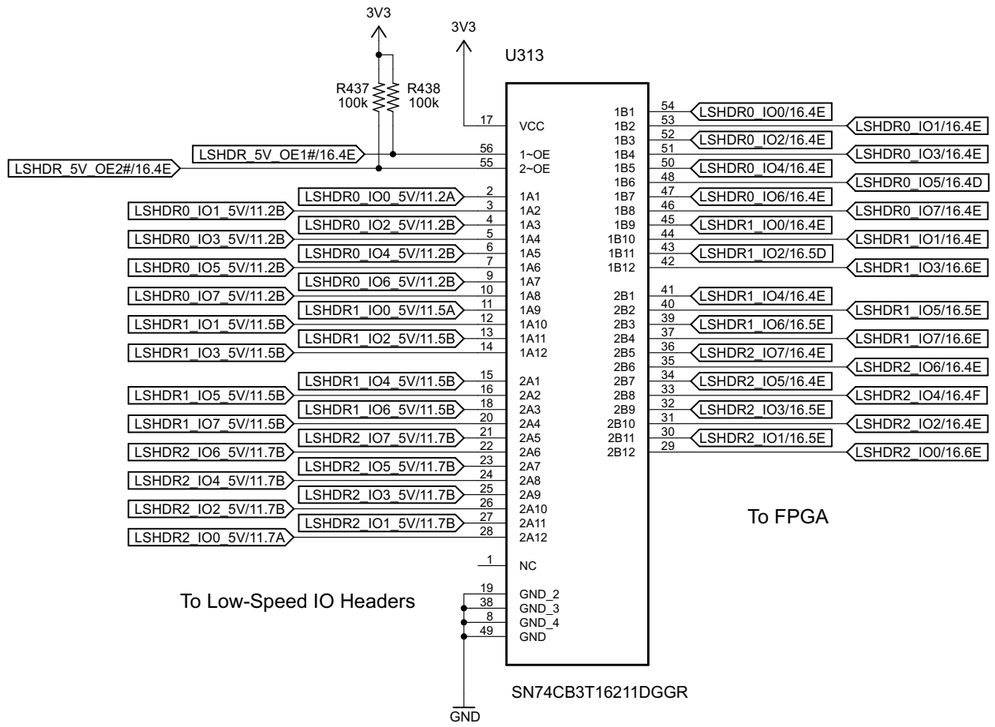
IO Signal Flow

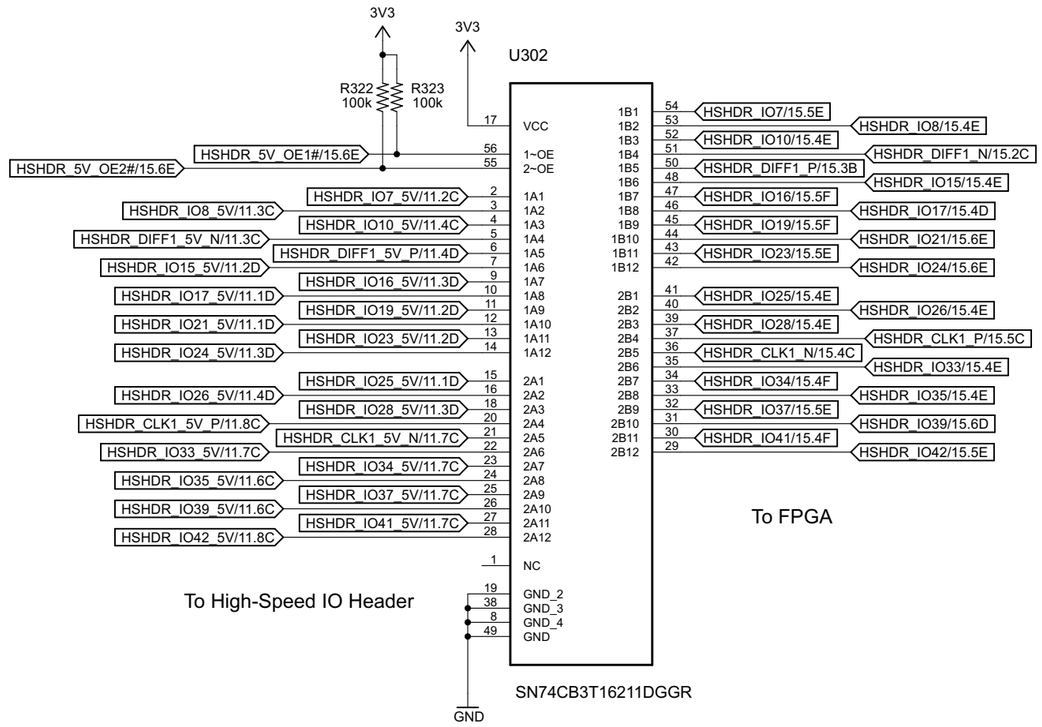


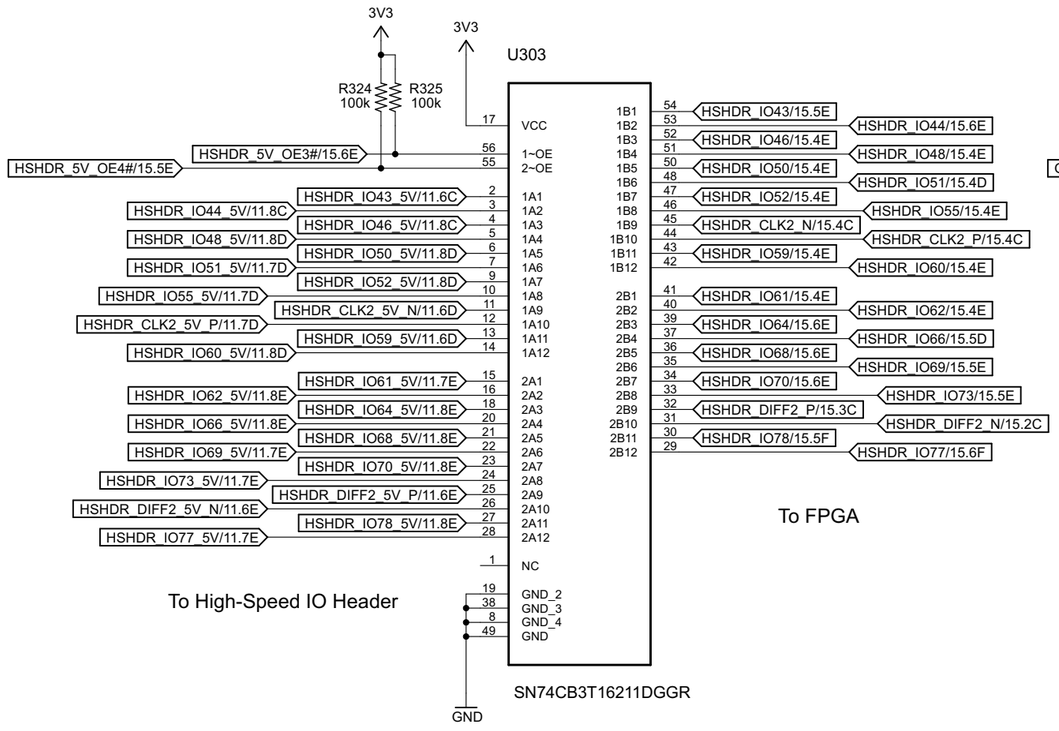
Note: '_5V' are Galileo/IO header signals and are 5V-tolerant.
Signals without '_5V' are 3.3V FPGA IOs (not 5V tolerant).

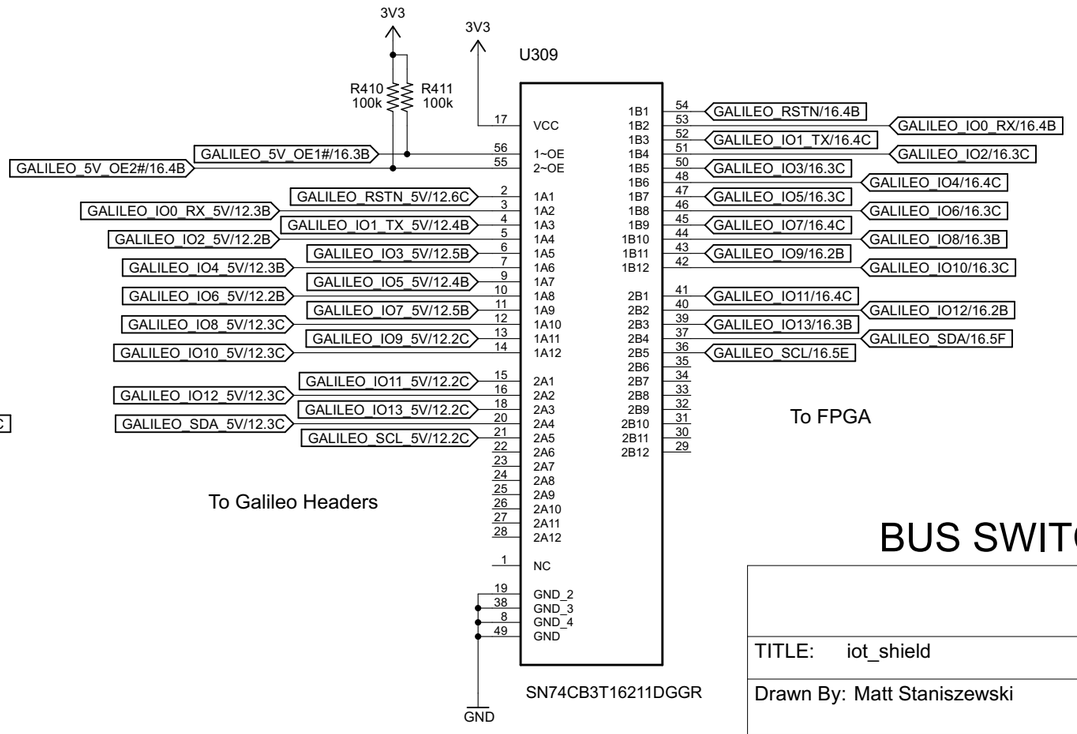
GALILEO HEADERS

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 12/22	





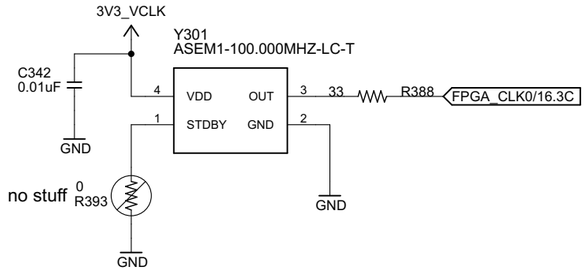




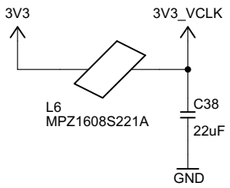
BUS SWITCHES

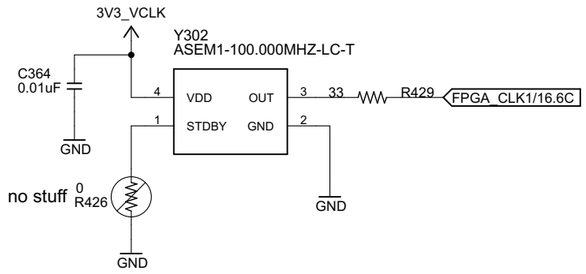
TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 13/22	

100MHz CMOS Oscillator

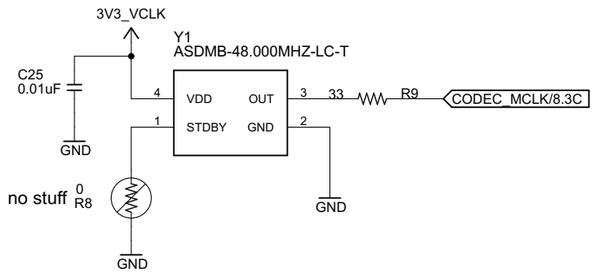


100MHz CMOS Oscillator





48MHz CMOS Oscillator

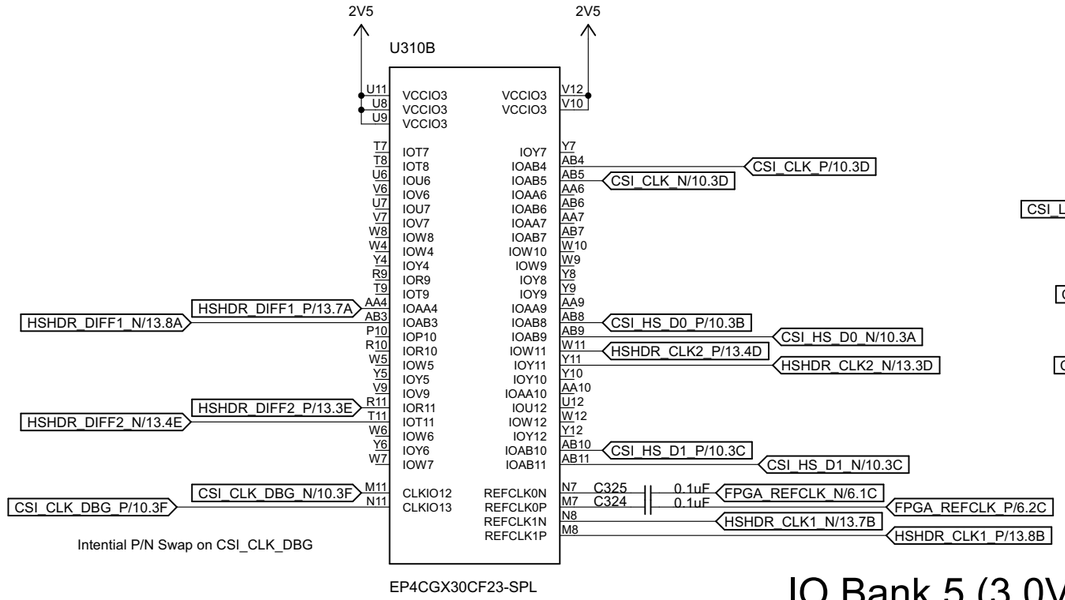


CLOCKS

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 14/22

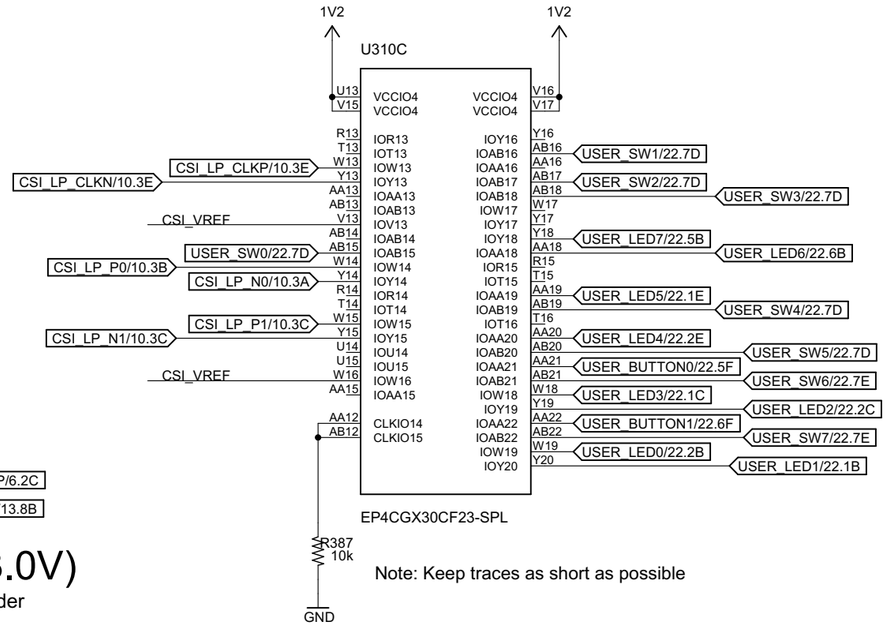
IO Bank 3 (2.5V)

MIPI/Clock/High-Speed IO Header



IO Bank 4 (1.2V)

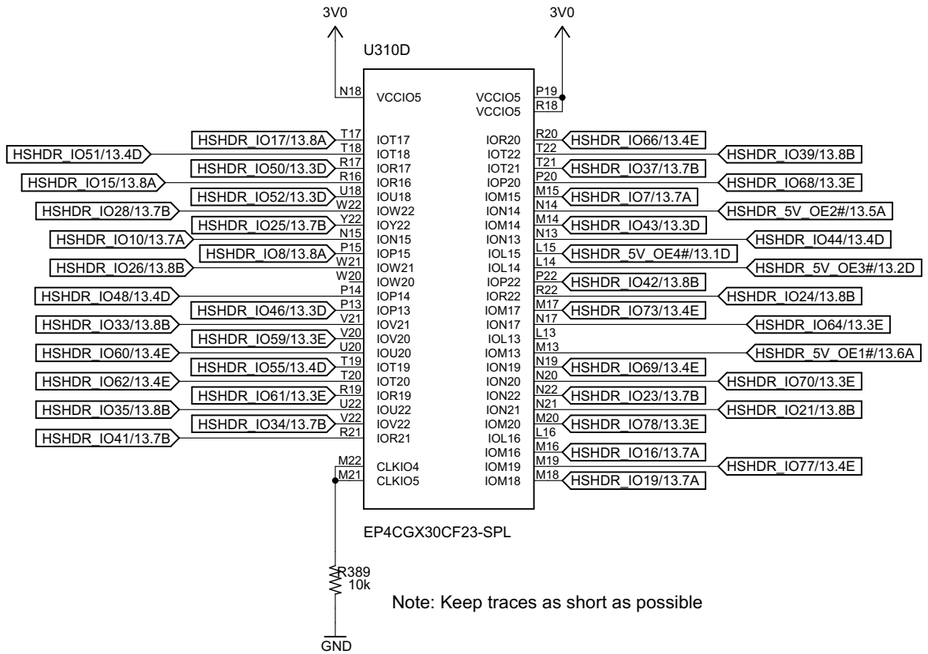
MIPI/LEDs/Buttons/Switches



Note: Keep traces as short as possible

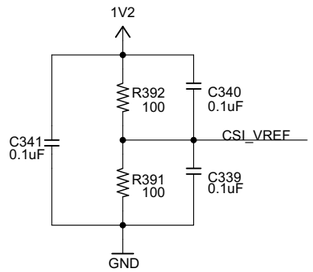
IO Bank 5 (3.0V)

High-Speed IO Header



Note: 3.0V IO Banks are compatible with 3.3V signaling

Note: Keep traces as short as possible

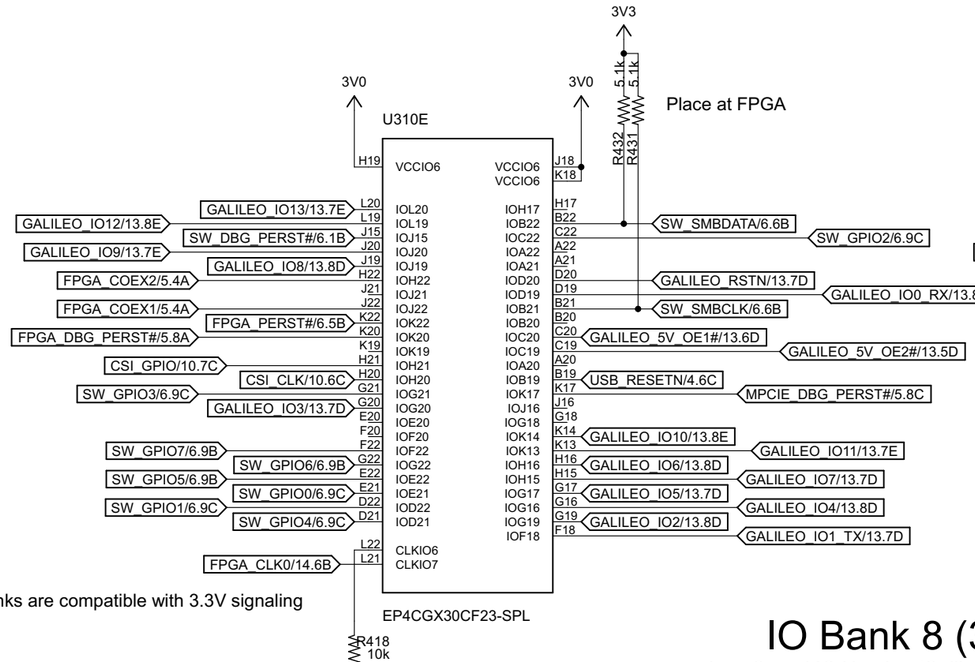


FPGA IO BANK 3 / 4 / 5

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 15/22	

IO Bank 6 (3.0V)

PCIe/Switch/Galileo IOs/Clock

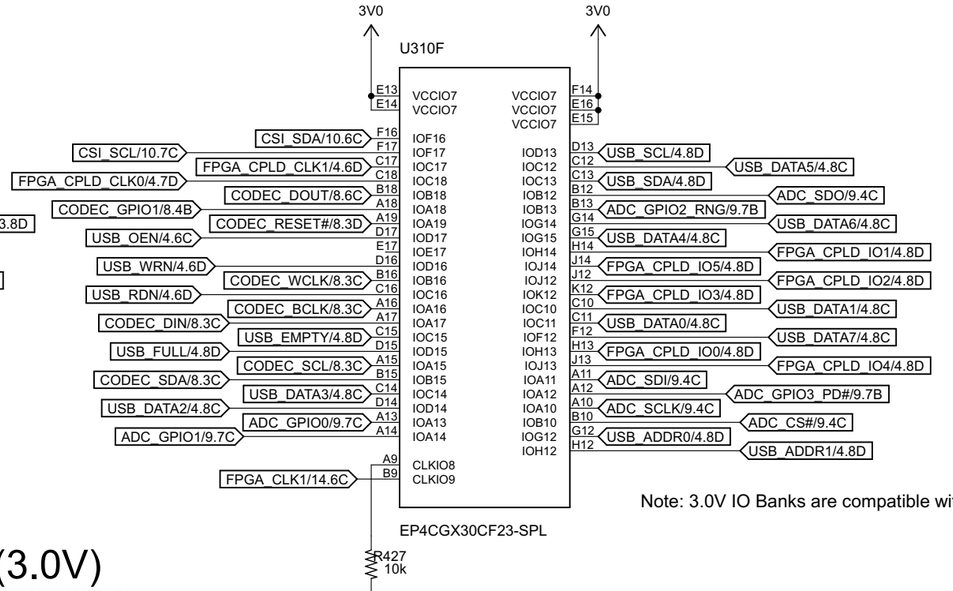


Note: 3.0V IO Banks are compatible with 3.3V signaling

Note: Keep traces as short as possible

IO Bank 7 (3.0V)

Codec/ADC/Clock/USB Blaster

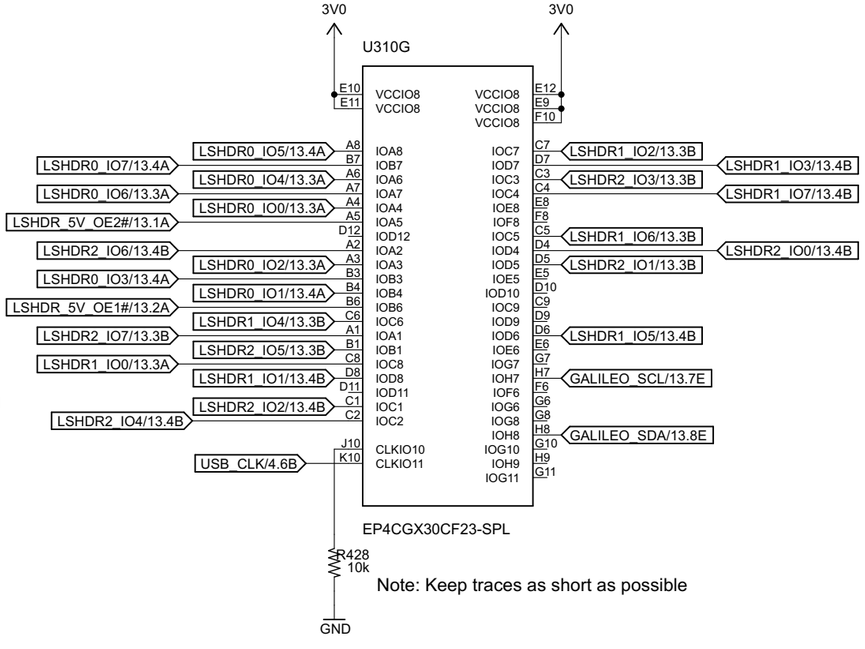


Note: 3.0V IO Banks are compatible with 3.3V signaling

Note: Keep traces as short as possible

IO Bank 8 (3.0V)

Low-Speed IO Headers/Galileo IOs/USB Blaster



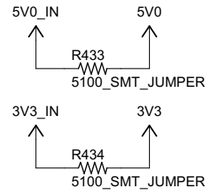
Note: 3.0V IO Banks are compatible with 3.3V signaling

Note: Keep traces as short as possible

FPGA IO BANK 6 / 7 / 8

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 16/22	

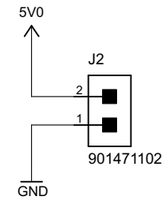
POWER IN JUMPERS



Metal jumpers; Place at least 75mil apart

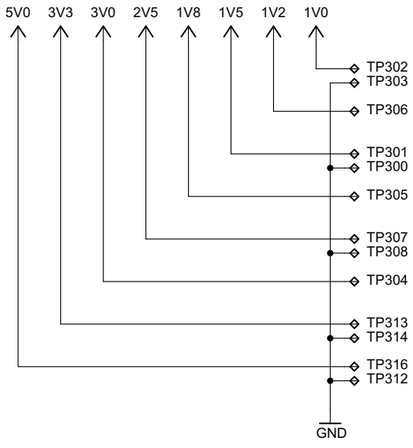
5V HEADER

Use 5V Header (J8) to supply 5V power to devices



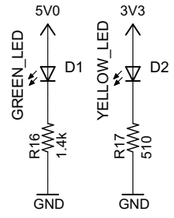
5V Header Total Current Limit: 100mA @ 5V

POWER PROBE TESTPOINTS

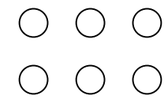


Place ground testpoint next to each rail testpoint
(except where a common ground pad can be shared)

POWER LEDs



BOARD FIDUCIALS



Note: Shield power limits assume all header current limits are used and a Mini-PCIe Gen1 card (i.e. Wi-Fi) is connected.

It is assumed that additional shields or USB devices are not connected to the Galileo; please use at your own risk.

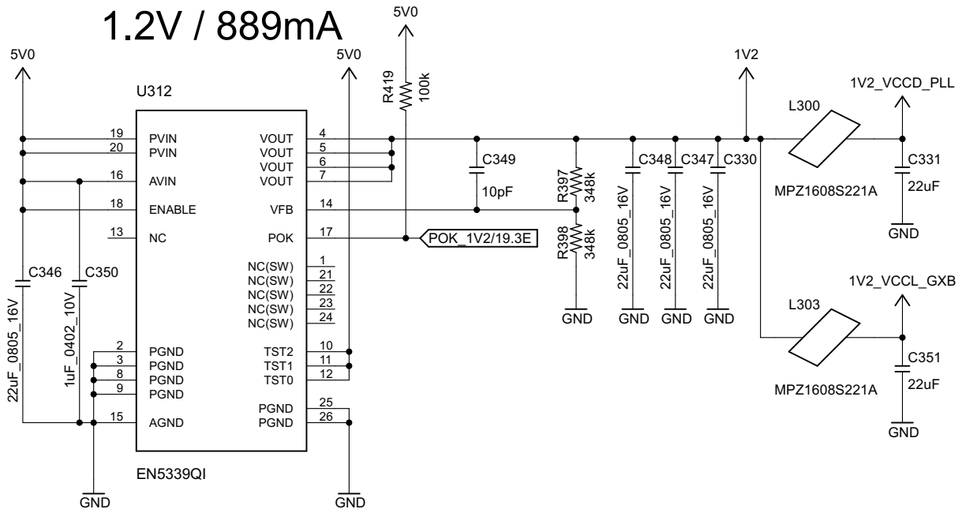
For larger FPGAs (GX50 and above), input power must be supplied externally. Remove R4 and R5 and power the 5V0 and 3V3 voltage rails from a separate source.

POWER IN

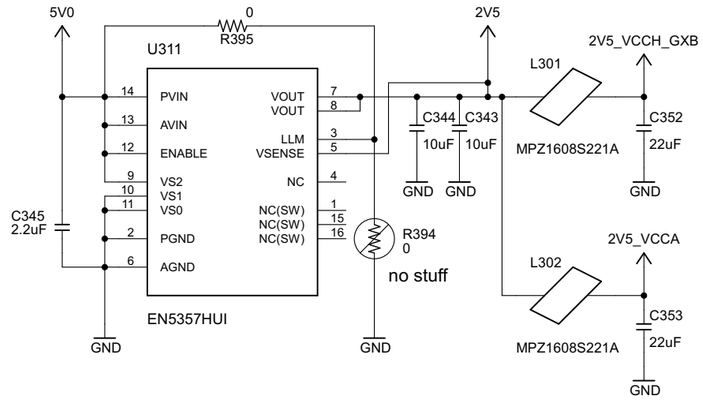
TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 17/22	

1.2V / 889mA

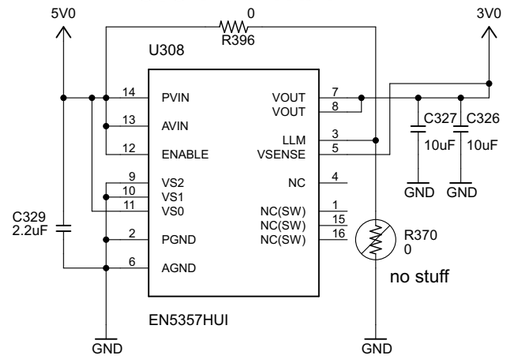
Place C21 as close to AVIN as possible



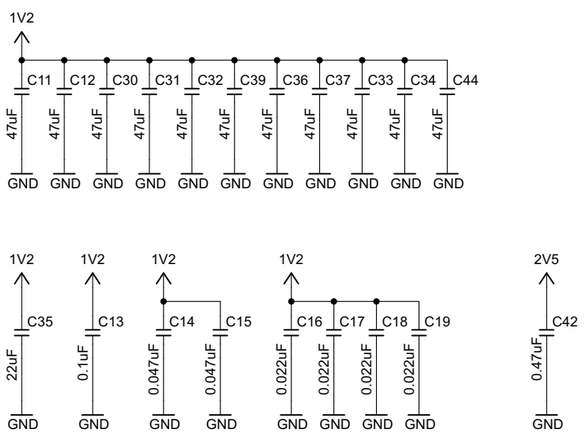
2.5V / 133mA



3.0V / 7mA



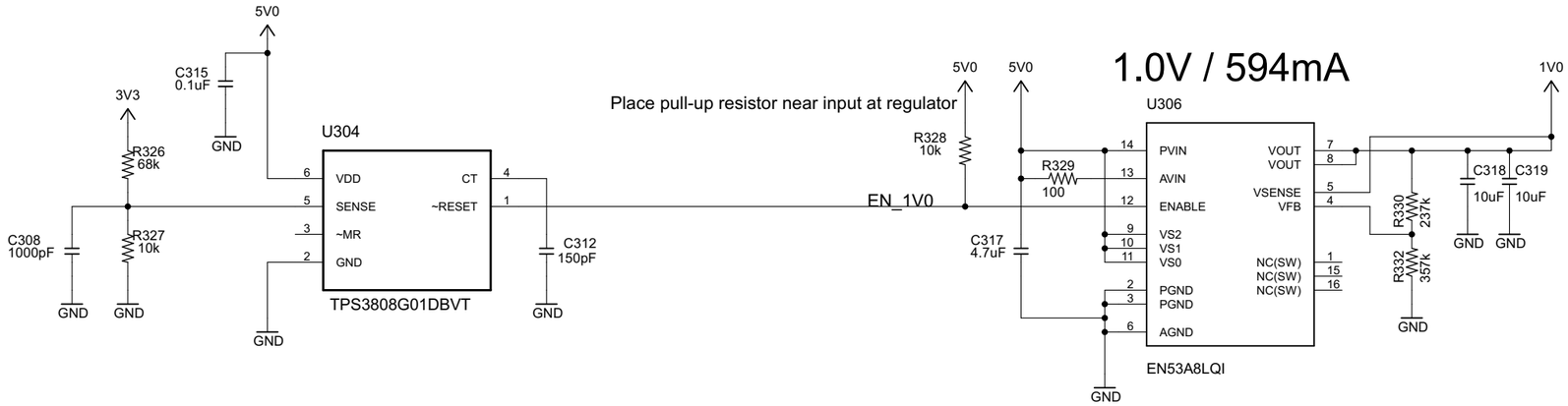
FPGA Decoupling

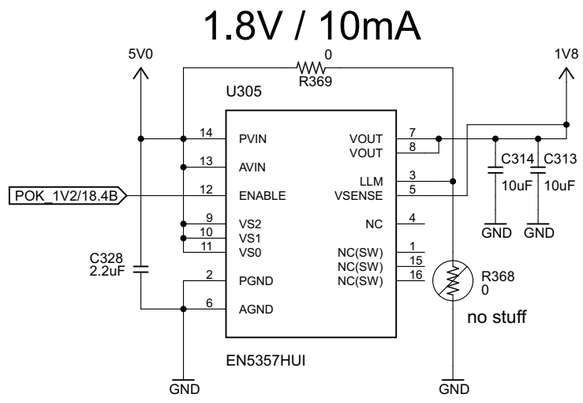


FPGA VREGS / DECOUPLING

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 18/22

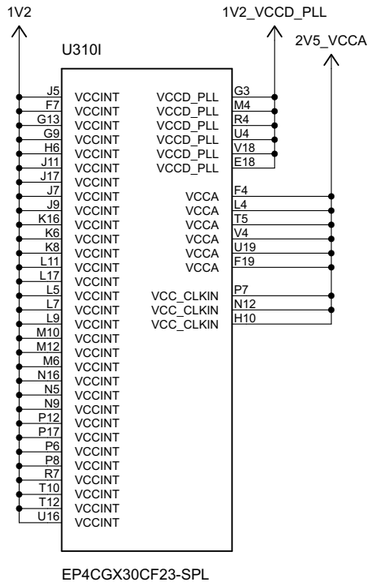
Supervisor (1.0V POK)

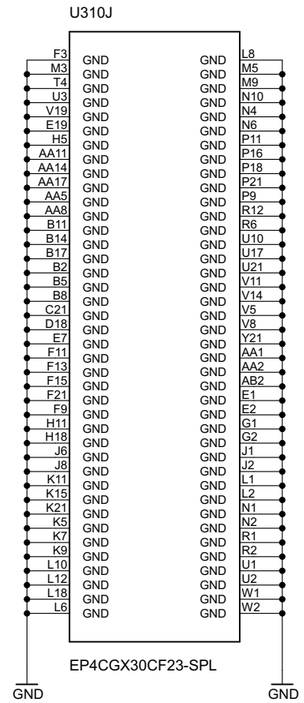




SYSTEM VREGS

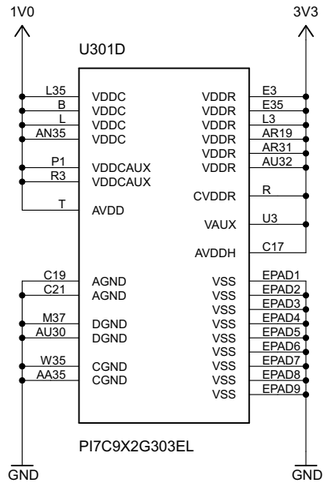
TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 19/22

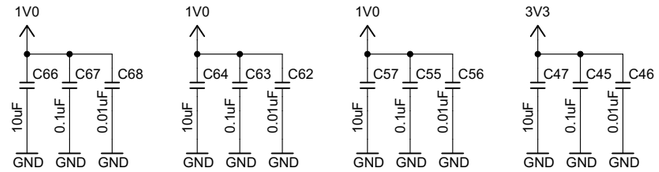




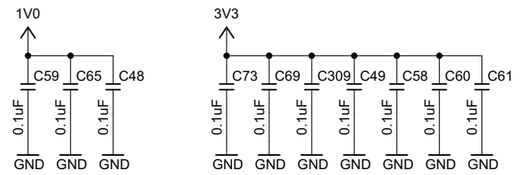
FPGA PWR / GND

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 20/22





Place groupings at each power pad (T, B, L, R)

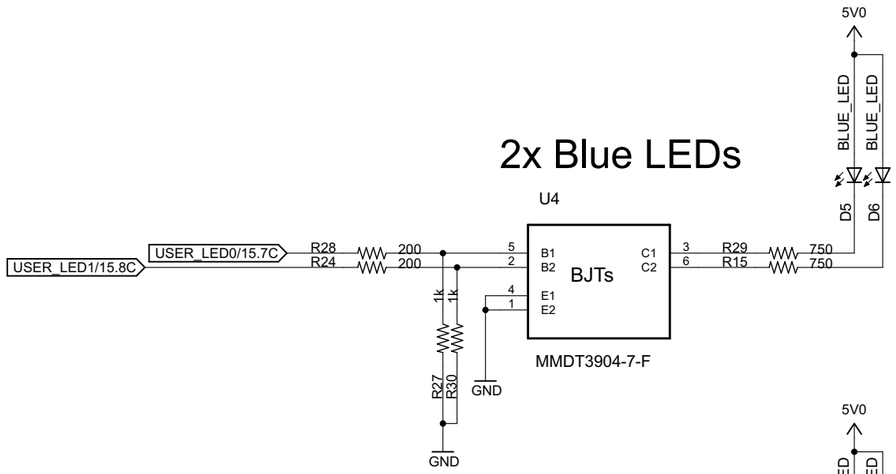


Place common capacitor between near pads with same voltage

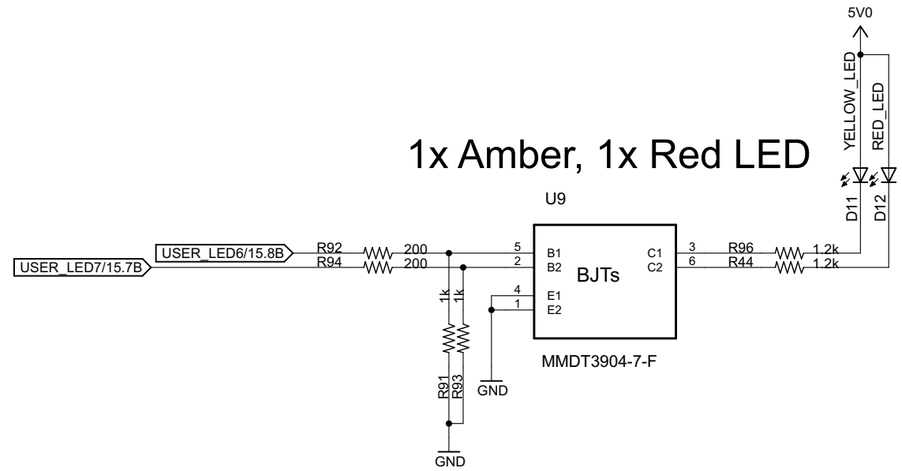
SW PWR / GND / DECOUPLING

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 21/22

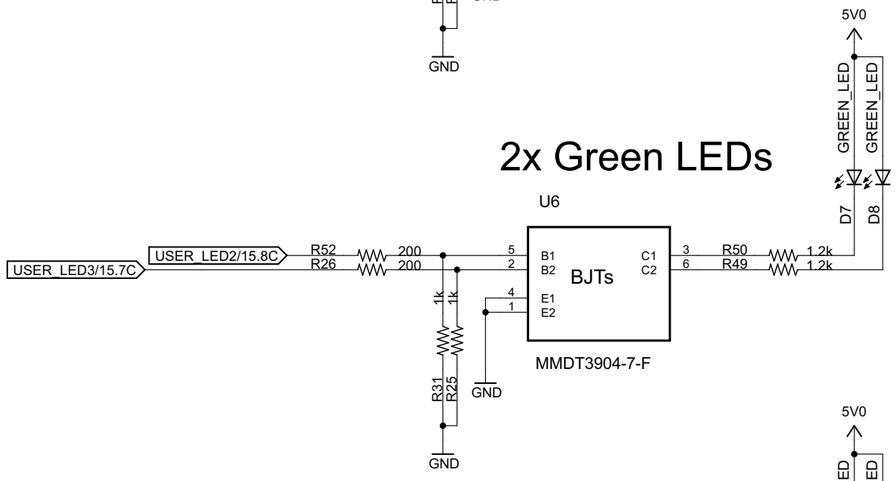
2x Blue LEDs



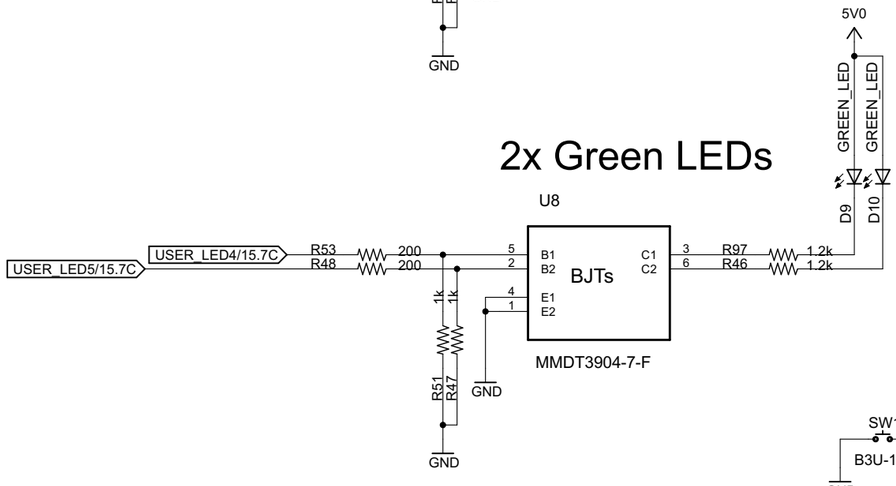
1x Amber, 1x Red LED



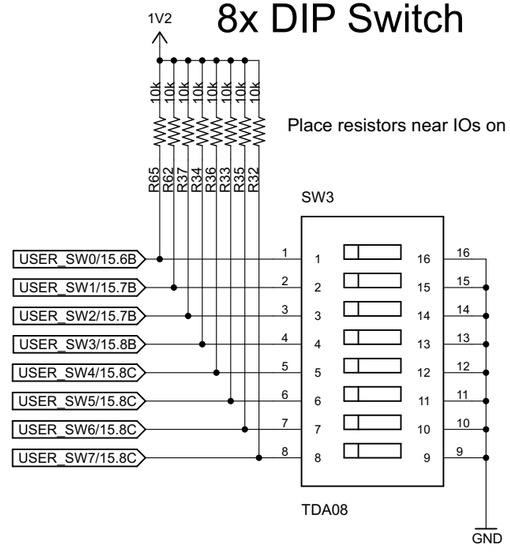
2x Green LEDs



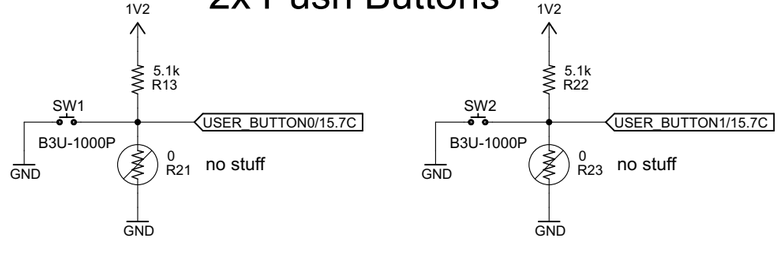
2x Green LEDs



8x DIP Switch



2x Push Buttons



LEDS / BUTTONS / SWITCHES

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.11
Date: 10/14/2014 9:58:22 AM	Sheet: 22/22	