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Drawn By: Matt Staniszewski		REV: 1.04
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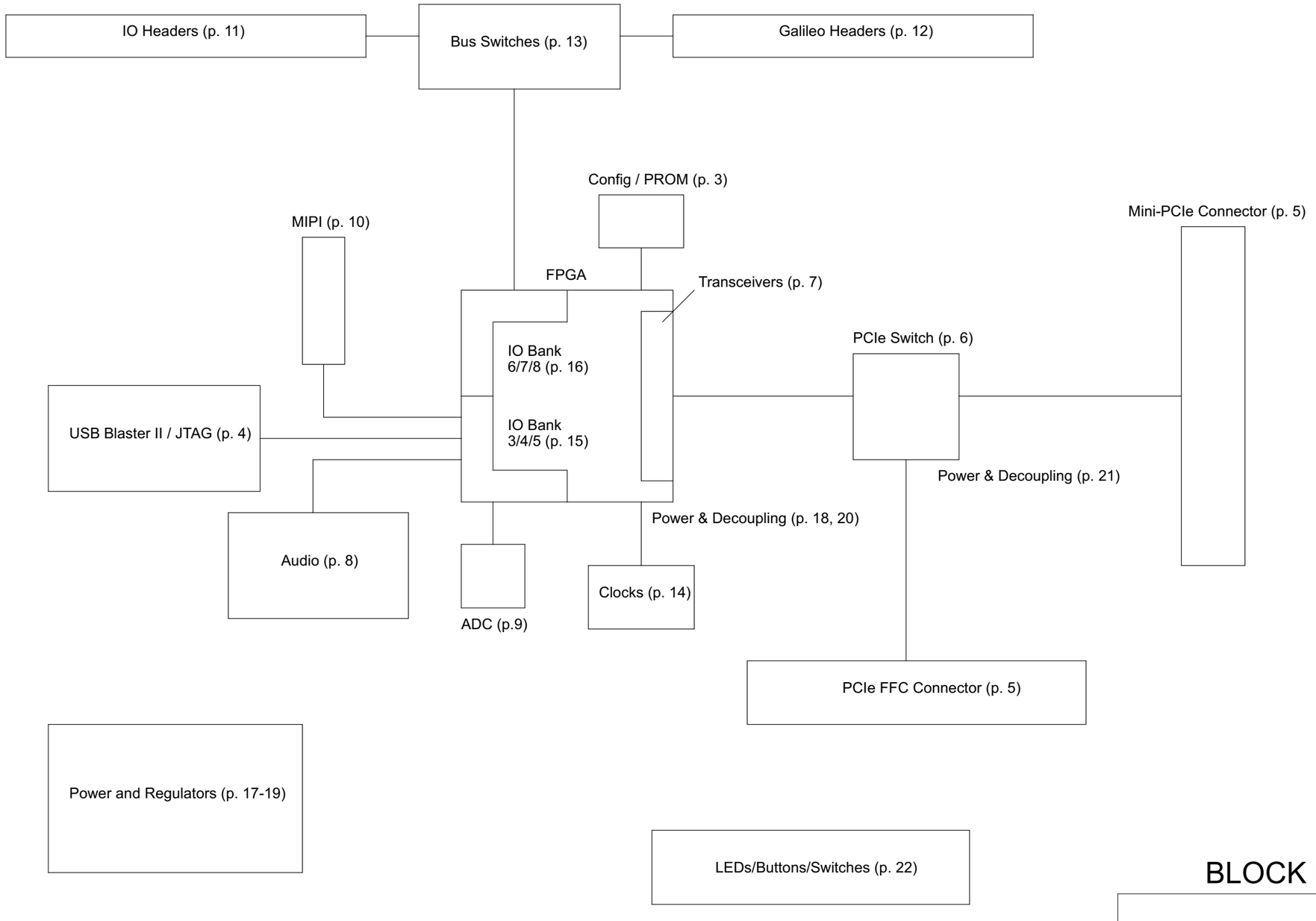

BLOCK DIAGRAM

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Drawn By: Matt Staniszewski		REV: 1.04
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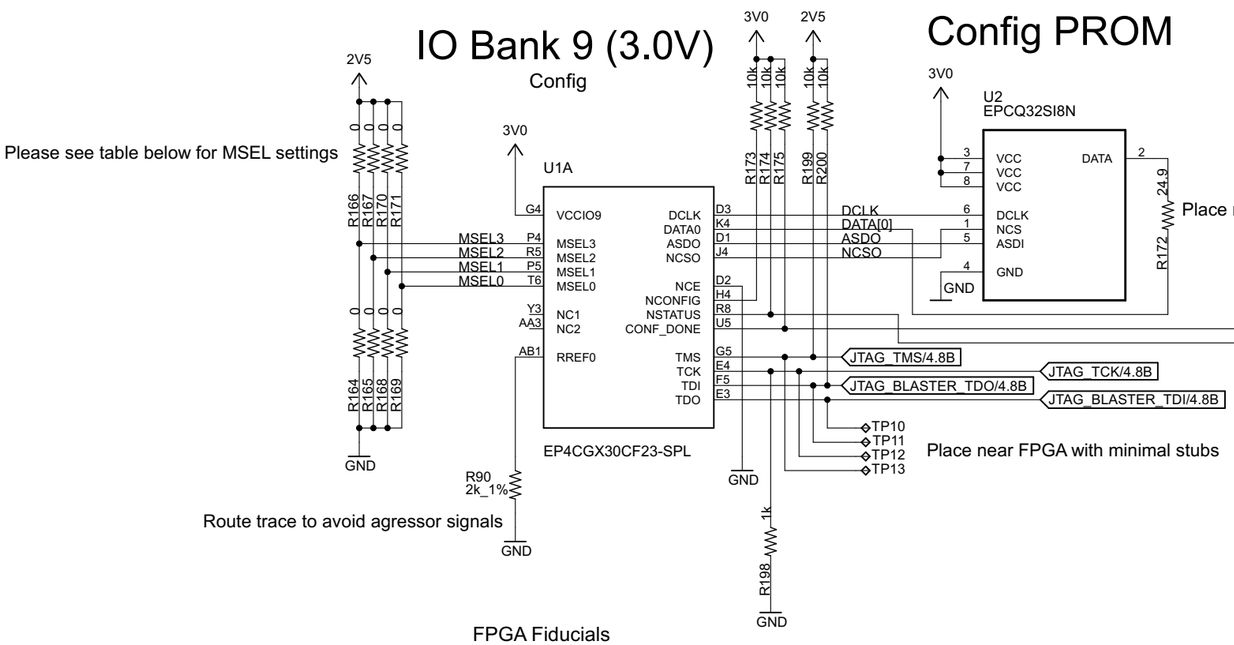
IO Bank 9 (3.0V)

Config

Please see table below for MSEL settings



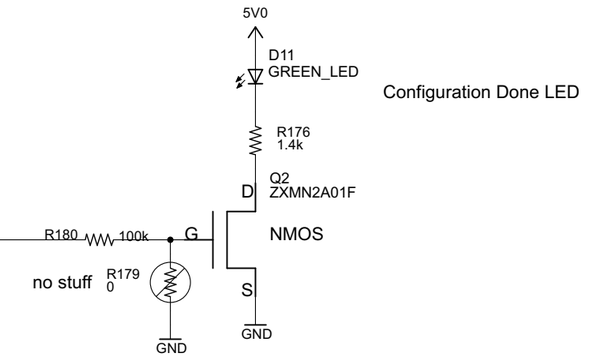
Place near FPGA with minimal stubs

FPGA Fiducials

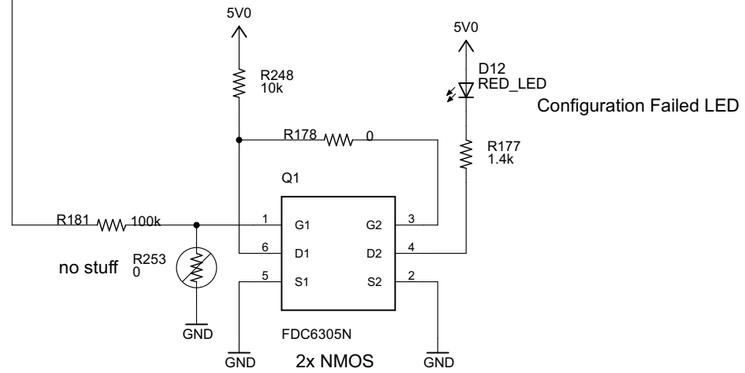
Config PROM

Place resistor near config device

CONF_DONE
NSTATUS



Configuration Done LED



Configuration Failed LED

MSEL Settings

Function	MSEL3		MSEL2		MSEL1		MSEL0	
Resistor	R166	R164	R167	R165	R170	R168	R171	R169
stuff	X			X	X		X	
no stuff		X	X			X		X

Current configuration: AS x1 Mode, Fast POR

FPGA CONFIG / JTAG

TITLE: iot_shield	
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Micro USB

J20
10118194-0001LF

Route high-speed USB signals carefully

VBUS_5V
FX2_D_N
FX2_D_P
R186 0
no stuff
GND

SH1 SH2 SH3 SH4 SH5 SH6
CH_GND

U22
ESD
D+
D-
GND
TPD2EUSB30DR

R193 10k

R185 1M
CH_GND C160 4700pF GND

Y4 24MHz
Crystal
C158 12pF
C159 12pF
GND

3V3
C66 0.1uF
GND

Place on USB peninsula for J20

FX2_SDA R188 0 MAX_SDA

3V3
MAX811SEUS+T
GND MR#
RESET# VCC
R187 100k FX2_RESETN
C161 0.1uF
GND
Voltage Monitor U23

3V3
R189 2k
R190 2k

USB Controller

U24
VCC

FX2_RESETN	49	RESET	PB0/FD0 25 FX2_PB0
			PB1/FD1 26 FX2_PB1
FX2_WAKEUP	51	WAKEUP	PB2/FD2 27 FX2_PB2
			PB3/FD3 28 FX2_PB3
24M_XTALIN	12	XTALIN	PB4/FD4 29 FX2_PB4
24M_XTALOUT	11	XTALOUT	PB5/FD5 30 FX2_PB5
			PB6/FD6 31 FX2_PB6
	5	CLKOUT/T1OUT	PB7/FD7 32 FX2_PB7
			PD0/FD8 52 FX2_PD0
			PD1/FD9 53 FX2_PD1
FX2_SLRDN	8	RDY0/SLRD	PD2/FD10 54 FX2_PD2
FX2_SLWRN	9	RDY1/SLRW	PD3/FD11 55 FX2_PD3
			PD4/FD12 56 FX2_PD4
USB_CLK R215 33	20	IFCLK/T0OUT	PD5/FD13 1 FX2_PD5
	21	RESEVED	PD6/FD14 2 FX2_PD6
			PD7/FD15 3 FX2_PD7
FX2_SCL	22	SCL	
FX2_SDA	23	SDA	PA0/INT0 40
			PA1/INT1 41 FX2_PA1
			PA2/SLOE 42 FX2_PA2
	15	DPLUS	PA3/WU2 43 FX2_PA3
	16	DMINUS	PA4/FIFOADR0 44 FX2_PA4
			PA5/FIFOADR1 45 FX2_PA5
	10	AVCC	PA6/PKTEND 46 FX2_PA6
	14	AVCC	PA7/FLAGD/SLCS 47 FX2_PA7
	17	AGND	CTL0/FLAGA 36 FX2_FLAGA
	13	AGND	CTL1/FLAGB 37 FX2_FLAGB
			CTL2/FLAGC 38 FX2_FLAGC

GND
19 48 35 33 7 4
CY7C68013A-56PVXC

20k R192
C162 0.1uF
GND GND

GND

JTAG Header

3V3
J18
C_USB_MAX_TCK
C_USB_MAX_TDO
C_USB_MAX_TMS
C_USB_MAX_TDI
R182 1k
R183 1k
R184 1k
GND GND
CLP-107-02-F-D-K

3V3
C169 C170 C171 C172 C173 C174 C175 C176
0.1uF
GND
Place near CY7C68013A

CPLD

U15A
CPLD Fiducials

3V3
R201 1k

FX2_PB5	2	IOB1_1	IOB1_17	28	FX2_PA5
FX2_PB4	3	IOB1_2	IOB1_18	29	FX2_PA4
FX2_PB3	4	IOB1_3	IOB1_19	30	FX2_PA3
FX2_FLAGA	5	IOB1_4	IOB1_20	33	FX2_SLRDN
FX2_PB7	6	IOB1_5	IOB1_21	34	FX2_SLWRN
FX2_PB6	7	IOB1_6	IOB1_22	35	FX2_PA7
	8	IOB1_7	IOB1_23	36	FX2_PA6
FX2_PB2	15	IOB1_8	IOB1_24	38	JTAG_TCK/3.5C
FX2_FLAGB	16	IOB1_9	IOB1_25	40	
FX2_FLAGC	17	IOB1_10	IOB1_26	41	FX2_PD6
FX2_SCL	18	IOB1_11	IOB1_27	42	FX2_PD7
FX2_PB1	19	IOB1_12	IOB1_28	47	FX2_PD4
FX2_PA1	20	IOB1_13	IOB1_29	48	FX2_PD5
FX2_PA2	21	IOB1_14	IOB1_30	49	JTAG_BLASTER_TDO/3.4C
USB_DISABLEN	26	IOB1_15	IOB1_31	50	JTAG_TMS/3.4C
	27	IOB1_16	IOB1_32	51	JTAG_BLASTER_TDI/3.5C
USB_CLK/16.4F	12	IOB1/GCLK0	TMS	22	C_USB_MAX_TMS R203 0 FX2_PD1
FX2_PB0	14	IOB1/GCLK1	TDI	23	C_USB_MAX_TDI R204 0 FX2_PD2
			TCK	24	C_USB_MAX_TCK R205 0 FX2_PD0
MAX_SDA	43	IOB1/DEV_OE	TDO	25	C_USB_MAX_TDO R206 0 FX2_PD3
FX2_RESETN	44	IOB1/DEV_CLRN			

EPM570GT100

3V3
R212 1k
R197 1k
R213 1k
R214 1k

U15B

JTAG_TX	52	IOB2_1	IOB2_20	77	USB_DATA0/16.7C
SC_RX	53	IOB2_2	IOB2_19	76	USB_DATA1/16.8C
SC_TX	54	IOB2_3	IOB2_18	75	USB_DATA2/16.6C
JTAG_RX	55	IOB2_4	IOB2_17	74	USB_DATA3/16.6C
	56	IOB2_5	IOB2_21	78	USB_DATA4/16.7B
USB_RESETN/16.3C	57	IOB2_6	IOB2_22	81	USB_DATA5/16.8B
USB_RESETN	58	IOB2_7	IOB2_23	82	USB_DATA6/16.8B
USB_OEN/16.6B	61	IOB2_8	IOB2_24	83	USB_DATA7/16.8C
USB_RDN/16.6C	66	IOB2_9	IOB2_25	84	
USB_WRN	67	IOB2_10	IOB2_26	85	USB_ADDR0/16.7C
USB_WRN/16.6B	68	IOB2_11	IOB2_27	86	USB_ADDR1/16.8C
	69	IOB2_12	IOB2_28	87	USB_FULL/16.6C
R207 0 M570_PCIE_JTAG_EN	70	IOB2_13	IOB2_29	89	USB_EMPTY/16.6C
	71	IOB2_14	IOB2_30	91	USB_SCL/16.7B
	72	IOB2_15	IOB2_31	92	
	73	IOB2_16	IOB2_32	95	USB_SDA/16.7B
FPGA_CPLD_CLK1/16.6B	62	IOB2/GCLK2	IOB2_33	96	FPGA_CPLD_IO0/16.7C
FPGA_CPLD_CLK0/16.6B	64	IOB2/GCLK3	IOB2_34	97	FPGA_CPLD_IO1/16.8B
			IOB2_35	98	FPGA_CPLD_IO2/16.8B
			IOB2_36	99	FPGA_CPLD_IO3/16.7C
			IOB2_37	100	FPGA_CPLD_IO4/16.8C
			IOB2_38	1	FPGA_CPLD_IO5/16.7B

EPM570GT100

1V8 3V3
U15C

11	GNDINT	VCCINT	13
37	GNDINT	VCCINT	39
65	GNDINT	VCCINT	63
90	GNDINT	VCCINT	88
10	GNDIO	VCCIO1	9
32	GNDIO	VCCIO1	31
46	GNDIO	VCCIO1	45
60	GNDIO		
79	GNDIO	VCCIO2	59
93	GNDIO	VCCIO2	80
		VCCIO2	94

EPM570GT100

1V8 3V3
C163 C164 0.1uF
C165 C166 C167 C168 0.1uF
GND
Place near MAX II

5V0
GREEN_LED D17
GREEN_LED D18

USB Blaster Status LEDs

U25
JTAG_RX R221 200
JTAG_TX R222 200
B1 B2 C1 C2 E1 E2
BJTs
MMDT3904-7-F
R202 1.2k
R220 1.2k
R223 1k
R224 1k
GND

5V0
GREEN_LED D19
GREEN_LED D20

U26
SC_RX R227 200
SC_TX R228 200
B1 B2 C1 C2 E1 E2
BJTs
MMDT3904-7-F
R225 1.2k
R226 1.2k
R229 1k
R230 1k
GND

USB BLASTER II

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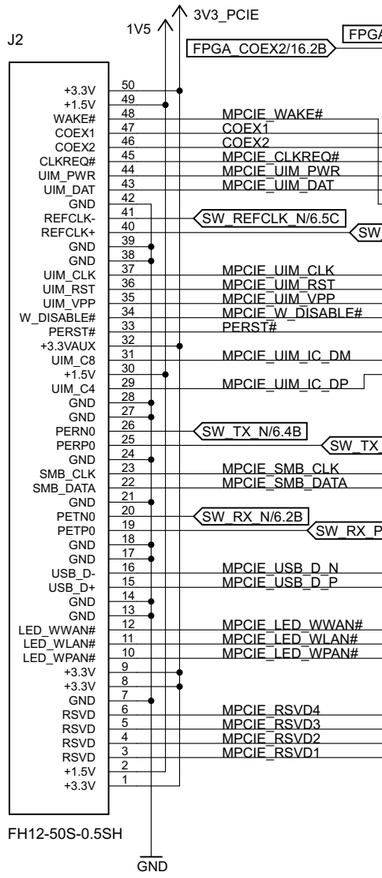
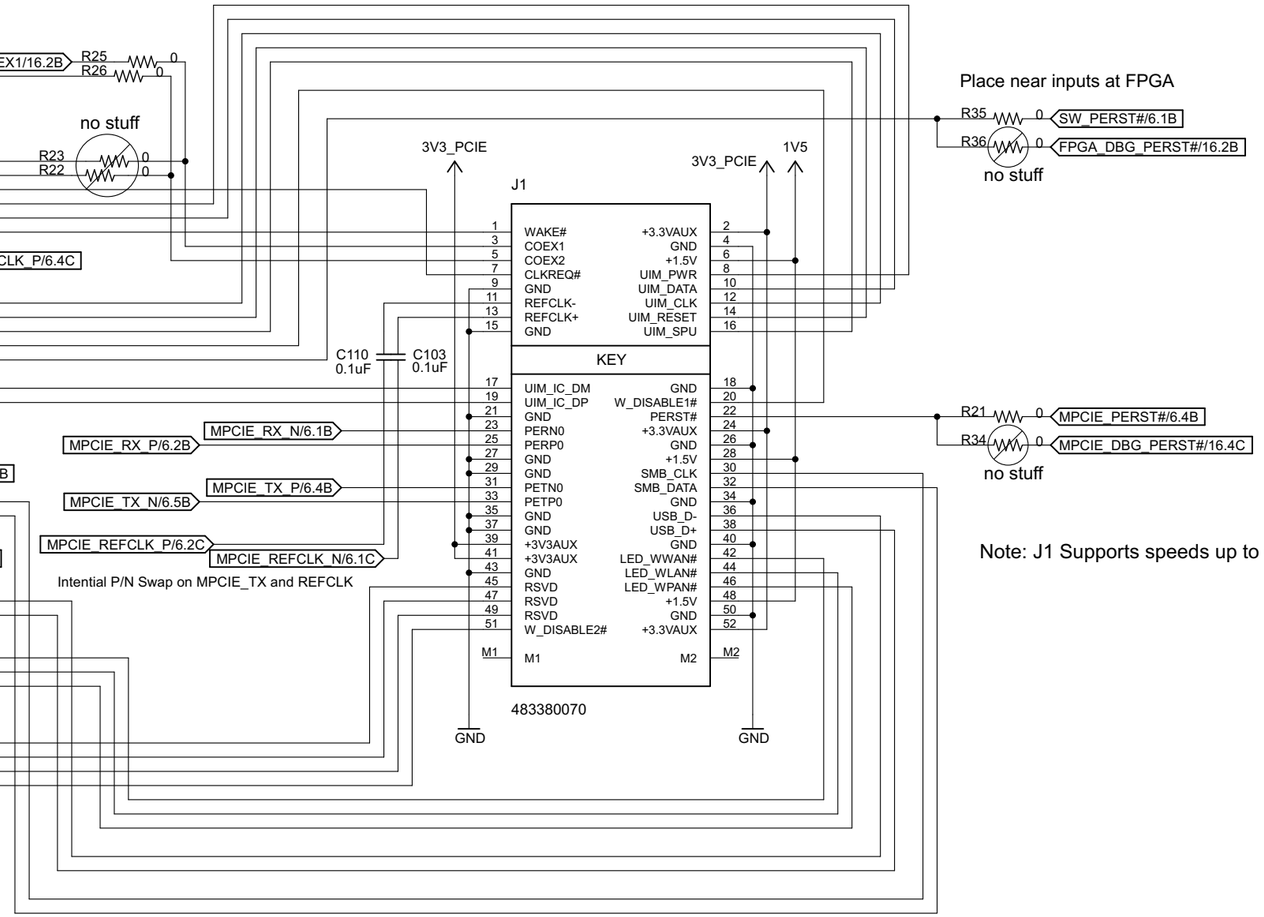
FFC Connector



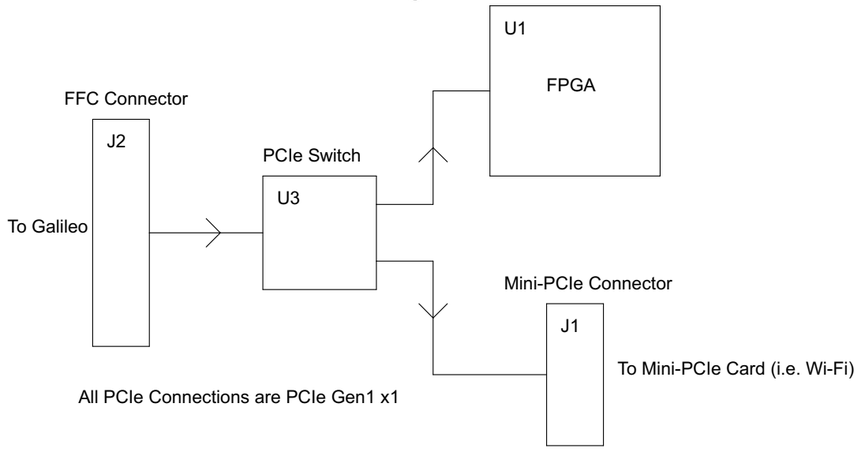
FFC Cable to Galileo

Mini-PCIe Connector



Note: J1 Supports speeds up to Gen1 (2.5Gbps)

PCIe Flow Diagram



All PCIe Connections are PCIe Gen1 x1

PCIe CONNECTORS

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.04
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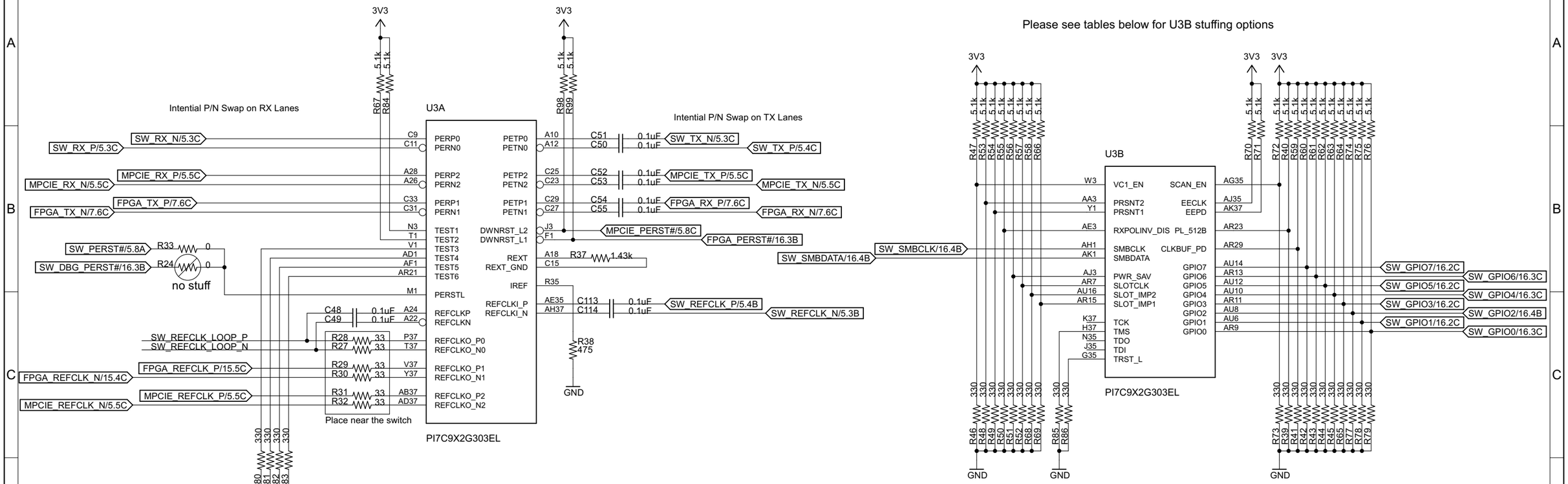

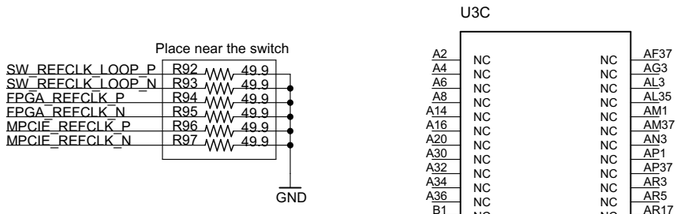

Function	VC1_EN		PRSNT2		PRSNT1		RXPOLINV_DIS		PWR_SAV		SLOTCLK		SLOT_IMP2		SLOT_IMP1	
Resistor	R47	R46	R53	R48	R54	R49	R55	R50	R56	R51	R57	R52	R58	R68	R66	R69
stuff		X		X		X		X	X		X		X		X	
no stuff	X		X		X		X			X		X		X		X

Function	SCAN_EN		PL_512B		CLKBUF_PD		GPIO7		GPIO6		GPIO5		GPIO4		GPIO3		GPIO2		GPIO1		GPIO0	
Resistor	R72	R73	R40	R39	R59	R41	R60	R42	R61	R43	R62	R44	R63	R45	R64	R65	R74	R77	R75	R78	R76	R79
stuff		X	X			X	X		X		X		X		X		X		X		X	
no stuff	X			X	X			X		X		X		X		X		X		X		X

PCIe SWITCH

TITLE: iot_shield		
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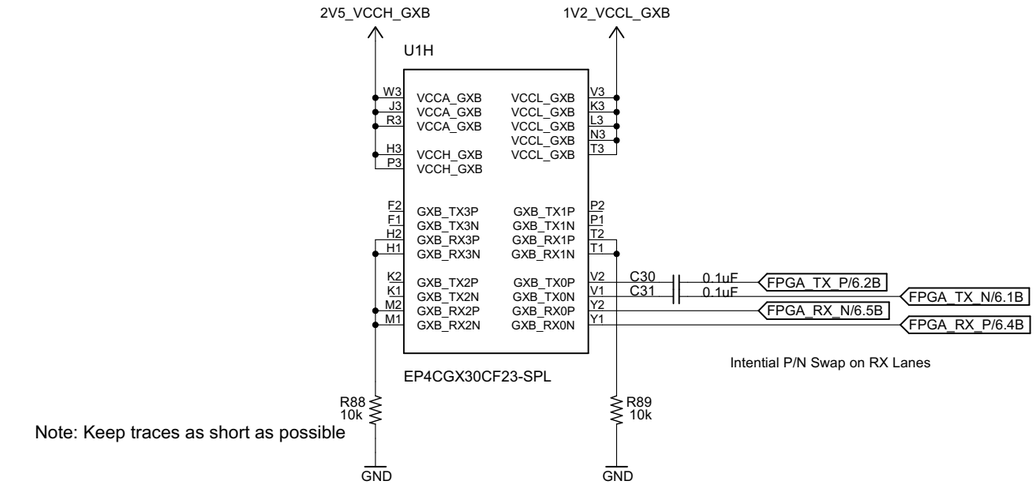

FPGA PCIe CONNECTIONS

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.04
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Codec

U5

TLV320AIC3100IRHBR

3V3 3V3

R108 2.7k
R109 2.7k
R111 10k

5V0 3V3 1V8

C115 0.1uF
C123 10uF
C124 0.1uF
C125 0.1uF
C140 100uF_1210_6.3V
C126 0.1uF
C127 0.1uF
C128 0.1uF
C129 10uF

GND

CODEC_GPIO1/16.6B

CODEC_DIN/16.6C
CODEC_WCLK/16.6B
CODEC_BCLK/16.6C
CODEC_MCLK/14.6E
CODEC_SDA/16.6C
CODEC_SCL/16.6C
CODEC_RESET#/16.6B

C139 0.1uF

CODEC_DOUT/16.6B

R110 2.2k
R129 2.2k
R130 2.2k

VOL_MICDET

C155 0.47uF
C154 0.47uF

Speaker Output

L2 MPZ1608S221A
L3 MPZ1608S221A
L4 MPZ1608S221A
L5 MPZ1608S221A

SPKP_R
SPKM_R
SPKP_L
SPKM_L

no stuff R100 0
no stuff R101 0

ED555/4DS
J9

Headphone Jack

C136 47uF
C137 47uF

HP_L
HP_R
HP_DET

J10
SJ-43516-SMT

GND

Microphone Jack

J17
SJ-43516-SMT

MIC1LP
MIC1RP

GND

Volume Control (optional)

0 R102

no stuff 0 R103

3V3

R105 48.7k
R270 3361S-1-503GLF
R104 0

C138 0.22uF

VOL

no stuff

GND

AUDIO

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.04
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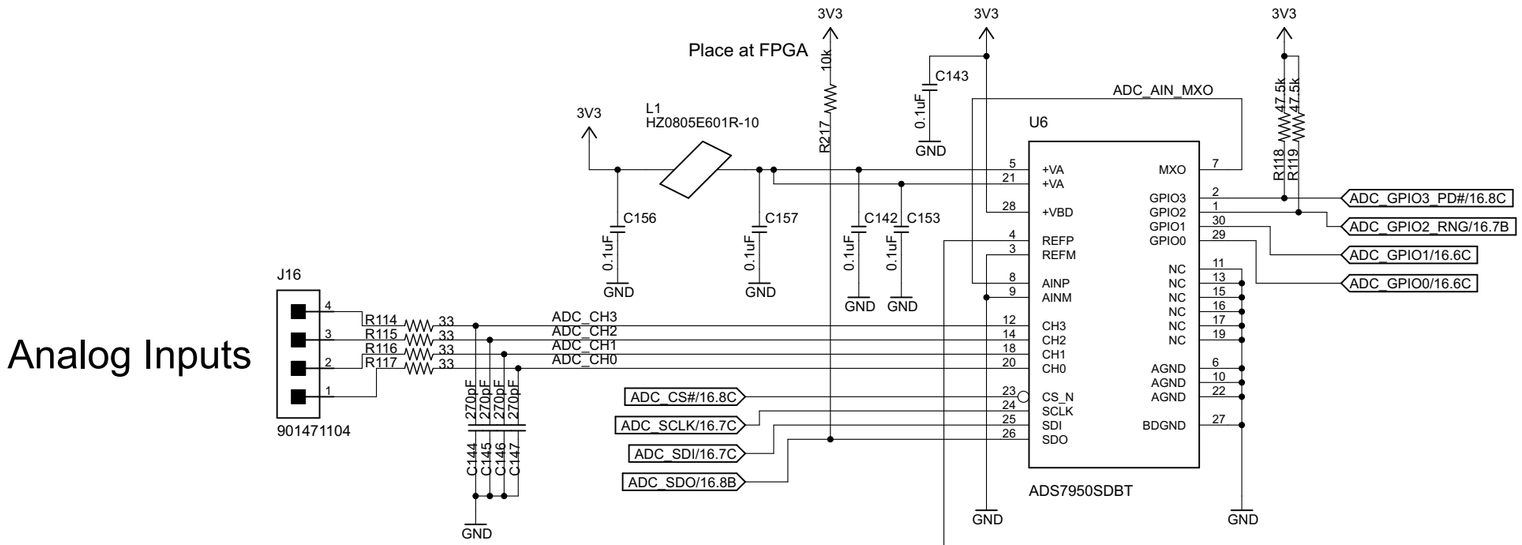
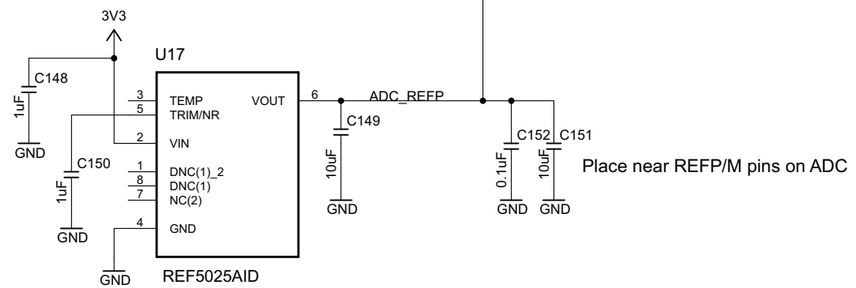
A/D Converter (ADC)



2.5V Reference



ADC

TITLE: iot_shield		
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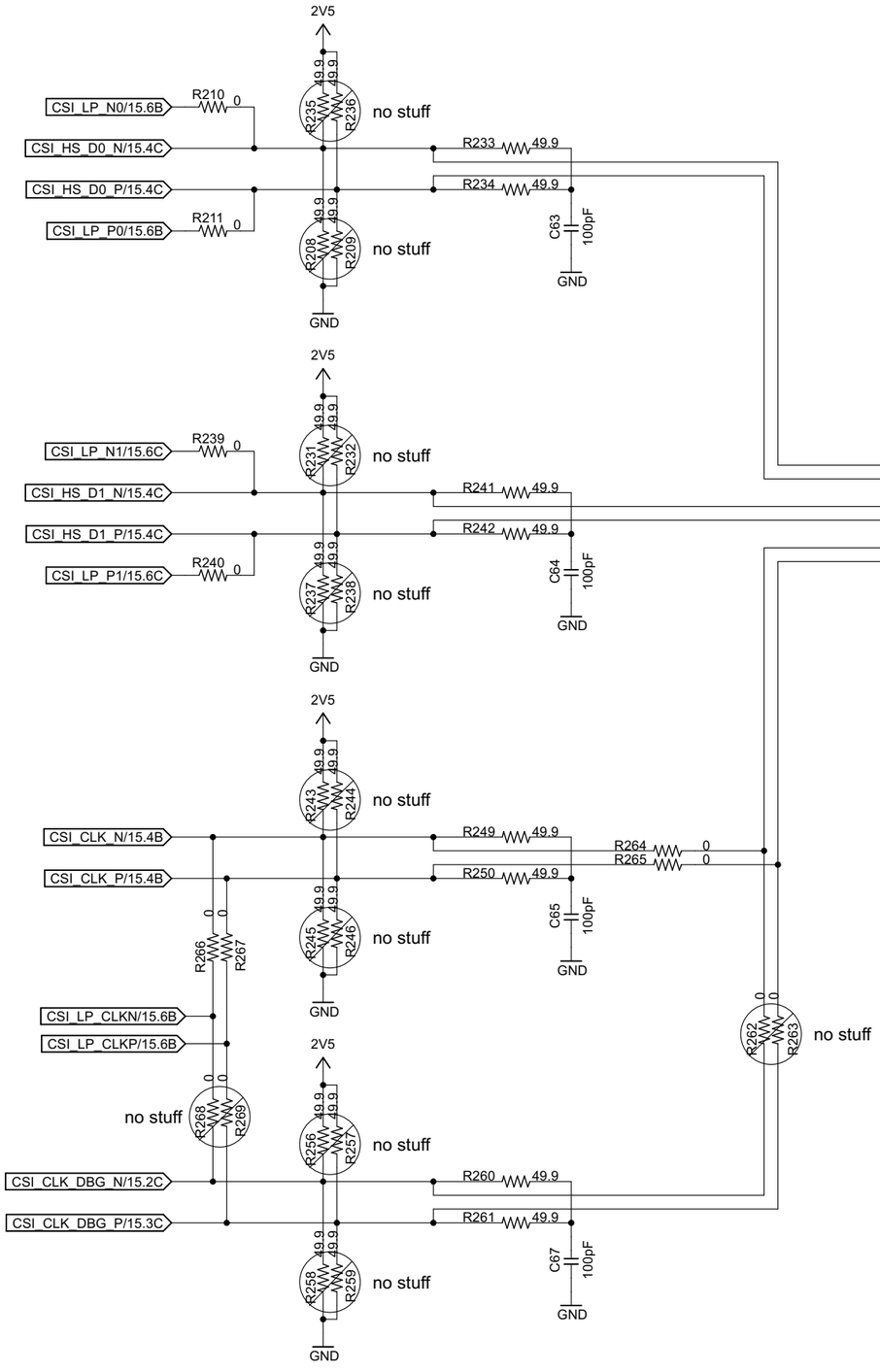
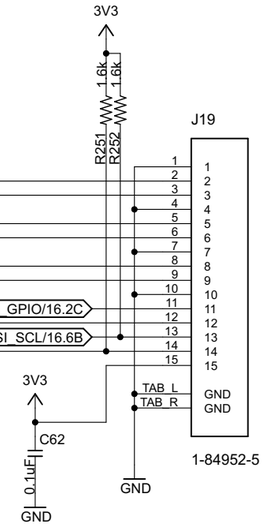


MIPI CSI-2 Connector



MIPI

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.04
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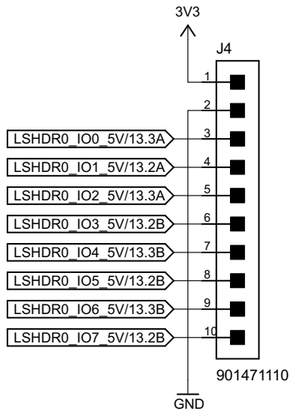
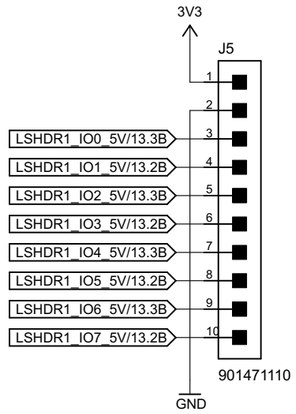
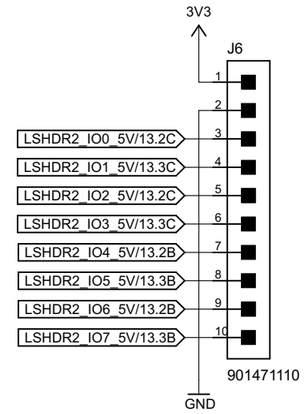
Low-Speed IO Header 0



Low-Speed IO Header 1

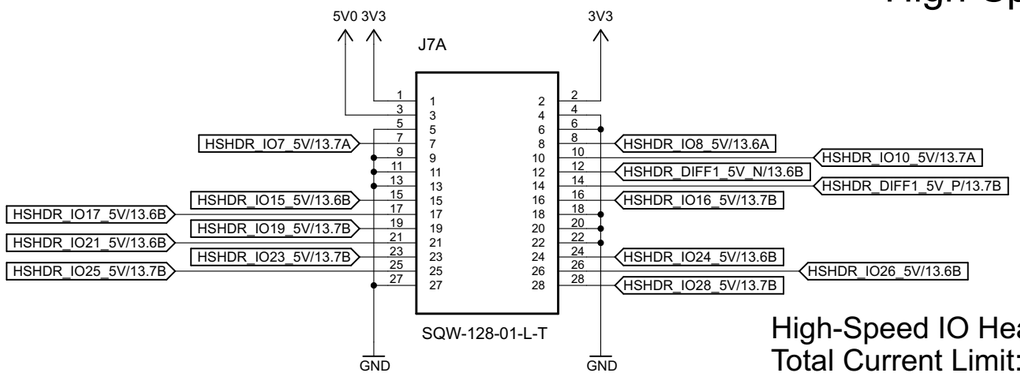


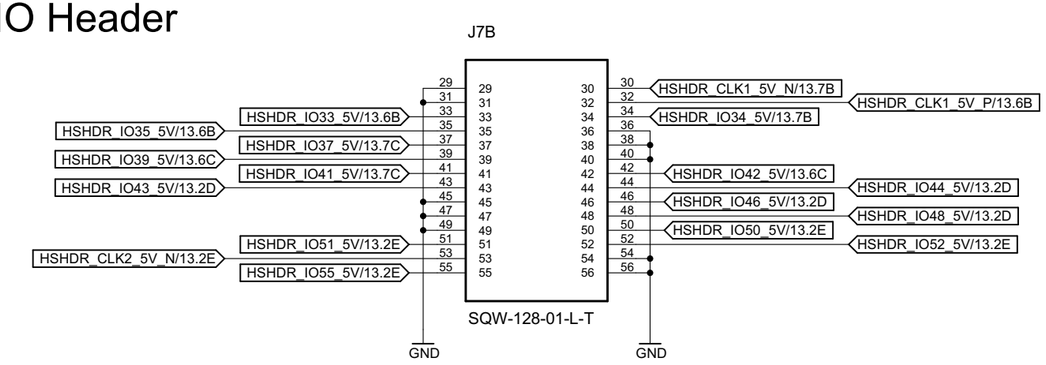
Low-Speed IO Header 2



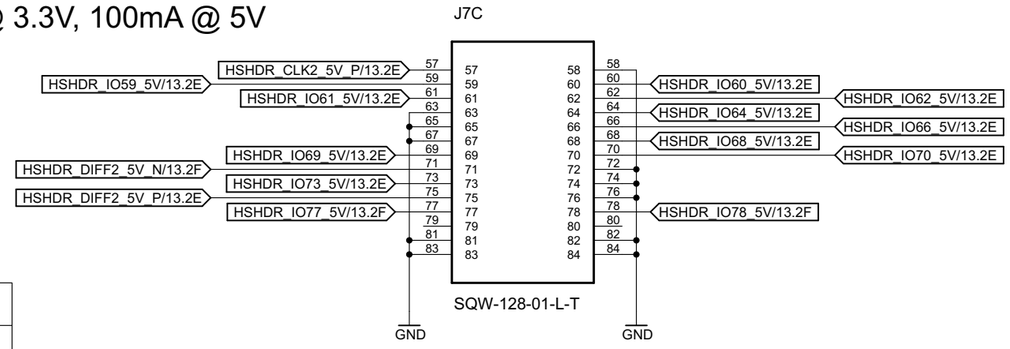
Low-Speed IO Header 0-2
Total Current Limit: 60mA @ 3.3V

High-Speed IO Header





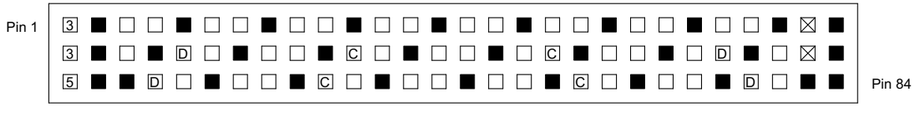
High-Speed IO Header
Total Current Limit: 40mA @ 3.3V, 100mA @ 5V



Low-Speed IO Header Pinout

Note: Use 5V Header (J8, p. 17) for 5V power

High-Speed IO Header Pinout



Note: Clock Pins 30 and 32 are FPGA input; Clock Pins 53 and 57 are FPGA output
Note: All differential and clock pairs are 2.5V

Key

- ☐ Digital IO
- ■ Ground
- 3 3.3V
- 5 5V
- D Differential Pair (+/-)
- C Clock Pair (+/-)
- ☒ No Connect

IO HEADERS

TITLE: iot_shield	
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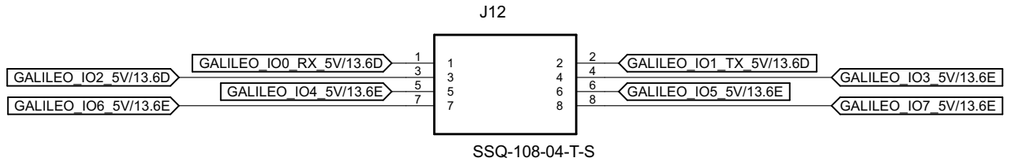
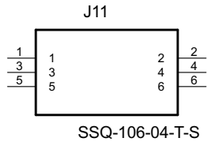
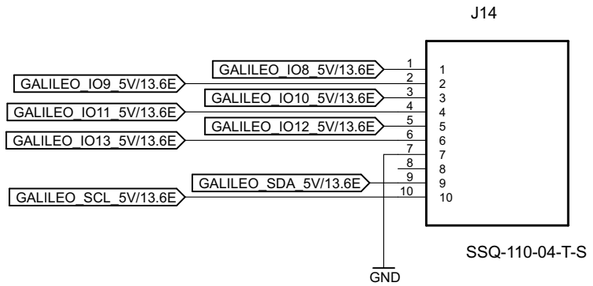
Date: 10/5/2014 11:06:41 PM	Sheet: 11/22

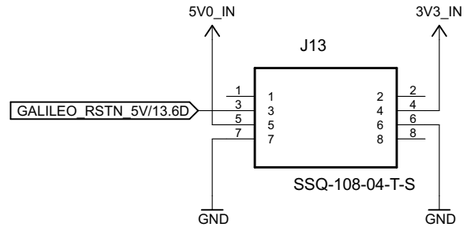
Note: Pin numbers match Galileo schematics



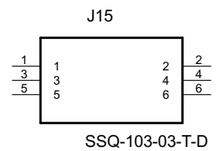


Analog input pins not connected to shield

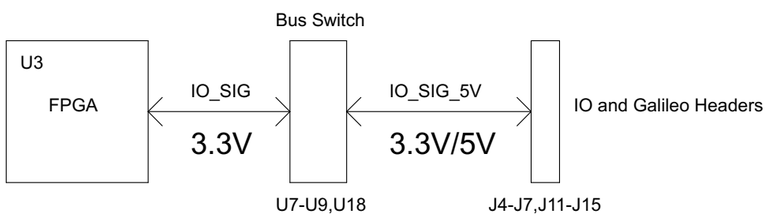




ICSP pins not connected to shield



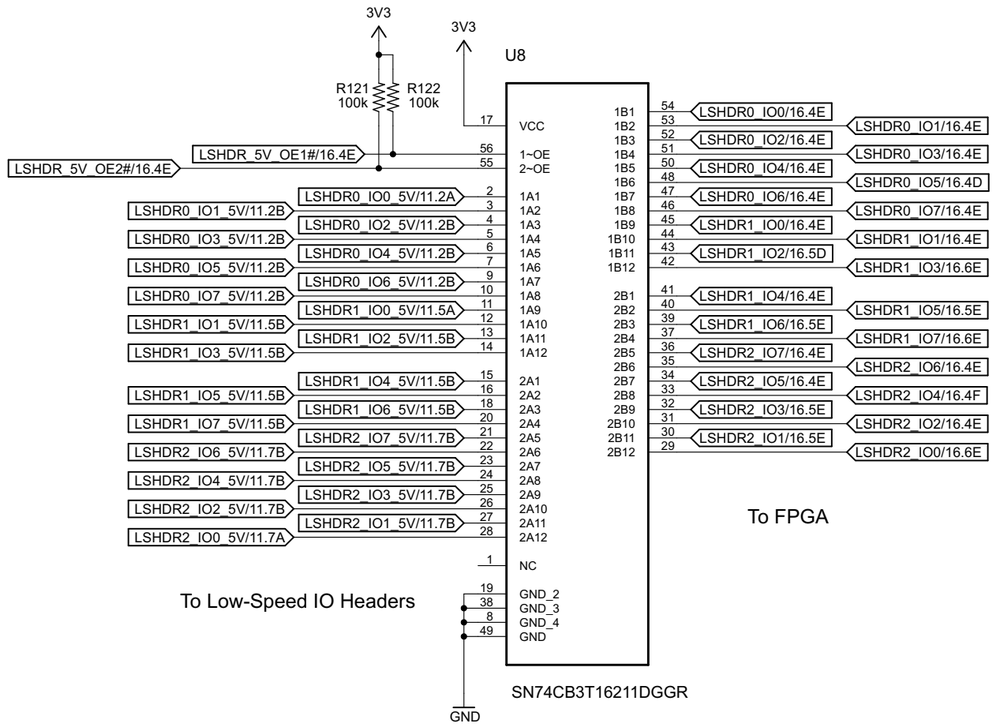
IO Signal Flow

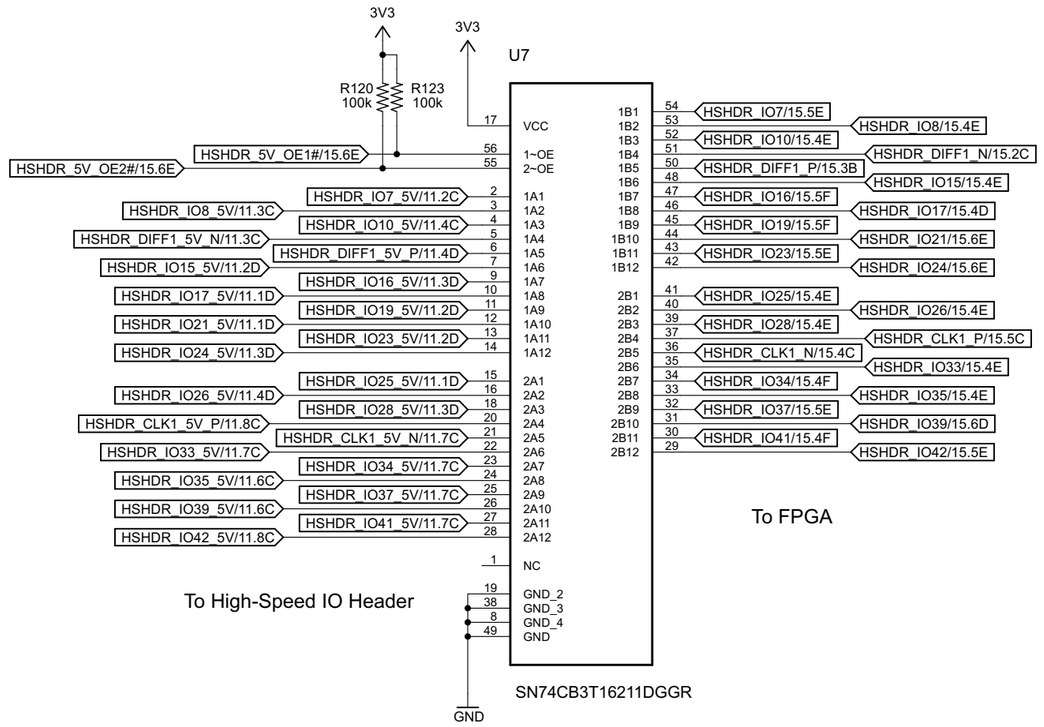


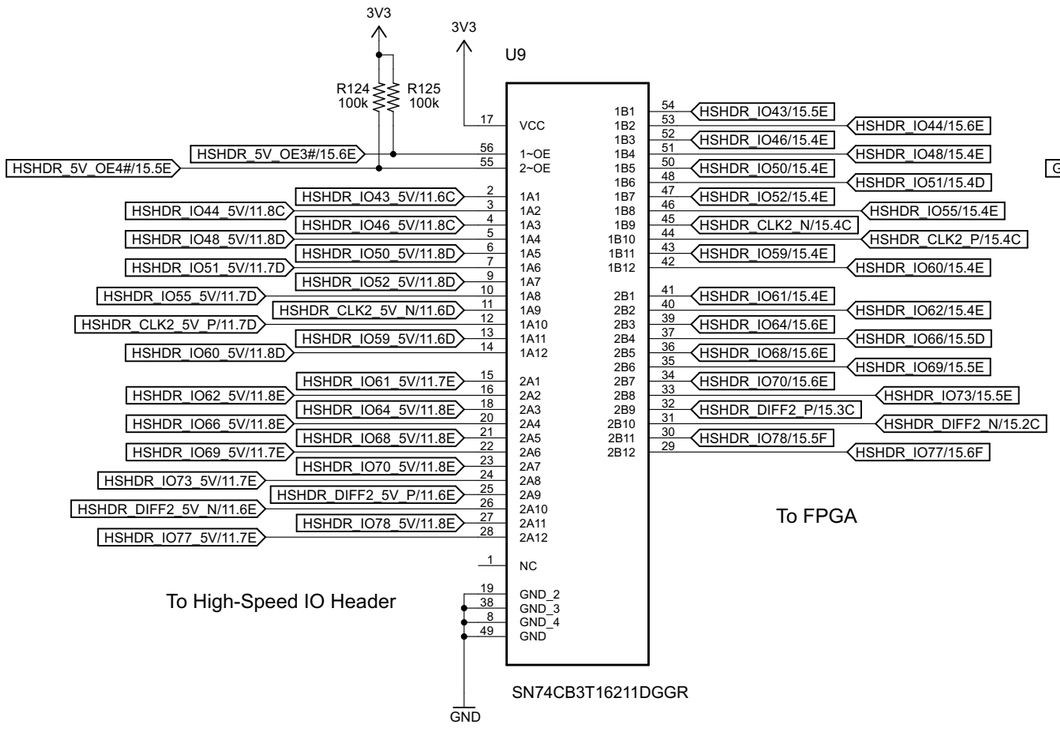
Note: '_5V' are Galileo/IO header signals and are 5V-tolerant.
Signals without '_5V' are 3.3V FPGA IOs (not 5V tolerant).

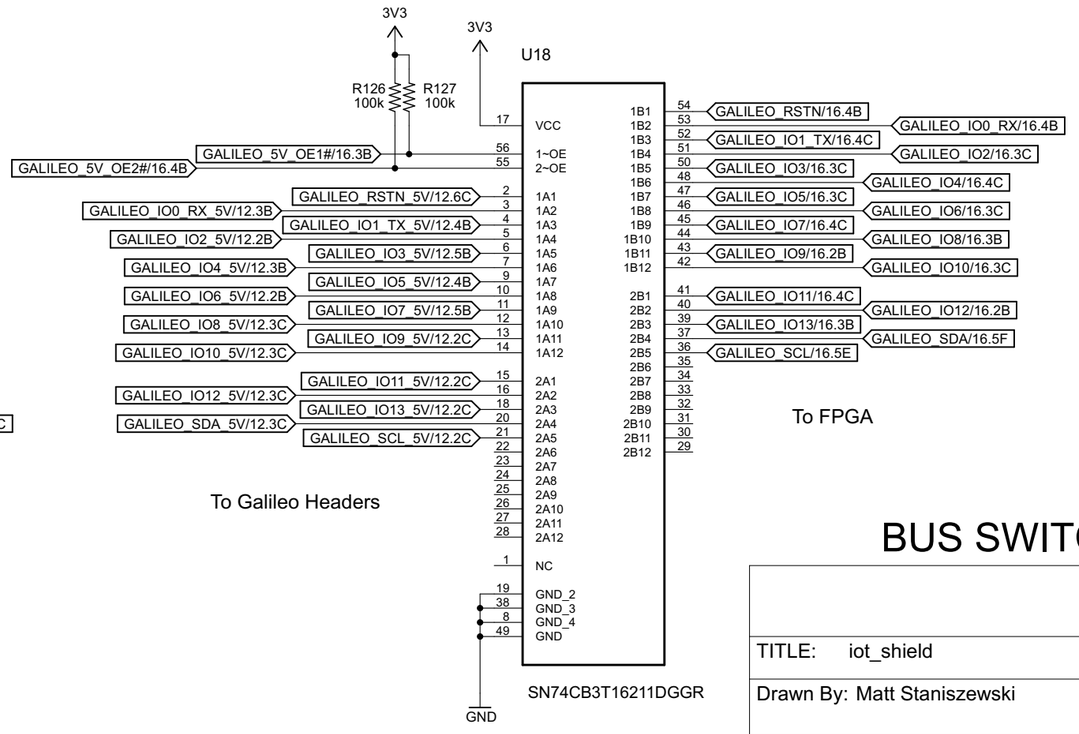
GALILEO HEADERS

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.04
Date: 10/5/2014 11:06:41 PM	Sheet: 12/22





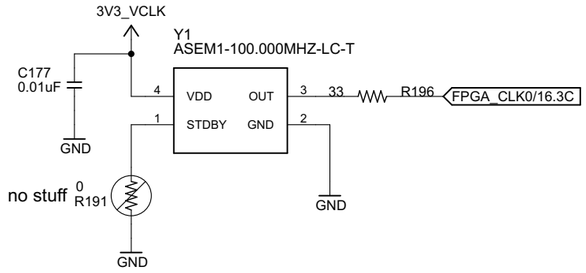




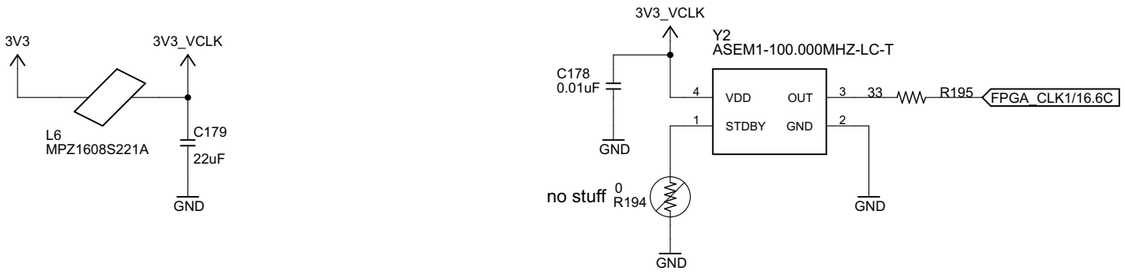
BUS SWITCHES

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.04
Date: 10/5/2014 11:06:41 PM	Sheet: 13/22	

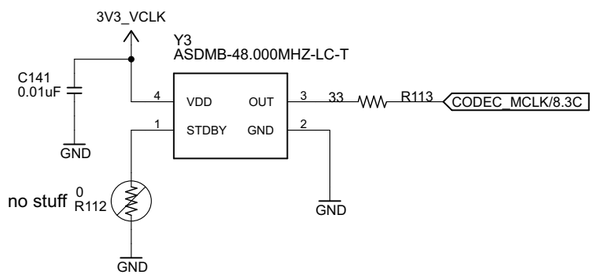
100MHz CMOS Oscillator



100MHz CMOS Oscillator



48MHz CMOS Oscillator

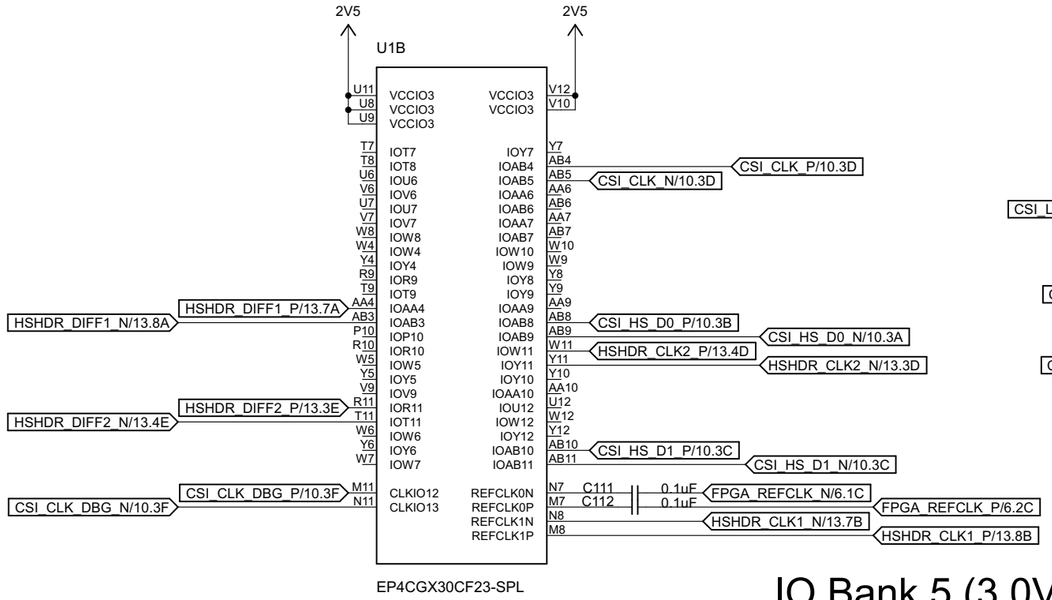


CLOCKS

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.04
Date: 10/5/2014 11:06:41 PM	Sheet: 14/22

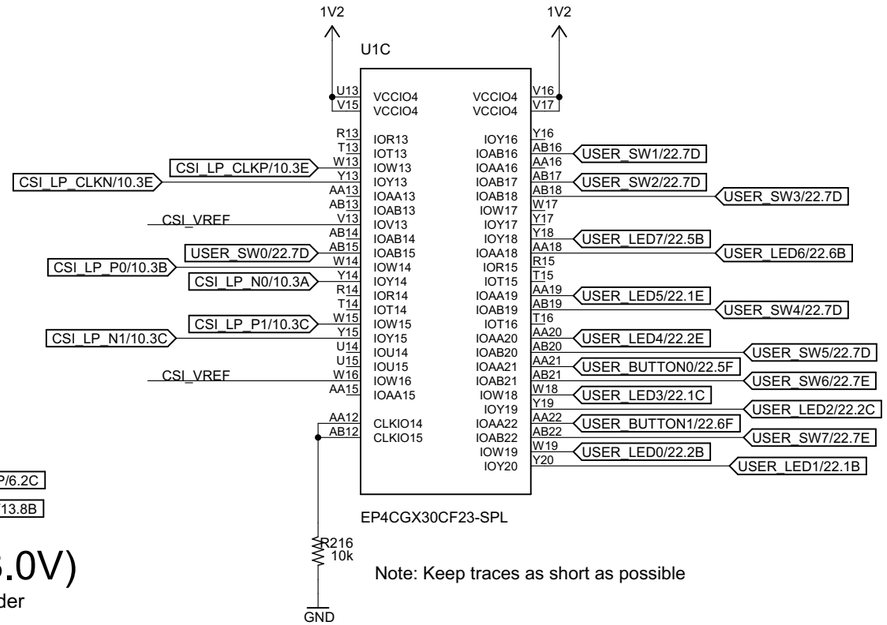
IO Bank 3 (2.5V)

MIPI/Clock/High-Speed IO Header



IO Bank 4 (1.2V)

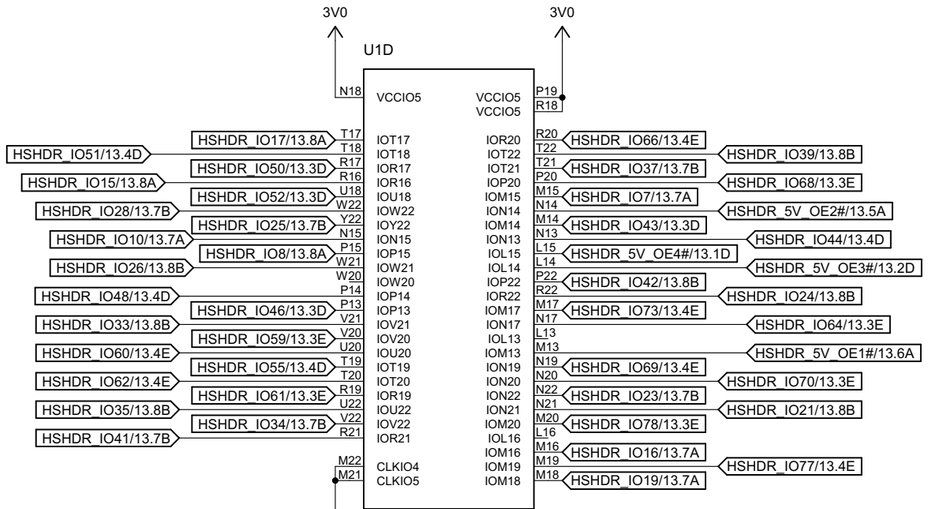
MIPI/LEDs/Buttons/Switches



Note: Keep traces as short as possible

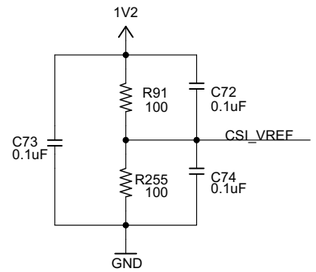
IO Bank 5 (3.0V)

High-Speed IO Header



Note: Keep traces as short as possible

Note: 3.0V IO Banks are compatible with 3.3V signaling

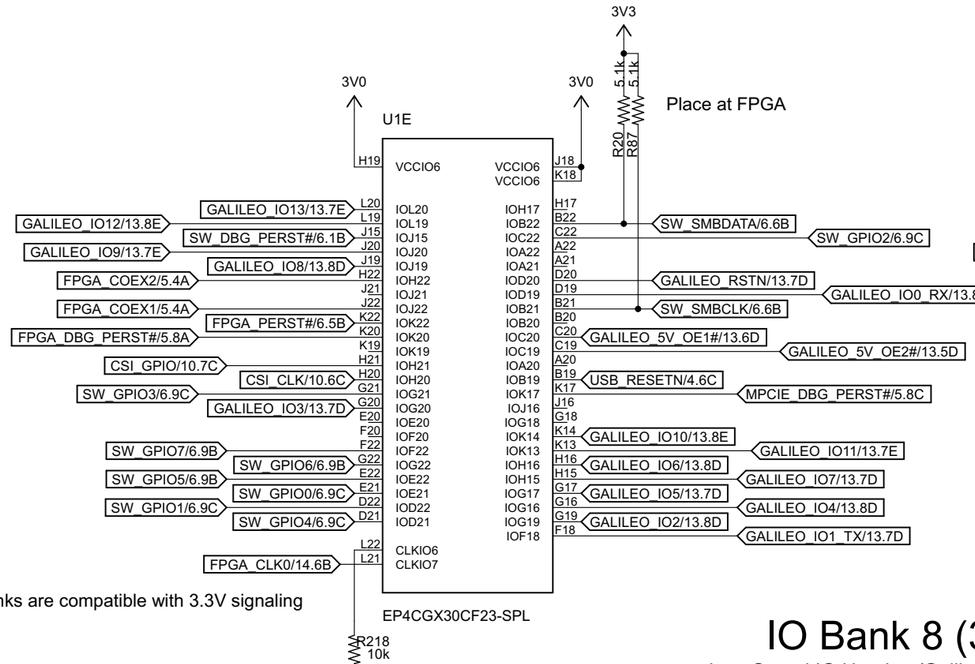


FPGA IO BANK 3 / 4 / 5

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.04
Date: 10/5/2014 11:06:41 PM	Sheet: 15/22

IO Bank 6 (3.0V)

PCIe/Switch/Galileo IOs/Clock

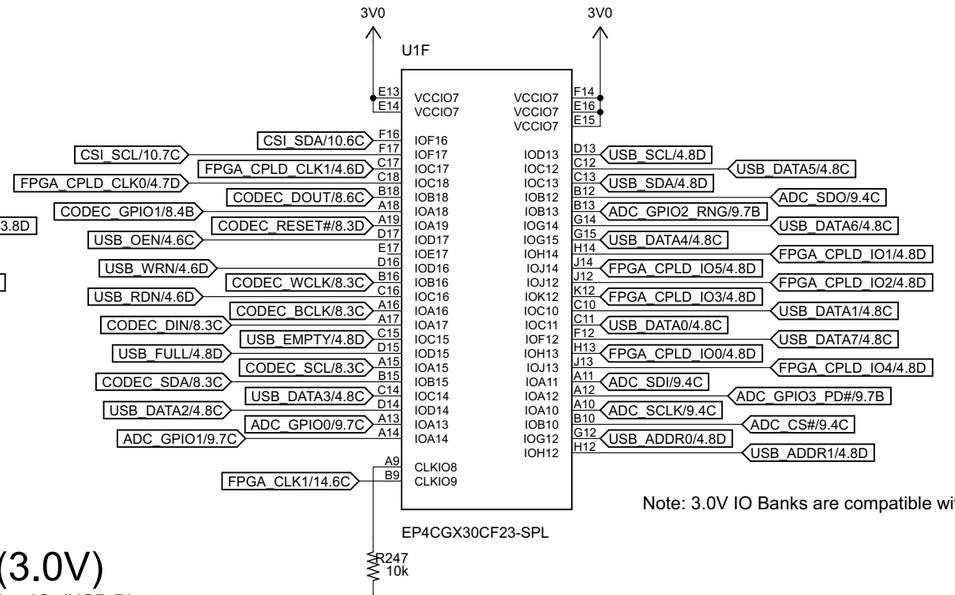


Note: 3.0V IO Banks are compatible with 3.3V signaling

Note: Keep traces as short as possible

IO Bank 7 (3.0V)

Codec/ADC/Clock/USB Blaster

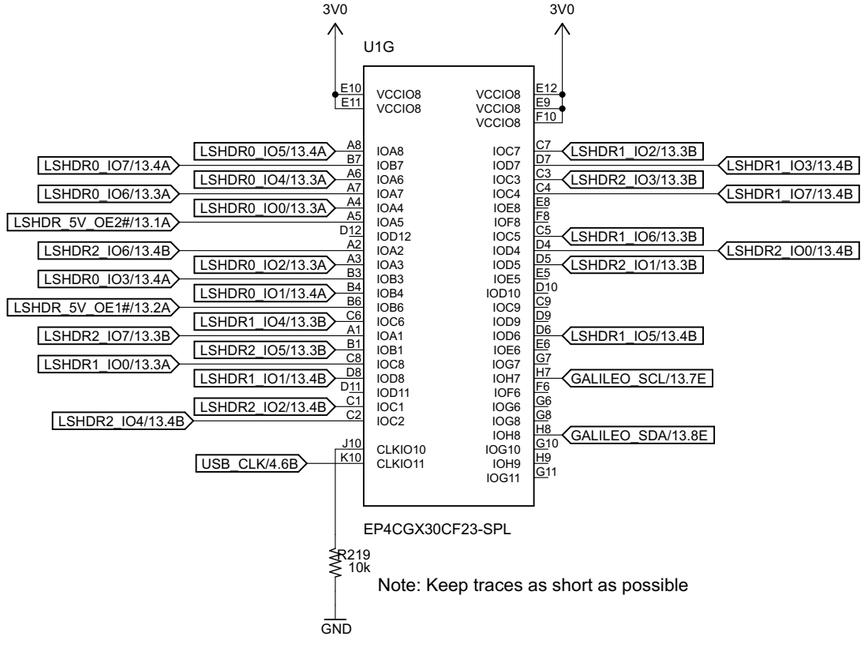


Note: 3.0V IO Banks are compatible with 3.3V signaling

Note: Keep traces as short as possible

IO Bank 8 (3.0V)

Low-Speed IO Headers/Galileo IOs/USB Blaster



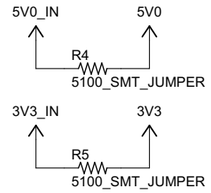
Note: 3.0V IO Banks are compatible with 3.3V signaling

Note: Keep traces as short as possible

FPGA IO BANK 6 / 7 / 8

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.04
Date: 10/5/2014 11:06:41 PM	Sheet: 16/22	

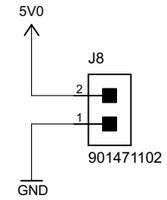
POWER IN JUMPERS



Metal jumpers; Place at least 75mil apart

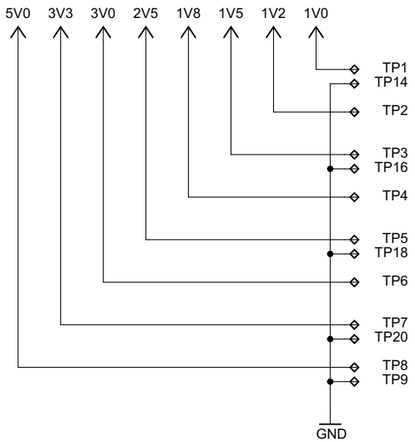
5V HEADER

Use 5V Header (J8) to supply 5V power to devices



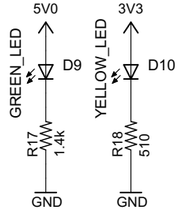
5V Header Total Current Limit: 100mA @ 5V

POWER PROBE TESTPOINTS

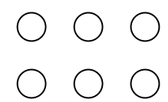


Place ground testpoint next to each rail testpoint
(except where a common ground pad can be shared)

POWER LEDs



BOARD FIDUCIALS



Note: Shield power limits assume all header current limits are used and a Mini-PCIe Gen1 card (i.e. Wi-Fi) is connected.

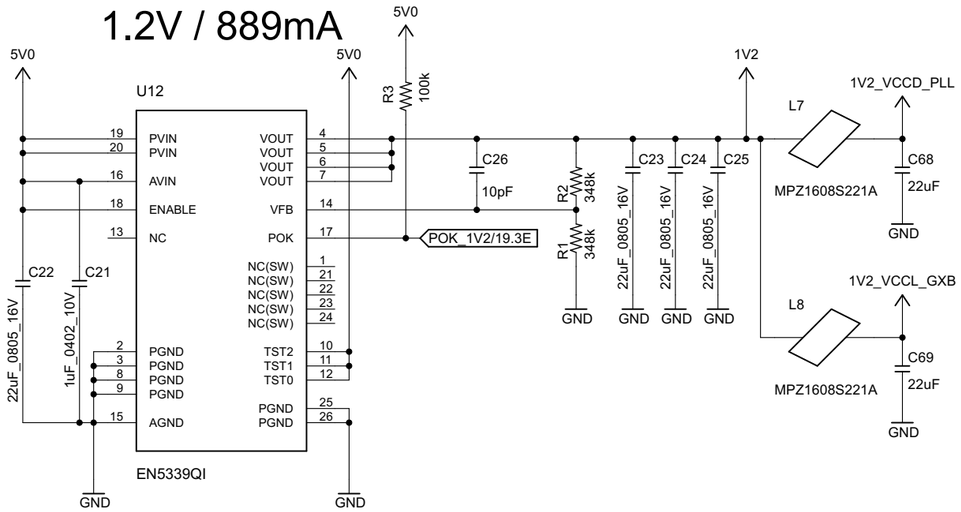
It is assumed that additional shields or USB devices are not connected to the Galileo; please use at your own risk.

POWER IN

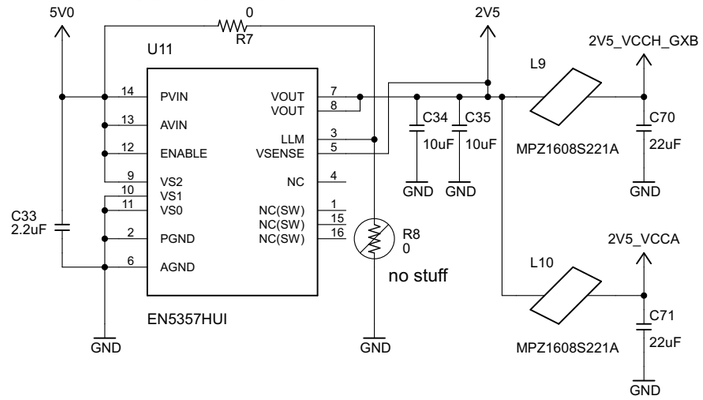
TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.04
Date: 10/5/2014 11:06:41 PM	Sheet: 17/22	

1.2V / 889mA

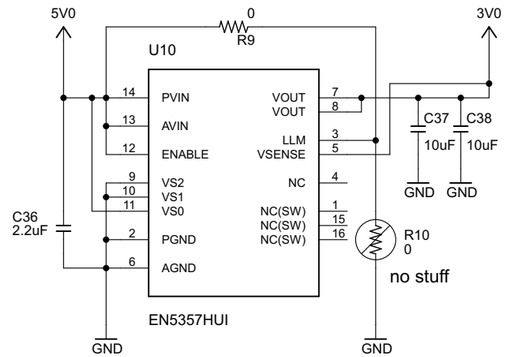
Place C21 as close to AVIN as possible



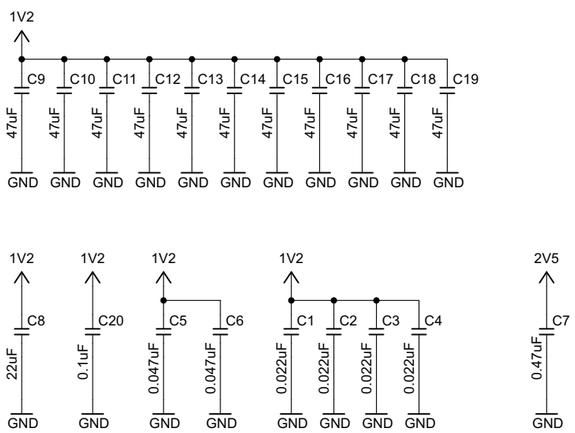
2.5V / 133mA



3.0V / 7mA



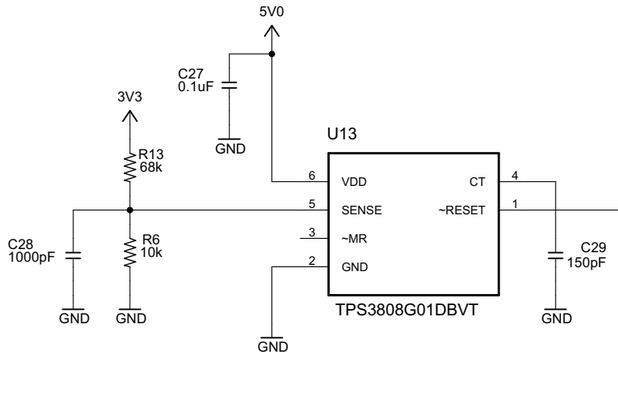
FPGA Decoupling



FPGA VREGS / DECOUPLING

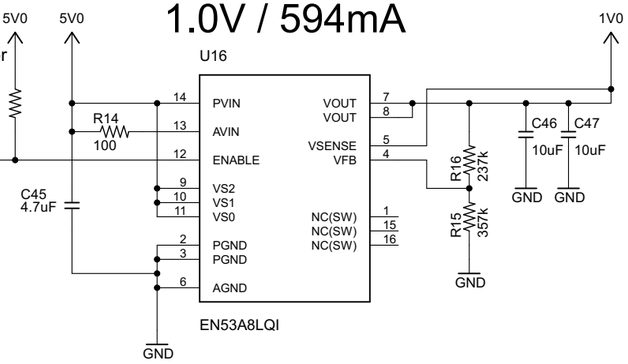
TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.04
Date: 10/5/2014 11:06:41 PM	Sheet: 18/22

Supervisor (1.0V POK)



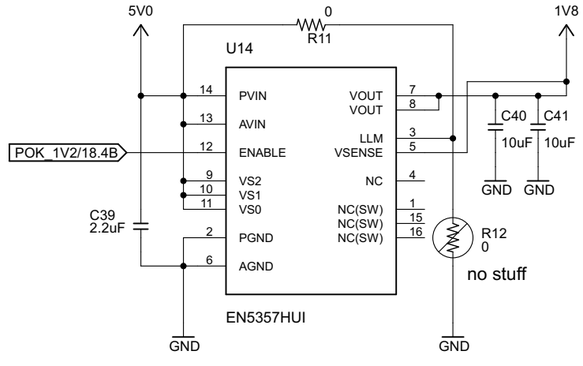
Place pull-up resistor near input at regulator

EN_1V0



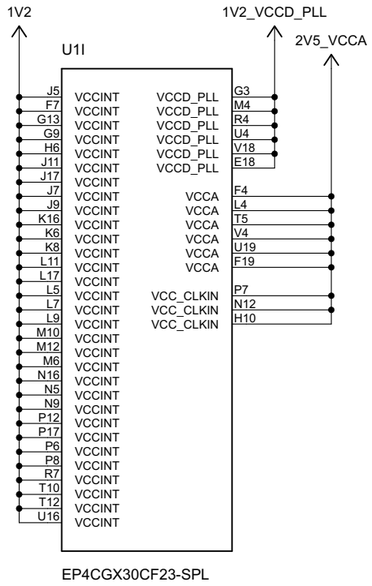
1.0V / 594mA

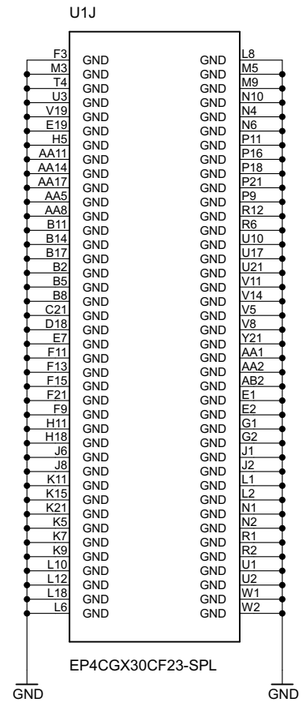
1.8V / 10mA



SYSTEM VREGS

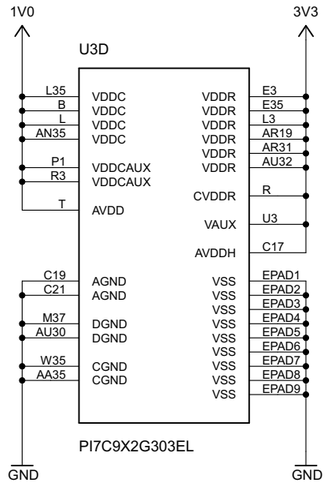
TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.04
Date: 10/5/2014 11:06:41 PM	Sheet: 19/22

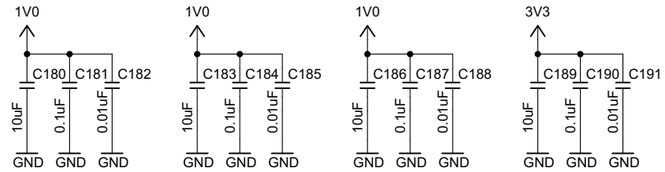




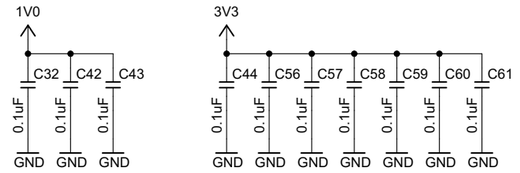
FPGA PWR / GND

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.04
Date: 10/5/2014 11:06:41 PM	Sheet: 20/22





Place groupings at each power pad (T, B, L, R)

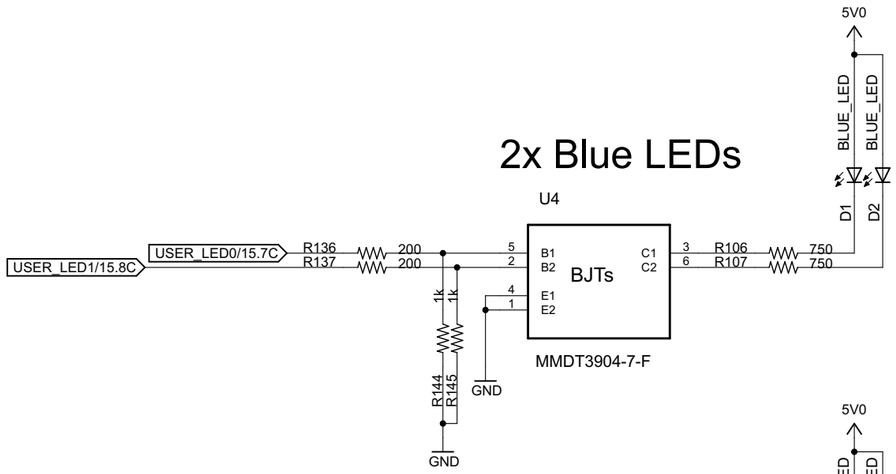


Place common capacitor between near pads with same voltage

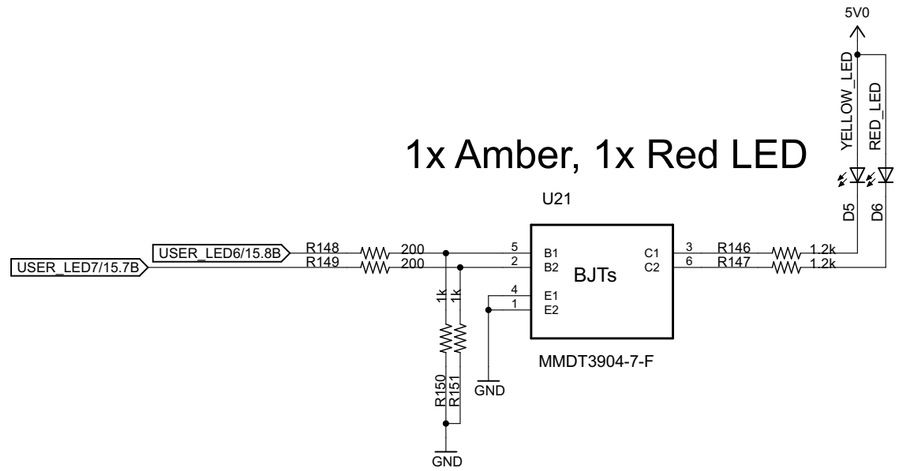
SW PWR / GND / DECOUPLING

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.04
Date: 10/5/2014 11:06:41 PM	Sheet: 21/22

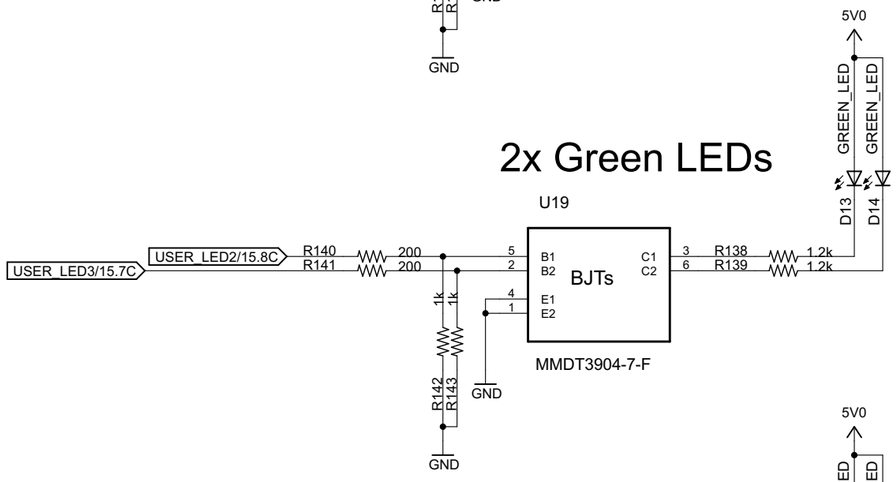
2x Blue LEDs



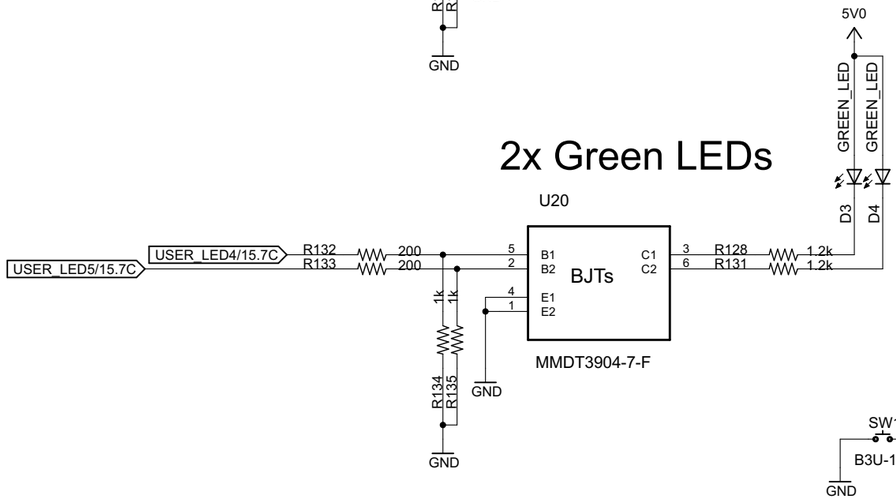
1x Amber, 1x Red LED



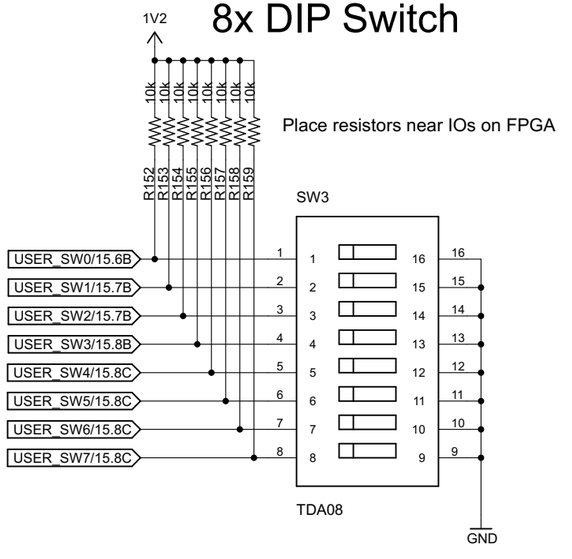
2x Green LEDs



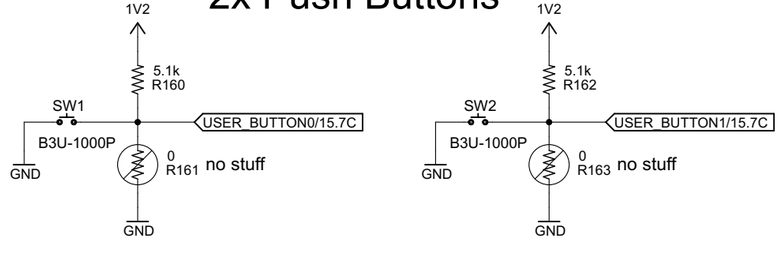
2x Green LEDs



8x DIP Switch



2x Push Buttons



LEDS / BUTTONS / SWITCHES

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.04
Date: 10/5/2014 11:06:41 PM	Sheet: 22/22	