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TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.02
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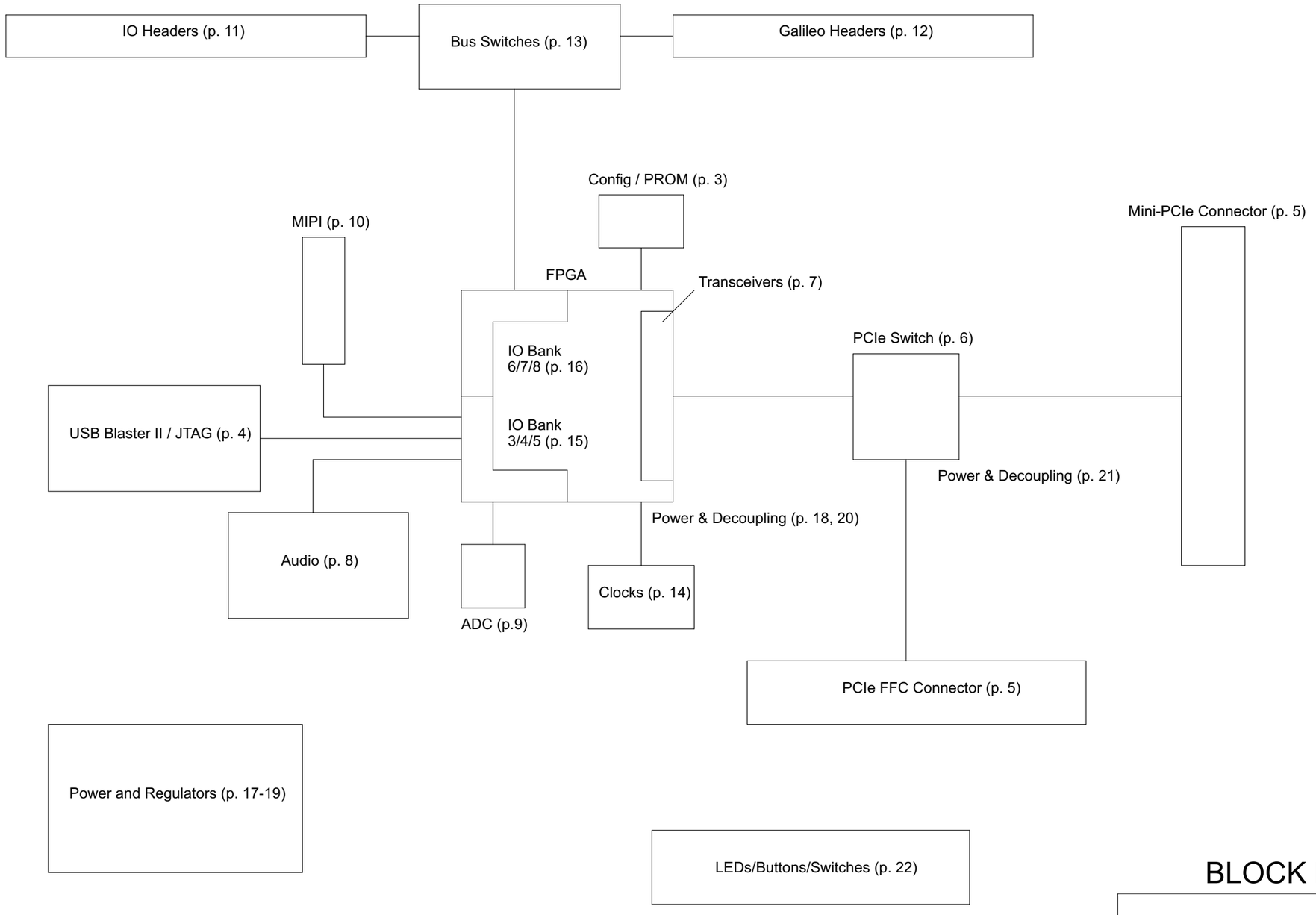

BLOCK DIAGRAM

TITLE: iot_shield		
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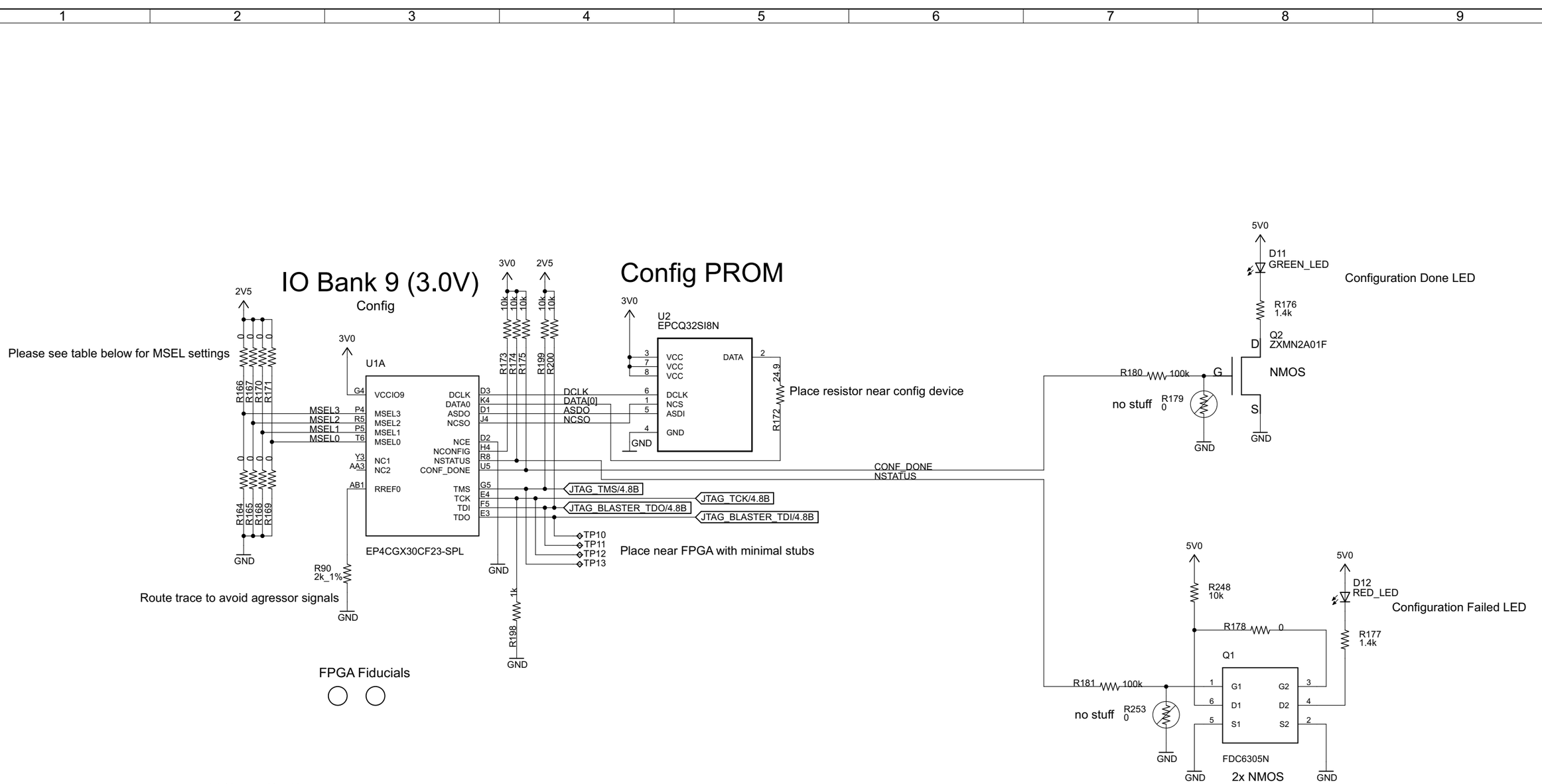

MSEL Settings

Function	MSEL3		MSEL2		MSEL1		MSEL0	
Resistor	R166	R164	R167	R165	R170	R168	R171	R169
stuff	X			X	X		X	
no stuff		X	X			X		X

Current configuration: AS x1 Mode, Fast POR

FPGA CONFIG / JTAG

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Micro USB

J20
10118194-0001LF

Route high-speed USB signals carefully

VBUS_5V
FX2_D_N
FX2_D_P
R186 0
no stuff
GND

SH1 SH2 SH3 SH4 SH5 SH6
CH_GND

R185
1M
CH_GND
C160
4700pF
GND

U22
ESD
D+
D-
GND
TPD2EUSB30DR
GND

R193 10k

Crystal
Y4
24MHz
GND
C158
12pF
C159
12pF
GND GND GND

3V3
C66
0.1uF
GND

Place on USB peninsula for J20

FX2_SDA R188 0 MAX_SDA

MAX811SEUS+T
GND MR#
RESET# VCC
R187 100k FX2_RESETN
GND
3V3
C161
0.1uF
GND
Voltage Monitor
U23

USB Controller

3V3
R189 2k
R190 2k

U24
VCC
RESET
WAKEUP
XTALIN
XTALOUT
CLKOUT/T1OUT
RDY0/SLRD
RDY1/SLRW
IFCLK/T0OUT
RESEVED
SCL
SDA
DPLUS
DMINUS
AVCC
AVCC
AGND
AGND
GND

PB0/FD0
PB1/FD1
PB2/FD2
PB3/FD3
PB4/FD4
PB5/FD5
PB6/FD6
PB7/FD7
PD0/FD8
PD1/FD9
PD2/FD10
PD3/FD11
PD4/FD12
PD5/FD13
PD6/FD14
PD7/FD15
PA0/INT0
PA1/INT1
PA2/SLOE
PA3/WU2
PA4/FIFOADR0
PA5/FIFOADR1
PA6/PKTEND
PA7/FLAGD/SLCS
CTL0/FLAGA
CTL1/FLAGB
CTL2/FLAGC

FX2_RESETN
FX2_WAKEUP
24M_XTALIN
24M_XTALOUT
FX2_SLRDN
FX2_SLWRN
USB_CLK
R215 33
FX2_SCL
FX2_SDA

20k R192
C162 0.1uF
GND GND

CY7C68013A-56PVXC

3V3
C169 C170 C171 C172 C173 C174 C175 C176
0.1uF
GND

Place near CY7C68013A

JTAG Header

3V3
J18
C_USB_MAX_TCK
C_USB_MAX_TDO
C_USB_MAX_TMS
C_USB_MAX_TDI
R182 1k
R183 1k
R184 1k
GND GND
CLP-107-02-F-D-K

CPLD

3V3
R201 1k

U15A
EPM570GT100

FX2_PA2
FX2_FLAGC
FX2_PA7
FX2_FLAGA
FX2_PA3
FX2_PA4
FX2_PB4
FX2_PA6
FX2_PB2
FX2_FLAGB
FX2_PB0
FX2_PA1
FX2_PB5
USB_DISABLEN
USB_CLK/16.4F
FX2_PB7
MAX_SDA
FX2_RESETN

IOB1_1 IOB1_2 IOB1_3 IOB1_4 IOB1_5 IOB1_6 IOB1_7 IOB1_8
IOB1_9 IOB1_10 IOB1_11 IOB1_12 IOB1_13 IOB1_14 IOB1_15 IOB1_16
IOB1/GCLK0
IOB1/GCLK1
IOB1/DEV_OE
IOB1/DEV_CLRN
IOB1_17 IOB1_18 IOB1_19 IOB1_20 IOB1_21 IOB1_22 IOB1_23 IOB1_24
IOB1_25 IOB1_26 IOB1_27 IOB1_28 IOB1_29 IOB1_30 IOB1_31 IOB1_32
TMS
TDI
TCK
TDO

FX2_PB6
FX2_PB1
FX2_PB3
FX2_SCL
FX2_PD6
FX2_PD4
FX2_SLWRN
JTAG_TCK/3.5C
FX2_SLRDN
FX2_PD7
FX2_PD5
FX2_PA5
JTAG_BLASTER_TDO/3.4C
JTAG_TMS/3.4C
JTAG_BLASTER_TDI/3.5C
C_USB_MAX_TMS R203 0 FX2_PD1
C_USB_MAX_TDI R204 0 FX2_PD2
C_USB_MAX_TCK R205 0 FX2_PD0
C_USB_MAX_TDO R206 0 FX2_PD3

CPLD Fiducials

3V3
R212 1k
R197 1k
R213 1k
R214 1k

U15B
EPM570GT100

JTAG_TX
SC_RX
SC_TX
JTAG_RX
USB_RESETN/16.7C
USB_RESETN
USB_OEN/16.8C
USB_OEN
USB_RDN/16.7C
USB_RDN
USB_WRN/16.8C
USB_WRN
R207 0 M570_PCIE_JTAG_EN
GND
FPGA_CPLD_CLK1/16.5E
FPGA_CPLD_CLK0/16.5E

IOB2_1 IOB2_2 IOB2_3 IOB2_4 IOB2_5 IOB2_6 IOB2_7 IOB2_8
IOB2_9 IOB2_10 IOB2_11 IOB2_12 IOB2_13 IOB2_14 IOB2_15 IOB2_16
IOB2/GCLK2
IOB2/GCLK3
IOB2_17 IOB2_18 IOB2_19 IOB2_20 IOB2_21 IOB2_22 IOB2_23 IOB2_24
IOB2_25 IOB2_26 IOB2_27 IOB2_28 IOB2_29 IOB2_30 IOB2_31 IOB2_32
IOB2_33 IOB2_34 IOB2_35 IOB2_36 IOB2_37 IOB2_38

USB_DATA0/16.8B
USB_DATA1/16.7B
USB_DATA2/16.8B
USB_DATA3/16.7B
USB_DATA4/16.8B
USB_DATA5/16.7B
USB_DATA6/16.6C
USB_DATA7/16.6C
USB_ADDR0/16.8B
USB_ADDR1/16.7B
USB_FULL/16.7B
USB_EMPTY/16.8B
USB_SCL/16.7C
USB_SDA/16.8C
FPGA_CPLD_IO0/16.7C
FPGA_CPLD_IO1/16.8C
FPGA_CPLD_IO2/16.7C
FPGA_CPLD_IO3/16.8C
FPGA_CPLD_IO4/16.7C
FPGA_CPLD_IO5/16.8C

USB Blaster Status LEDs

5V0
GREEN_LED
GREEN_LED
D17
D18

U25
JTAG_RX R221 200
JTAG_TX R222 200
B1 B2 E1 E2 C1 C2
BJTs
MMDT3904-7-F
R202 1.2k
R220 1.2k
R223 1k
R224 1k
GND

U26
SC_RX R227 200
SC_TX R228 200
B1 B2 E1 E2 C1 C2
BJTs
MMDT3904-7-F
R225 1.2k
R226 1.2k
D19
D20
R229 1k
R230 1k
GND

U15C
EPM570GT100
GNDINT
GNDIO
VCCINT
VCCIO1
VCCIO2
1V8 3V3
GND

1V8
3V3
C163 C164
C165 C166 C167 C168
0.1uF
GND

Place near MAX II

USB BLASTER II

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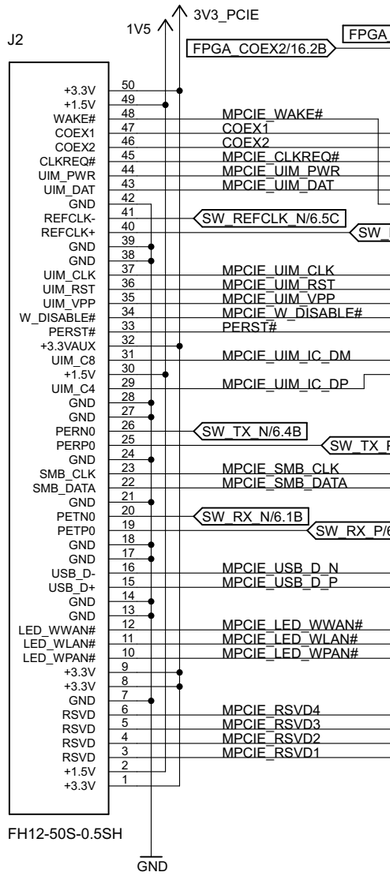
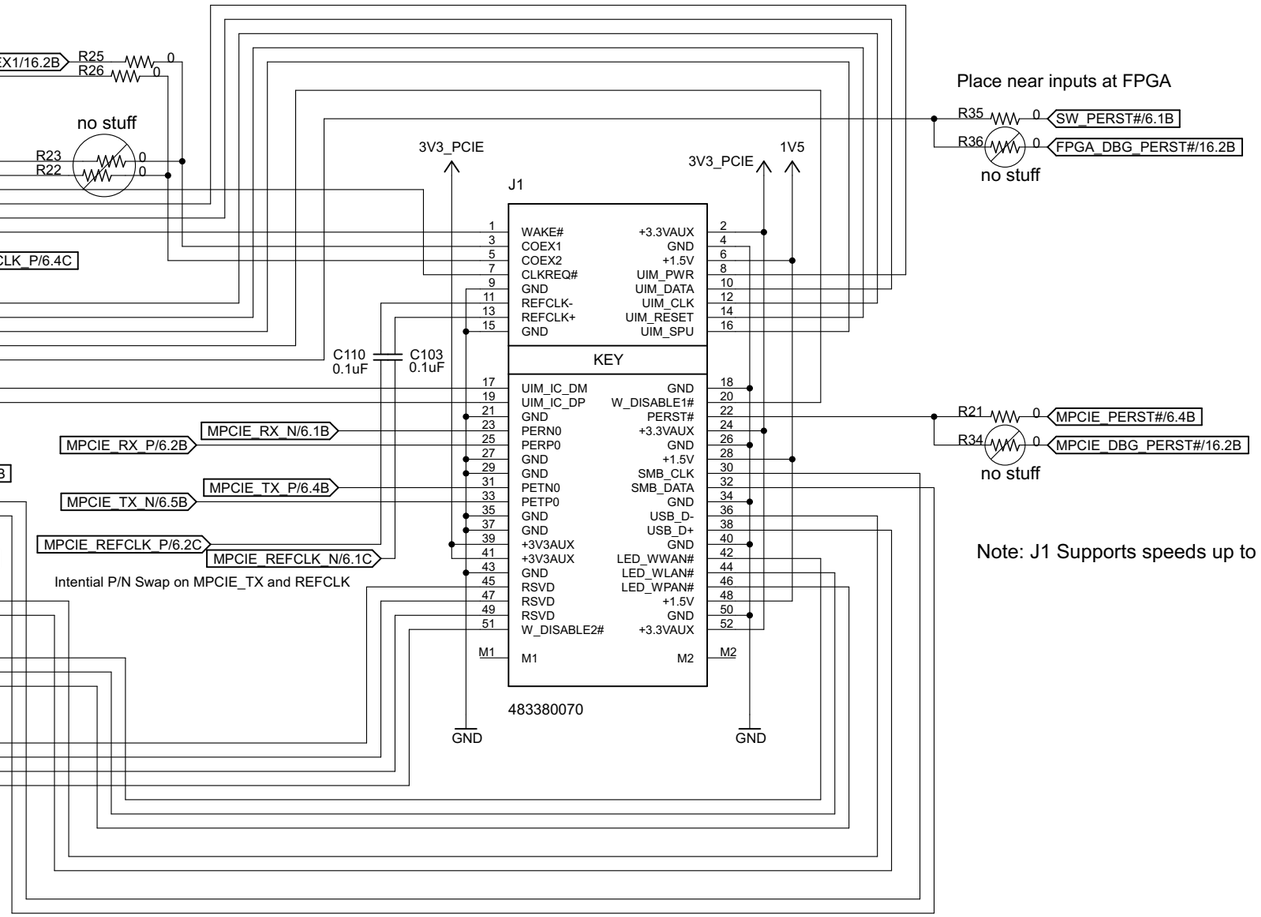
FFC Connector



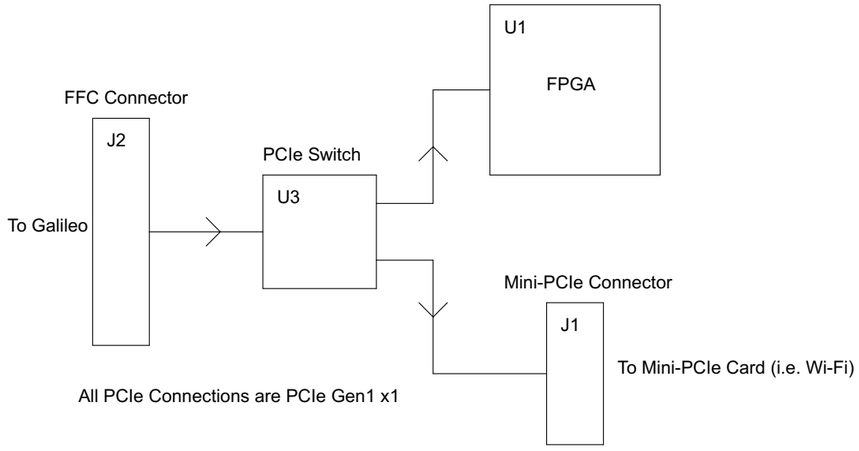
FFC Cable to Galileo

Mini-PCIe Connector



Note: J1 Supports speeds up to Gen1 (2.5Gbps)

PCIe Flow Diagram



PCIe CONNECTORS

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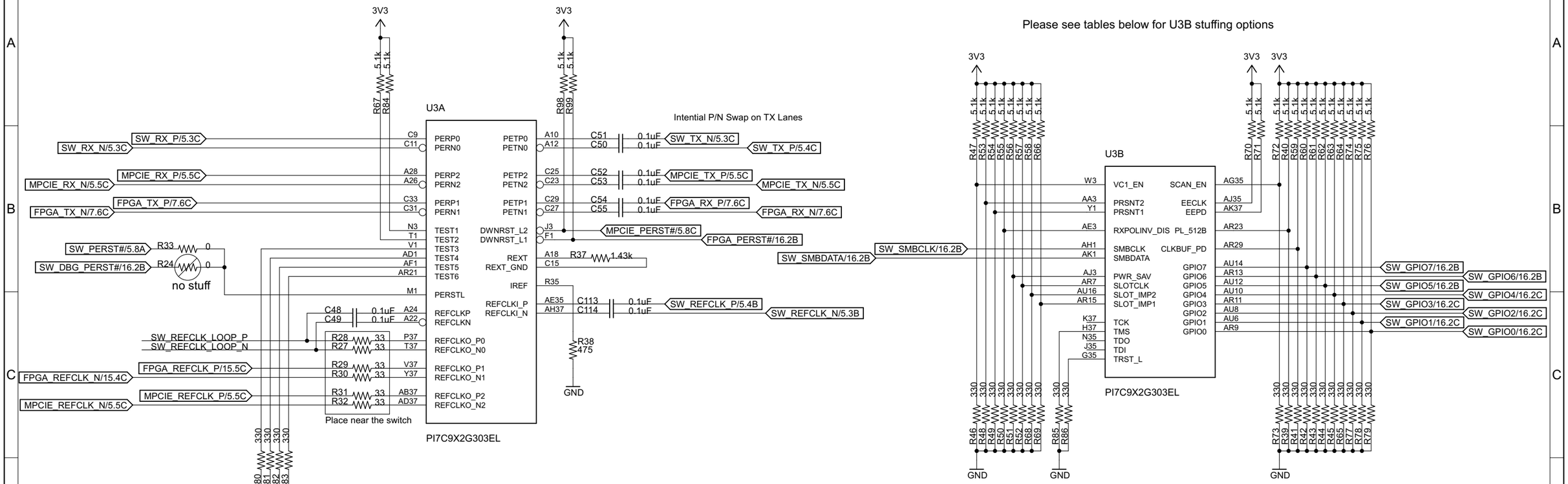

Function	VC1_EN		PRSNT2		PRSNT1		RXPOLINV_DIS		PWR_SAV		SLOTCLK		SLOT_IMP2		SLOT_IMP1	
Resistor	R47	R46	R53	R48	R54	R49	R55	R50	R56	R51	R57	R52	R58	R68	R66	R69
stuff		X		X		X		X	X		X		X		X	
no stuff	X		X		X		X			X		X		X		X

Function	SCAN_EN		PL_512B		CLKBUF_PD		GPIO7		GPIO6		GPIO5		GPIO4		GPIO3		GPIO2		GPIO1		GPIO0	
Resistor	R72	R73	R40	R39	R59	R41	R60	R42	R61	R43	R62	R44	R63	R45	R64	R65	R74	R77	R75	R78	R76	R79
stuff		X	X			X	X		X		X		X		X		X		X		X	
no stuff	X			X	X			X		X		X		X		X		X		X		X

PCIe SWITCH

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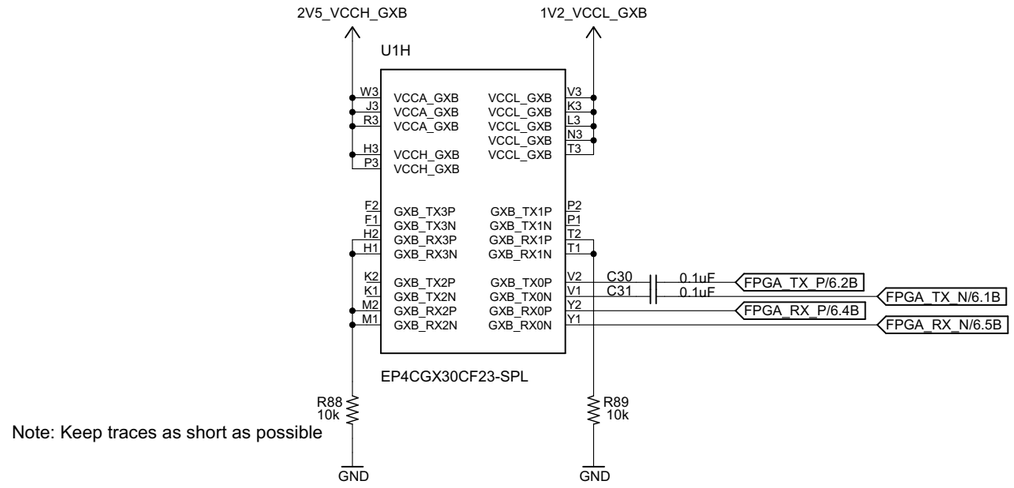

Note: Keep traces as short as possible

FPGA PCIe CONNECTIONS

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Codec

U5

TLV320AIC3100IRHBR

AVDD, IOVDD, DVDD, SPLVDD, SPRVDD, HPVDD, WCLK, BCLK, MCLK, SDA, SCL, GPIO1, DIN, ~RESET, VOL/MICDET, MIC1LP, MIC1LM, MIC1RP, EP, DVSS, SPLVSS, SPRVSS, IOVSS, AVSS, HPVSS, HPL, SPRM, HPR, SPLM, SPRP, DOUT, SPLP, MICBIAS

3V3 3V3

R108 2.7k, R109 2.7k, R111 10k

5V0 3V3 1V8

C115 0.1uF, C123 10uF, C124 0.1uF, C125 0.1uF, C140 100uF_1210_6.3V, C126 0.1uF, C127 0.1uF, C128 0.1uF, C129 10uF — GND

CODEC_GPIO1/16.6B

CODEC_DIN/16.6B

CODEC_WCLK/16.6B

CODEC_BCLK/16.6B

CODEC_MCLK/14.6E

CODEC_SDA/16.6B

CODEC_SCL/16.6B

CODEC_RESET#/16.6B

C139 0.1uF — GND

R110 2.2k, R129 2.2k, R130 2.2k

VOL_MICDET

C155 0.47uF, C154 0.47uF

Speaker Output

L2 MPZ1608S221A — SPKP_R

L3 MPZ1608S221A — SPKM_R

L4 MPZ1608S221A — SPKP_L

L5 MPZ1608S221A — SPKM_L

R100 0 no stuff, R101 0 no stuff

ED555/4DS

J9

CODEC_DOUT/16.6B

Headphone Jack

C136 47uF — HP_L

C137 47uF — HP_R

HP_DET

J10

SJ-43516-SMT — GND

Microphone Jack

J17

MIC1LP

MIC1RP

SJ-43516-SMT — GND

0 R102

no stuff 0 R103

Volume Control (optional)

3V3

R105 48.7k

R270 3361S-1-503GLF

R104 0

C138 0.22uF — GND

VOL

no stuff

GND

AUDIO

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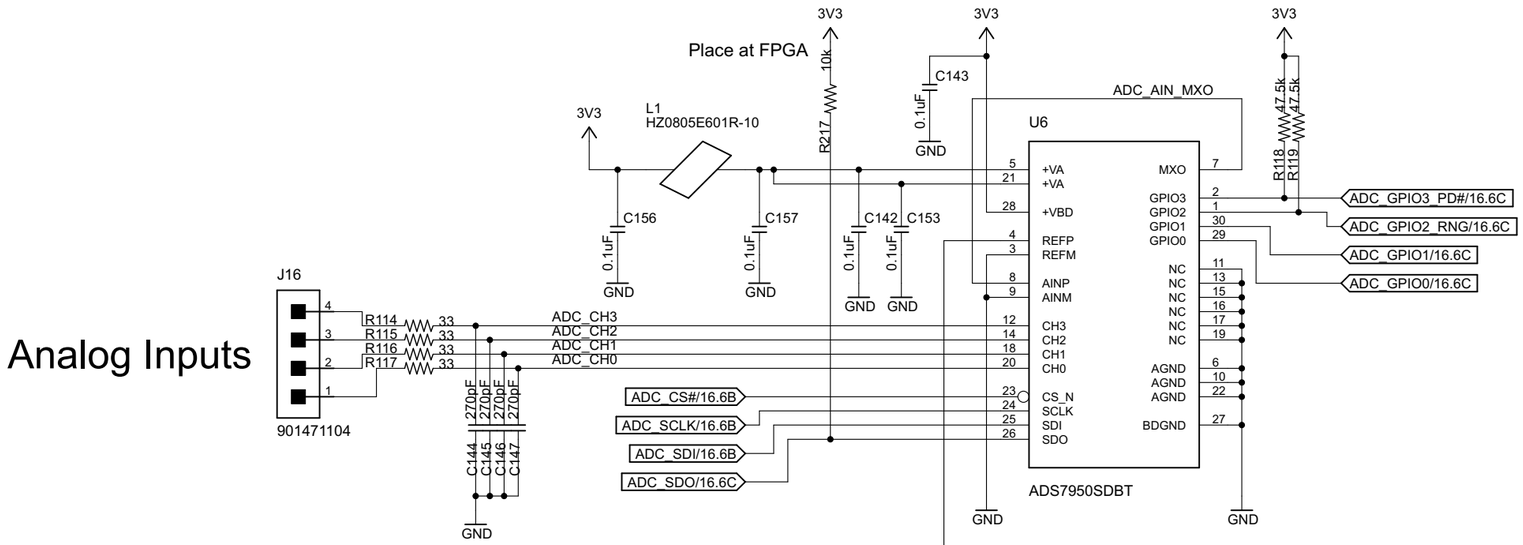
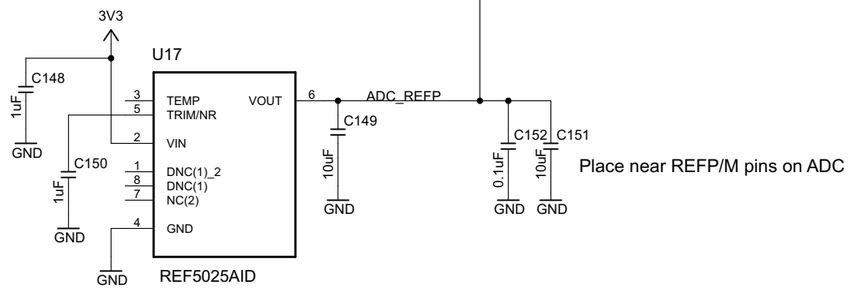
A/D Converter (ADC)



2.5V Reference



ADC

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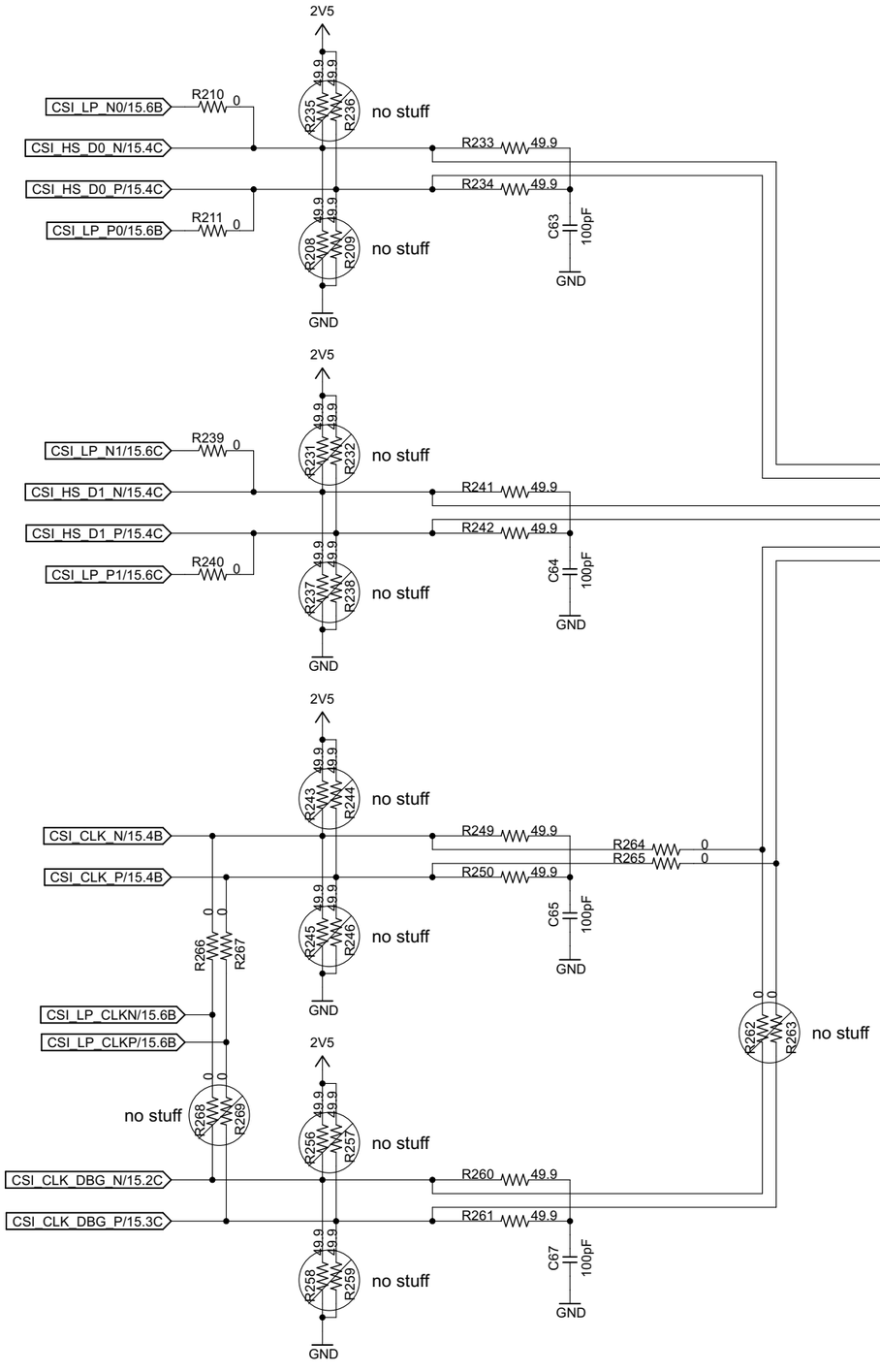
MIPI CSI-2 Connector



MIPI

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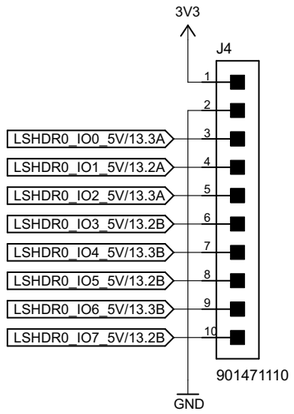
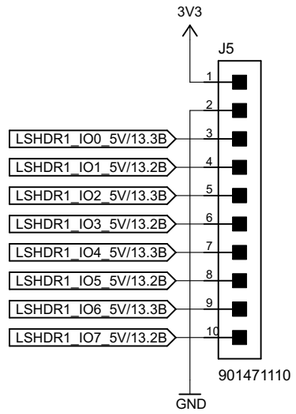
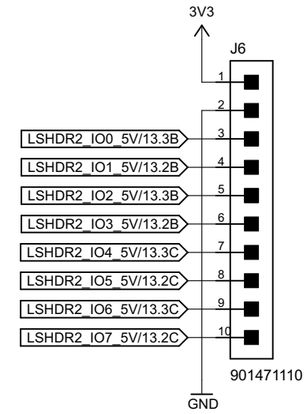
Low-Speed IO Header 0



Low-Speed IO Header 1

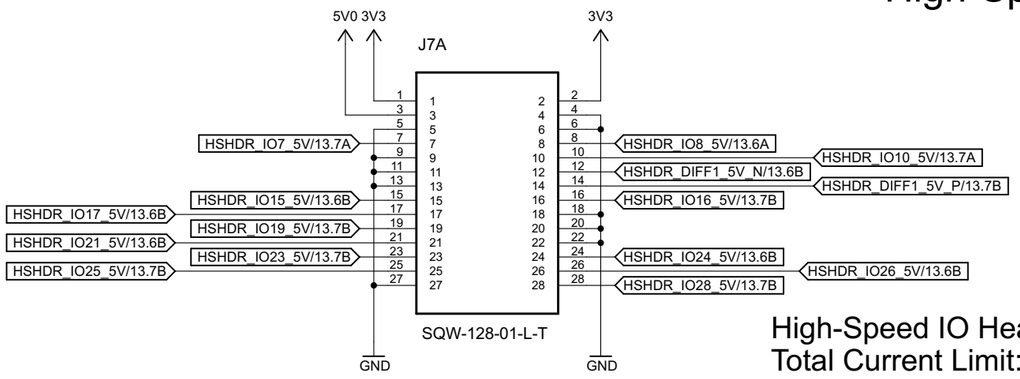


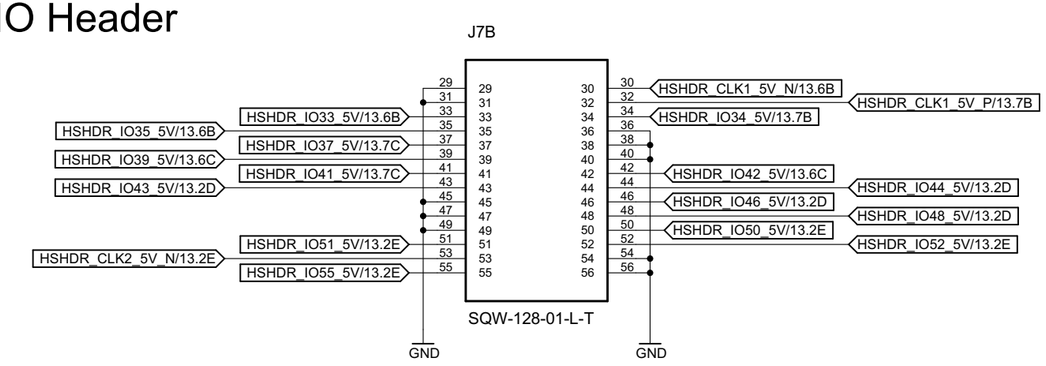
Low-Speed IO Header 2



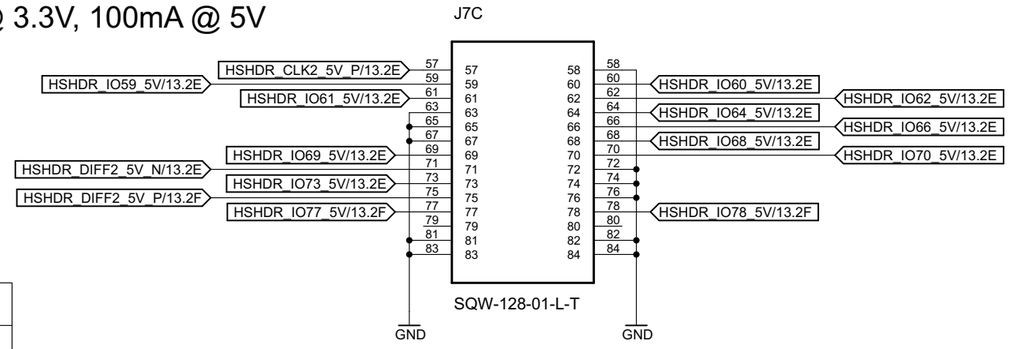
Low-Speed IO Header 0-2
Total Current Limit: 60mA @ 3.3V

High-Speed IO Header





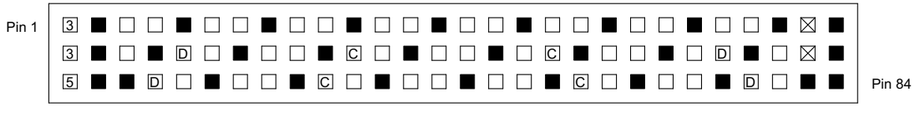
High-Speed IO Header
Total Current Limit: 40mA @ 3.3V, 100mA @ 5V



Low-Speed IO Header Pinout

Note: Use 5V Header (J8, p. 17) for 5V power

High-Speed IO Header Pinout



Note: Clock Pins 30 and 32 are FPGA input; Clock Pins 53 and 57 are FPGA output
Note: All differential and clock pairs are 2.5V

Key

- ☐ Digital IO
- ■ Ground
- 3 3.3V
- 5 5V
- D Differential Pair (+/-)
- C Clock Pair (+/-)
- ☒ No Connect

IO HEADERS

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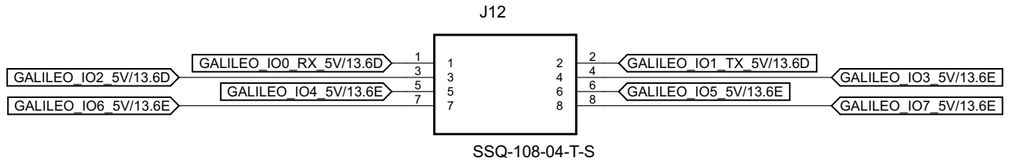
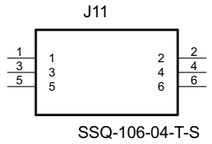
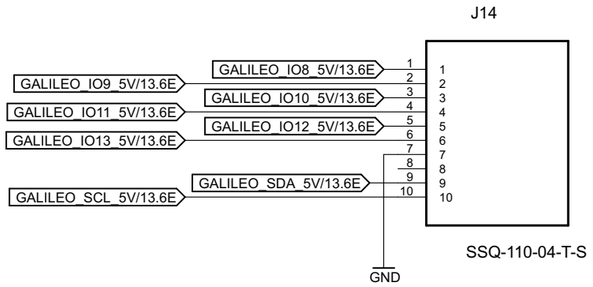
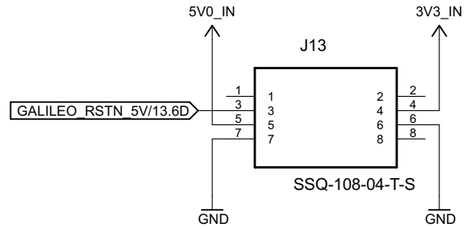
Note: Pin numbers match Galileo schematics



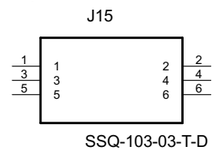


Analog input pins not connected to shield

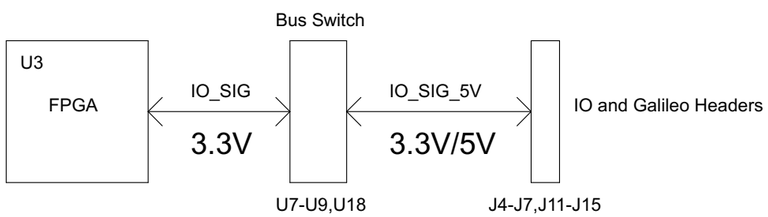




ICSP pins not connected to shield



IO Signal Flow



Note: '_5V' are Galileo/IO header signals and are 5V-tolerant.
Signals without '_5V' are 3.3V FPGA IOs (not 5V tolerant).

GALILEO HEADERS

TITLE: iot_shield		
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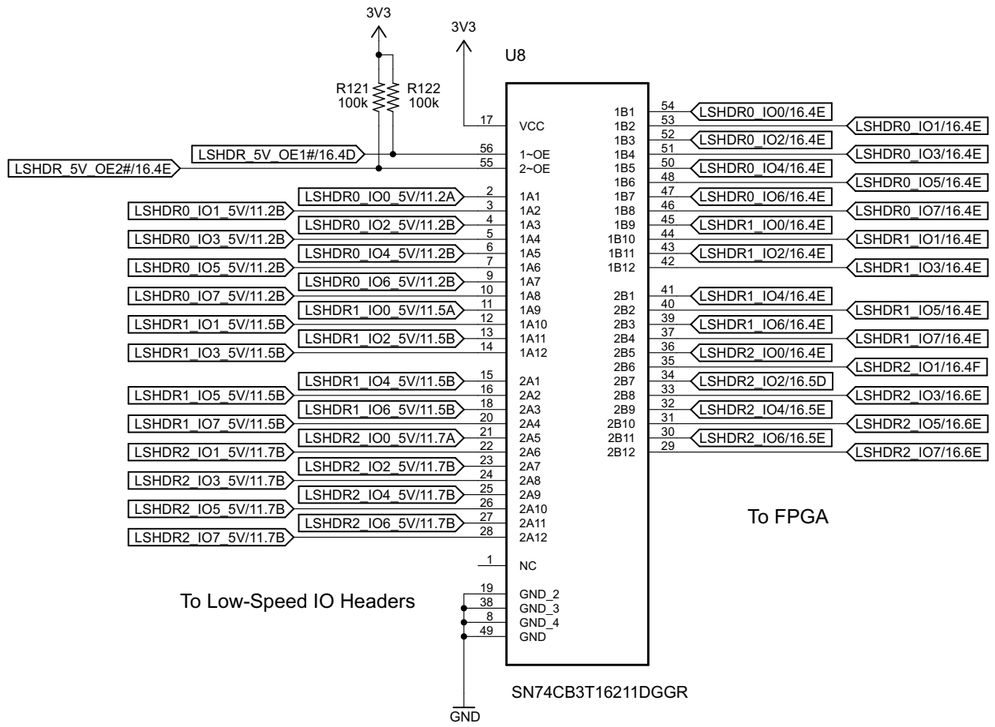
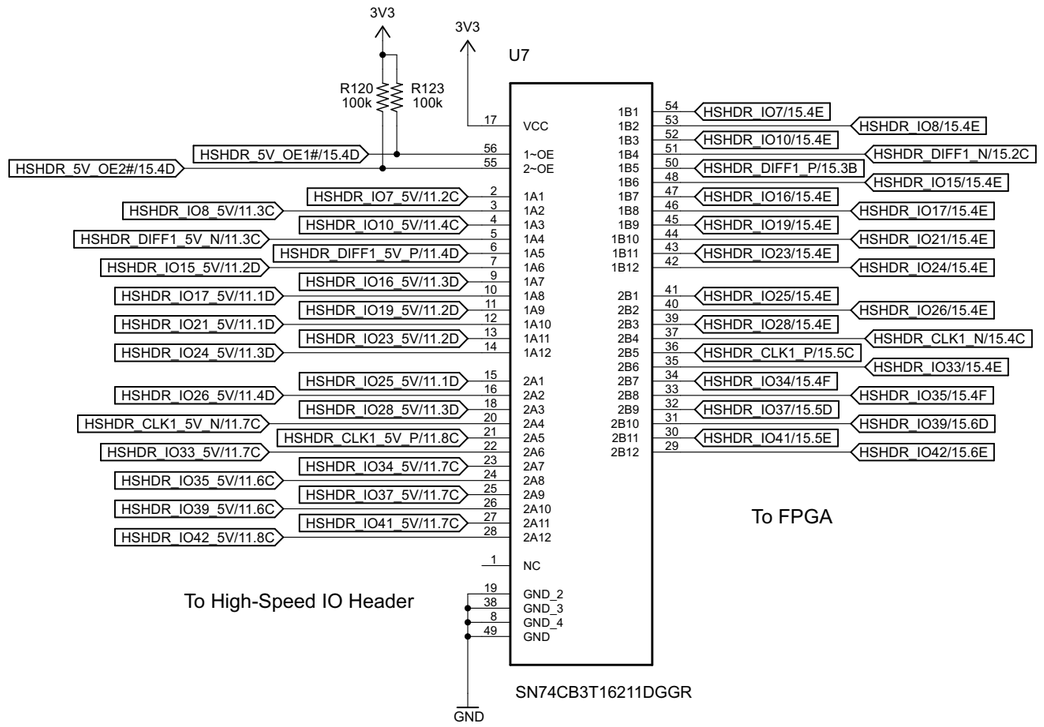
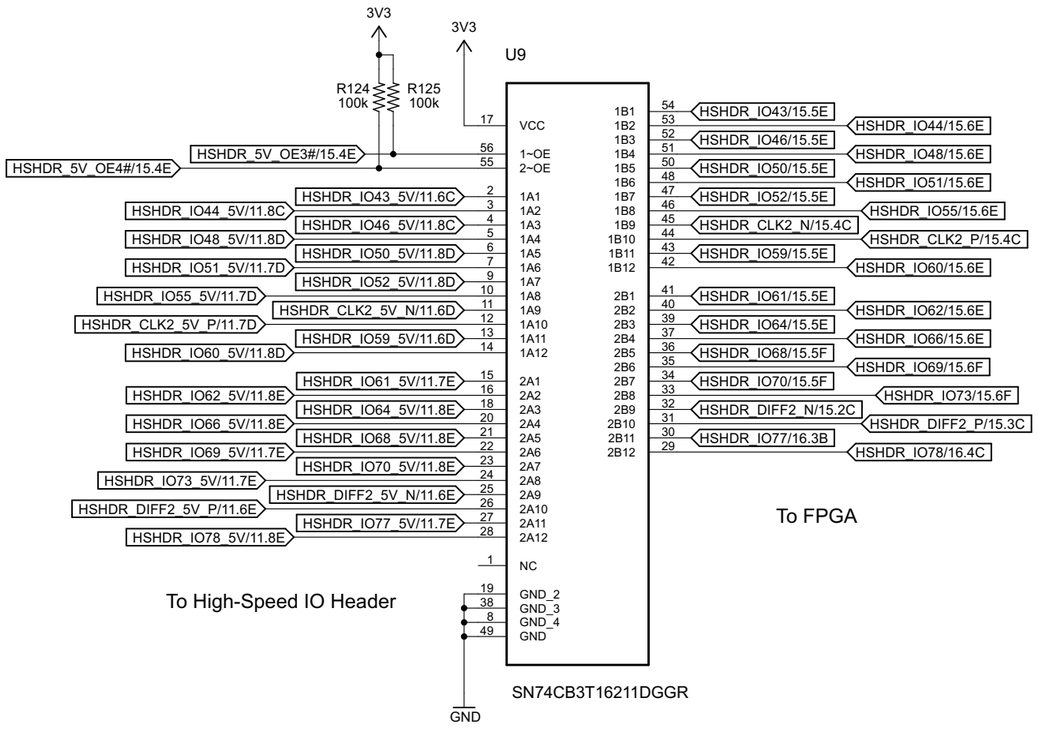
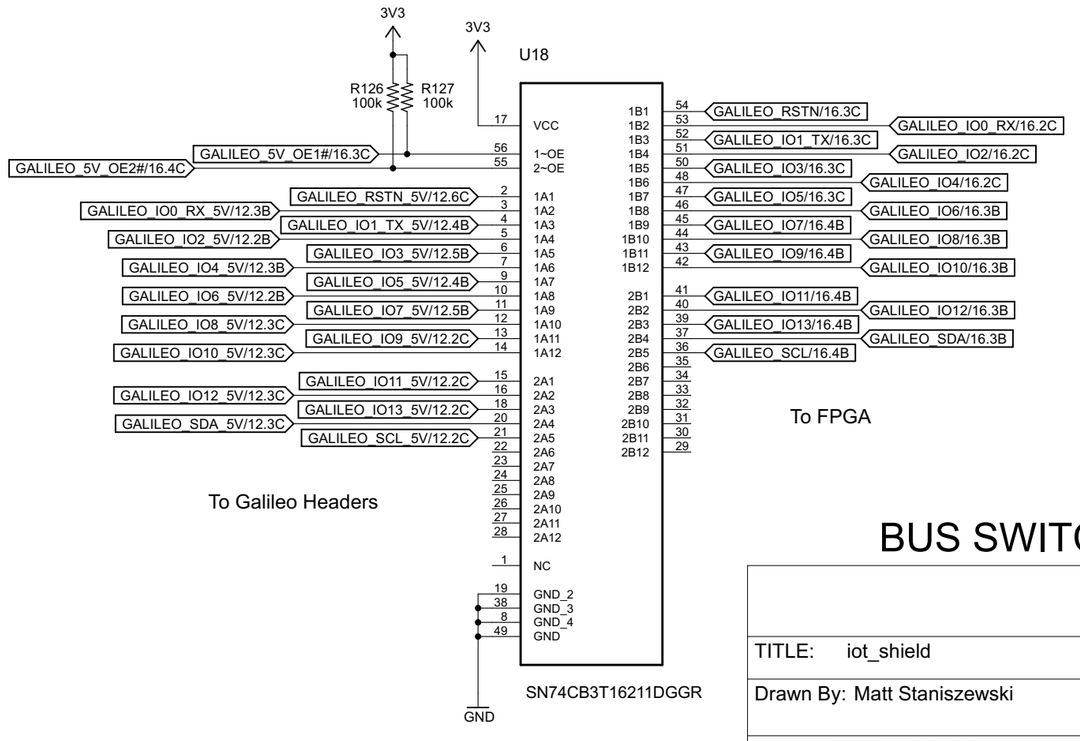
Date: 9/12/2014 11:53:03 AM	Sheet: 12/22	





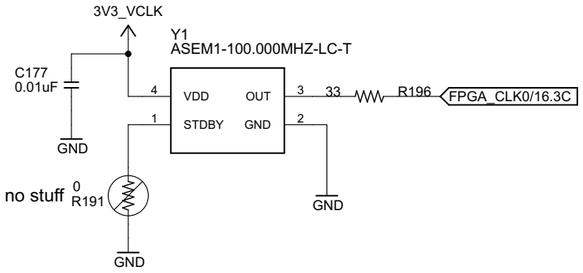




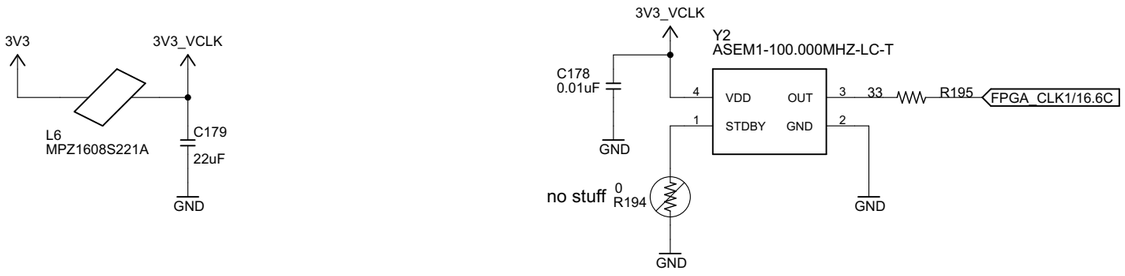
BUS SWITCHES

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.02
Date: 9/12/2014 11:53:03 AM	Sheet: 13/22	

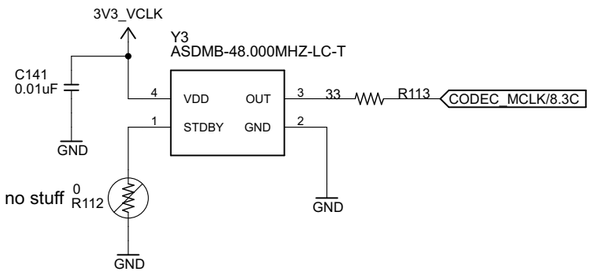
100MHz CMOS Oscillator



100MHz CMOS Oscillator



48MHz CMOS Oscillator

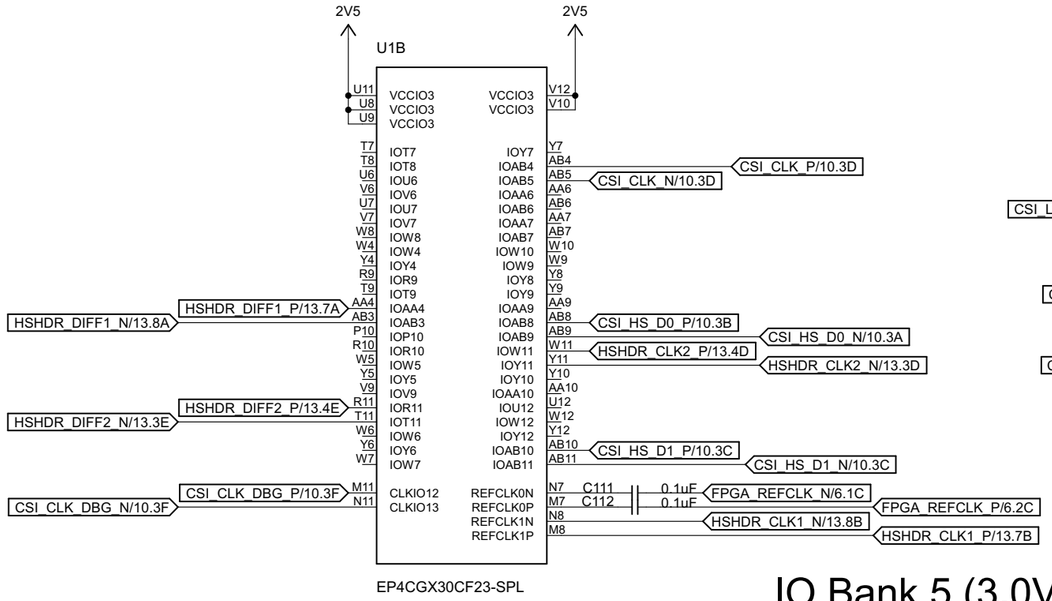


CLOCKS

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.02
Date: 9/12/2014 11:53:03 AM	Sheet: 14/22

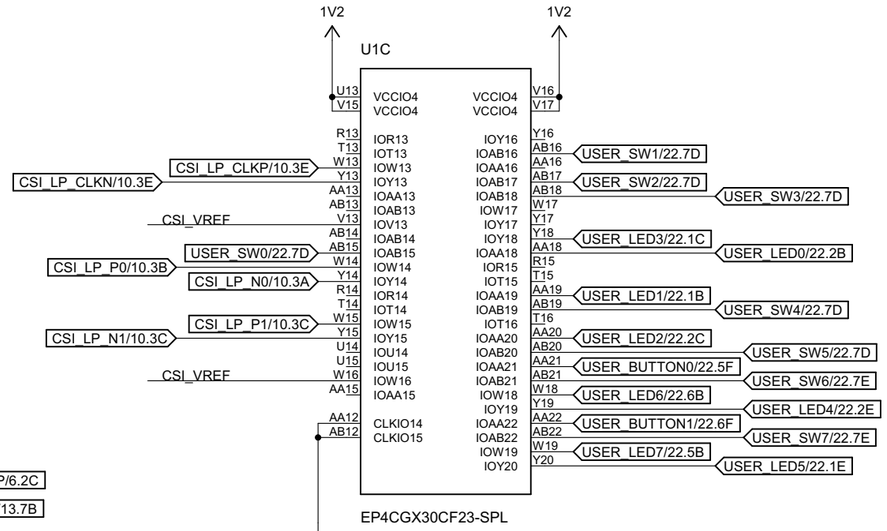
IO Bank 3 (2.5V)

MIPI



IO Bank 4 (1.2V)

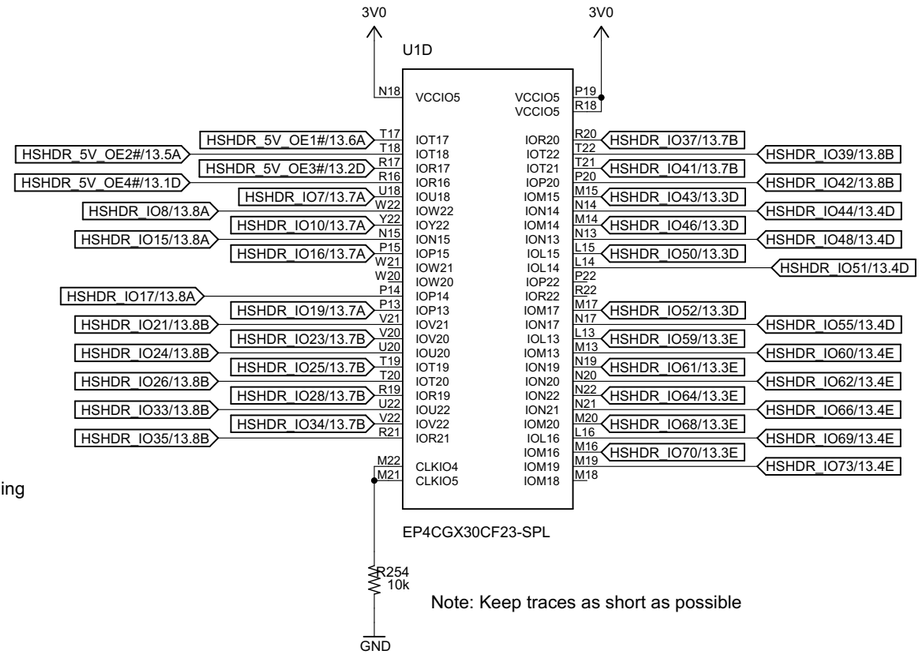
MIPI/LEDs/Buttons/Switches



Note: Keep traces as short as possible

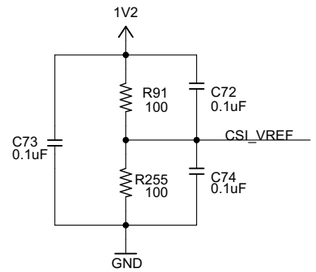
IO Bank 5 (3.0V)

High-Speed IO Header



Note: 3.0V IO Banks are compatible with 3.3V signaling

Note: Keep traces as short as possible

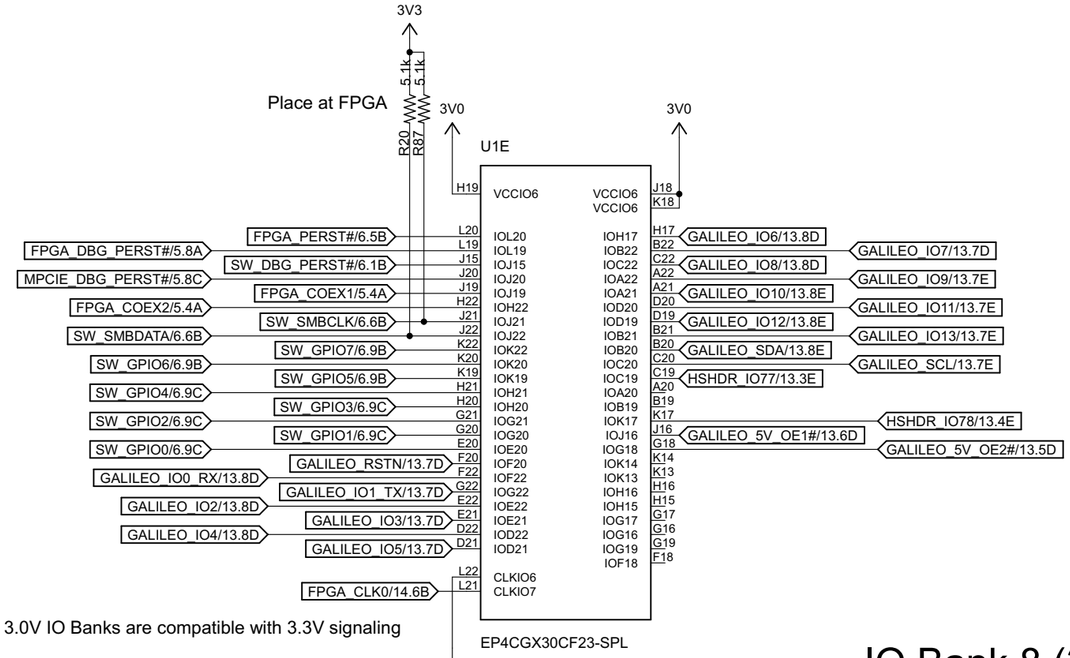


FPGA IO BANK 3 / 4 / 5

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.02
Date: 9/12/2014 11:53:03 AM	Sheet: 15/22	

IO Bank 6 (3.0V)

PCIe/Switch/Galileo IOs/Clock/High-Speed IO Header

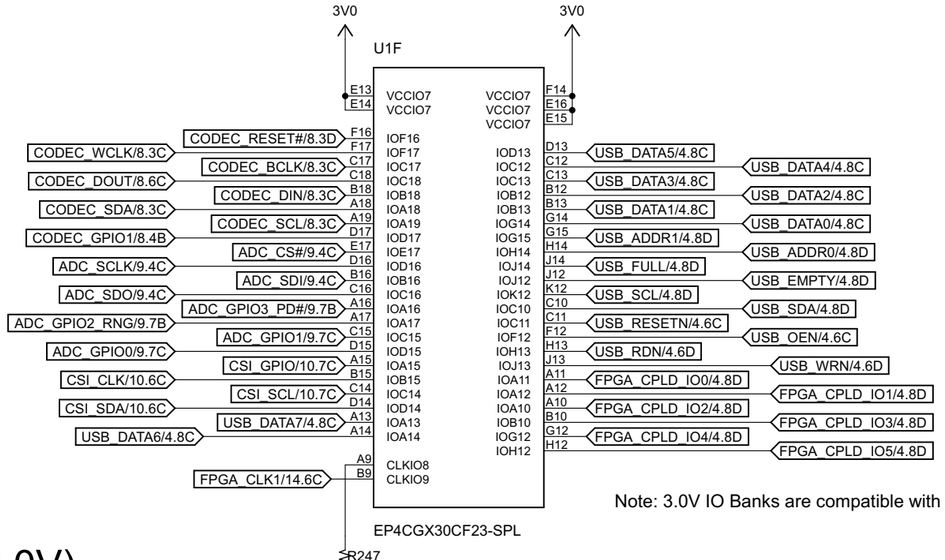


Note: 3.0V IO Banks are compatible with 3.3V signaling

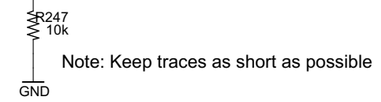
Note: Keep traces as short as possible

IO Bank 7 (3.0V)

Codec/ADC/MIPI/Clock/USB Blaster



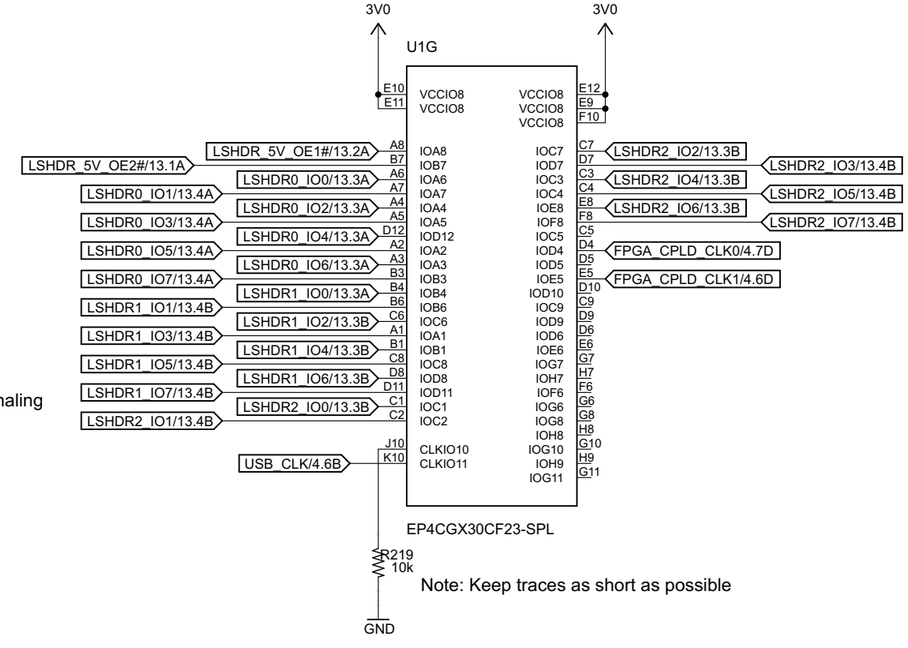
Note: 3.0V IO Banks are compatible with 3.3V signaling



Note: Keep traces as short as possible

IO Bank 8 (3.0V)

Low-Speed IO Headers/USB Blaster



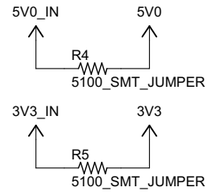
Note: 3.0V IO Banks are compatible with 3.3V signaling

Note: Keep traces as short as possible

FPGA IO BANK 6 / 7 / 8

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.02
Date: 9/12/2014 11:53:03 AM	Sheet: 16/22

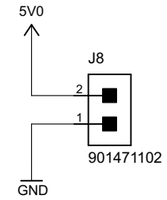
POWER IN JUMPERS



Metal jumpers; Place at least 75mil apart

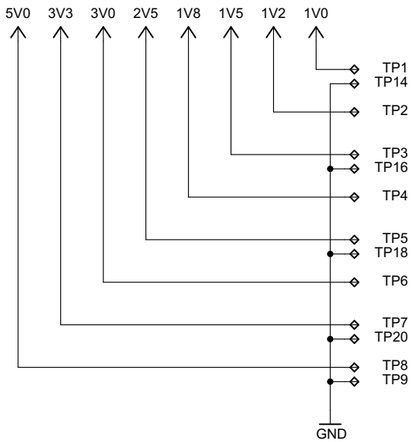
5V HEADER

Use 5V Header (J8) to supply 5V power to devices



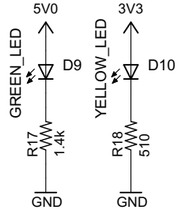
5V Header Total Current Limit: 100mA @ 5V

POWER PROBE TESTPOINTS

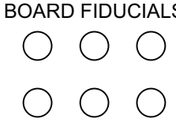


Place ground testpoint next to each rail testpoint
(except where a common ground pad can be shared)

POWER LEDs



BOARD FIDUCIALS



Note: Shield power limits assume all header current limits are used and a Mini-PCIe Gen1 card (i.e. Wi-Fi) is connected.

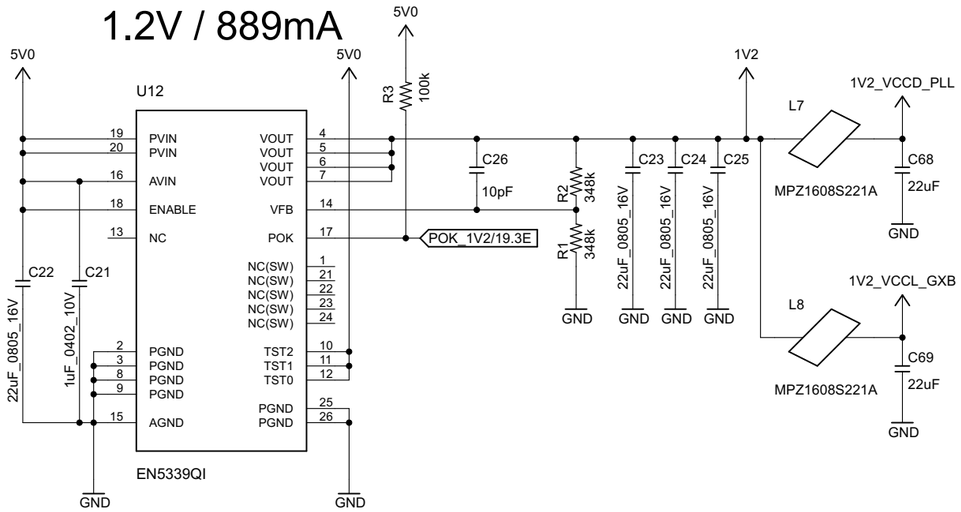
It is assumed that additional shields or USB devices are not connected to the Galileo; please use at your own risk.

POWER IN

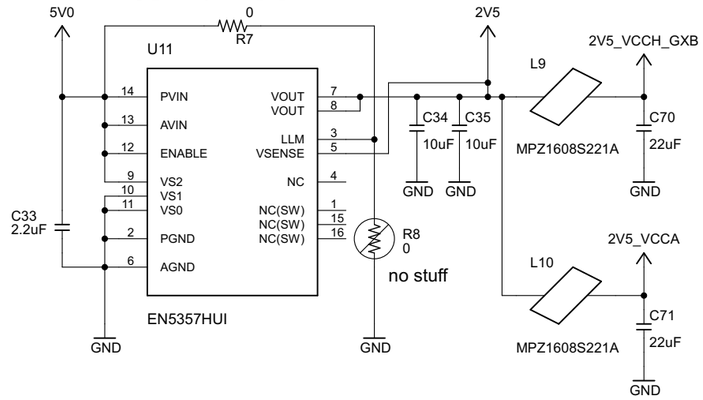
TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.02
Date: 9/12/2014 11:53:03 AM	Sheet: 17/22

1.2V / 889mA

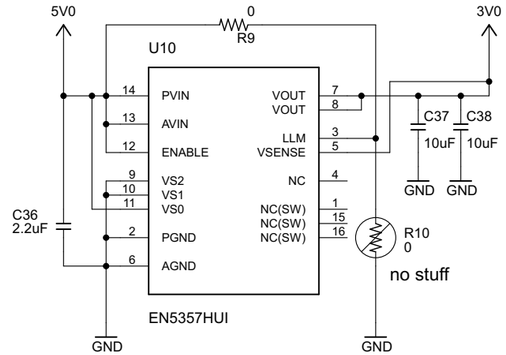
Place C21 as close to AVIN as possible



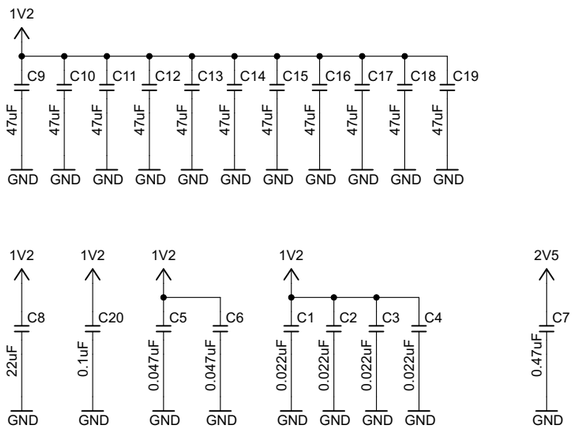
2.5V / 133mA



3.0V / 7mA



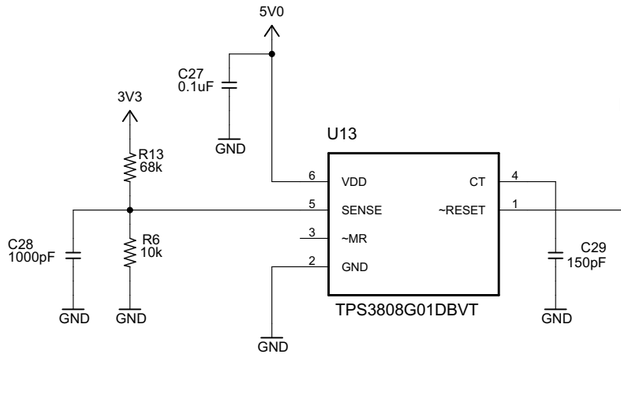
FPGA Decoupling



FPGA VREGS / DECOUPLING

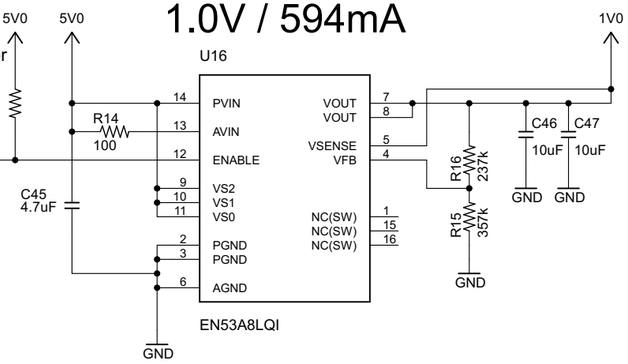
TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.02
Date: 9/12/2014 11:53:03 AM	Sheet: 18/22

Supervisor (1.0V POK)



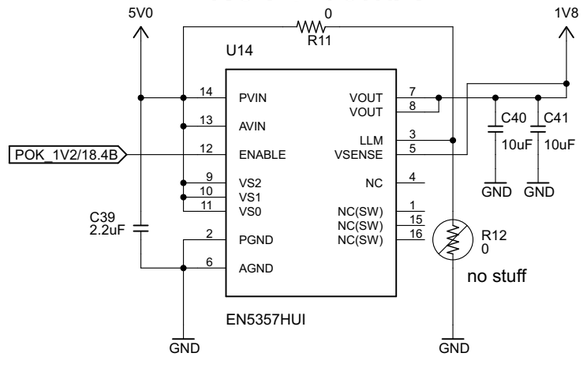
Place pull-up resistor near input at regulator

EN_1V0



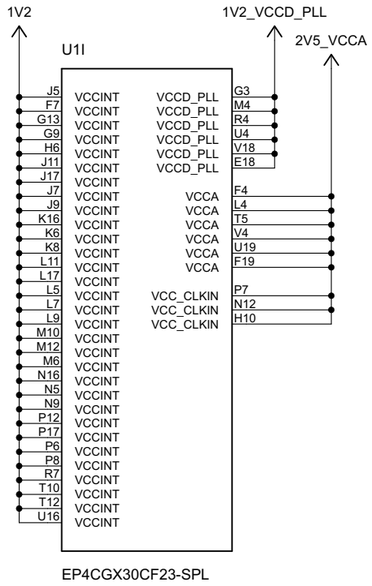
1.0V / 594mA

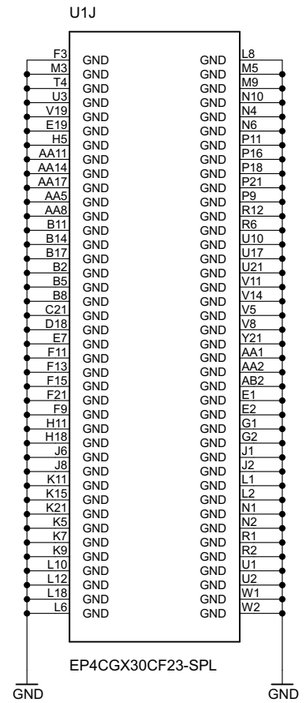
1.8V / 10mA



SYSTEM VREGS

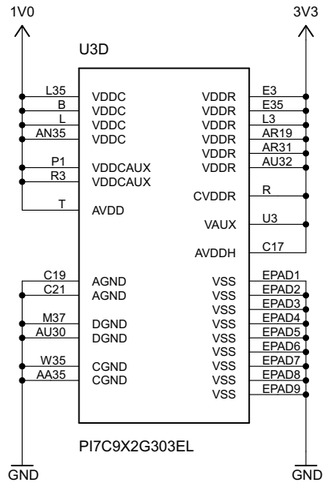
TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.02
Date: 9/12/2014 11:53:03 AM	Sheet: 19/22	

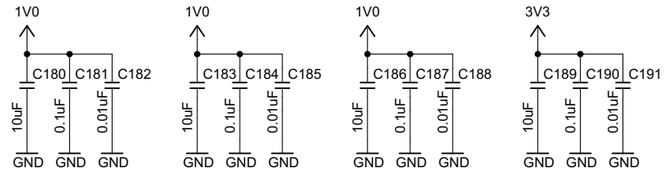




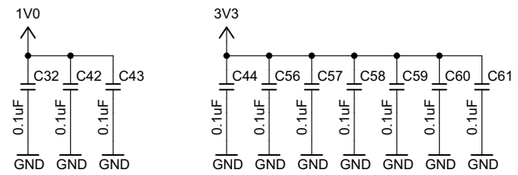
FPGA PWR / GND

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.02
Date: 9/12/2014 11:53:03 AM	Sheet: 20/22





Place groupings at each power pad (T, B, L, R)

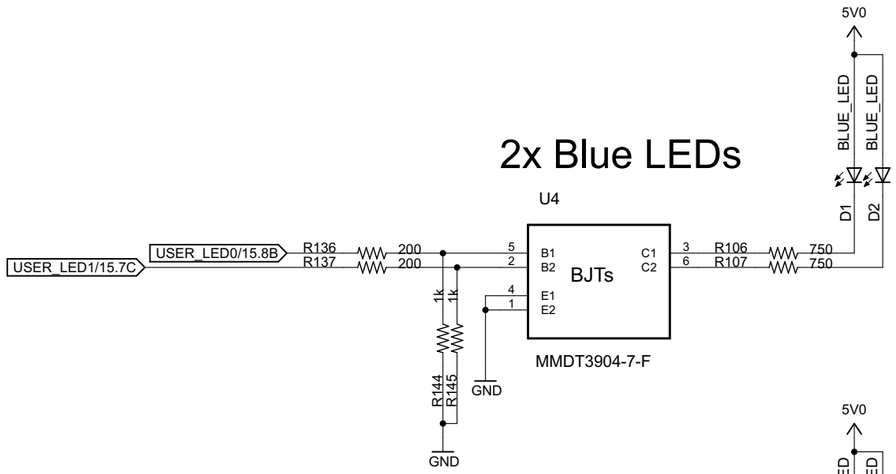


Place common capacitor between near pads with same voltage

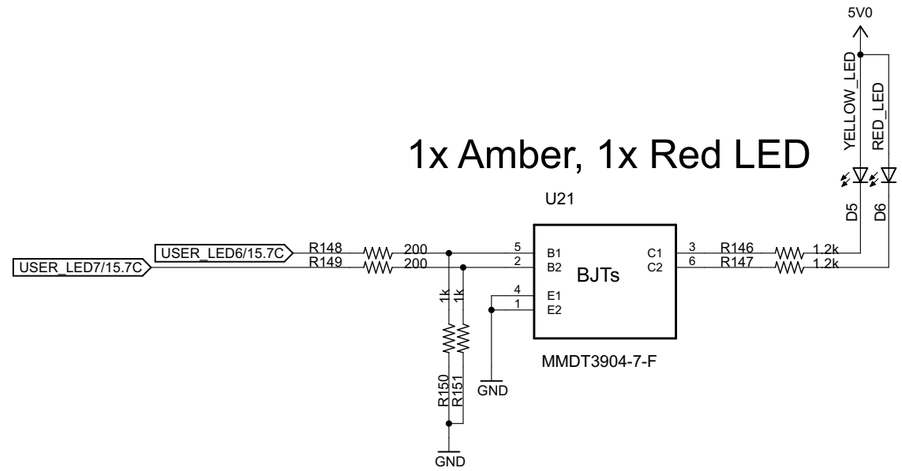
SW PWR / GND / DECOUPLING

TITLE: iot_shield	
Drawn By: Matt Staniszewski	REV: 1.02
Date: 9/12/2014 11:53:03 AM	Sheet: 21/22

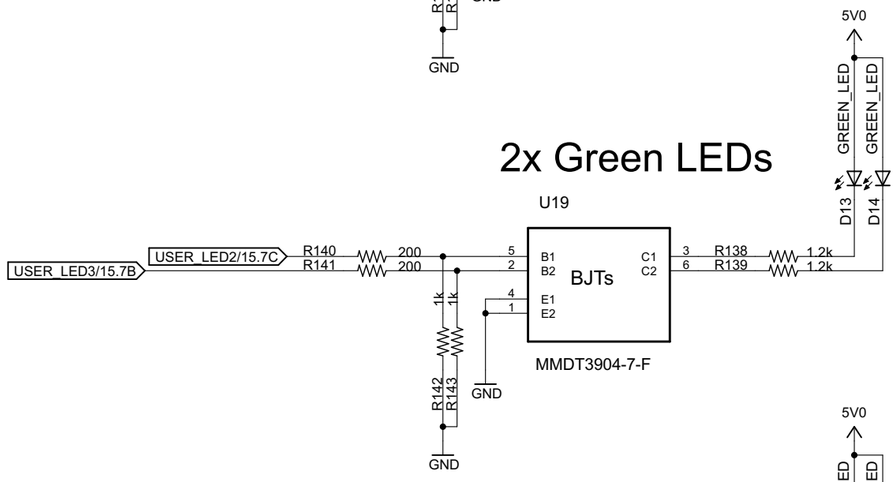
2x Blue LEDs



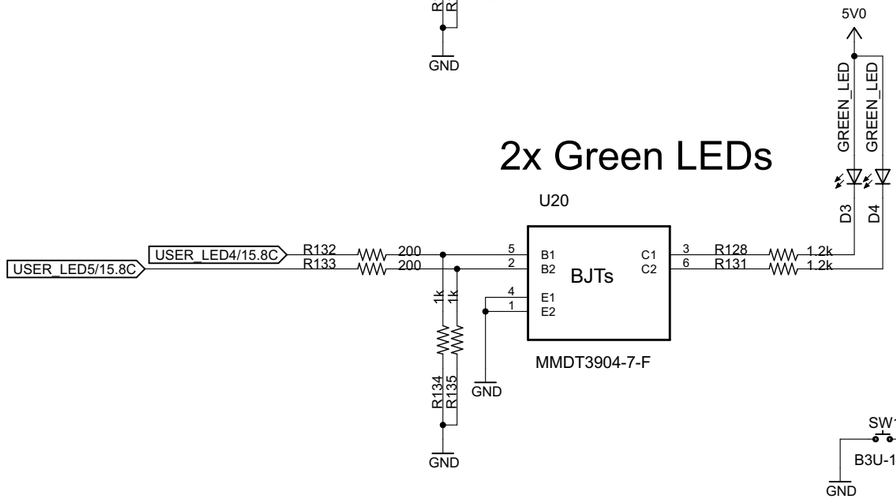
1x Amber, 1x Red LED



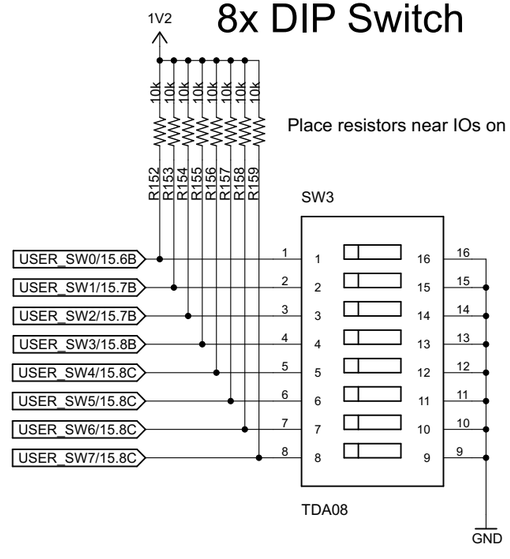
2x Green LEDs



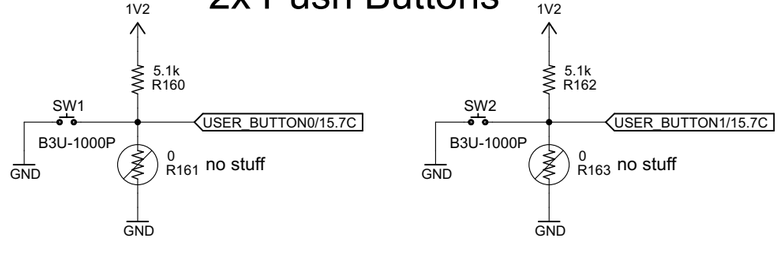
2x Green LEDs



8x DIP Switch



2x Push Buttons



LEDS / BUTTONS / SWITCHES

TITLE: iot_shield		
Drawn By: Matt Staniszewski		REV: 1.02
Date: 9/12/2014 11:53:03 AM	Sheet: 22/22	