

**SVR-LT2**

**Dual Channel Low Cost**

**MIPI CSI2 Receiver IP**

**For FPGA Implementation**

**Preliminary Data Sheet**

**(Subject to Change without Notice)**

**August 2014**

***VLSI Plus’ SVR-LT2 is an IP for FPGA implementations, providing basic 2-lane MIPI CSI2 Rx functionality with rates over 1Gbps (500Mbps per lane), using no off-FPGA active components***

**Highlights**

* Configurable 1 or 2 data lanes; one clock lane
* Up to 500 Mbps per lane;
* Support of all Raspberry Pi (Rpi) Camera video formats (see below)
* Simple video-stream output interface
* Avalon interface to all registers

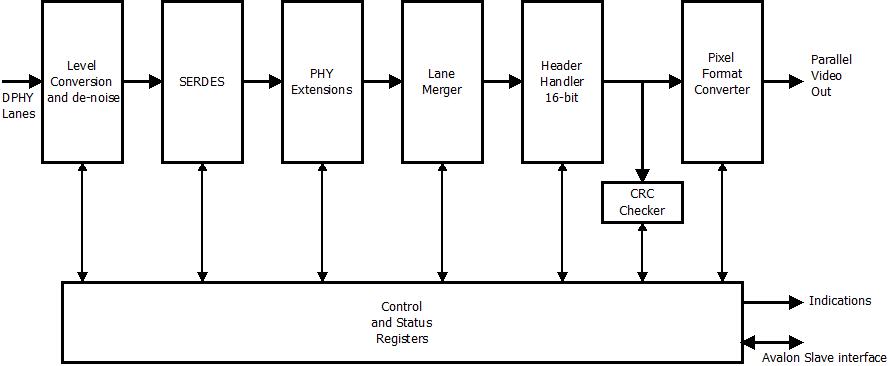
## Clocks

The user should input two clock signals to the SVR-LT2 IP:

* FCLK – the main internal clock; minimum frequency is 100MHz
* PCLK – clock used for accessing the SVR registers.

***In a typical implementation, the user may connect both FCLK and PCLK to the PCIe 125Mhz source. However, PCLK frequency determines register access speed, which, in a practical use case, can be done in the KHz range. Hence, PCLK frequency can be set to very low values (e.g. 100 KHz), to ease the timing closure of the complete FPGA.***

# SVR-LT2 Block Diagram



Simplified SVR-LT2 Block Diagram

# Pads

The following table comprises the full list of the SVR-LT2 pads.

| **Symbol** | **Dir** | **Description** |
| --- | --- | --- |
| ***Lane interface (source-synchronized)*** | | |
| hs\_clk\_p | In | clock lane differential pair, positive input |
| hs\_clk\_n | In | clock lane differential buffer, negative input |
| hs\_d1\_p | In | data lane 1 differential buffer, positive input |
| hs\_d1\_n | In | data lane 1 differential buffer, negative input |
| hs\_d2\_p | In | data lane 2 differential buffer, positive input |
| hs\_d2\_n | In | data lane 2 differential buffer, negative input |
| lpck\_p | In | CMOS level of clock lane P wire |
| lpck\_n | In | CMOS level of clock lane N wire |
| lpd1\_p | In | CMOS level of data lane 1 P wire |
| lpd1\_n | In | CMOS level of data lane 1 N wire |
| lpd2\_p | In | CMOS level of data lane 2 P wire |
| lpd2\_n | In | CMOS level of data lane 2 N wire |
| ***Registers and Control; PCLK-synchronized*** | | |
| svr\_cpu\_int | Out | Packet-received or error-received Interrupt. |
| address[5:0] | In | Avalon Address bus. All registers are 32 bit |
| writedata[31:0] | In | Avalon Data-in bus; used to write data into the SVR-LT2 registers. |
| readdata[31:0] | Out | Avalon Data-out bus; used to read data from the SVR-LT2 registers |
| write | In | Avalon Write. Activates a registers-write cycle. |
| read | In | Avalon Read. Activates a registers-read cycle. |
| ***Clock, reset*** | | |
| fclk | In | General clock; 100MHz Minimum. |
| pclk | In | Avalon clk. No minimum is specified |
| reset\_n | In | Active low asynchronous reset |
| ***Pixel / Indications Output Bus (synchronized to FCLK)*** | | |
| svr\_pixel[9:0] | Out | Pixel bus, in one of several programmable formats. (See Tables below for the description of the data formats). |
| svr\_pixel\_valid | Out | Qualifier for svr\_pixel sampling |
| svr\_fs | Out | Frame Start indicator; valid for a single clock cycle |
| svr\_fe | Out | Frame End indicator; valid for a single clock cycle |
| svr\_ls | Out | Line Start indicator; valid for a single clock cycle. Issued when a long packet starts |
| svr\_le | Out | Line End indicator; valid for a single clock cycle. Issued when a long packet ends |
| svr\_data\_type [5:0] | Out | Data-Type field, from the packet header, after ECC correction. |
| svr\_channel\_id[1:0] | Out | Virtual Channel field, from the header, after ECC correction |

# Supported Video Formats

The SVR-LT2 automatically detects and fully supports all video formats used by the Rpi camera module:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Format** | **Frame Rate** | **Horizontal Resolution** | **Vertical Resolution** | **Bit Depth** |
| QSXGA | 15 | 2592 | 1944 | 8/10 |
| 1080P | 30 | 1920 | 1080 | 8/10 |
| 960P | 45 | 1280 | 960 | 8/10 |
| 720P | 60 | 1280 | 720 | 8/10 |
| VGA | 90 | 640 | 480 | 8/10 |
| QVGA | 120 | 320 | 240 | 8/10 |

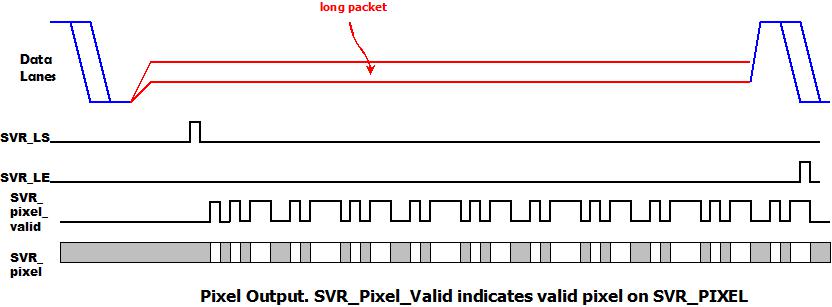
# 

# Timing Waveform

# timing_lt.jpeg

FS, FE, LS and LE Timing Waveform

The figure above depicts the timing waveforms of the SVR-LT2’s Frame-Start, Frame-End, Line-Start and Line-End signals (SVR\_FS, SVR\_FE, SVR\_LS, and SVR\_LE). Frame-Start and Frame-End events are signaled by the camera with dedicated short packets. The SVR-LT2 detects those packets and asserts a single FCLK pulse on the SVR\_FS or SVR\_FE pads, respectively.



Pixel, Pixel-valid Timing Waveforms

The figure above depicts the waveform of svr\_pixel and svr\_pixel\_valid.

When a long packet header is detected in the SVR, the SVR\_LS output is pulsed for one FCLK cycle. Then when pixels are ready at the output, svr\_pixel\_valid is asserted, and the pixel value is output on the svr\_pixel bus. Note that svr\_pixel\_valid is not continuous, and has gaps as a result of the difference between FCLK rate and the pixel rate of the source, and as a result of the packing of pixels in MIPI® CSI2 specification.

When the SVR detects that the long packet has terminated, it asserts SVR\_LE for a single FCLK cycle.

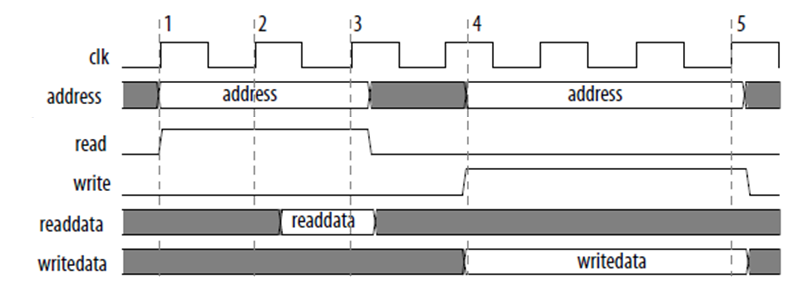
# Accessing the SVR-LT2 Registers

# All SVR-LT2 registers are 32 bits; they are accessed using Avalon non-burst fixed-wait-state cycle Read and Write protocols.

# The following signals are used for registers read/write:

* address[5:0]: 6 bit address bus; selects one of the SVR-LT2 registers
* write: Set to logic-1 to initiate a Write cycle
* read: Set to logic-1 to initiate a Read cycle
* writedata: 32 bit input bus; the data to be written into the addressed register in a Write cycle
* readddata: 32 bit out bus; contains the data from the read register in a Read cycle.

The timing waveforms of a Read and a Write cycle, for write-Wait-Time = 2 and read-Wait-Time = 1, are shown in the figure below.



Note: All register accesses are 32 bits; byte accesses are not implemented.

# Interrupts

The SVR-LT2 detects error as well as normal events such as video frame completion. The user can program the SVR-LT2 to generate an Interrupt in one of several events:

* Detection of a communication Error
* Completion of a video frame
* Completion of a video line

See chapter on Interrupt registers below.

# Registers

There are several 32-bit registers in SVR-LT2 IP:

|  |  |  |
| --- | --- | --- |
| **Address** | **Name** | **Function** |
| 0x00 | Enable | SVR-LT2 operation is enabled by writing 1 into this register. |
| 0x01 | Configuration | General Configuration |
| 0x09 | ISR | Interrupt Status Register |
| 0x0A | IMR | Interrupt Mask Register |
| 0x0C | IRC | Interrupt Read and Clear registers – reading from this register returns the contents of the ISR, and also clears its contents |
| 0x10 – 0x17 | BER Measurement Registers | Optional set of registers, used to measure the BER (Bit Error Rate) of the link to the camera. |
| 0x38 | Watermark Removal Key | When a unique 32 bit value is written into this register, the VLSI+ watermark will be removed from the image |
| 0x39 | BER Measurement Enable Key | When a unique 32 bit value is written into this register, the BER measurement option will be enabled |
| 0x3E | IP Vendor Code | VLSI Plus’ MIPI® Manufacturer Code (0x0206). The high order 16 bits are not used. (Read-Only) |
| 0x3F | Version | VLSI Plus’ 32 bit version code (Read-Only) |

# *Enable Register (R/W). Address = 0x00*

|  |  |  |
| --- | --- | --- |
| **Bit** | **Name** | **Description** |
| 0 | SVR\_En | This bit enables and disables the activity of the SVR-LT2: 0 –Disable 1-Enable |
| 31:1 |  | Not implemented |

# *Configuration Register (R/W). Address = 0x01*

|  |  |  |
| --- | --- | --- |
| **Bit** | **Name** | **Description** |
| 0 | Cont\_Clk | Set if the camera uses DPHY continuous clock mode |
| 1 | Lanes | Number of data lanes: 0: 1 data lane 1: 2 data lanes |
| 31:2 |  | Not implemented |

# 

# *Interrupt Handling Registers*

It is possible to generate Interrupt to the host CPU in case an error or other event occurs. The ISR register indicates the status of active interrupt sources. The IMR register can mask any of the sources. The svr\_cpu\_int pad will be asserted (pulled high) if at least one interrupt source is active, and the corresponding mask bit in the IMR register is clear.

## *ISR (Interrupt Status Register, R/W). Address – 0x09*

|  |  |  |
| --- | --- | --- |
| **Bit** | **Name** | **Description** |
| 0 | Double-Write-Error | The register has been written at least twice since it was last read |
| 1 | Hard Error | A Hard (irrecoverable ) Error has occurred (since the last time this bit has been cleared) |
| 2 | Recoverable Error | A Recoverable Error has occurred (since the last time this bit has been cleared) |
| 5:3 | Not used |  |
| 6 | Long Packet | A Long Packet has been received |
| 7 | Video Frame | A complete video frame has been received |
| 15:8 | Header | Header ID byte |
| 31:16 | Bytes | Number of bytes in last long packet |

* Bit 0 is set to indicate that a change in this register (bits 7:1) has been missed by the CPU.
* Bits 7:1 are interrupt events, and correspond to events in the SVR-LT2. Whenever any of the events occur, if it is not masked (see below), the corresponding bit in the register will be set. In normal operation, those bits can be cleared by a CPU Write into the register, or by a CPU read from Int\_Read\_And\_Clear register. (They are also cleared with SVR-LT2 Reset or Disabled).
* Bits 15:8 indicate the header ID byte. They are written into as follows:
* Since short packets are used to indicate frame-end, bits 15:8 are updated whenever a short packet or a long packet – generic or specific – completes, UNLESS Video-Frame interrupt bit is unmasked.   
  In case Video-Frame interrupt is unmasked, bits [15:8] will not be updated when a non-generic short packet ends, and thus the ID byte of the last long packet will be read from the register.
* Bits [31:16] are updated whenever a long packet ends, indicating how many bytes have been received. The SVR-LT2 counts the received bytes, and compares the count to the WC (word-count) field which is extracted from the packet header. The counter contents are not accessible by the host, as they constantly change. When the packet ends the actual number of received bytes is stored in bits [31:16], and it is available for the host to read.

***If any of bits [7:0] is set, and the corresponding mask bit (see below) is not set, the SVR-LT2 will assert the svr\_cpu\_int output.***

### *IMR (Interrupt Mask Register, R/W). Address = 0x0A*

|  |  |
| --- | --- |
| **Bit** | **Name** |
| 0 | Mask Double-Write-Error Interrupt |
| 1 | Mask Hard Error Interrupt |
| 2 | Mask Recoverable Error Interrupt |
| 5:3 | Not Used |
| 6 | Mask Long Packet Interrupt |
| 7 | Mask Video Frame Interrupt |

Mask bit at logic-0 allows interrupt from that event. Logic-1 blocks the interrupt source.

## *IRC (Interrupt Read and Clear Register, Read-Only). Address = 0x0C*

Reading from this address returns the ISR contents, and then clears it.

# *IP Vendor Code (Read Only). Address = 0x3E*

The IP Vendor Read-Only register holds the manufacturer code assigned to VLSI Plus by MIPI® (0x0206) in the 16 LS bits. The high order 16 bits are not used.

|  |  |
| --- | --- |
| **Bit** | **Description** |
| 31:16 | Not implemented |
| 15:0 | 0x0206 |

# *Version (Read Only). Address = 0x3F*

The Version Read-Only register contains a unique code for each hardware release.

|  |  |
| --- | --- |
| **Bit** | **Description** |
| 31:0 | 32 bit hardware version code |

# *BER Measurement Registers*

BER measurement is an optional feature for the SVR-LT2.

With this option, it is possible to count communication errors, over a pre-defined period of time.

The period of time is from 1 to (232 – 1) units, where each unit is 1024 \* FCLK period (8.192 micro-second for FCLK=125MHz). When the maximum value is programmed, errors are counted in an interval of some 35184 second – time enough to prove BER of 10-12 with high certainly

Counted errors include SOT (Start-of-Transmission) errors on either of the two lanes, CRC errors, single-ECC errors and double-ECC errors.

**BER Measurement Registers Summary**

|  |  |  |
| --- | --- | --- |
| **Register** | **Address** | **Note** |
| Timer-Counter | 0x10 | Set by user to count-down value. When not at zero, counts down from a FCLK divided by 1024 source. Stops at 0. |
| SOT1\_error\_counter | 0x11 | Counts SOT errors on lane 1 |
| SOT2\_error\_counter | 0x12 | Counts SOT errors on lane 2 |
| CRC\_error\_counter | 0x15 | Counts CRC errors |
| ECC\_SE\_counter | 0x16 | Counts ECC soft (single) errors |
| ECC\_HE\_counter | 0x17 | Counts ECC hard (two or more) errors |

* All registers are R/W
* The error counters do not overflow – if they reach all-1 they stop counting.
* All registers reset at power-up and when Enable Register =0

# Instantiation Instructions

TBD

# Options

* Watermark Removal option. There is a small VLSI+ logo at the bottom of the image. The watermark can be removed by writing a unique 32 bit code to the Watermark Removal Key register. For more details, please go to <http://www.vlsiplus.com/gallileo/watermark_removal>
* BER Measurement (see above) is optional. BER Measurement can be activated by writing a unique 32 bit code to the BER Measurement Key register. For more details, please go to <http://www.vlsiplus.com/galileo/ber_option>