CS 303 Logic and Digital System Design Term Project [Fall 2022]

Elevator Contoller System

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Abstract

The project aimed to design and implement a controller for an elevator using Verilog. The controller handles inputs from buttons and outputs signals to control the movement of the elevator and indicate its state. The design uses a state machine to handle the different states of the elevator, such as moving up, down, or being idle. The state is determined by the current and next floor and whether the elevator is busy. The controller also uses a counter and wait time to simulate the time between moving between floors. The simulation results showed that the code successfully simulates the behavior of an elevator system.

Introduction

The goal of this project was to design and implement a controller for an elevator system using Verilog. The controller is responsible for handling inputs from various buttons and outputting signals to control the elevator's movement and indicate the system's current state. The elevator system is designed to control the movement of the elevator between 5 floors, with input buttons inside and outside the elevator, and output LEDs and seven segment displays to indicate the elevator status.

Design

The design of the controller utilizes a state machine to handle the different states of the elevator, such as whether it is moving up, down, or being idle. The state of the elevator is determined by the current and next floor, and whether or not the elevator is busy.

The controller takes in an input clock signal `clk_in` and an input reset signal `rst` which are used for synchronizing the internal state of the controller. It also takes input signals for each floor button presses, both inside and outside of the elevator, `floor_0_p`, `floor_1_p`, `floor_2_p`, `floor_3_p`, and `floor_4_p`; `floor_0_d`, `floor_1_d`, `floor_2_d`, `floor_3_d`, and `floor_4_d`. It also takes input signals for the direction switches `direction_1`, `direction_2`, and `direction_3` that indicate the direction of the elevator movement.

The controller uses a counter and wait time to handle the delay between moving between floors. This allows the elevator to properly simulate the time it takes to move between floors. The waitTime and counter registers are used to keep track of the time for this delay.

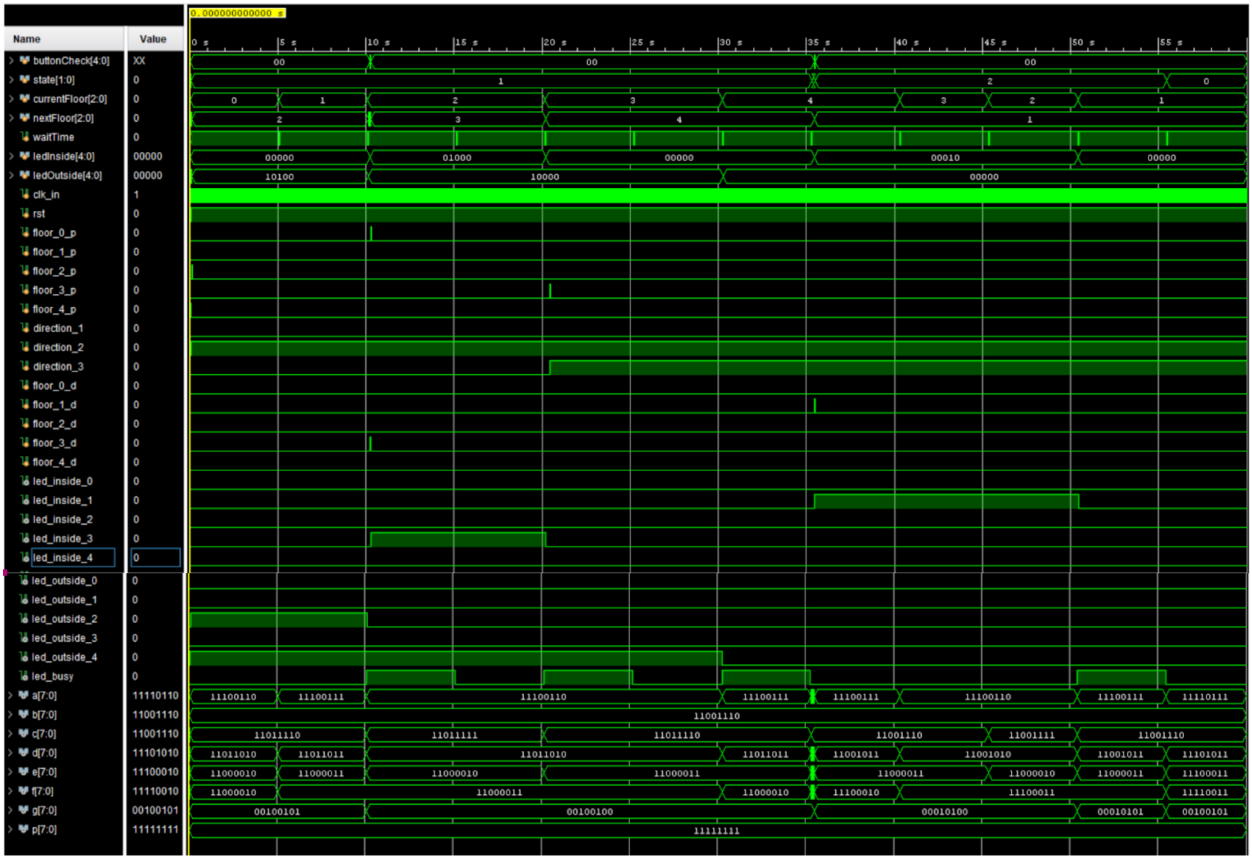
The controller has various output signals to indicate the state of the elevator, such as the LEDs and seven segment display indicating which floor the elevator is on, `led_inside_0`, `led_inside_1`, `led_inside_2`, `led_inside_3`, and `led_inside_4`, and the LEDs indicating the status of the elevator doors, `led_outside_0`, `led_outside_1`, `led_outside_2`, `led_outside_3`, and `led_outside_4`. It also has an output signal led_busy that indicates whether the elevator is currently in use or not.
The controller also uses various registers to store internal state information, such as state, currentFloor, and nextFloor which are used to keep track of the current and next floor of the

elevator and the state of the elevator. ledInside, ledOutside, and buttonCheck are used to keep track of the button press status.

Simulation and Results

The Verilog code was simulated using a simulation software and the results were consistent with the expected behavior of an elevator system. The elevator moved between floors and stopped at the correct floor when a button was pressed. The LED indicators and seven segment display also properly indicated the current state of the elevator, such as which floor it was on.

The simulation results show that when a button press is detected on a particular floor, the elevator moves to that floor, and the corresponding LED inside and outside the elevator turn on, also the seven segment display updates it’s status to indicate the elevator's position. The LED busy signal also turns on, indicating that the elevator is in use.



Settings Edit

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Project location:	C:/Users/BERNA/Desktop/CS303/TERM PROJECT/ElevatorController_CS303_TermProject
Product family:	Artix-7
Project part:	xc7a100tcsg324-1
Top module name:	top_module
Target language:	Verilog
Simulator language:	Mixed

Synthesis

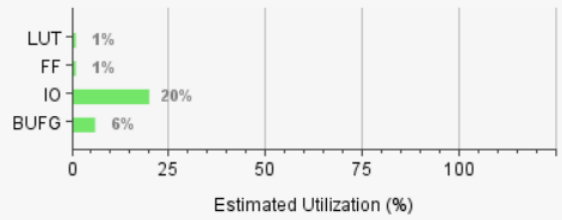
Status:	✓ Complete
Messages:	9 warnings
Part:	xc7a100tcsg324-1
Strategy:	Vivado Synthesis Defaults
Report Strategy:	Vivado Synthesis Default Reports

Implementation Summary | Route Status

Status:	✓ Complete
Messages:	No errors or warnings
Part:	xc7a100tcsg324-1
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental compile:	None

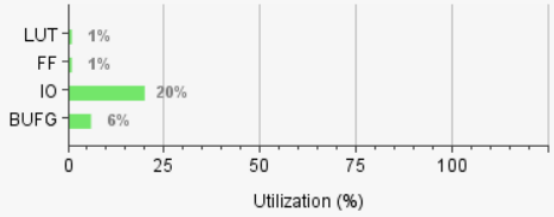
Utilization Post-Synthesis | Post-Implementation

Graph | Table



Utilization Post-Synthesis | Post-Implementation

Graph | Table



Utilization Post-Synthesis | Post-Implementation

Graph | Table

Resource	Estimation	Available	Utilization %
LUT	157	63400	0.25
FF	138	126800	0.11
IO	42	210	20.00
BUFG	2	32	6.25

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Conclusion

The Verilog code provided was able to successfully simulate the behavior of an elevator system. The state machine design allows the elevator to handle multiple states and the use of a counter and wait time allows for proper simulation of the time.