Homework 2
Embedded Systems

Question 1:

Part A: Timer A 500 KHz, what is timer period in seconds if continuous

cycles / sec

Div	Id	Cycles		
11	0	500,000	~~.131 seconds~~	7.629
12	1	250,000	~~.262 seconds~~	3.814
14	2	125,000	~~.524 sec~~	1.907
18	3	62,500	~~1.048 sec~~	.9536

Part B: 500 kHz w/ .4 second goal using up mode
Find a suitable TAccO and Id

$500{,}000 \cdot \frac{.4}{1\,sec} =$

Div	ID	cycles	
11	0	200,000	200,000
12	1	100,000	
14	2	50,000	✓
18	3	25000	✓

TAccRO = 50,000 or 25000

ID = 2, 3

Question 2:

part A ADC configured to 8kHz (8192 hz)
Find timer period

Div	ID	Period	
/1	0	8192	.125
/2	1	4096	.0625
/4	2	2048	.03125
/8	3	1024	.015625

Part B: 6 000 000 hz can we configure a delay of .5 seconds? Show analysis

$$6{,}000{,}000 \text{ hz} \cdot \frac{.5}{1 \text{ sec}} = 3{,}000{,}000$$

Div	ID	Period	
/1	0	3000000	x
/2	1	1500000	x
/4	2	750000	x
/8	3	375000	x

Because the cycle period is greater than the maximum 64kHz limit, ~~for each~~ it's not possible to use 6,000,000 hz all @ .5 seconds

Question 3

a. FRAM Size : ~~128B~~ 128 KB

b. SRAM Size : 2KB

c. TIMER_A modules w/ 3 Channels?
0, 1 or 2 ((from) notes)) 3 from datasheet

d. Timer_A modules w/ 5 channels
0 to 4 (from notes) 2 from datasheet

e. eUSCI modules?
~~0~~ 4

f. Vcc absolute max ratings
4.1V

g. Vcc recommended?
1.8V – 3.6V

h. It is not acceptable because it states running at that temp can cause rapid degradation of components. We should use the recommended settings.

Question 4.

a. Current and freq of VLO

100mA max (same)	min freq	6 kHz
	typical freq	9.4 kHz
	max freq	44 kHz

b. Current and freq of MoDose

25 μA	min	4.0 Mhz
	typical	4.8 Mhz
	max	5.4 Mhz

c. Typical resistor Value + min/max

min	20 kΩ
typical	35 kΩ
max	50 kΩ

d. Max current and power @ 2.2 and 3.0 V

Max 100mA (between ±100mA) @ 2.2V is 220mW power and Vcc Volts

Max 100 mA (±100mA) @ 3.0V 300 mW power Vcc max Volts

e. A0 higher priority

~~0x0FF8, A0~~

~~0x0FE~~

0x0FFE8 A0

0x0FFDE A1

F. TimerC0_A

g. base off (PIPIR)

0200 04

~~04~~

0200 → 0000 0010 0000 0000

04 → 0000 0000 0000 0100

0x0204 → 0000 0010 0000 0100

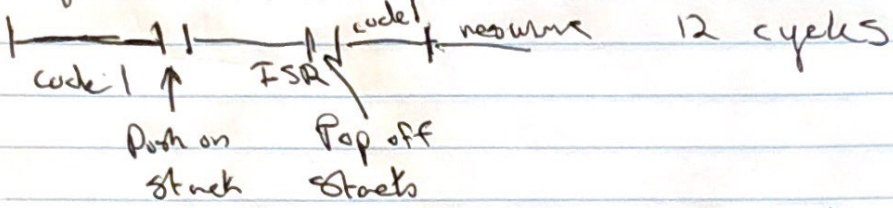
Question 5

a. Channel 1 and 2, who clears interrupt
Users responsible, Software clears interrupt

b. Channel 0
hardware clears ~~flag~~ interrupt

c. PC is pushed on stack when the ~~the~~ interrupt occurs then is retrieved from stack after the ISR

Ex:



d. At interrupt, we push SR on stack and change to zero, ~~After~~ After ISR, It is retrieved Turns CPU back on. 6 cycles

e. Not preemptable because it processes the interrupt at the end

f. Interrupt priority is determined by position in the ~~SR~~ Vector table. The higher it is, the sooner it triggers

g. SR or System reset is the highest priority Vector. located at the top of the vector table (OFFFE) It turns ~~the~~ many systems on and off Including timers, MPU Seg faults, FRAM bit detection.

h. @ active low button the resistor should be pulled down.
@ active ~~bright~~ high, the resistor should remain up.

ex