Analysis

At 32khz in ACLK and continuous mode with a divider of /1.

$$\frac{64 \cdot 2^{10}}{32 \cdot 2^{10}} = \frac{2 \cdot 2^{10}}{2^{10}} = 2 \text{ second delay}$$

where $64 \cdot 2^{10} = 65536$ cycles of the original clock speed
and $32 \cdot 2^{10} = 32768$ cycles of our new ACLK speed we set

Expected

Divisor	Id	Delay	
/1	0	2sec	~7 blinks
/2	1	4sec	~3 blinks
/4	2	8 sec	~2 blinks
/8	3	16sec	~1 blink

20 second Observation

/1 Observable only 7 blinks, does not match Kind of

/2 Observable 3 blinks into 4 almost close

/4 observable 2 blinks as expected yes

/8 observable 1 blink as expected yes