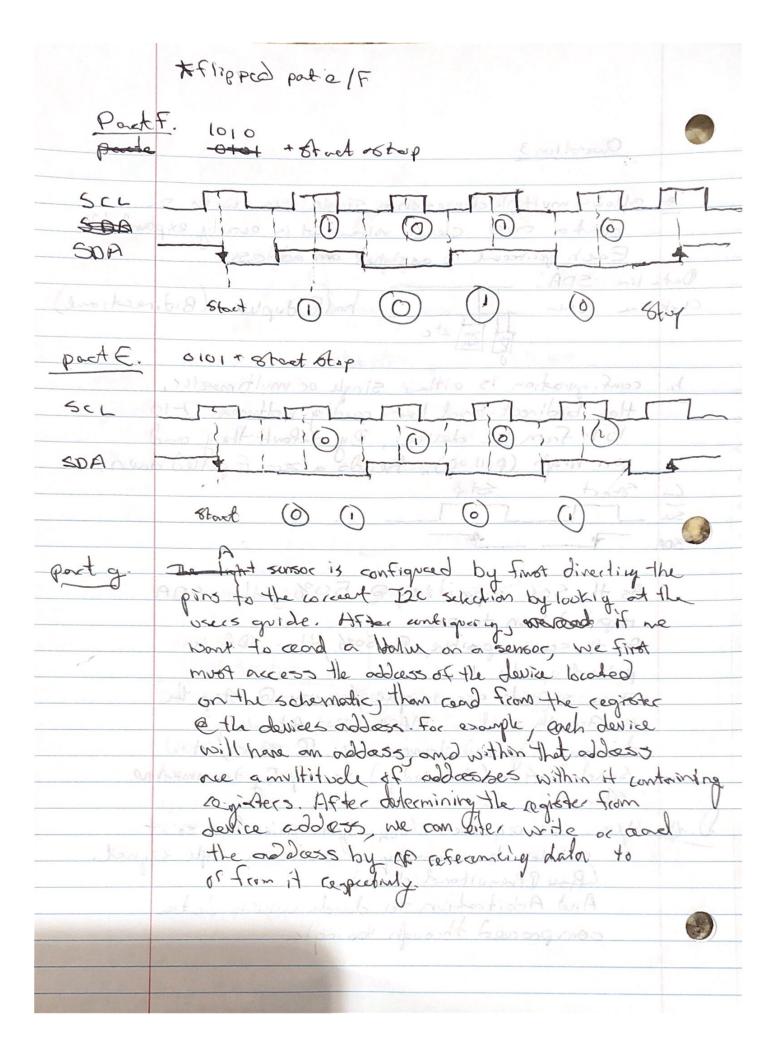
Quedion 1 Pins III RXD PISELI = BLT1 1.2 TXD PISE22 1= BITZ PISEL = (BIT1 | BIT2), ((1,1) PISELA = (BIT1 | BITZ); b. Oversampling is during a transmission rate for UART, the current bandrate would have a secondary signed that would and 16x now thom the bond rate ons long as both systems can handle the Eccopency, Px Forter than TX. Ex. boud rate = 9600 hz onesamp = 16.9600= 153600hz C. yes where smilk = 1948,000 hz (1.048 Mmg) if 9600-16 5 LOYEMBZ them are sampling is 9600-16= 153600 hz < 1,048,000 hz V Oversampling Possible d. No where ACLK = 32768 hz (32Khz) if 9000-16 < 32 Khz then oversampling is 153600 hz = 32768hz X Oversampling not possible e. Dividers and modulators are found by Clock Frequency over our selected band cate or Oversompling.

5 PKLIG @ 32 Hbz n/ 9600 band n/ oversompling 1454 1.048Mhz = 6.82 (14.9600) I modulator, (divide We look @ the family vacsgoids to determine the values
for the cognisters VEBR= Divider, UCBRS= Divider Modulator

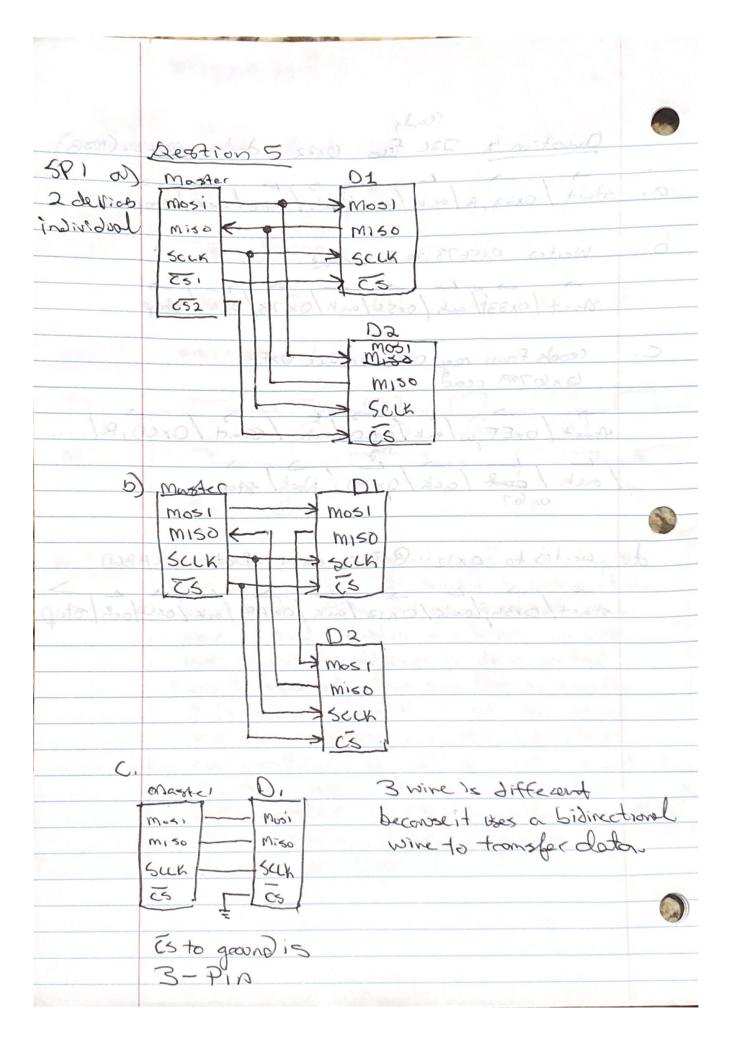
A) Theorem 2: The stop bit, no Flow control Ore stop bit, no Flow control VCACTE = B To 0101 out The stop Idle Stop Idle Stop Idle Stop Idle Stop Idle C. SMCLK IMPO Cothbord UCAICTUWO Down 38,400 Low UCPEN Doton 7 bit UCPEN Frobbit MyB UCMBD Remind even UCSPB Ship even UCSPB UCSPB UCAIBRU I Initialize UART() E UCBRF = 10 UCAICTUWO I UCARFULLEN UCMBD UCTBIT UCAIMCTUW I Tothalize UART () E UCAIMCTUW I E TOTAR UCCEN UCMBD UCTBIT UCAIMCTUW I E TOTAR STOP UCCBRF 3: UCAIMCTUW I E TOTAR STOP UCCBRF 3: UCAIMCTUWE UCBRF 3 UCBRF 1 UCOS16; UCAIMCTUWE I INCOME INCOME INCOME D. IF the configuration document match, that the doule			9
A) 9600 bowd = bit dala no pocity LSB first One step bit no flow control VCACTL = B To 0101 out 1 John 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Queation 2.	
Description of low control Verent = B The old out	(A	9600 boud obit data no marity 158 first	
B TX 0101 00/11 TOLERHAM 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	one star but no start	
B TX 0101 00/11 TOLERHAM 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Maria Carlo	VCACTE = B	
### 100000 00 00 00 00 00 00 00 00 00 00 00	B	A STATE OF THE STA	
Sent 000100 C SMCLK IMM2 cotibertod UCA1CTCWO Donod 38,4000 Low UCPEN Dotod 7 bit UCPAR Fredbit MSB UC MSB Bonity ENON UCSPB UCA1BRW = 1 UCA1BRW = 1 UCBRF = 10 UCBR = 000 UCBR = 000 UCA1MCTLW I Initialize UART() E UCBR = 000 UCBR = 000 UCBR = 000 UCBR = 000 UCA1MCTLW & UCBR UCAN UCSSEL - 3 UCA1MCTLW & UCBR = 000 UCA1MCTLW & UCBR = 0000 UCA1MCTLW & UCBR = 00000 UCA1MCTLW & UCBR = 00000 UCA1MCTLW & UCBR = 00000 UCA1MCTLW & UCBR = 000000 UCA1MCTLW & UCBR = 000000 UCA1MCTLW & UCBR = 0000000 UCA1MCTLW & UCBR = 00000000000 UCA1MCTLW & UCBR = 00000000000000000000000000000000000		Faledhigh 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	6
C SMCLK IMNZ coliberto UCAICTUMO Dond 38,400 Law UCPEN Dolow 7 b.t UCPAR FIRST UCMSO Banto ENDA UCMSO Banto ENDA UCMSO UCSEL 3 UCAIBRW = 1 UCAIMCTLW I Initialize UART () E UCBRS = 000 UCAICTL WO = UCPAR UCPEN UCMSO UCTBIT UCAIMCTLW &= 1 UCBRS 3: (UCBS = 000) UCAI MCTLW &= 1 UCBRF 3 UCBRF 1 UCOS 16; UCAIMCTLW 7 UCAIMCTLW 6			
C SMCLK IMNZ coliberto UCAICTUMO Dond 38,400 Law UCPEN Dolow 7 b.t UCPAR FIRST UCMSO Banto ENDA UCMSO Banto ENDA UCMSO UCSEL 3 UCAIBRW = 1 UCAIMCTLW I Initialize UART () E UCBRS = 000 UCAICTL WO = UCPAR UCPEN UCMSO UCTBIT UCAIMCTLW &= 1 UCBRS 3: (UCBS = 000) UCAI MCTLW &= 1 UCBRF 3 UCBRF 1 UCOS 16; UCAIMCTLW 7 UCAIMCTLW 6	100000000000000000000000000000000000000	set : 00 10 10	6
Dobose 7 b.t UCPAR F. of bit UC PAR F. of bit M5B UC MSB Bonity even UC 5PB UCS 16 UCAL BRW = 1 UCAL WAT UCAEN UCMSB UCTBIT UCAL MCTLW Initialize UART () E UCAL MCTLW UCAEN UCMSB UCTBIT UCAL MCTLW UCBRS3; // UCBRS = 0x0 UCAL BRW = 1° UCAL MCTLW & NCBRF3 UCBRF 1 UCOS 16°; UCAL MCTLW & UCBRF3 UCBRF 1 UCOS 16°; UCAL MCTLW & SRF3 UCBRF 1 UCOS 16°;			
Dobose 7 b.t UCPAR F. of b.t MSB Bonity even UCSPB UCSSEL 3 UCAIBRUE 1 UCBRE U UCBRE UCPAR UCPEN UCMSB UCTBIT UCBRE UCAIBRUE WART UCPEN UCMSB UCTBIT UCAIBRUE 1 UCBRES 3 UCBRES 3 (UCBRES 2 020) UCAIBRUE 1 UCAIBRUE 1 UCAIBRUE 1 UCAIBRUE 1 UCAIBRUE 1	2)	SMCLK IMAZ coliberto	
First Did MSB UC MSB Brita ENEW UCSPB WEAL DOT UCSPB UCAI BRW = 1 UCAI BRW = 1 UCAIMCTLW I Initialize UART () E UCBRF = 10 UCBRF = 10 UCBRF = 070 UCAICTL W0 = UCPAR UCPEN UC MSB UC7BIT UC SPB WAP UCSSEL - 3° UCAI MCTLW &= ~ UCBRS3; (UCBR = 020) UCAI MCTLW &= ~ UCBRF 3 UCBRF 1 UCOS16° UCAI MCTLW & UCBRF 3 UCBRF 1 UCOS16° UCAI MCTLW & G		JE 400 LAW UCPEN	6
UCSEL 3 UCAIBRW = 1 UCBRF = 10 UCBRF = 10 UCBRF = 00 UCBRF = 000 UCBRF = 0000 UCBRF = 00000 UCBRF = 00000 UCBRF = 00000 UCBRF = 000000 UCBRF = 00000000000000000000000000000000000			8
DCSPB UCSSEL 3 UCAIBRW = 1 UCAIBRW = 1 UCAIMCTLW I Initialia UART () { UCBRF = 10 UCBR > = 0x0 UCBR > = 0x0	1:1646	d msB	8
UCAIBRW = 1 UCAIBRW = 1 UCAIBRW = 1 UCBRF = 10 UCBR = 10 UCBR = 0x0		0 701	6
UCAIBRW = 1 UCAIBRW = 1 UCAIMCTLW Initialia UART() { UCBRF = 10 UCBR = 20x0 UCAICTL WO = UCPAR UCPEN UCMSB UCTBIT UC SPB WAD UCSSEL - 3; UCAIMCTLW &= ~ UCBRS3; // UXBR = 0x0 UCAIBRW = 1° UCAIMCTLW = UCBRF3 UCBRF1 UCOS16; UCAIMCTLW = 3		2 Doit UCSPB	
UCAIBRW = 1 UCAIBRW = 1 UCAIBRW = 1 UCBRF = 10 UCBR = 10 UCBR = 0x0 UCAICTL WO = UCPAR UCAEN UCMSB UCTBIT UC SPB WAD UCSSEL - 3; UCAIMCTLW &= ~ UCBR = 0x0 UCAIBRW = 1° UCAIMCTLW = UCBR = 1 UCOS 16; WCAIMCTLW = 1) (a	hone Ucos 16	
UCAIBRW = 1 UCBRF = 10 UCOSIG UCBR > = 0 x0 UCAICTL WO = UCPAR UCPEN UCMSB UCTBIT UC SPB WAD UCSSEL - 3° UCAI MCTLW &= ~ UCBRS3; (UCBPS = 0x0) UCAI MCTLW = ~ UCBRF3 UCBRF 1 UCOSIG; UCAI MCTLW = 1° UCAI MCTLW = 1°		UCSSEL 3	
UCBRF=10 UCOSIG UCBR==00 UCBR==00 UCBR==00 UCBR==000 UCBRE=000 UCBRE=10 UCBRE=			-
UCBRS = 0x0 UCA 1 LT L WO = UCPAR UCPEN UCMSB UCTBIT UC SPBAB WAD UCSSEL - 3° UCA 1 MCTLW &= ~ UCBRS 3° / UCBRS = 0x0 UCA 1 BRW = 1° UCA 1 MCTCW = UCBRF 3 UCBRF 1 UCOS 16°; WEALMET LARE }		VCAIMCTLW / Initialize UART () &	6
UCBRS = 0x0 UCAILTLWO = UCPAR UCPEN UCMSB UCTBIT UC SPBAD WAD UCSSEL - 3° UCAI MCTLW &= ~ UCBRS3; (UCBRS = 0x0) UCAI MCTLW = UCBRF3 UCBRF 1 UCOSI6; UCAI MCTLW = J		UCBRF=107AD Lay Loon Tal = 11. wads	6
UC SPB W WAD UCTBIT UC SPB W WAD UCSSEL-3° UCA 1 MCTLW &= ~ UCBR53; / UCBR5 = 0x0 UCA 1 MCTLW = UCBRF3 UCBRF 1 UCOS 16°; WEALMETIME }		Ocosib Adams of the morning	3
UCAICTLWO = UCPAR UCPEN UCMSB UC7BIT UC SPBAD WAD UCSSEL-3°, UCAI MCTLW &= ~ UCBRS3; // UCBRS = 0x0 UCAI MCTLW = UCBRF3 UCBRF 1 UCOSI6°, WEALMOST LOVE }		UCBRS = Oxo	
UCSPBAR VC55EL-3°, UCAIMCTLW &= ~ UCBR53; //UCBR5 = 0x0 UCAIMCTLW = UCBRF3 UCBRF 1 UCO516°, WEALMOSTINE }		UCASCTLWO = UCPAR UCPEN VCMSB UCTBIT	2
UCAIBRW=1° UCAIMCTUW= UCBRF3 UCBRF1 UCOS16°;		UC SPBAD WAD VCSSEL-3°	0
UCAIBRW=1° UCAIMCTUW= UCBRF3 UCBRF1 UCOS16°;		UCAIMCTLW &= ~ UCBRS3: (LUCBIS = 0x0	
UCAIMCTUWE UCBRF3 UCBRF1 (UCOS16)			6
WERLINGE }			6
D. IF the confincation doesn't match, they the darks	300 80		6
	0	IF the continuation docon't match that the doctor	6
will appear as garbargs.		will appear or markeners	

1 stop coop got of (P) Question 3 allows multiple devices on a single bus with data and clash wire. It is easily explandable Each perstered is assigned an address. half duplex (Bidirections) SCL Clerk line configuration is either single or multimoster, Has bidirectional line gooding between 7-10 bits from the device. By defort they and on high (pull up) a Bends a zero if pulled down. As the SCC is positive, @ 50%, the 50A is pulled down to zero As the sais positive, @ 50% the SDA is pulled up to 1 These signeds are unique because @ Stop the mantecell sevel a NACH (Not Acknowledge) to signify end transmission. @ start, it sends ACK (Acknoledge) to signify I consmissions 8 4tract yes. It agrines clock symchronizertion so it collides harmonionsly to could a siroll signal.

(Asu Presultand clock) -1 And Advitation to decide which data 4 PER can proceed through too logic.



P Question 4 Jac From 0x22 dota = 0x1234 (MSB) Rlack lox 12 lack loxAB / nack / 8fop 0x5678 to IZC 0x33 Start / 02338/ ack / 0256/ack/0278/ack/8top Gx6789 cead. OXEF, Wack loxCo lack / Start loxCo, Rl... / Lock / Ox 89/ Noch. @ J20 0x34 Data 0x ABCD weites to 0x12 start/0x34/Plack/0x12/ack/0xAB/ack/0xcp/ack/8top 6



Question 6 ADC CLK [10-20]hz SHT = 3 seconds and Parta 10-2012 voing highest ocequency for analysis or 3 seconds . 10 = 30 cycles Depending on implementation we could us. 80 cycles for a further coording @ 2012 W/ 60 cycles or 40 cycles for less power consuption @ 10 hz w/30 cycles Part B) Total time = SHT+ Conversion, 5 < 4 therefore 0 2 A SAB 5 > 3 VR theofore 1 BUR . Bit P Bit 1 Bit 1

software stock provides services to the layer above and ofilizes the secures from below. 4 layers to the grouphic steek From the bottom, the displant graphics libery provides info to the driver for Driver software I the bosic parameters for images Display hardware which are size, color composty and The driver uses this info to pass though to the graphic library to correte the images to be displayed, Finally the application uses this to produce the -> Display pulse on ceset to stact/shut display for Dixplay Translates color from > Displang Sends command data -Display (mcu specific)

Pixel cesolution and Ocaphil library

Touch position to Graphic library Provides Draw pixel Function to Craptic library Resolution, color, features and command data is command specific Oses draw Function from driver. Crownter Shapes to be used in application Display agrostic Can be used w/ any driver (displa

0000000000000000 6 A graphics Context is an acea on a display where different of graphic objects can be implemented. It can contain many objects of georphics. The logical display The clipping Region is an ace within the graphic context where images can be displayed. For example you can define an image with the context but if it is not in the clipping region, it want be displayed. Display Context region 6666 6 -0 -P

Overstion 9. b. int get available time to channel (); int get available timer chand () & TAOCCTLO |= CCIE; TAOCCTLO &= 1 CCIFG°, return 0° 3 else if (CTAOCCTLA & CCTE)==0) { TAOCCILA LE VICIFG: 3 etse if (TAOCCTL2 & CCIE)==0) & TADOCCTUZ = COTE;
TADOCCTUZ = NCKIFG;
return 2;
Pelse retven - 1;

	Question 10 Data:
	76543210
	2009 2000
	parta) read bit 4 of data into lemp
	# defina bito Oxxxxx
	# define bit1 0x2001
	# define bita 0x2002
	# define bit3 0x2003
	# define 6:44 Ox2004
	A define bits Oxzas
	# define bith 0x200b
	# define bit) 0x2007
	the despir
	ungiqued it temped
	orginal int temp=00 AptrE7=3&bito, bbit1 &bit2, bb+B, bb+4, bbit5 bitb, bb+73
	temp= * ptr [4]; // part A
	Cemp- pri Las, especial
	pod b)
	DITES DE
	*ptr[5] = new Data;
	part C)
	int n=0; int count=0;
	ist count=0;
	while $(n < 7)$ ξ
	} (= [[[]]] ; [= 0) }
(0)	2 count++;
	7 n++°
	2