Timer_A Help Sheet (Interrupts)

The table below shows the main events in Timer_A, the interrupt enable bits (xIE), the interrupt flag bits (xIFG), the main registers, the configuration registers and the vector mapping.

Timer_A Elements	Event	Bits	Main Register (16-bit)	Configuration Register (16-bit)	Vector
Main	TAR rolls back to zero	TAIE / TAIFG	TAR	TACTL	TIMERA1_VECTOR (shared)
Channel 0	TAR = TACCR0 (compare)	CCIE / CCIFG	TACCR0	TACCTL0	TIMERA0_VECTOR (single-source)
Channel 1	TAR = TACCR1 (compare)	CCIE / CCIFG	TACCR1	TACCTL1	TIMERA1_VECTOR (shared)
Channel 2	TAR = TACCR2 (compare)	CCIE / CCIFG	TACCR2	TACCTL2	

The table below shows the main configuration register of Timer_A.

Fields of TACTL	
TASSELx	Source select [0: TACLK] [1: ACLK] [2: SMCLK] [3: Inverted TACLK]
IDx	Clock input divider [0: Div by 1] [1: Div by 2] [2: Div by 4] [3: Div by 8]
MCx	Mode [0: Stop] [1: Up] [2: Continuous] [3: Up/Down]
TACLR	Clear TAR to zero; Reset clock divider; Reset count direction
TAIE	Interrupt Enable
TAIFG	Interrupt Flag

Interrupt Programming Checklist

- Set the event interrupt enable bit (xIE)
- Clear the event interrupt flag bit (xIFG)
- Set the global interrupt enable (GIE) bit
- Write the ISR and link it to the vector table
- Ensure the ISR clears the interrupt flag (xIFG) – either by hardware or by software