Configurable Digit-Serial Array Architectures for Digital Signal Processing

EXECUTIVE SUMMARY - The next generation of electronic warfare requires reconfigurable Digital Signal Processors (DSP) with order of magnitude improvements in throughput, power, latency, and capacity. Field Programmable Gate Arrays (FPGA) are struggling to keep up with application requirements and have proven to be very difficult to use. Coarse Grained Reconfigurable Arrays (CGRA) promise software programmability, and improve throughput, power, and latency. However, bit-parallel CGRAs lack the capacity for large programs because of the area needed on-chip to route wide datapaths, and digit-serial array architectures reduce the width of the datapath, but sacrifice configurability in the face of complex timing and control. Broccoli is using asynchronous control to solve the complex timing and control problems for digit-serial CGRAs. The resulting chip will easily map and efficiently execute large dataflow applications, opening the door to a diverse set of new capabilities on mobile platforms.

PROBLEM/OPPORTUNITY - Applications in electronic warfare, radar systems, software defined radios, and missile tracking, guidance, and intercept require extremely low latency and high bandwidth processing of radio signals for obstacle and target detection and tracking, state estimation, path planning, jamming, spoofing, beamforming, waveform generation, and other tasks, and are often on mobile platforms with limited power. Today's approaches use advanced FPGAs to handle these tasks efficiently. However, FPGAs are notoriously difficult to program and application requirements have long exceeded the FPGA's capabilities. When energy efficiency isn't absolutely necessary, designers often reject FPGAs in favor of CPU and GPU clusters. Rather than dealing with circuit design, pipeline management, placement and routing, timing, and capacity, they need to focus on adapting their algorithms quickly in response to new threats. When energy efficiency is necessary, designers often need to integrate multiple FPGAs on the board to fit the whole application, dramatically increasing the complexity of the design.

HISTORY - Xilinx introduced the Virtex-II FPGA targeting embedded high-performance applications in 2001, relegating microprocessors to embedded low-performance domains. Since then, FPGA innovations focused on application specific operator integration and network optimization, ease of use, system integration, and run-time partial reconfigurability. However, diminishing returns from architectural innovations, the end of Dennard Scaling, and the decline of Moore's Law have made FPGAs a complex and stale solution for modern embedded DSP.

SOLUTION - Broccoli's asynchronous control natively solves the pipeline management and timing problems in hardware, enabling digit-serial dataflow to dramatically improve capacity and facilitating a turn-key mapping process to allow designers to focus on their algorithms. A request/acknowledge handshake protocol between nodes implements flow control with back-pressure, guaranteeing that a computation will not execute without all of its inputs. Local digit-stream length management allows for variable-length computation, saving energy and increasing throughput. Worm-hole routing allows routing decisions per-stream, ensuring all of the digits in a digit-stream follow the same path through the array. Finally, multiplication and pipelining resources can be allocated on demand, preventing deadlock in several scenarios and increasing total capacity.

BENEFITS - Alongside the digit-serial CGRA's native improvements to throughput, power, latency, and capacity, these control structures automatically allocate arithmetic precision and pipeline slack at runtime allowing the user to focus on their algorithmic performance rather than complex platform specific features. They take advantage of average bit width distributions in the program workload to halve energy-per-operation and double throughput-per-transistor by avoiding computation on unused bits, and untether sequential operator execution from frequency, facilitating lower input to output latency.

CALL TO ACTION - Broccoli is currently focused on three blockers. First, there are very few EDA tools to facilitate asynchronous circuit design. Help us by contributing to and sponsoring open source tools in the community (github.com/sponsors/broccolimicro). Second, there are very few engineers trained in asynchronous circuit design. Help us build that community by taking our course and contact us to help further develop that material (broccolimicro.io/courses.py). Third, we are actively looking for funding to continue our research through grants and sponsorship. Please contact us if you would like to help.

ABOUT BROCCOLI - Broccoli develops efficient configurable platforms for DSP on the edge, specializing in design of complex and non-deterministic control structures that adapt to program workload at runtime.

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