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Fast readout of the Skipper CCD for astronomy and quantum imaging

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ABSTRACT

The Skipper is a special type of charge-coupled device (CCD) that allows pixel measurements with sub-electron noise levels due to its non-destructive readout operation. Over the last decade, these sensors have been used as particle detectors on a variety of experiments, such as the direct detection of galactic dark matter and neutrino experiments. Skipper CCD achieves low-noise by reading multiple times, and sequentially, the pixel charge packet, which translates to longer readout times. This becomes a limiting factor for those applications that require sub-electron detection and faster readout speeds. A novel analysis method for reducing the total pixel readout time is presented in this work. The method relies on analyzing the time-domain properties of the video signal including the clock feedthroughs and their shapes to optimize the clock transitions that define the pixel. The analysis technique is experimentally demonstrated using a standard scientific detector and also with a Skipper CCD with single photon sensitivity. In both cases the sensors are operated and readout using the Low Threshold Acquisition (LTA) controller with an updated firmware for faster clock sequencing. A good compromise between noise performance and total readout time was achieved. This will allows the use of the Skipper CCD and/or the LTA for astronomy, quantum imaging, and other applications that require faster readout times than previous uses of the sensor and the controller.

Keywords: Skipper CCD, Single Photon, Fast Readout, Quantum Imaging, LTA controller

1. INTRODUCTION

Skipper CCDs are widely used in applications that require the ability to count single electrons, such as dark matter detection[1–3] and neutrino experiments.[4] These applications do not usually require high readout speeds in data collection due to the low rate of background signal reaching the sensor. However, there are still a large number of applications that could benefit from the low noise threshold of the sensor but they are still limited by the readout speed. Among these applications, we can mention quantum imaging[5,6] and ground-based and space-based astronomy.[7,8] To achieve low noise, the Skipper CCD relies on reading the pixel multiple times[9,10] (each of them called samples), which increases the overall pixel duration. Due to the lack of readout time restrictions in the current applications, the readout speed is a few dozens of kilo-samples per second.

Different alternatives exist to speed up the readout process. Some applications may restrict the low-noise section of the image to regions of interest.[11] Other applications can use an energy threshold to turn on and off the low-noise readout capability.[12] Finally, when low-noise is required over the entire image, decreasing the pixel time is the alternative to speed up the readout process. One of the objectives is to show that the Skipper-CCD, when using a single sample per pixel, can achieve a similar readout speed of standard CCD used

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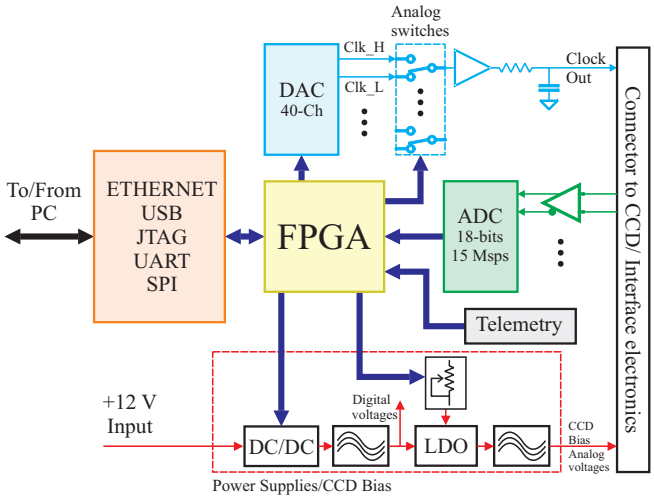


Figure 1: Block diagram of the main hardware components in the Low Threshold Acquisition (LTA) controller.

in astronomical applications.[13] The results show that single electron resolution can be achieved using a readout speed of approximately 200 kilo-samples per second and 900 samples per pixel. The proposed method allows to optimize time-noise trade-off to speed up a system without modifying the existing electronics. Optimizations of the front-end electronics can be done in later stages to achieve even better performance or to subsequently repeat the optimization.

In addition to the noise analysis method presented for pixel-time reduction, a firmware update to the Low Threshold Acquisition (LTA) controller[14] is introduced to allow fast clock sequencing. No hardware modification were made to the controller, the new firmware includes a "time procesor" that integrates the so-called timed instructions, which can be executed at specific times. The synchronized raw video acquisition capabilities of the LTA are exploited for the noise analysis technique presented in this paper.

The paper is organized as follows. Section 2 introduces the LTA readout system that was used for the experiments with the new firmware solution to control the clock signals at the required speed. An statistical analysis for the readout speed optimization using the video signal is presented in Section 3. Experimental results and the application of the proposed method are shown in Section 4, which also includes a summary of the steps that could be applied to reduce the readout time while keeping the noise bounded. Finally, the conclusions can be found in Section 5.

2. LOW THRESHOLD ACQUISITION READOUT SYSTEM

The LTA is a system that allows the simultaneous readout of up to four video channels, and integrates the bias voltages and control required to readout a CCD on a single board.[14] The board includes programmable fixed-voltage bias sources, nano-second accurate timing signals with programmable low and high voltages values for moving the charge on the CCD, four analog-to-digital converters running at 15 MSPS with low-noise differential input, telemetry and 1 GB Ethernet data transmission. The core of this board is a Xilinx Artix XC7A200T FPGA, which provides the necessary control signals for the different components and interacts with the user through a Ethernet-capable terminal window. The FPGA firmware can be easily modified for testing and debugging different CCD's control strategies. In its basic implementation, the pixel value is computed by digitally applying a Dual Slope Integration (DSI, also known as Correlated Double Sampling (CDS)) technique over the ADC output samples. A block diagram of the LTA is shown in Fig. 1. In the core of the diagram is the FPGA, in light blue is the CCD clocks generation using a 40 channels DAC, analog switches and operational amplifiers. In green the 18 bits analog-to-digital converters are indicated. There are also digital voltages sources and CCD bias that are implemented with DC/DC converters, filters and a low-drop-out (LDO) voltage regulator. Also, the communication block that includes Ethernet, USB, JTAG, UART and SPI, and a telemetry block to measure actual clock and bias voltages.

The following sections highlight some features of this system, specially those that were particularly useful for the development of this work. For a more detailed description refer to.[14]

2.1 Oscilloscope mode

A simplified diagram of the firmware running on the FPGA of the LTA board can be seen on Fig. 2. The main processor of the FPGA is the Xilinx IP processor μBlaze ®. It also has a dedicated processor in charge of generating the clock sequence (Seq block). In the new firmware reported in this work, the sequencer is implemented using a time critical processor. There are four digital inputs coming from four independent 18-bit, 15 MSPS ADCs. These incoming data streams are routed to both the Dual Slope Integration (DSI) and, a so-called, Smart Buffer block. The latter provides some basic functionality for raw video capture and data analysis. The Smart Buffer can capture 65536 ADC samples at full speed, with option to synchronize the capture with a trigger signal which is controlled by the clock generator sequencer or tProcessor, which will be described on a separate section. Depending on the pixel time, the capture buffer can represent hundreds of raw pixels of the video signal. The intention of this oscilloscope mode is not to compute an entire image, but rather to help with synchronizing the pixel structure, integration window and other debugging purposes. For convenience of use, a CSV file is created for further processing. This module gives the user the ability to evaluate noise performance and correlation, optimize readout speed and detect problems in the video chain. This mode of operation was crucial to perform the data analysis required to achieve a significant reduction of the pixel time.

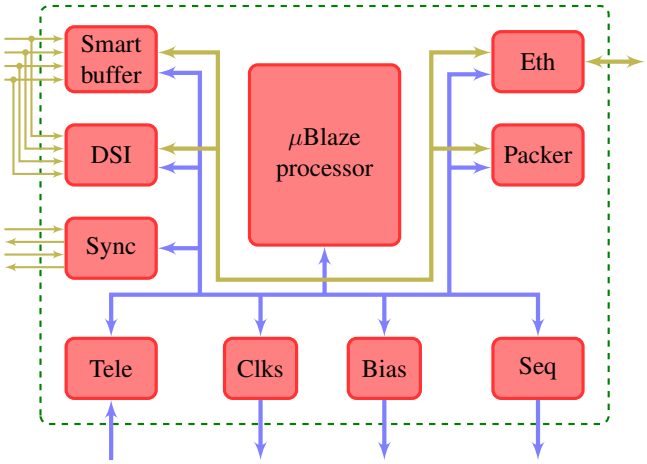


Figure 2: Details of the FPGA firmware.

2.2 The time processor (tProcessor)

The pixel charge is moved across the CCD using a sequence of transitions of clock signals. Shorter pixels times require to squeeze the pixel readout structure, which calls for an increased number of clock transitions per unit of time.

The sequence of events is generated with a custom processor referred to as tProcessor or tProc. It provides generic instructions for data movement, arithmetic, bit-wise operations and loops, which are used to write the basic structure of the readout sequence. This processor includes the so-called timed instructions, which can be executed at specific times. Timed instructions are used to create time-critical events, these events are state changes of the clocks that drive the CCD that must occur at specific moments of time . The block diagram of the tProc can be seen in Fig 3.

The tProcessor has an AXI interface that is connected to the main Micro Blaze processor that controls the board (From μBlaze). This allows to set a few registers that control the start source and data memory write and read. The data memory can be accessed when running programs on the tProcessor and can be initialized for holding clock states or general looping variables. The Run Control block (Run Ctrl.) indicates when the tProcessor is running and allows to synchronize the end of image capture at the user level. The core of the

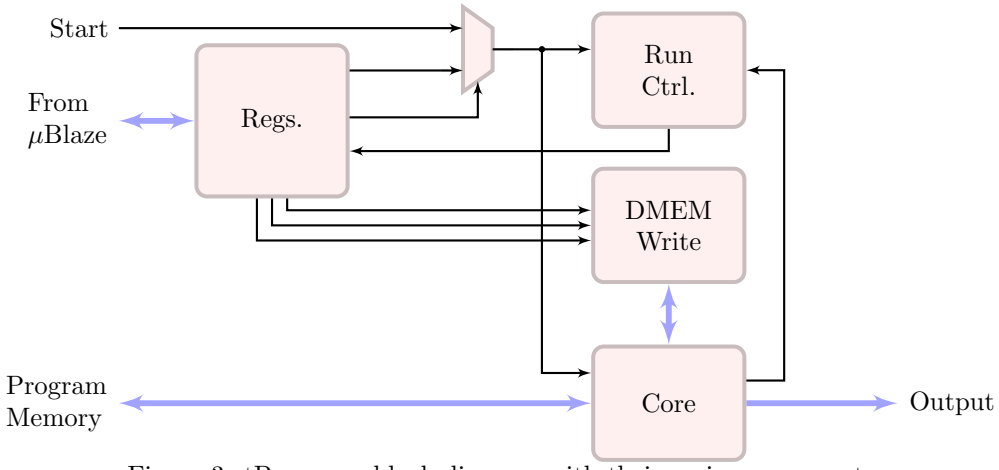


Figure 3: tProcessor block diagram with their main components.

tProcessor is build by using a standard processing pipeline around five stages: Instruction Fetch (IF), Instruction Decode (ID), Execution (EX), Memory Accesss (MEM) and Write Back (WB), which are part of the Core block. The IF stage fetches the next opcode from the instruction memory and updates the Program Counter to either the next instruction or the jump address. ID stage will apply most of the control logic to control the register file source/destination, Arithmetic Logic Unit (ALU) functions and memory address. During the EX stage, the ALU computes the required operation for either register write back, memory address or time computation. Data memory is read or written during MEM stage. Finally, WB stage generates the register file and timed-fifo write control signals. The core implements some advanced features like hazard control, data forwarding and fast jump address computation. This allows to run an algorithm without almost any gap. In average, the core will execute one instruction per clock cycle. Branch prediction was not implemented as the fast jump computation logic will penalize only by 1 cycle the conditional branching instructions. All other instructions run at full speed moving through the pipeline.

Timed instructions make this block different from standard processors. To decouple core execution time from real-time operation of the timed events, the tProcessor has a dual clock-domain FIFO that allows queuing timed-instructions for future execution. This queue is read from the output side at a different clock speed, usually synchronized with the ADC sampling frequency. The associated logic reads the instruction together with a time stamp, and executes the required functionality at the time specified. To keep the timed-machinery as simple as possible, timed instructions make use of two components for accurate event scheduling: Master Clock and Time Offset register. The master clock is a counter that starts counting when the software starts at address 0 and never stops. The time offset register t_{off} acts as a time reference for timed-instructions. It can only be manipulated with special instructions and is used to compute the absolute time at which the timed-instruction needs to be executed. As way of example, let's say the processor starts executing and a timed instruction is scheduled to happen at time 150. This means that when the master clock reaches 150, that particular instruction will be executed. In the case of looping through an algorithm, having to specify absolute times would be rather difficult. The processor includes special instructions to sync the time offset register. Back to our example, let's imagine the algorithm needs to loop 10 times executing the timed instruction at time 150 for the first time, at time $T + 150$ the second time, at $2T + 150$ for the third time, and so on. Using the sync mechanism, the user would need to provide the timed instruction with a specification of 150 and then a sync instruction with T as the value. The first execution of the loop will have a value of 0 for t_{off}, and the timed instruction will be scheduled to happen at 150 units. After the first sync instruction is provided, the internal t_{off} register will be set to T. On the second pass of the loop, the timed instruction will be scheduled at a time $t_{off} + 150$, resulting in an absolute time of $T + 150$. This process continues until the loop is completed. In summary, when the processor decodes a timed instruction it will compute the absolute time with the time offset register before dispatching it into the timed-instruction control queue. This simple mechanism simplifies the procedure to specify time-critical events, and lowers the number of bits that are needed to specify the time tag. Additionally, because the absolute time

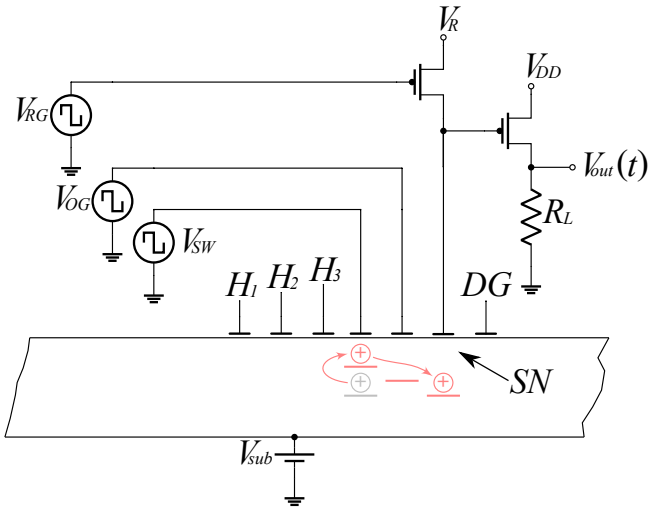


Figure 4: Skipper CCD output stage including the output transistor amplifier and reset transistor. Also shown are the horizontal clocks (H_1, H_2 and H_3), the summing well clock (V_{SW}), output gate clock (V_{OG}), reset gate clock (V_{RG}) and dump gate (DG). The sense node (SN) is indicated with a dark rectangle.

of instructions is computed before dispatching them into the time queue, the processor can continue decoding and looking ahead of the program as the synchronization mechanism is nothing but defining a time reference for instructions.

3. RAW VIDEO SIGNAL ANALYSIS

In this section a raw video analysis method based on the capabilities of the readout electronics previously described is presented. This method is used to increase the readout speed of two types of CCDs sensors: a standard scientific grade CCD with floating diffusion sense node[15] and a Skipper CCD with floating gate sense node that allow multiple nondestructive readouts and sub-electron readout noise capabilities.

3.1 Standard CCD and Skipper CCD

The output stage of the Skipper CCD is presented in Fig. 4. It has the horizontal clocks (H_1, H_2 and H_3) used to transfer the charge along the horizontal or serial register, a sensing node, the reset gate clock (V_{RG}), the dump gate (DG), the output gate clock (V_{OG}) and the summing well clock (V_{SW}).

Using the horizontal clocks, the charge of one pixel in the serial register is transferred to the summing well (SW). After that, the sense node (SN) is reseted via the reset gate, setting a reference value for the charge measurement known as *pedestal* level. The charge is then transferred to the specially designed floating SN,[9] passing through the OG, where it is measured; this value is known as *signal* level. The pixel value is obtained by ADC sampling of the raw video signal and applying a digital equivalent of the Dual Slope Integrator (DSI), computing the difference between the signal and the pedestal levels. The charge packet is then returned to the SW using the OG and the process is repeated a total of N_{SAMP} times, resulting in independent measurements of the same charge packet. Finally, the charge is discarded through the dump gate (DG). Averaging the N_{SAMP} measurements of each pixel the noise is reduced as $1/\sqrt{N_{SAMP}}$.

The operation of the standard CCD is simpler since it does not have the ability to return the charge back to the SW to perform multiple non-destructive readouts. Because of this, the OG is set to a fixed voltage and is not changed. Once the charge has been measured one time, it is discarded when the sense node is reseted. The DG is not present in this CCD.

The total readout time of a full CCD in seconds, assuming a single readout amplifier, is given by

$$t_{rout} = \{[(t_{pix} N_{SAMP} + t_H) N_{COL}] + t_V\} N_{ROW} \quad (1)$$

where t_{pix} is the readout time of a single pixel sample, N_{SAMP} is the number of measurements (samples) of each pixel ($N_{SAMP} = 1$ for standard CCDs), t_H is the horizontal time required for the clock sequence of H_1, H_2 and H_3, N_{COL} is the number of columns, t_V is vertical time required to transfer each ROW of the CCD to the serial register and N_{ROW} is the number of rows.

For a Skipper CCD N_{SAMP} in (1) may take any value, in[14] this value has been tested experimentally up to 5000 samples. The true pixel total readout time, taking into accounts the dead times introduced by the clocking sequences is given by

$$\hat{t}_{pix} = \frac{t_{rout}}{N_{COL} N_{ROW} N_{SAMP}}. \tag{2}$$

3.2 Video signal analysis

One of the objectives of this work is to reduce $\hat{t}_{pix}$ in a controlled manner without excessively increasing the noise. A raw "pixel model" is obtained by averaging the signal structure of many empty pixels. This pixel model captures the average effect of all the feedthroughs of the clocks in the pixel signal.

This signal is subtracted from each raw pixel measurement obtaining as a result a noise instance for each pixel. A covariance analysis of the noise is finally done.

The proposed analysis method is described mathematically. The first step, is to remove the individual offset of each raw pixel, produced by the reset noise, which results in a different pedestal level for each pixel. A few averaged samples at the beginning of the pedestal interval or end of the single level can be use for this purpose. After this subtraction, there are $0 \leq i < M$ instances of raw pixels $P_i[n]$ with $0 \leq n < N$ (not to be confused with the Skipper samples). The pixel model is computed as the expected value $\mathbb{E}$ of the empty pixels $P_i[n]$ as

$$\mathbb{E}\{P_i[n]\} \cong P_M[n] = \frac{1}{M} \sum_{i=0}^{M-1} P_i[n] \qquad 0 \leq n < N; 0 \leq i < M \tag{3}$$

where each raw pixel instance P_i is aligned and synchronized with each other; the average is computed over the instances for the same sample instant.

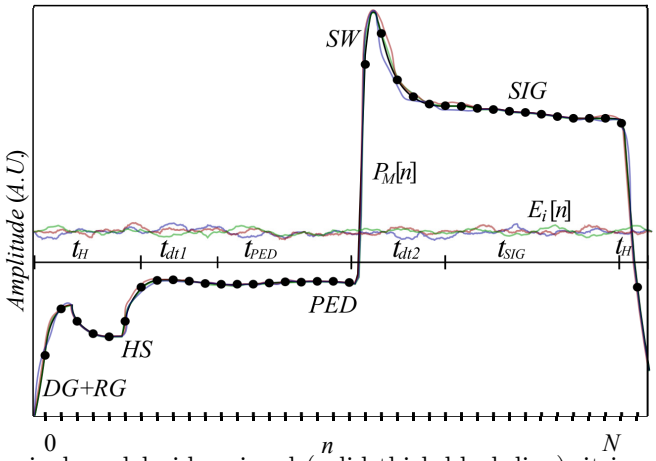


Figure 5: Illustration of the pixel model video signal (solid thick black line), it is possible to identify the effect of dump and reset gate ($DG + RG$), the swing due to the horizontal clock sequence (HS), both comprise the t_H zone. Following, is the pedestal (PED), and the signal (SIG) windows, with the summing well (SW) between them. Also, three error instances denoted with $E_i[n]$ are illustrated.

In Fig. 5, a pixel model $P_M[n]$ (solid thick black line) computed from three raw video signals $P_0[n], P_1[n], P_2[n]$ (colored thinner lines below $P_M[n]$), is illustrated. Subtracting the raw pixel model $P_M[n]$, to each raw pixel video signal results in error instances

$$E_i[n] = P_i[n] - P_M[n] \qquad 0 \leq n < N; 0 \leq i < M \tag{4}$$

Fig. 5 also illustrates these error instances. For fast readouts, as the integration periods are shortened (signal and pedestal levels), the feedthroughs from the clocks that couple into the video signal become closer or over the integration regions. As this happens, the noise might no longer be stationary and the correlation between samples could be higher. To further analyse the noise we calculate the covariance matrix C using the noise instances computed in (4), each element n, m of the matrix is calculated as[16]

$$C_{n,m} = \frac{1}{M}\sum_{i=0}^{M-1}(E_i[n]-\mu[n])(E_i[m]-\mu[m]) \quad 0 \leq n < N; 0 \leq m < N; 0 \leq i < M \tag{5}$$

where the statistic is again computed over the instances and not over the time samples and it is assumed that $\mu[n] = \mathbb{E}\{E_i[n]\} = \mathbb{E}\{P_i[n] - P_M[n]\} = \mathbb{E}\{P_i[n]\} - P_M[n] = 0$. This is done to capture the non stationary nature of the correlation between samples.

In Fig. 5 the typical feedthroughs patterns are also illustrated. Two of them are produced by the dump gate (DG) and reset gate (RG) within the initial (final) part of a pixel measurement. These feedthroughs are usually big because they are produced by clocks signals applied very close to the sense node with a high coupling, and therefore they have a higher impact in the noise. A softer swing is caused by the switch of the horizontal clocks (HS). The summing well (SW) causes a considerable feedthrough in the video signal between the pedestal and signal levels, although it is not as abrupt as the DG and RG, it is critical since it is followed by the signal integration region. This feedthrough will propagate along the signal level and will have a direct impact in the readout noise. The SW clock was kept high during the signal interval and, because of this, a jump between pedestal and signal intervals is observed (despite there is no charge in the pixel).

Reducing the integration intervals to reduce the pixel time also implies working closer to the feedthrough which could increase the noise, not only because of the noisier samples but also because the detector gain can be reduced. If the signal interval is very close to the time instant where the SW is set to high, then the charge packet will not be completely settled in the video signal when it is being integrated, this is seen as a reduction of the gain.

From Fig. 5 it can be seen that $t_{pix} = t_{dt1} + t_{PED} + t_{dt2} + t_{SIG}$, where t_{dt1} indicates the dead time of the pedestal integration window and t_{dt2} the dead time of the signal integration window. These are resting time intervals with samples that are not being integrated in either the pedestal ($t_{dt1} + t_{PED}$) nor the signal window ($t_{dt2} + t_{SIG}$). These dead times increase the integration windows while the real number of samples being used to compute the signal and pedestal levels are only the ones contained in t_{PED} and t_{SIG}:

$$PED = \sum_{n \in t_{PED}} P_i[n], \quad SIG = \sum_{n \in t_{SIG}} P_i[n], \tag{6}$$

where $n \in t_{PED,SIG}$ indicates summing over all the sampling instants n that are contained in the time intervals t_{PED} and t_{SIG} respectively. Each pixel value is computed as $PIX = SIG - PED$. If either the noise of SIG or PED is increased, the noise of the pixel value will increase.

As assumed in this analysis, the noise random process $E_i[n]$ could be non stationary, with some sampling instants n being noisier than others. The diagonal of matrix C, which is obtained from equation (5) for $n = m$ represents the variance of the noise for different sampling instants

$$\sigma^2_{n=m} = \mathrm{diag}(C) = \frac{1}{M}\sum_{i=0}^{M-1}(E_i[n]-\mu[n])^2 = \frac{1}{M}\sum_{i=0}^{M-1}(E_i[n])^2 \quad 0 \leq n = m < N \tag{7}$$

In this situation, sample instants n with higher $\sigma^2_{n=m}$ should be avoided for computing the pedestal o signal levels.

The variance of either SIG or PED (assuming a pixel with no charge) in (6) is given by the variance of the

sum of the random process $P_i[n]$, for example, for the pedestal

$$\begin{aligned}\mathrm{Var}\,(PED) &= \sum_{n\in t_{PED}} \mathrm{Var}\,(P_i[n]) + 2 \sum_{n,m\in t_{PED}, n<m} \mathrm{Cov}\,(P_i[n], P_i[m]) \\ &= \sum_{n\in t_{PED}} \sigma^2_{n=m} + 2 \sum_{n,m\in t_{PED}, n<m} C_{n,m} \end{aligned} \tag{8}$$

where we used that $\mathrm{Var}\,(P_i[n]) = \mathbb{E}\{(P_i[n] - P_M[n])^2\} = \mathbb{E}\{(E_i[n])^2\} = \sigma^2_{n=m}$ and

$$\begin{aligned}\mathrm{Cov}\,(P_i[n], P_i[m]) &= \mathbb{E}\{P_i[n]P_i[m]\} - P_M[n]P_M[m] \\ &= \mathbb{E}\{(E_i[n] + P_M[n])(E_i[m] + P_M[m])\} - P_M[n]P_M[m] \\ &= \mathbb{E}\{E_i[n]E_i[m]\} \\ &= \mathrm{Cov}\,(E_i[n], E_i[m]) \\ &= C_{n,m} \end{aligned} \tag{9}$$

using that $\mathbb{E}\{E_i\} = 0$. The same deviation could be computed for the SIG level. Equation (8) shows that an increase in correlation between samples (covariance increases) would result in increase in the noise of the pixels. For this reason highly correlated samples should be also avoided.

4. EXPERIMENTAL RESULTS

The Low Threshold Acquisition (LTA) controller was used as the readout electronic. A new firmware was developed aiming to manage time critical events for generating the clocking sequences as described in Section 2.2. Using the oscilloscope mode of the LTA board it was possible to collect raw video data and to calculate the error instances and the covariance matrix described in the previous section to analyze the clocks signal impact on the video signal. The correlation patterns revealed, that the resultant noise could be non-stationary, i.e., statistical moments depend on the specific time instants in the pixel signal. The aforementioned analysis was applied to two scientific detectors, one is a standard CCD, and the other one is a Skipper CCD with nondestructive readout that is being developed for astronomy applications,[17] this requires faster readouts times than previous applications for Skipper CCDs.[3] Both sensors were tested using the experimental setups shown in the top and the bottom of Fig. 6a respectively. Both of the setups have the CCD detector inside the dewar under vacuum conditions at a working temperature of 140$^{\mathrm{o}}$K, connected to the LTA readout system presented in the Section 2.

Fig. 6b also shows a sample image with cosmic-rays events and other interactions, obtained with the standard CCD detector after its readout time optimization. The single white dots, are produced by a X-ray source located inside the cube, near the detector, used to calibrate the gain of the system. An overscan region at the right of the image it also appreciated.

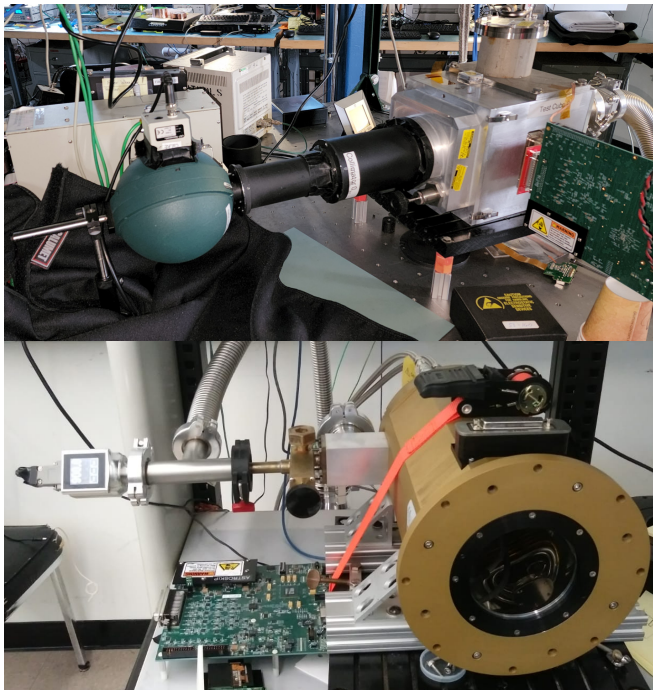
4.1 Readout time optimization for the standard CCD

As mentioned in Section 2 the LTA can store up to 65536 ADC samples per raw video file, that is equivalent to around a thousand raw video pixels per file at the actual readout speed. To perform this analysis, 150 raw video files were acquire to have a large enough number M of pixel instances. Applying the analysis described in Section 3.2 the pixel model along with the error instances were calculated.

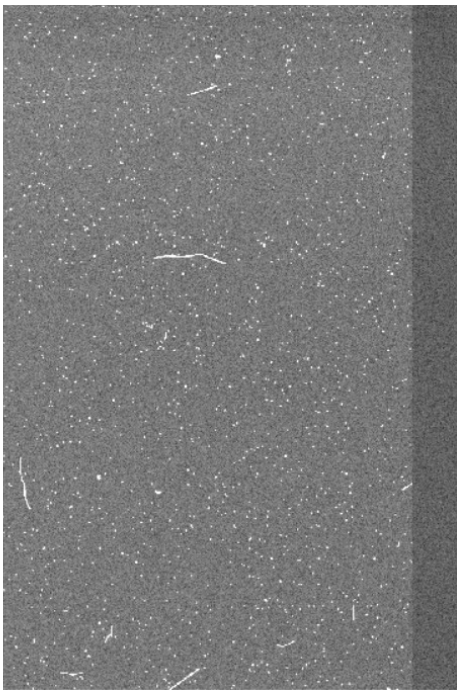
In Fig. 7, 1000 error instances $E_i[n]$ are shown from a total of around 100k that have been used for the analysis. It can be seen that when the pixel model $P_M[n]$ has clock feedthorughs, the samples are noisier.

The covariance matrix is presented in Fig. 8. As there are certain samples that have much higher correlation than others, in order to achieve a good visualization, absolute value was applied and the maximum value was saturated to a value of 1500 ADUs.

Five areas of interest have been marked in the figure using squares. The first one, $DG + RG$, corresponds to the effect that the dump gate and the reset gate have on the video signal, the bottom row and right column of the figure also corresponds to the effect produced by $DG + RG$. The correlated noise is very high, and all



(a)



(b)

Figure 6: (a) setups used to do the measurements with the standard CCD (top) and Skipper CCD (bottom). (b) image with cosmic and X-ray events taken with the standard CCD.

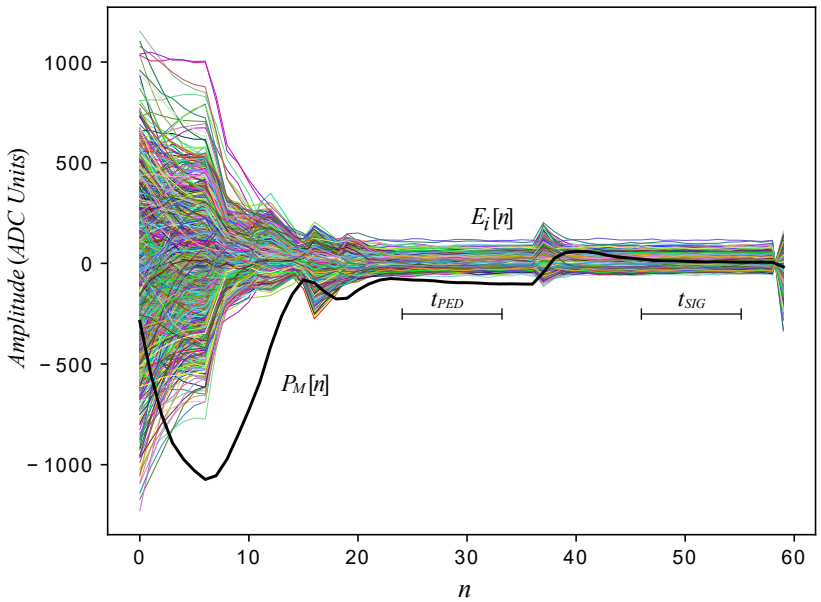


Figure 7: A thousand instances of noise $E_i[n]$ and superimposed and scaled (in black) the pixel model $P_M[n]$.

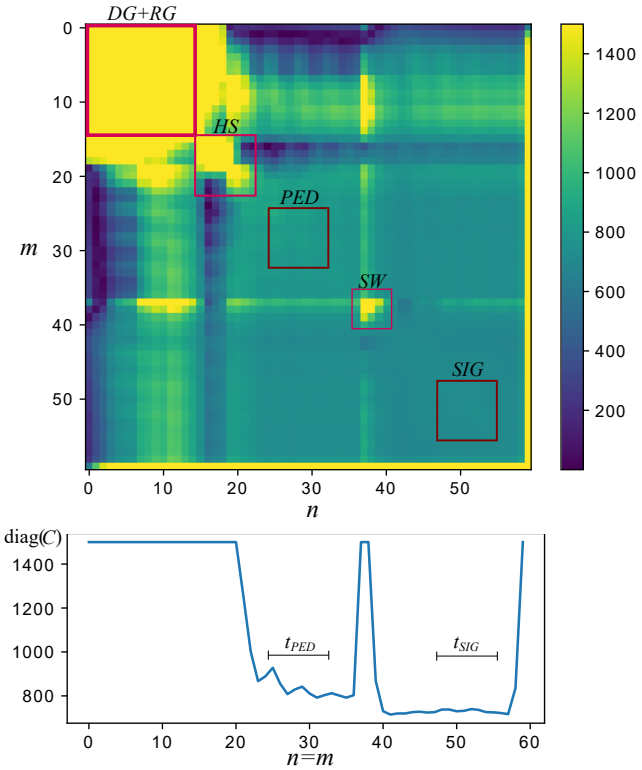


Figure 8: At the top the covariance matrix for a data set of the standard CCD setup, where the most important zones have been indicated, dump gate and reset gate, horizontal clocks, pedestal integration, summing well feedthrough and signal integration. At the bottom, the diagonal of the covariance matrix (the noise variance) is shown.

this area is in the saturation value. The next zone that is indicated with HS, corresponds to the small swing that the horizontal clocks (H_1, H_2, H_3) produce in the video signal, most of this area is also in the saturation value, indicating a high correlation of the samples produced by the horizontal clocks feedthorughs. The third area (PED) corresponds to the samples that are integrated during the pedestal interval, a faded and very slight pattern of yellow dots is observed within this window. The fourth region of interest corresponds to the summing well (SW) feedthrough, it can be seen that it generates a correlation pattern for the samples in the same columns and rows (n and m constants). Finally, the last region (SIG) is the one that corresponds to the samples that are integrated during the signal level. The integration windows $(PED$ & $SIG)$ should be chosen in the regions with low correlation and away from high correlated samples (yellow color) in the matrix.

In the bottom part of Fig. 8 the diagonal of the covariance matrix $\sigma^2_{n=m}$ is shown, also, saturated to a maximum absolute value of 1500 ADUs. From this graph, it is clearer that the signal and the pedestal integration regions framed in the matrix are avoiding the noisier samples. Different diagonal values in the matrix and non diagonal symmetry is a sign of a non stationary noise that is added to the video signal in addition to the stationary noise added by the output MOS transistor of the sensor.

Using the information gathered from the covariance matrix, and following the steps later described in Section 4.3, it was possible to reduce the total pixel time $\hat{t}_{pix}$ from 27.63μS to 4μS, achieving a time reduction of 6.9 times, with an increment in the noise from $2.5e^-$ to $7e^-$ (2.8 times) as expected if the noise of the output transistor is the dominant source. This is the first time this speed-noise performance is achieved with the LTA. In the top of Fig. 9 a fragment of the raw video signal that includes the measurement of 7 pixels is shown. In the bottom part, a zoom of the $4\mu S$ pixel achieved for this detector is shown (sample time $T_s = 66.6$nS). The noise was measured in the overscan region for a value of 42 ADUs with a gain of 6 ADU/e^-.

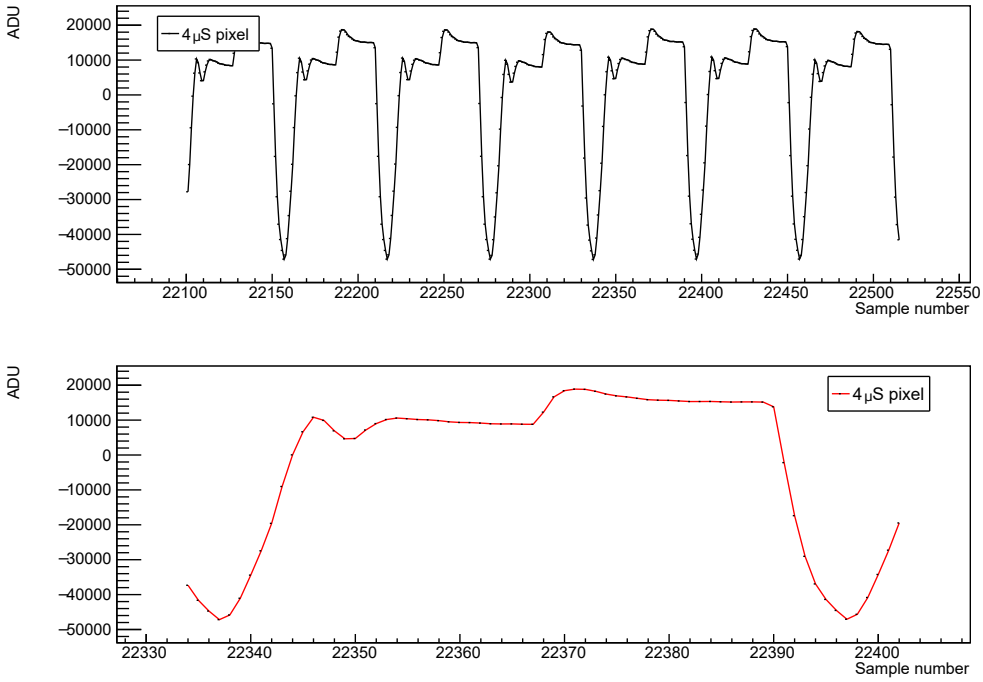


Figure 9: Top image: raw video signal of 7 pixels; Bottom image: zoom of a single pixel (sample time $T_s = 66.6$nS; $t_{pix} = 4\mu S$).

4.2 Skipper CCD

Following the same procedure than for the standard CCD, presented in the previous subsection, it was possible to speed up the Skipper CCD readout time. For an image of dimension 154×450, and using $N_{SAMP} = 900$ nondestructive measurements per pixel, it was possible to obtain single electron counting with a total image readout time $t_{rout} = 316$s, resulting in a single Skipper sample time of $\hat{t}_{pix} = 5.071$ μs while keeping the single electron resolution of the sensor. This is a high reduction compared to previous applications of the Skipper sensor where $\hat{t}_{pix} \approx 45$ μs.[3] For the optimization of the Skipper CCD readout time, the correlation analysis revealed that it was critical to perform the resets (RG) as far away from the beginning of the pedestal integration region in the skipping sequence (multiple readouts) as possible, to prevent the noise from increasing abruptly when skipping at high speeds.

Fig. 10 shows a histogram computed by using part of the pixels in the active region of the sensor. The single-electron capability of the Skipper CCD can be observed, as peaks at integers number of electrons emerge over the noise. A fitting of the histogram was computed and is also shown in Fig. 10 with a solid red line. The fit was calculated using a sum of normal distribution, similar to the one presented in,[18] but assuming electron peaks separation to be perfectly equidistant:

$$\sum_{k=0}^{N_{pk}} \frac{A_k}{\sigma\sqrt{2\pi}} e^{\frac{-(x-\mu_k)^2}{2\sigma^2}} \tag{10}$$

where N_{pk} is the number of peaks fitted by the model, A_k represents a constant that scales each peak in the histogram, x are the bin centers in ADU, μ_k is the mean or peak centers of each of the Gaussians, also in ADUs and with the restriction $\mu_k - \mu_{k-1}$ to be constant (each electron multiplicity should have the same separation). σ is the standard deviation of the noise, which is considered constant in our model because the noise is independent of the charge packet, σ is the readout noise of the system.

The readout noise of the pixels measured in the overscan was $0.35e^-$ which is similar to the expected value from the extrapolation of the noise for one sample reduced by the square root of the number of samples. The

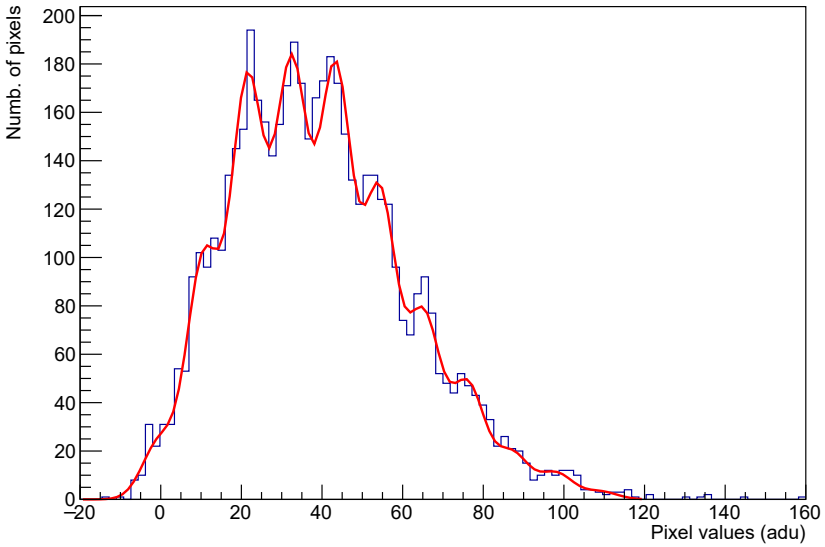


Figure 10: Histogram produced with a fraction of the pixels in the active area. Single electron peaks of the Skipper CCD are observed even when the readout speed has been dramatically increased.

gain of the system is $\mu_k - \mu_{k-1} = 10.92\text{ADU}/e^-$ which was calculated using the difference between the peaks in the fit of figure 10.

4.3 Summary of basic steps to reduce readout time

Based on what has been presented in this work we introduce a series of guidance steps that can be followed to reduce the readout time of an standard CCD detector or Skipper CCD, while keeping the noise at reasonable levels. As a general consideration, it is important to track possible gain changes during each of the steps, if the gain is reduced dramatically, there will be a severe impact in the noise. This is an iterative procedure and the order of the steps maybe altered depending on the performance of the sensor.

- Take an image in a good noise condition with larger pixel period and dead times. For this step the pixel time could be as long as necessary. Register the noise, gain and timings of the clock sequences.
- Without modifying the integration parameters t_{PED} and t_{SIG}, start increasing readout speed by shortening the dead times t_{dt1} and t_{dt2} (see Fig. 5), without increasing the noise significantly. The idea on this step is to reduce any extra delay that does not have impact in the noise performance.
- In this point the integration parameters t_{PED} and t_{SIG} should be shortened to reduce the readout time, it is expected that the noise will increase. Start by reducing t_{PED} and t_{SIG}, until the noise has a reasonable value for the application, without changing t_{pix} by compensating with an increase in the dead times. In this way any noise increase caused by the proximity of the integration periods to the feedthrough pulses is avoided. The dead-times t_{dt1} and t_{dt2} will be optimize in the following steps.
- Using the synchronized raw video acquisition verify that the end of t_{PED} is aligned with the beginning of the rising edge produced by the summing well feedthrough, and to verify that t_{SIG} ends before the falling edge generated by DG and RG.
- Take raw video files and implement the analysis presented in Section 3, use the information of the covariance matrix to reduce t_{dt1} and t_{dt2} until reaching the maximum tolerable noise for the application. The intervals t_{PED} and t_{SIG} should be located where the samples have lower variance and covariance. As the noise could be not stationary and therefore, using or discarding a single sample for the integration can have a significant impact on the noise.

- Normally t_{pix} is larger than the time required by the horizontal clocks, t_H. If after applying the previous steps t_H is a big portion of the pixel time. It is possible to consider decreasing t_H. This is because at this point t_{pix} and t_H contribute the same to $\hat{t}_{pix}$. If t_H is reduced, it might be necessary to repeat the last step.

5. CONCLUSIONS

This work presented an analysis technique to reduce the readout speed of single electron sensitivity Skipper CCDs or standard scientific CCDs using synchronized raw video signal acquisition. This type of image sensors, with nondestructive output, are currently used for applications that do not have stringent restrictions in terms of the readout time but are now being considered for other applications, like quantum imaging and astronomy, that have tighter timing restriction. A new firmware which includes a time oriented processor was developed for the readout system. This update allows to specify the readout sequences with nanosecond precision and allows the acquisition of synchronized raw video for testing, analysis and debugging. The noise analysis technique was applied to an standard CCD and a Skipper CCD to increase the readout speed achieving pixels readout time of a few microseconds with readout noise levels tolerable by the applications. At the same time the non stationary nature of the noise in the video signal was exposed together with a procedure to calculate its covariance matrix.

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