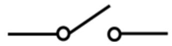
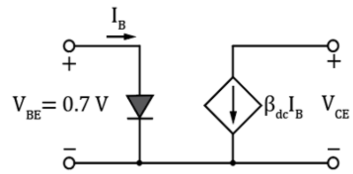
ECEN 350 – Equation Sheet 2 (12/27/2024)

BJT Cutoff Region: The Base-Emitter junction is not forward biased, resulting in the transistor behaving like an open switch between the Collector and Emitter. 

2rd Approximation of a BJT in the Active Region

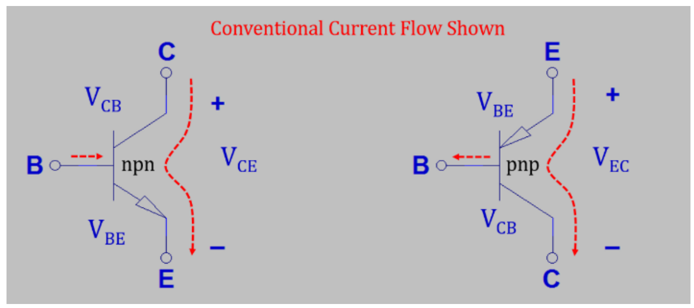


BJT Active Region: The Base-Emitter junction is forward biased, with the Collector-Base Junction not forward biased, resulting in the transistor approximating a dependent current source with $I_C = \beta I_B$. The active region is the desired operating region for transistor amplifiers.

BJT Saturation Region: BJT saturation occurs when the Base-Emitter junction is forward biased,with the Collector-Base junction also slightly forward biased. BJT saturation, implies that $V_{CE} \leq 0.3$ V for an npn BJT and $V_{EC} \leq 0.3$ V for a pnp BJT. The 1st approximation for BJT saturation is a closed switch between Collector and Emitter. 

For a BJT in the active region:

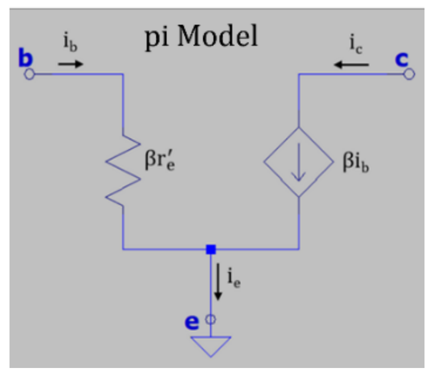
$\alpha \triangleq I_C/I_E.\ \beta \triangleq I_C/I_B.$
$I_C = \beta I_B.\ \ I_E = I_C + I_B \approx I_C.$



Good coupling: $X_C < 0.1R$, where R is the equivalent input or output resistance, with $X_C = 1/2\pi fC$.

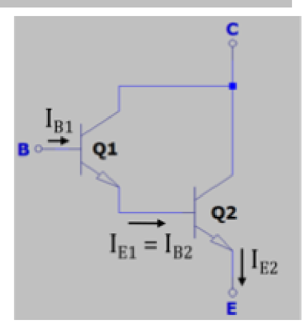
Good bypassing: $X_C < 0.1R$, where R is the equivalent resistance of the parallel element to short out for ac signals.

$$\text{Small – Signal Analysis:}\ \ i_c = \beta i_b,\ \ i_e = \beta i_b,\ \ r'_e = \frac{25\text{ mV}}{I_E}.$$



$$V_{BE}\ \text{Current Limit:}\ \ I_{limit} = \frac{0.66\text{ V}}{R_{cl}}.$$

$$\text{Darlington Configuration:}\ I_{B2} \approx I_{E2}/\beta_2.\ I_{B1} \approx I_{E1}/\beta_1.\ \beta_{total} = \beta_1\beta_2.$$



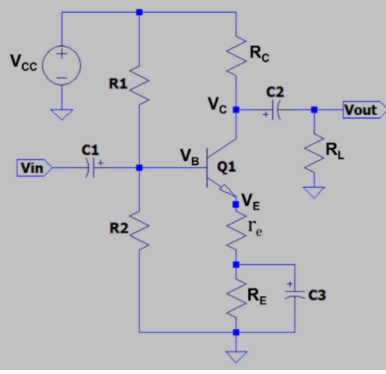
Voltage Divider Bias Amplifier with ac and dc Emitter Resistors

$\mathbf{A_v} = \dfrac{-r_c}{r_e'}$ for $r_e = 0$.

$\mathbf{A_v} = \dfrac{-r_c}{r_e' + r_e}$ for $r_e \neq 0$.

$Z_{in} = R1 \| R2 \| Z_{in(base)}$.

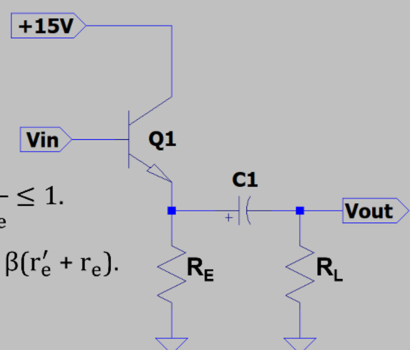
$Z_{in(base)} = \beta(r_e' + r_e)$.



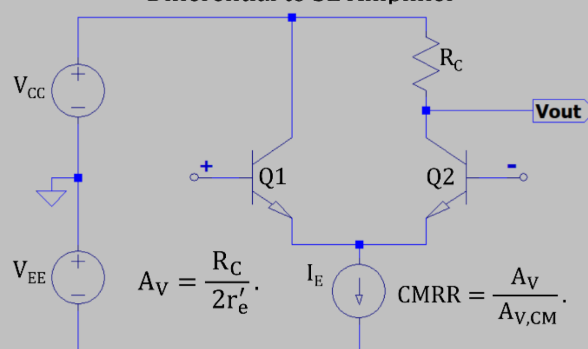
Common Collector (Emitter Follower) Amplifier

$\mathbf{A_v} = \dfrac{r_e}{r_e' + r_e} \leq 1$.

$Z_{in(base)} = \beta(r_e' + r_e)$.



Differential to SE Amplifier



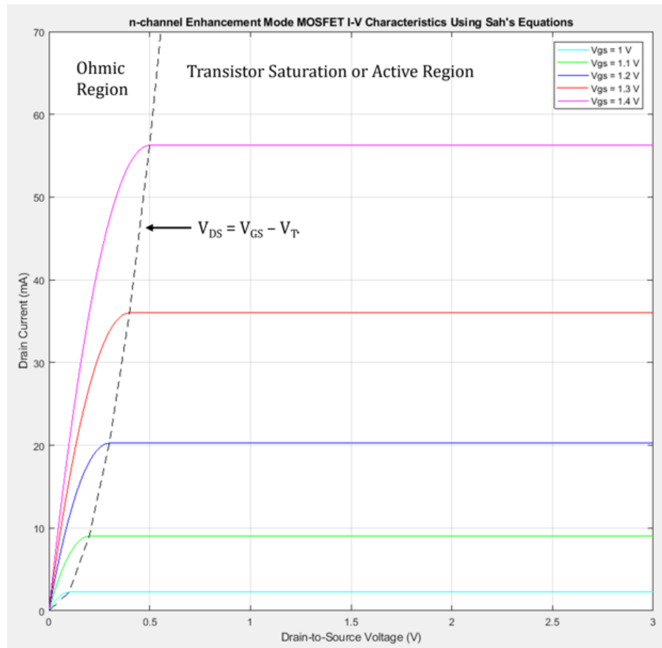
$A_V = \dfrac{R_C}{2r_e'}$.

$CMRR = \dfrac{A_V}{A_{V,CM}}$.

$CMRR_{dB} = 20\log(CMRR)$

n-Channel Enhancement Mode MOSFET
$V_{GS} < V_T, I_D = 0$. (Cutoff),
For $V_{GS} \geq V_T, 0 < V_{DS} < V_{GS} - V_T$. (Ohmic)
$I_D = \beta_n\left[(V_{GS} - V_T)V_{DS} - \dfrac{V_{DS}^2}{2}\right]$, where $\beta_n = \mu_n C_{OX}\dfrac{W}{L}$.
For $V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T$. (Transistor Saturation)
$I_D = \dfrac{\beta_n}{2}(V_{GS} - V_T)^2$.

p-channel Enhancement Mode MOSFET
$V_{SG} < \lvert V_T \rvert, I_D = 0$. (Cutoff),
For $V_{SG} \geq \lvert V_T \rvert,\ 0 < V_{SD} < V_{SG} - \lvert V_T \rvert$. (Ohmic)
$I_D = -\beta_p\left[(V_{SG} - \lvert V_T \rvert)V_{SD} - \dfrac{V_{SD}^2}{2}\right]$, where $\beta_p = \mu_p C_{OX}\dfrac{W}{L}$.
For $V_{SG} \geq \lvert V_T \rvert,\ V_{SD} \geq V_{SG} - \lvert V_T \rvert$. (Transistor Saturation)
$I_D = -\dfrac{\beta_p}{2}(V_{SG} - \lvert V_T \rvert)^2$.



CMOS Dynamic Power Dissipation: $P_{Dynamic} = C_{Load}N_{SW}V_{DD}^2 f$, where V_{DD} is the supply Voltage, N_{SW} is the number of nodes switching and f is the switching frequency.

Sizing CMOS Digital Logic: $W_p = \dfrac{\mu_n}{\mu_p}W_n$, where μ is mobility, W_n is the relative width of the n-channel transistor and W_p is the relative width of the p-channel transistor.