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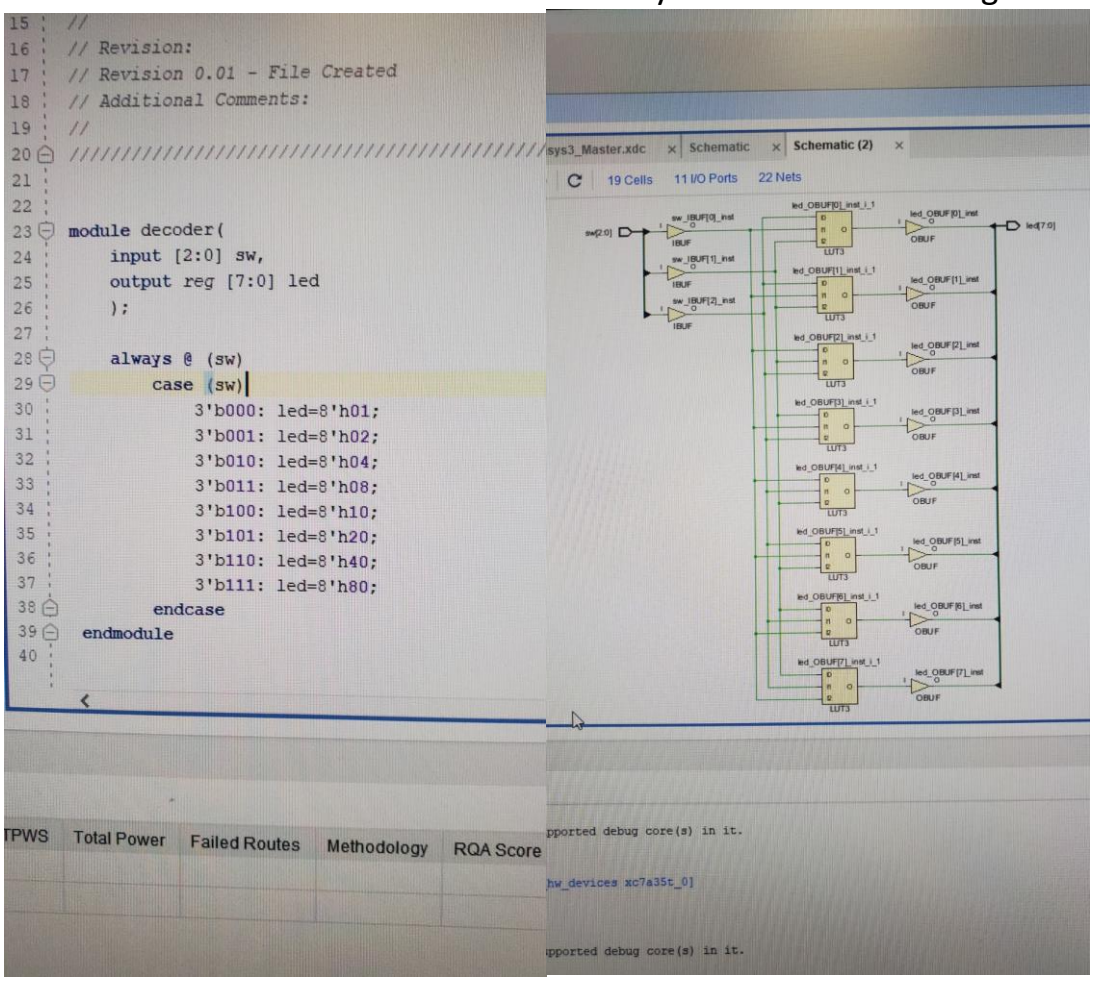
ECEN 340
Lab 2 – Vivado Intro / Structural Decoder

Purpose:

1. To review the Basys 3 board
2. To review Vivado usage
3. To implement a simple structural Verilog design

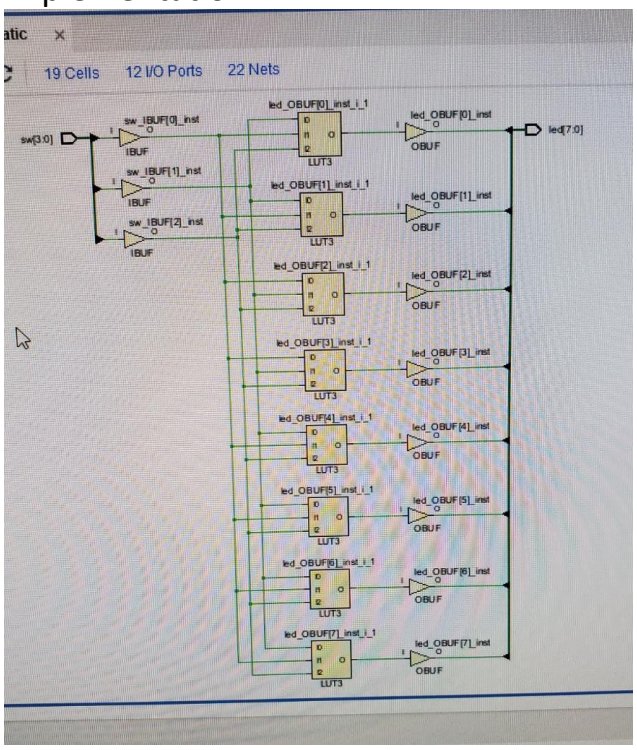
Procedure:

Part 1 (First Lab Day). Download the Basys3 Vivado Decoder Tutorial. Follow the instructions in the tutorial until you have a functioning decoder.

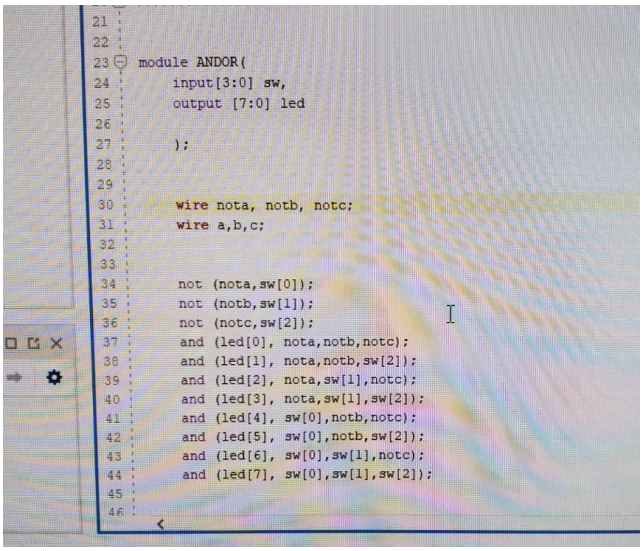


Part 2 (Second Lab Day). Create a new decoder project with a different name and implement the same design using structural Verilog (gate-level) design techniques.

A. Open the schematic view in Vivado, and study/understand the implementation.



B. Use “or, and”, and other structural Verilog statements to implement the Decoder.



```
module ANDOR(
    input[3:0] sw,
    output [7:0] led

    );


    wire nota, notb, notc;
    wire a,b,c;


    not (nota,sw[0]);
    not (notb,sw[1]);
    not (notc,sw[2]);
    and (led[0], nota,notb,notc);
    and (led[1], nota,notb,sw[2]);
    and (led[2], nota,sw[1],notc);
    and (led[3], nota,sw[1],sw[2]);
    and (led[4], sw[0],notb,notc);
    and (led[5], sw[0],notb,sw[2]);
    and (led[6], sw[0],sw[1],notc);
    and (led[7], sw[0],sw[1],sw[2]);

endmodule
```

Conclusion:

In this lab, we used Vivado to program an FPGA in Verilog code to behave as a decoder. We did this twice in two different ways. From part 1, we did it using behavioral and in part 2 we did structural. Both of which behaved, as we had hoped, like a decoder. Both ways were 100% functional. We tested this using the switches and saw the correct output lights light up for a given input switch combination.