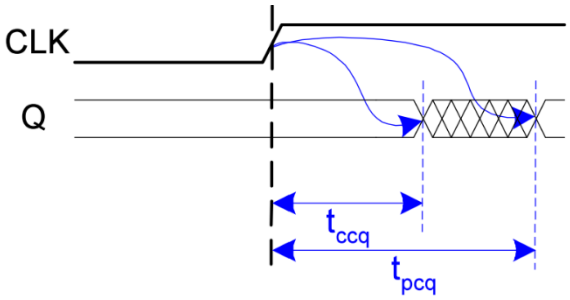
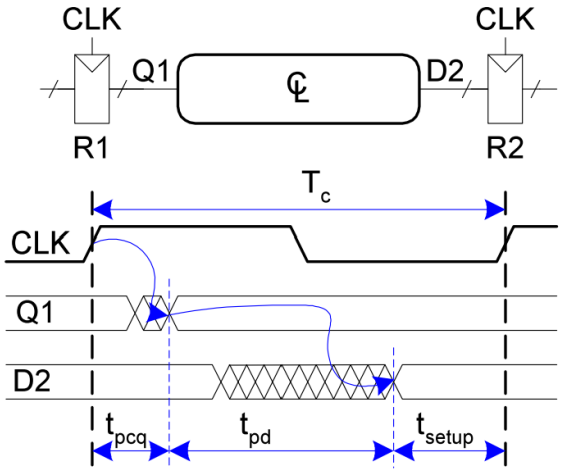
ECE 310 Spring 2025
Dr. Mihail Cutitaru

Homework 6
Assigned: March 24, 2025
DUE: March 31, 2025 by 11:59PM in Gradescope

Show all work for full credit.

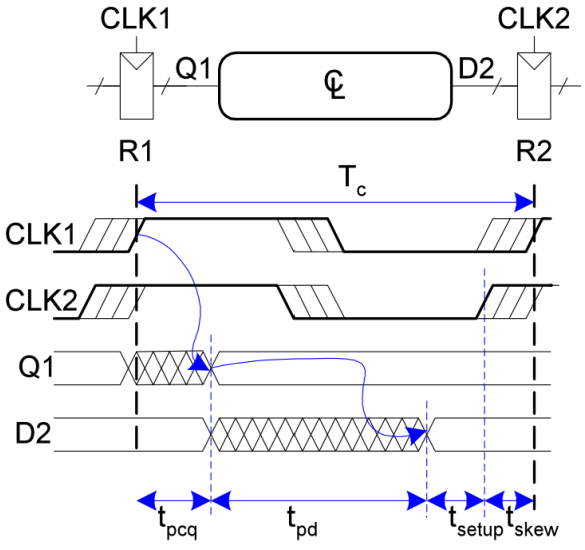
1. The outputs of a flip-flop have timing issues similar to the input timing constraints. The time after the clock edge that the output is guaranteed to be stable is known as propagation delay (t_{pcq}). Contamination delay is the time after the clock edge when the output may be unstable (t_{ccq}).





Given 2 flip-flops with some combinational logic between them in the waveform below, extract an equation for the maximum value of the propagation delay for the combination logic portion (t_{pd}) as a function of clock cycle time (T_c), DFF setup time (t_{setup}) and t_{pcq}. **(20 pts)**

2. When clock skew is taken into account, there will may be a case where the 2nd flip-flop receives the clock earlier than the 1st flip-flop (skew time is given as t_{skew}). What is the maximum t_{pd} value for this case? **(20 pts)**



3. List and give reasoning for 1 advantage and 1 disadvantage of a tree clock distribution network. **(20 pts)**

4. List and give reasoning for 1 advantage and 1 disadvantage of a mesh clock distribution network. **(20 pts)**

5. What is inertial delay? How does it differ from transport delay? **(20 pts)**