ECE 310 Spring 2025
Dr. Mihail Cutitaru

Homework 6
Assigned: March 5, 2025
DUE: March 17, 2025 by 11:59PM in Gradescope

Show all work for full credit.

1. How does a Moore FSM differ from a Mealy FSM? Be specific. There are several differences, but one of them is more important than others. **(10 pts)**

2. In the Mealy FSM Verilog model, is it possible to implement the next-state calculations and output calculations in 2 separate **always** statements? If not, why not? If yes, are there any advantages to doing so? **(15 pts)**

3. Are there any advantages to using an active-low reset signal over an active-high signal in the design of a sequential system? Justify your answer. **(20 pts)**

4. Explain why performing logic synthesis is important. **(15 pts)**

5. What is the synthesis result of running the code below? Draw the hardware with as much detail as possible. **(20 pts)**

```
module q5(    input [1:0] a, b, c, d, sel,
              output [1:0] y);
assign y =    (sel == 0) ? d : (sel == 1) ? c :
              (sel == 2) ? b : (sel == 3) ? a : 2'b0;
endmodule
```

6. What is the synthesis result of running the code below? Draw the hardware with as much detail as possible. Assume the model has a DFF as part of the hardware (inputs: d, clk; output: q). **(20 pts)**

```
module q6 (   output reg q,
              input d, clk, a, capture);
always @(posedge clk)
        if (capture)
              q <= a;
        else
              q <= d;
endmodule
```