ECE 310 Spring 2025
Dr. Mihail Cutitaru

Homework 9

SOLUTIONS

Show all work for full credit.

1. Given the Verilog ROM declaration in the Memory slides, what would need to change in the module to describe a RAM? You do not need to write the code, a description of signals and operations suffices. **(20 pts)**

   The ROM code in the slides only covers the reading of data at a given memory location. A RAM has the ability to both read and write, so a control signal is needed to select the operation. For a write operation, the RAM will also need a data line (din). The always statement would need to be change to account for the addition of these 2 signals.

2. List and briefly describe the function of 3 busses present in any modern processor. **(20 pts)**

   - **Data: bidirectional bus to send and receive data**
   - **Address: unidirectional bus to send an address to write to or read from**
   - **Control: bus to send signals that control operations**

3. Explain the 3-step process of running an instruction in a CPU. Include as much detail as needed to understand the operation. **(20 pts)**

   - **Fetch: read memory address to load instruction into the instruction register (IR)**
   - **Decode: "understand" instruction – read opcode, read register(s), set proper control signals**
   - **Execute: perform operation**

4. Briefly compare and contrast CISC and RISC approaches to processor design. **(20 pts)**

   RISC opts for short simple instructions, whereas RISC performs large complex operations in one instruction. RISC has many advantages compared to CISC, including smaller cost in cases where the wrong instruction is run.

5. Show the memory contents based on the memory file given below. Assume 16-bit words. If there are any unused locations between other populated locations, set the unused location values to zeros. If a location does not have enough bits to be fully populated, set the remaining least significant bits to zeros. **(20 pts)**

```
@00 11 22 33 44 55 66 77
@05 aa bb cc dd ee ff
77
88
99
@04 ab
```

00:	**1122**
01:	**3344**
02:	**5566**
03:	**7700**
04:	**ab00**
05:	**aabb**
06:	**ccdd**
07:	**eeff**
08:	**7788**
09:	**9900**