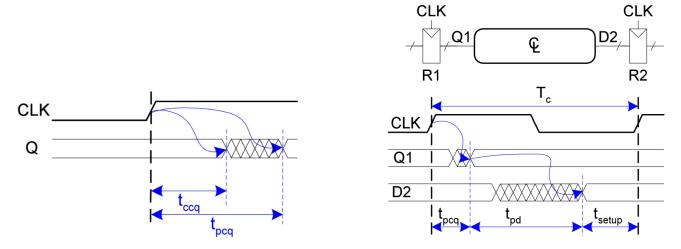
Homework 7

SOLUTIONS

Show all work for full credit.

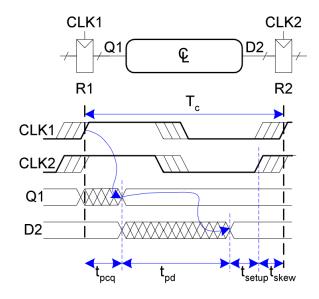
1. The outputs of a flip-flop have timing issues similar to the input timing constraints. The time after the clock edge that the output is guaranteed to be stable is known as propagation delay (t_{pcq}). Contamination delay is the time after the clock edge when the output may be unstable (t_{ccq}).



Given 2 flip-flops with some combinational logic between them in the waveform below, extract an equation for the maximum value of the propagation delay for the combination logic portion (t_{pd}) as a function of clock cycle time (T_c) , DFF setup time (t_{setup}) and t_{pcq} . (20 pts)

$$t_{pd} \le T_c - t_{pcq} - t_{setup}$$

2. When clock skew is taken into account, there will may be a case where the 2^{nd} flip-flop receives the clock earlier than the 1^{st} flip-flop (skew time is given as t_{skew}). What is the maximum t_{pd} value for this case? (20 pts)



$$t_{pd} \leq T_c - t_{pcq} - t_{setup} - t_{skew}$$

3. List and give reasoning for 1 advantage and 1 disadvantage of a tree clock distribution network. (20 pts)

Advantage: low cost in terms of wires, easy to do clock-gating

Disadvantage: susceptible to variations in implementation (wire width, etc)

4. List and give reasoning for 1 advantage and 1 disadvantage of a mesh clock distribution network. (20 pts)

Advantage: robust to variations, low skew

Disadvantage: high cost (wiring, capacitance, etc)

5. What is inertial delay? How does it differ from transport delay? (20 pts)

Inertial delay is the delay associated with the inertia of a circuit to change a value. Transport delay is the delay associated with propagating a value through a module. Inertial delay modeling captures the behavior of the circuit such as glitches, metastability, and offers insight in the behavior of the circuit under various conditions. Transport delay modeling helps identify critical paths and improves accuracy of simulation by having a more accurate propagation time representation.