INSTITUTE OF TECHNOLOGY

BLANCHARDSTOWN

Year	Year 2
Semester	Semester 3 repeat
Date of Examination	**Thursday 19th August 2010**
Time of Examination	**1.00pm - 3.00pm**

Prog Code	BN002	**Prog Title**	Higher Certificate in Computing in Information Technology	**Module Code**	COMP H2015
Prog Code	BN013	**Prog Title**	Bachelor of Science in Computing in Information Technology	**Module Code**	COMP H2015
Prog Code	BN104	**Prog Title**	Bachelor of Science (Honours) in Computing	**Module Code**	COMP H2015

Module Title	Switching Basics and Intermediate Routing

Internal Examiner(s): *Mr Mark Cummins*
External Examiner(s): *Dr Richard Studdert, Mr John Dunnion*

Instructions to candidates:

1) **To ensure that you take the correct examination, please check that the module and programme which you are following is listed in the tables above.**
2) **Attempt ALL PARTS of Question 1 and any THREE other questions.**
3) **This paper is worth 100 marks . Question 1 is worth 40 marks and all other questions are worth 20 marks each.**

DO NOT TURN OVER THIS PAGE UNTIL YOU ARE TOLD TO DO SO

Section A: Attempt ALL parts of this question

Question 1: All parts are worth 4 marks each

a) Explain in detail the root bridge election process.

b) Outline how someone might perform a denial-of-service attack on a wireless access point.

c) What is the purpose of VTP transparent mode?

d) List any four of the benefits associated with hierarchical network design.

e) Explain each of the following terms

1. Default VLAN
2. Management VLAN

f)

1. What is the primary advantage in using VLAN Trunking?
2. What are the two possible encapsulation types for a VLAN trunk, when using a Cisco switch?

g) What is the function of VTP Pruning?

h) Outline the functions of the distribution layer of the hierarchical design model.

i) An Ethernet switch has built the MAC address table shown. What action will the switch take when it receives the frame shown at the bottom of the exhibit?

MAC address table

Station	Interface 1	Interface 2	Interface 3	Interface 4
00-00-3d-1f-11-01			X	
00-00-3d-1f-11-02				X
00-00-3d-1f-11-03	X			

Frame

Destination	Source
00-00-3d-1f-11-03	00-00-3d-1f-11-01

j) How does an Ethernet switch process the incoming traffic using port-based memory buffering?

Section B: Answer ANY 3 questions from this section

(All questions carry equal marks)

Question 2:

a) Describe with the aid of a diagram; the two problems associated with redundant switched Ethernet topologies.

(10 marks)

b) Describe each of the five possible states that a switch port could transition through during the operation of the spanning tree protocol.

(10 marks)

Question 3:

a) Explain how a switch populates it CAM table and forwards incoming frames.

(6 marks)

b) Describe **each** of the **three** possible switch forwarding methods for switching data between network ports.

(6 marks)

c)

a. Explain the difference between full duplex and half duplex operation.
b. Explain the difference between symmetric and asymmetric switching.

(4 marks)

d) There are **two** methods of memory buffering, port based buffering and shared memory buffering. Briefly describe **each** method.

(4 marks)

Question 4:

a) Compare and contrast each of the four wireless LAN standards 801.11a, 801.11.b, 801.11g and 801.11n, under each of the following headings.

1. Band,
2. Modulation
3. Data rates

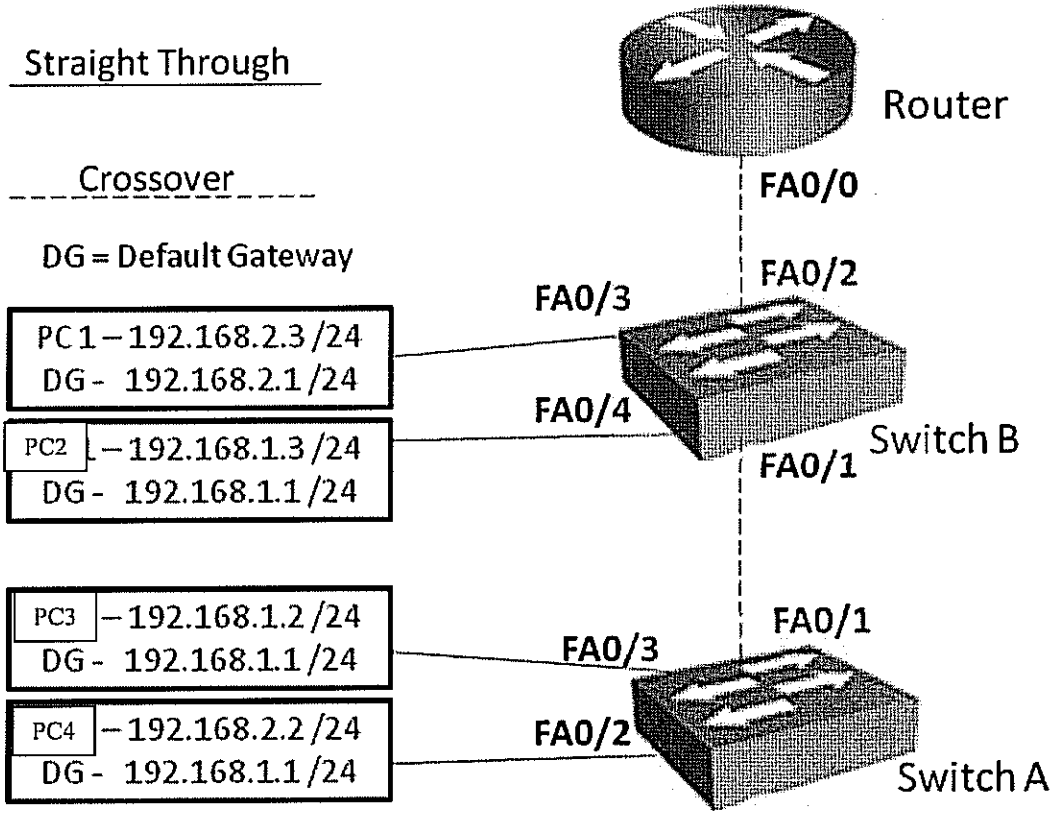
(12 marks)

b) Wireless access points use CSMA/CA. Explain the hidden node problem and outline how CSMA/CA overcomes this problem.

(8 marks)

Question 5:

a) Troubleshoot the network shown below. It contains a total of five errors. Correct each of the errors so that the network will be fully functional. Outline the errors and how you would correct each problem.



(Some output omitted)

Switch B# show run

Interface fa0/1
    Switchport mode trunk
    Switchport trunk encapsulation dot1q
Interface fa0/2
    Switchport mode trunk
    Switchport trunk encapsulation isl
Interface fa0/3
    Switchport mode access
    Switchport access vlan 20
Interface fa0/4
    Switchport mode access
    Switchport access vlan 10

Switch A# show run

Interface fa0/1
    Switchport mode access
    Switchport trunk encapsulation dot1q
Interface fa0/2
    Switchport mode access
    Switchport access vlan 10
Interface fa0/3
    Switchport mode access
    Switchport access vlan 20

Router# show run

    Interface fa0/0
        Interface fa0/0.1
            Encapsulation dot1q 10
            ip address 192.168.1.1 255.255.255.0
        Interface fa0/0.2
            Encapsulation dot1q 20
            ip address 192.168.2.1 255.255.255.0

(20 marks)