0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	DATA	EXPR	NOTES
COND				OP TYPE				OP CODE			S	OP FLAGS				ADDR MODE																		
																																		R13: SP R14: LR R15: PC X: DATA
																																		MEMORY ADDR MODE: 0: DIRECT/INDIRECT 1: OFFSET/NO OFFSET 2: BASE REG/IMD 3: OFFSET REG/IM
			OP				ADDR MODE																											ARTH ADDR MODE: 3: REG/IMD
			MOV				ALL																											
		?					DIRECT									0	0	0	0	R1				X	X	X	X	X	X	X	X	32 BIT IMD	R1 = X	
							R DIRECT									0	0	1	0	R1				R2				X	X	X	X		R1 = R2	
			LD				ALL																											
		?					IMD									0	0	0	X	R1				X	X	X	X	X	X	X	X	32 BIT IMD	R1 = X	
							IND									1	0	0	X	R1				X	X	X	X	X	X	X	X	32 BIT ADDR	R1 = *X	
							R IND					X	P	I	T	1	0	1	X	R1				R2				X	X	X	X		R1= *R2	P: PROCESS (I: INCREMENT ~I: DECREMENT, T: POST ~T: PRE)
							R IMD OFFSET					X	P	I	T	1	1	1	0	R1				R2				X	X	X	X	32 BIT IMD	R1= *(R2 + X)	P: PROCESS (I: INCREMENT ~I: DECREMENT, T: POST ~T: PRE)
		?					R REG OFFSET					X	P	I	T	1	1	1	1	R1				R2				R3					R1 = *(R2 + R3)	P: PROCESS (I: INCREMENT ~I: DECREMENT, T: POST ~T: PRE)
			LDM				ALL					X	W	I	T																			W: WRITEBACK ADDR TO BASE ~W: NO WRITEBACK, I: INCREMENT ~I: DECREMENT, T: POST ~T: PRE
							R IND									1	0	0	X	R1				R2				X	X	X	X	16 BIT REG LIST	R1= *R2	
							R REG OFFSET									1	1	1	1	R1				R2				R3				16 BIT REG LIST	R1 = *(R2 + R3)	
			STM				ALL					X	W	I	T																			W: WRITEBACK ADDR TO BASE ~W: NO WRITEBACK, I: INCREMENT ~I: DECREMENT, T: POST ~T: PRE
							R IND									1	0	1	X	R1				R2				X	X	X	X	16 BIT REG LIST	R1= *R2	
		?					R REG OFFSET									1	1	1	1	R1				R2				R3				16 BIT REG LIST	R1 = *(R2 + R3)	
			JMP / CALL				ALL					X	X	X	S																			S: LR = PC + 8 ~S: LINK NOT SET
							DIRECT									0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	32 BIT ADDR	PC = X	
							R DIRECT									0	0	1	0	R1				X	X	X	X	X	X	X	X		PC = R1	
							R OFFSET									0	1	1	0	R1				X	X	X	X	X	X	X	X	32 BIT IMD	PC = R1 + X	
			ADD				ALL					X	X	X	C																			S: COND FLAG SET ~S: COND FLAG NOT SET, C: INCLUDE CARRY ~C: NO CARRY
							IMD									X	X	X	0	R1				R2				X	X	X	X	32 BIT IMD	R1 = R2 + X	ADD CARRY + 1 IF C OP FLAG SET
							REG									X	X	X	1	R1				R2				R3					R1 = R2 + R3	ADD CARRY + 1 IF C OP FLAG SET
			SUB				ALL					X	X	X	C																			S: COND FLAG SET ~S: COND FLAG NOT SET, C: INCLUDE CARRY ~C: NO CARRY
							IMD									X	X	X	0	R1				R2				X	X	X	X	32 BIT IMD	R1 = R2 - X	ADD CARRY - 1 IF C OP FLAG SET
							REG									X	X	X	1	R1				R2				R3					R1 = R3 - R2	ADD CARRY - 1 IF C OP FLAG SET
			RSUB				ALL					X	X	X	C																			S: COND FLAG SET ~S: COND FLAG NOT SET, C: INCLUDE CARRY ~C: NO CARRY
							IMD									X	X	X	0	R1				R2				X	X	X	X	32 BIT IMD	R1 = X - R2	ADD CARRY - 1 IF C OP FLAG SET
							REG									X	X	X	1	R1				R2				R3					R1 = R2 - R3	ADD CARRY - 1 IF C OP FLAG SET
			LSL / ASL				ALL					X	X	X	A																			S: COND FLAG SET ~S: COND FLAG NOT SET, A: ARITHMETIC SHIFT ~A: LOGICAL SHIFT
							IMD									X	X	X	0	R1				R2				X	X	X	X	32 BIT IMD	R1 = R2 << X	
							REG									X	X	X	1	R1				R2				R3					R1 = R2 << R3	
			LSR / ASR				ALL					X	X	X	A																			S: COND FLAG SET ~S: COND FLAG NOT SET, A: ARITHMETIC SHIFT ~A: LOGICAL SHIFT
							IMD									X	X	X	0	R1				R2				X	X	X	X	32 BIT IMD	R1 = R2 >> X	
							REG									X	X	X	1	R1				R2				R3					R1 = R2 >> R3	
			AND				ALL					X	X	X	X																			S: COND FLAG SET ~S: COND FLAG NOT SET, A: ARITHMETIC SHIFT ~A: LOGICAL SHIFT
							IMD									X	X	X	0	R1				R2				X	X	X	X	32 BIT IMD	R1 = R2 & X	
							REG									X	X	X	1	R1				R2				R3					R1 = R2 & R3	

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	DATA	EXPR	NOTES
COND				OP TYPE				OP CODE			S	OP FLAGS				ADDR MODE																		
			OR				ALL					X	X	X	X																			S: COND FLAG SET ~S: COND FLAG NOT SET, A: ARITHMETIC SHIFT ~A: LOGICAL SHIFT
							IMD									X	X	X	0	R1				R2				X	X	X	X	32 BIT IMD	R1 = R2 | X	
							REG									X	X	X	1	R1				R2				R3					R1 = R2 | R3	
			XOR				ALL					X	X	X	X																			S: COND FLAG SET ~S: COND FLAG NOT SET, A: ARITHMETIC SHIFT ~A: LOGICAL SHIFT
							IMD									X	X	X	0	R1				R2				X	X	X	X	32 BIT IMD	R1 = R2 ^ X	
							REG									X	X	X	1	R1				R2				R3					R1 = R2 ^ R3	
			ROR				ALL					X	X	X	X																			S: COND FLAG SET ~S: COND FLAG NOT SET, A: ARITHMETIC SHIFT ~A: LOGICAL SHIFT
							IMD									X	X	X	0	R1				R2				X	X	X	X	32 BIT IMD		
							REG									X	X	X	1	R1				R2				R3						
			ROL				ALL					X	X	X	X																			S: COND FLAG SET ~S: COND FLAG NOT SET, A: ARITHMETIC SHIFT ~A: LOGICAL SHIFT
							IMD									X	X	X	0	R1				R2				X	X	X	X	32 BIT IMD		
							REG									X	X	X	1	R1				R2				R3						
			MUL				ALL					X	X	X	X																			S: COND FLAG SET ~S: COND FLAG NOT SET, A: ARITHMETIC SHIFT ~A: LOGICAL SHIFT
							IMD									X	X	X	0	R1				R2				X	X	X	X	32 BIT IMD		
							REG									X	X	X	1	R1				R2				R3						

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	DATA	EXPR	NOTES
COND				OP TYPE				OP CODE			S	OP FLAGS				ADDR MODE																		

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