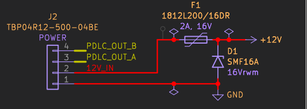
POWER TERMINAL BLOCK

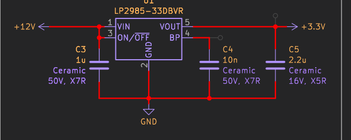
Circuit protection for power input:
- Internal: 2 A polyfuse, reverse polarity, overvoltage
- External: 3 A fuse, 20 AWG minimum recommended

Pin 1: Power input, ground
Pin 2: Power input, 12 V DC nominal, 16 V DC maximum
Pin 3/4: PDLC output A/B, 60 V AC (peak-to-peak) nominal



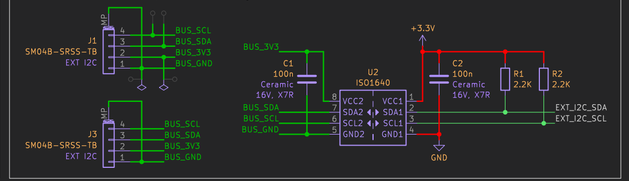
3.3 V POWER SUPPLY

Supplies 150 mA, ultra low quiescent current (microamps)
The whole system draws less than 5 mA while idle



EXTERNAL I2C INTERFACE (QWIIC)

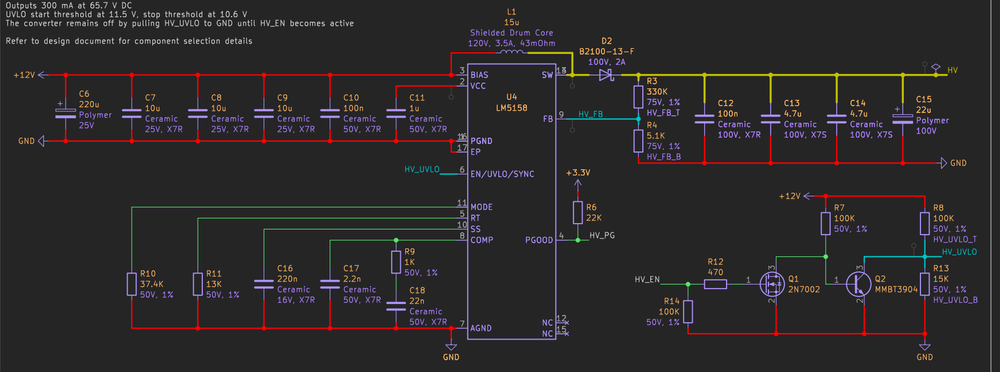
ISO1640 provides bidirectional isolation, hot swap, and ESD protection
- Side 1 drives the internal bus, intended for a low-capacitance node
- Side 2 drives the external bus, can withstand stronger ESD and short circuit events



HIGH VOLTAGE BOOST CONVERTER

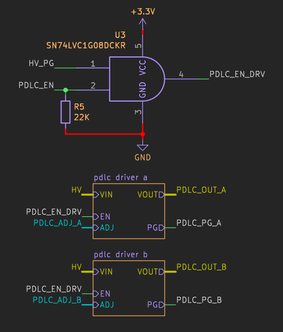
Outputs 300 mA at 65.7 V DC
UVLO start threshold at 11.5 V, stop threshold at 10.6 V
The converter remains off by pulling HV_UVLO to GND until HV_EN becomes active

Refer to design document for component selection details



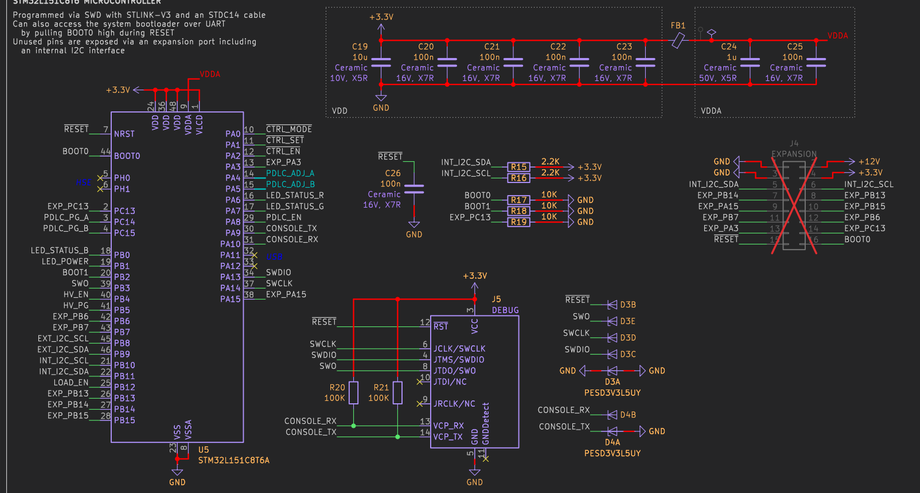
PDLC DRIVER

Outputs 300 mA between the terminals at 60 V AC RMS
The drivers remain off unless HV_PG and PDLC_EN are both high (for functional safety) and thereby ensures that VIN > 3.3 so UVLO/EN remains below VIN + 0.3 V as required by the IC



STM32L151C8T6 MICROCONTROLLER

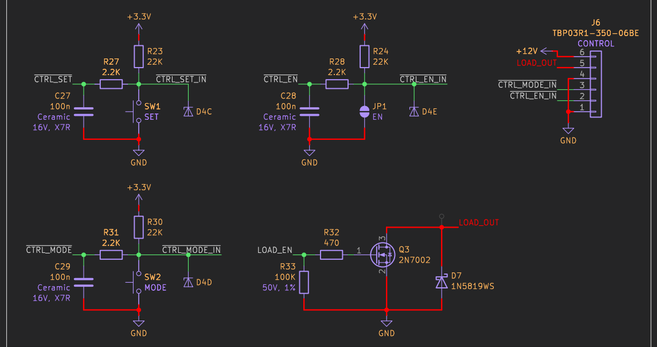
Programmed via SWD with STLINK-V3 and an STDC14 cable
Can also access the system bootloader over UART
  by pulling BOOT0 high during RESET
Unused pins are exposed via an expansion port including
  an internal I2C interface



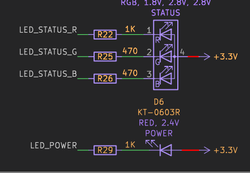
Datasheet: In STM32L151xxxxA devices VLCD should be connected to VDD

CONTROL I/O

Load output rated for 200 mA at 20 V, sufficient for an indicator, optocoupler, or small relay coil
The SET button cannot be wired remotely because its function requires the indicators to be visible
ESD protection on all switch inputs



INDICATORS



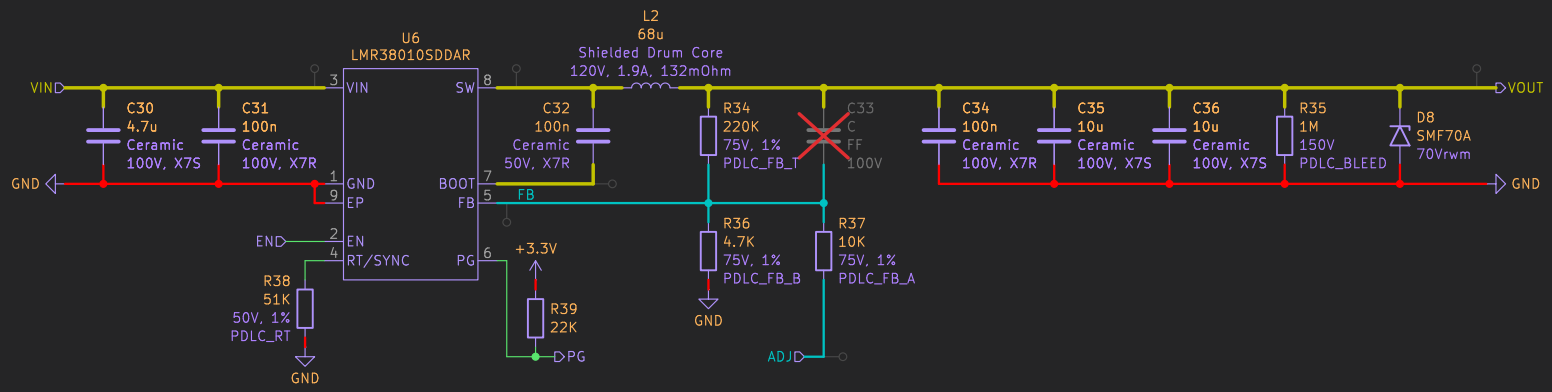
github.com/brown-studios/pdlc
Brown Studios LLC
Sheet: /
File: pdlc.kicad_sch
Title: PDLC driver
Size: A2 | Date: 2026-01 | **Rev: v2.0**
KiCad E.D.A. 9.0.6 | Id: 1/3

PDLC OUTPUT DRIVER (VARIABLE VOLTAGE BUCK CONVERTER)

Outputs 1 A at 3 V to 63 V depending on the voltage at ADJ

EN enables output when above 1.4 volts, it must be clamped between 0 V and VIN + 0.3V even in the case where VIN = 0 V

Refer to the design document for component selection details



github.com/brown-studios/pdlc

Brown Studios LLC

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File: pdlc-output.kicad_sch

Title:

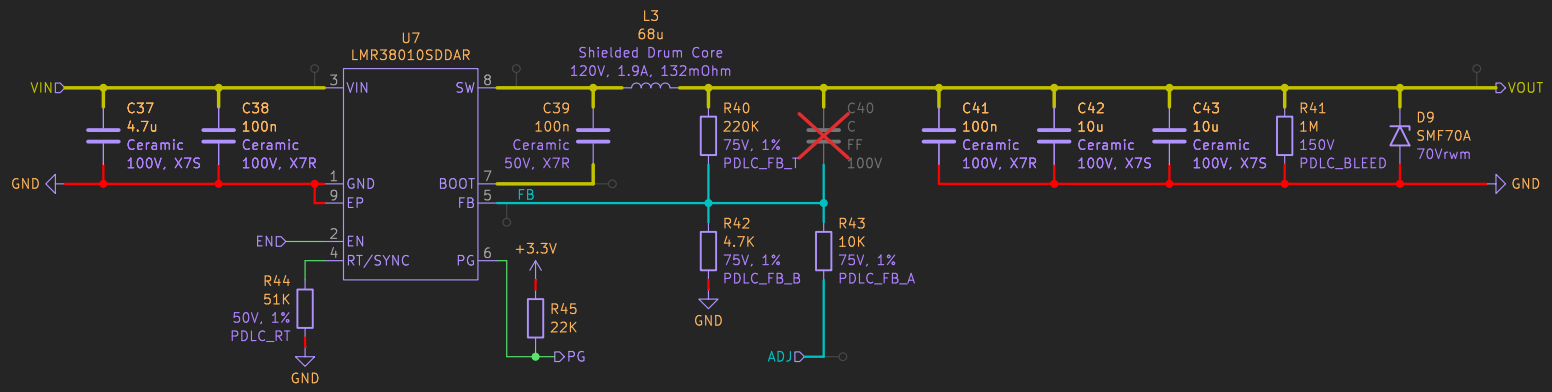
Size: A4	Date: 2026-01	**Rev: v2.0**
KiCad E.D.A. 9.0.6		Id: 2/3

PDLC OUTPUT DRIVER (VARIABLE VOLTAGE BUCK CONVERTER)

Outputs 1 A at 3 V to 63 V depending on the voltage at ADJ

EN enables output when above 1.4 volts, it must be clamped between 0 V and VIN + 0.3V even in the case where VIN = 0 V

Refer to the design document for component selection details



github.com/brown-studios/pdlc

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Sheet: /pdlc driver b/

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Title:

Size: A4	Date: 2026-01	**Rev: v2.0**
KiCad E.D.A. 9.0.6		Id: 3/3