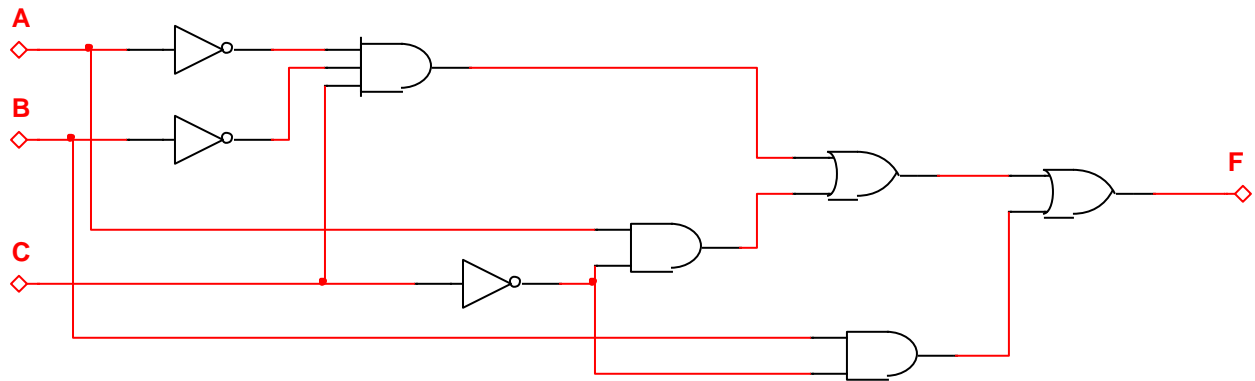



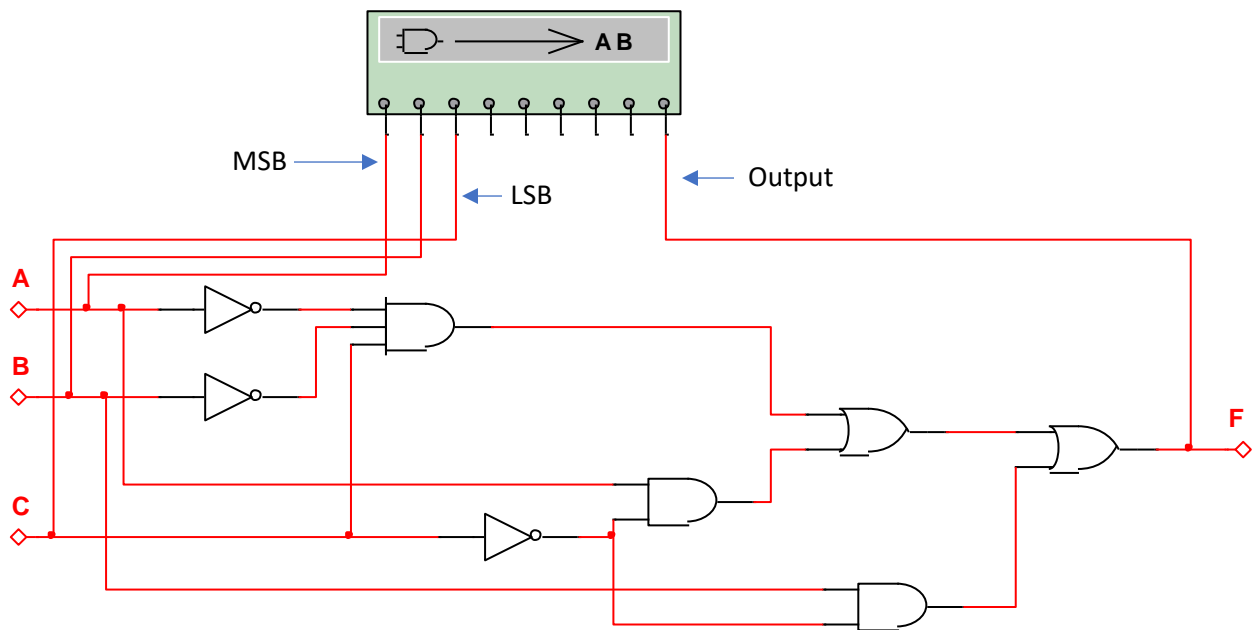
ESET 219 Lab 1 – Logic Gates In Multisim

Objective – The purpose of the lab is to become familiar with using Multisim to create and simulate a digital circuit before it is implemented into physical hardware. This lab uses the word generator, logic analyzer, and logic converter virtual instruments in Multisim. These tools help to create or verify a digital circuit. The circuit's behavior will be observed on the Basys3 board after design in Multisim.

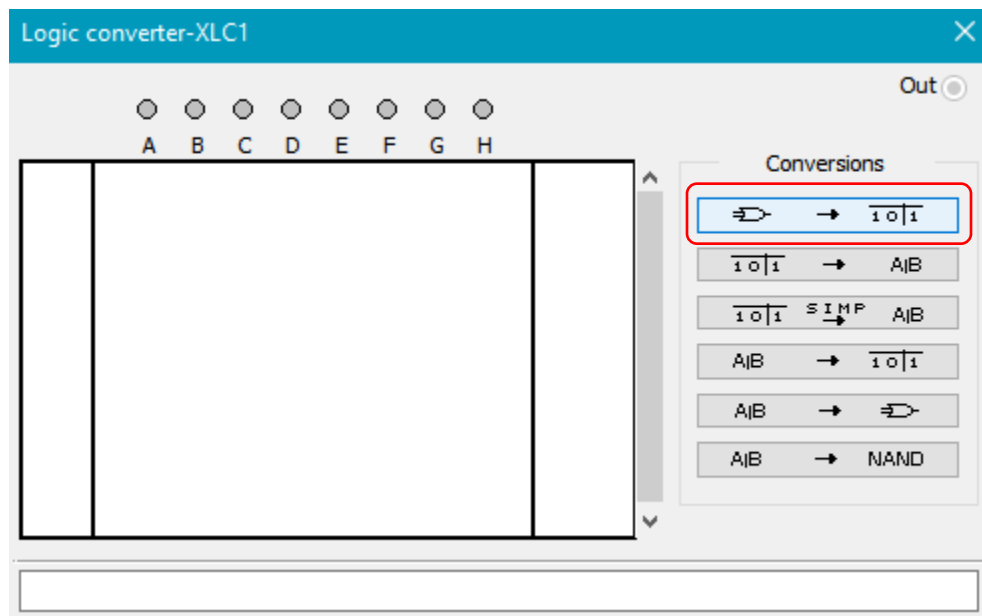
Task 1 – Create the following circuit in Multisim.



A tool for creating truth tables is the logic converter. Click on the logic converter icon  from the virtual instrument toolbar on the far right. You can also go to "Simulate" -> "Instruments" -> "logic converter". Setup the logic converter as shown below. Input A is the MSB



Double click the logic converter. Press the “circuit to truth table” button. Notice the truth table is created.



Replace the on-page connectors with Basys3 input and output pins. Load the circuit design onto the Basys3 board. Use the switches and LEDs to verify the board behavior is the same as the truth table. Show the TA your circuit is functioning correctly on the Basys3 board. For verification, the switch is up when TRUE, and down when FALSE. The LED is on when TRUE, and off when FALSE. Pay attention to which switch you use as the MSB and LSB.

Task 2 – The following truth table describes a logic circuit. It has four inputs A,B,C,D and one output F.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

The logic converter can also be used to create a logic circuit from a truth table. Double click on the logic converter, and fill in the truth table by first selecting a number of inputs. Then click on the output value to make it a 1 or 0. The logic converter can generate both simplified and non-simplified Boolean equations for a truth table. Press the “generate equation” and notice how large the Boolean equation is in the equation display. Press the “generate simplified equation” button and notice how the equation becomes smaller. Generate a simplified equation, and press the “create schematic” button. You will notice a logic schematic is generated for the truth table. Load the design onto the Basys3 board and verify the behavior is correct with TA.

Click to add input

Click to change value

Logic converter-XLC1

Out ☐

	A	B	C	D	E	F	G	H	
000	0	0	0	0					1
001	0	0	0	1					0
002	0	0	1	0					?
003	0	0	1	1					?
004	0	1	0	0					?
005	0	1	0	1					?
006	0	1	1	0					?
007	0	1	1	1					?
008	1	0	0	0					?
009	1	0	0	1					?
010	1	0	1	0					?
011	1	0	1	1					?
012	1	1	0	0					?
013	1	1	0	1					?

Conversions

$\Rightarrow \rightarrow \overline{101}$

$\overline{101} \rightarrow A|B$ ← Generate equation

$\overline{101} \xrightarrow{\text{SIMP}} A|B$ ← Generate simplified equation

$A|B \rightarrow \overline{101}$

$A|B \rightarrow \Rightarrow$ ← Create schematic

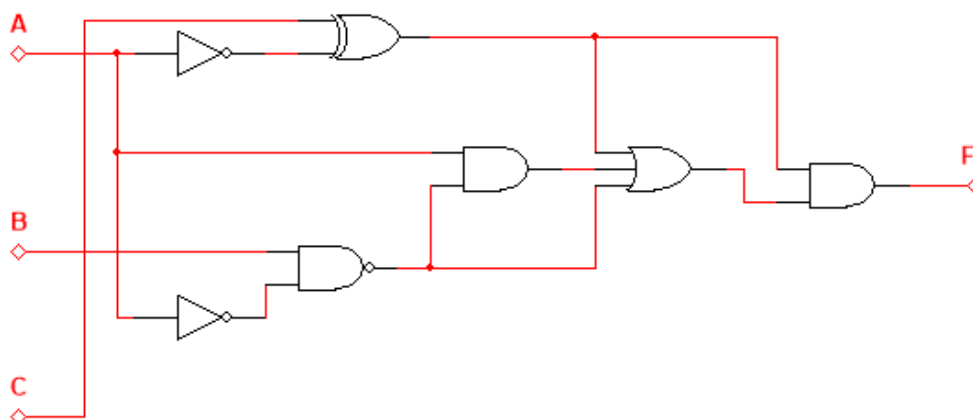
$A|B \rightarrow \text{NAND}$


Equation display

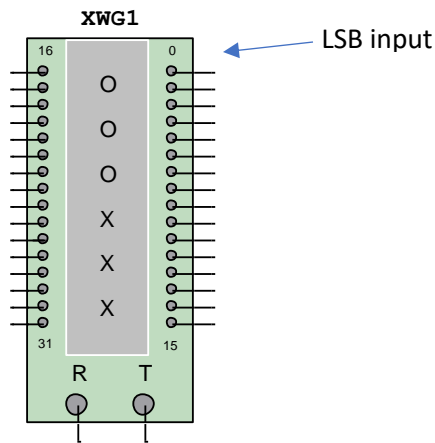
Question 1. What is the max number of inputs to any logic gate from the created schematic by the logic converter? What is a disadvantage of using the logic converter to create a schematic?

Question 2. What is the Boolean equation generated from the logic converter when the generate equation button was pressed?

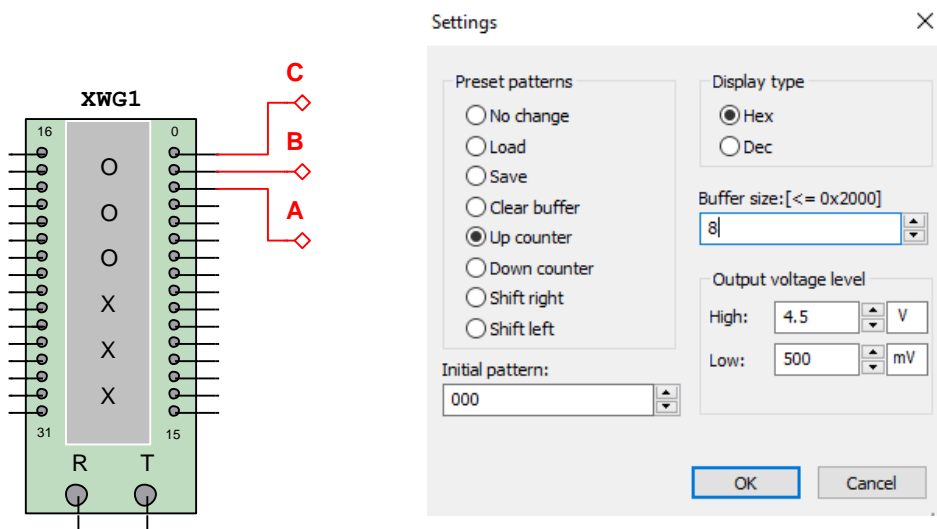
Task 3 – The word generator and logic analyzer are used to input signals to a logic circuit and observe the output. Create the following logic circuit in Multisim. A will be the MSB on the input.




Add the word generator virtual instrument by clicking on the word generator icon . You can also go to “Simulate” -> “Instruments” -> “word generator”. The word generator generates a series of patterns to test all the possible combinations of input to a logic circuit.

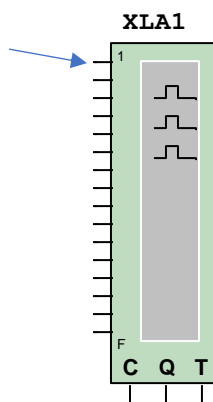


Hook up the word generator to the logic circuit. (Recommend using on-page connectors). Double click the word generator to set it up. Press the “set” button. On the “Settings” window select “Up Counter” for “Preset patterns”. The buffer size is the total possible number of input combinations. Set the initial pattern to 0 for each input. Press “OK”.

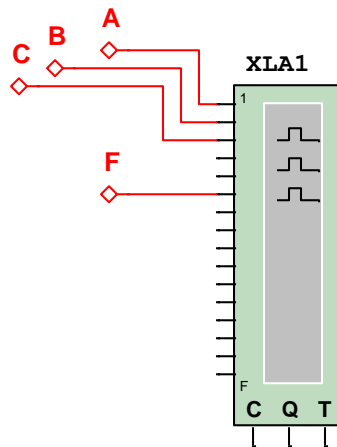


Add the word generator virtual instrument by clicking on the word generator icon . You can also go to “Simulate” -> “Instruments” -> “logic analyzer”. The logic analyzer will show the timing diagram for the circuit.

Waveform input

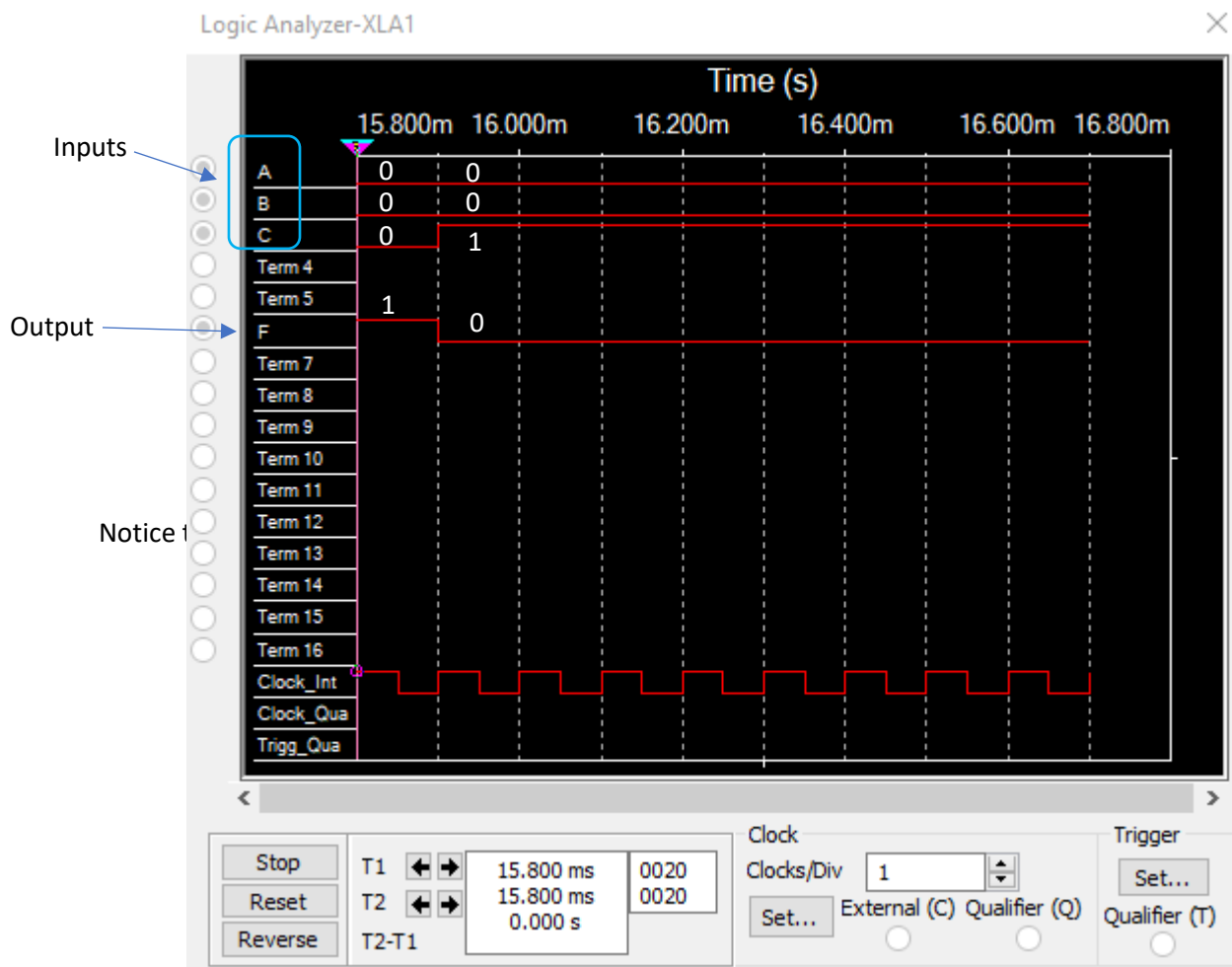


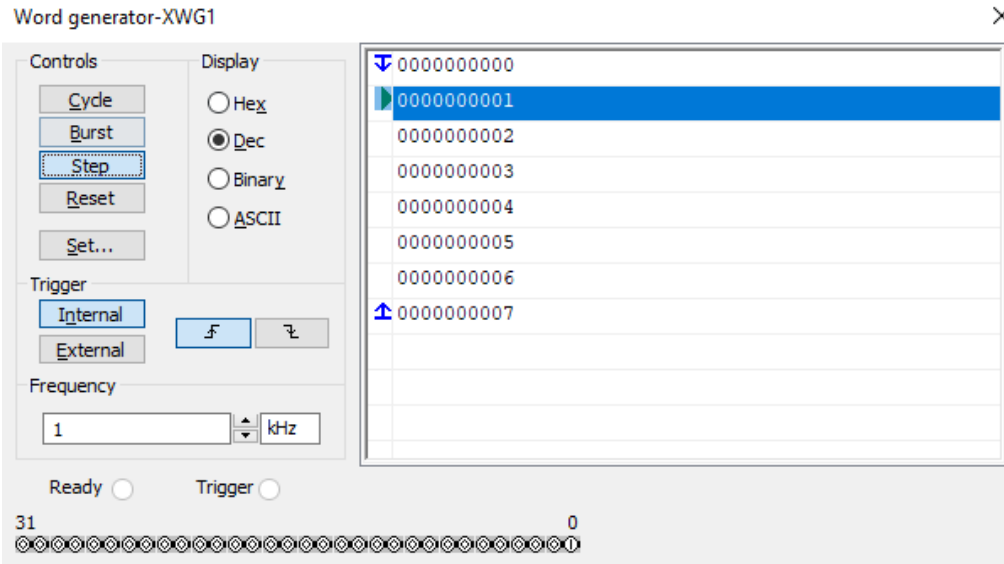
Connect the circuit to the logic analyzer. Recommend using on-page connectors. The input will be the first three waveforms on the display. The output F is placed a couple inputs below to give space to make the signal easier to read on the analyzer.



Open both the word generator and logic analyzer windows by double clicking on each instrument. The word generator has a frequency input (default is 1 KHz). This is how fast it will cycle through the input patterns. The logic analyzer also has a clock/div setting. This is how many cycles to display per segment in the window. The default clock is 10 KHz.

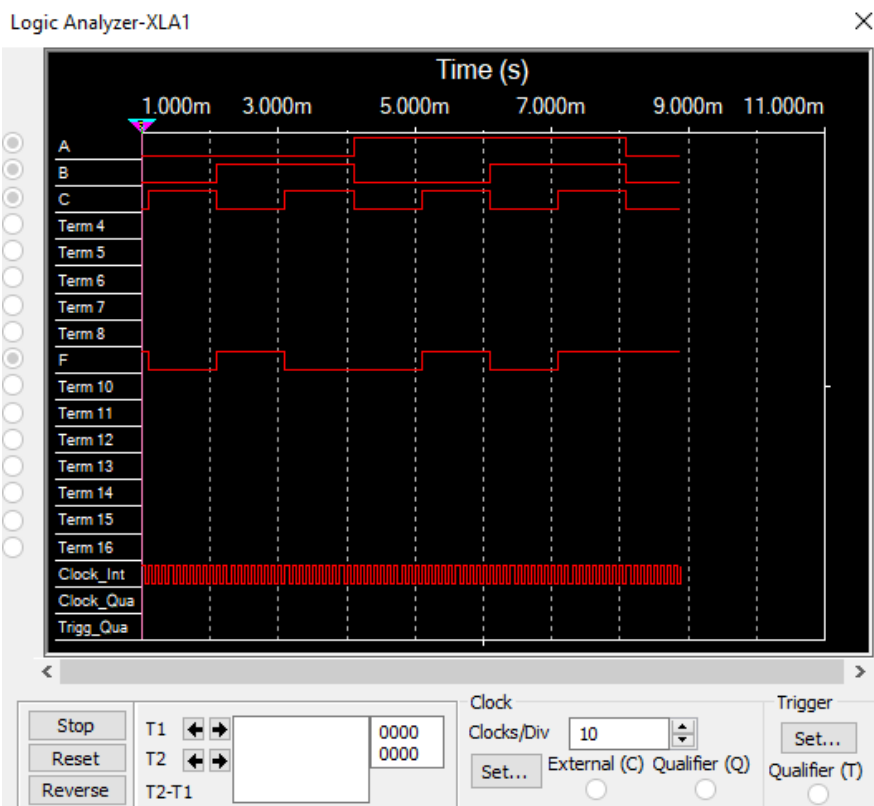
With both windows open, press the “Step” button on the word generator. You will see a waveform appear on the logic analyzer similar to below.



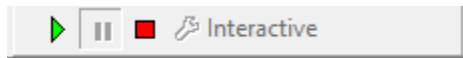


Pressing “Step” on the word generator will go to the next input pattern, and the change can be seen on the logic analyzer. To clear the logic analyzer window, press the “Reset” button.

Adjusting the clocks/div on the logic analyzer will display more input patterns onto the logic analyzer. The example below shows 10 clocks/div for an arbitrary logic circuit. The frequency of the word generator can be adjusted as well.



To quit the simulation, close both the word generator and logic analyzer. Press the stop button on the simulation toolbar. The simulation must be stopped before any changes can be made to the schematic.



Use the word generator and logic analyzer to fill in the output F of the below truth table for the circuit created in task 3. Load the design onto the Basys3 board and have TA verify behavior matches the truth table.

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	