DATA SHEET

GP328520A

ARM926EJ-S Multi-Media Camera w/ PPU SoC Platform

Preliminary

Sep. 24, 2020

Version 0.1

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MULTI-MEDIA CAMERA w/ PPU SoC PLATFORM

1. GENERAL DESCRIPTION

GP328520A, a highly integrated SoC (System-On a Chip) by Generalplus, is a high cost-performance ratio solution for multi-media and video streaming applications. It is developed with a high performance and power efficient ARM's ARM926EJ-S core operating at up to CPU/system 513/171MHz with significant enhancements in image, video processing, and power savings. Other features include DDR memory, GPDLA deep learning accelerator, Chroma key engine, JPEG CODEC engine, TFT-LCD interface, MIPI DSI interface, Display adjustment engine, CMOS sensor interface, MIPI CSI interface, scaling engine, Picture Process Unit (PPU), 16-channel Sound Process Unit (SPU), audio compressor, USB 2.0 OHCI/EHCI, USB 2.0 HS device, etc. GP328520A processor is designed to connect with various types of memory card interfaces such as SD and MMC. For more information about its features, please refer to the following section.

2. FEATURES

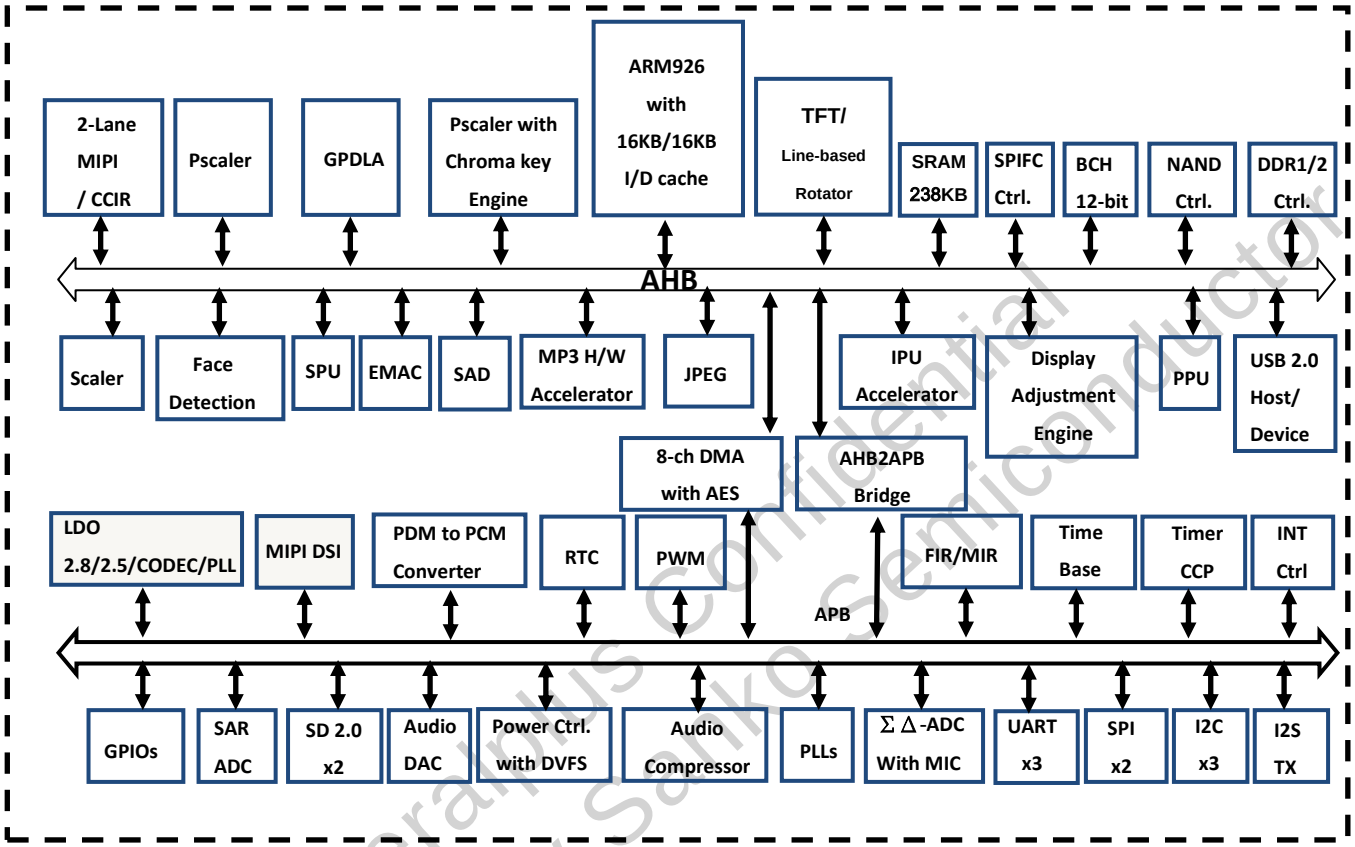
- ARM926EJ-S CPU with both 16K-byte I/D-cache, embedded JTAG ICE, and working frequency up to 513MHz
- Up to 238KB SRAM for local data buffer
- Embedded 128Mb DDR SDRAM
- GPDLA is a deep learning accelerator which supports various deep neural network models, applications such as object classifications, object detection and face detection are all possible and will enrich user experience.
- Chroma key engine with robust mechanism and low bandwidth requirements
- SPI FLASH controller, allowing CPU directly runs program on it. 1-bit/2-bit/4-bit IO mode supported
- Picture Process Unit. (PPU)
  - 4 Text layers + 1024 internal Sprites + 4096 extended Sprites
  - Virtual 3D effect for text and sprite
  - QVGA/VGA/D1 and arbitrary size up to 2032x2032 output
  - Line-based or frame-based operation
  - Max. 1024x768 LCD Resolution output
  - Texture mapping with anti-aliasing and bilinear interpolation
  - High precision sprite rotate effect supports up to 256-step (each step 360 degree/256).
  - High precision sprite zoom effect supports up to 256-step adjustment
  - Supports both alpha blending and additive blending
- Sound Process Unit (SPU)
  - 16 hardware PCM/ADPCM channels
  - Dynamic volume compressor
  - MP3 decoder
- Audio compressor engine which enhances audio quality
- JPEG CODEC
  - ISO/IEC 10918-1 baseline JPEG
  - High-speed decoding and encoding with resolution up to 64M pixels
  - Hardware Motion JPEG decoding and encoding (up to 1080p@30fps) for real-time video record and playback application
- Video-in & CMOS sensor interface and CCIR601/CCIR656 CSI standard supported.
- 2/1-lane MIPI CSI input supported
- Face Detection Engine for interactive application
- NAND FLASH controller with ECC and 4/8/12-bit BCH
- Eight-channel DMA controller with AES function
- Mono and 16 gray levels STN-LCD controller
- Rotating engine supports 90/180/270/360/Mirror/Flip function
- Y only rotating engine supports rotate at any angle
- Line-based rotating engine supports panels with different orient with frame buffer without extra bandwidth consumption.
- Two sets of TFT-LCD controller.
  - UPS051. (serial RGB)
  - UPS052. (serial RGB dummy)
  - Parallel RGB (6-6-6, 7-7-7, 8-8-8).
  - I80 (8-bit/16-bit/18-bit system bus) I/F type
  - CCIR601/CCIR656
  - Timing Controller for TFT-LCD drivers
  - Scaling engine inside with programmable up-scaling and down-scaling factor
  - Gamma Table Adjustment(TFT1 Only)
- Up to 4-lane MIPI DSI interface which supports panel resolution up to 1280x720 or 720x1280.
- Display adjustment engine which provides edge enhancement, R/G/B gamma table and auto hue adjustment
- Two sets of PSCAL supporting transform and zoom-in/out image data to the format supported by JPEG/ PPU/ DRAM
- One Y-only PSCAL for face-detection engine
- Image Processing Unit
  - Max. width more than 2048 pixels
  - Address-remap supporting direct addressing and

Coordinates addressing
- Color-remap-only supporting ARGB155 and RGB565
- Sixteen OP modes supported
- Support Alpha transform

- Universal Serial Bus (USB) 2.0 high/full speed compliance device and USB OHCI/EHCE host controller with built-in transceiver.
- Watchdog timer
- Real-time clock
- Eight 32-bit timers/counters with PWM output capability.
- Eight-channel quadrature decoder
- Two sets of SD 2.0/MMC interface
- Two sets of SPI (master/slave) interface with data rate up to 24Mbps.
- Three sets of UART (asynchronous serial I/O) or IrDA interface with baud rate up to 1.8432Mbps and 115.2Kbps; smart card interface (ISO7816) supported
- Three sets of I2C controller
- Four sets of I2S input with 24-bit resolution and up to 192KHz sample rate
- Four sets of I2S output with 24-bit resolution and up to 192KHz sample rate
- PDM to PCM converter which supports MEMS microphones with PDM interface
- Embedded Ethernet MAC hardware
- One set hardware SAD (Sum of Absolute Difference) engine
- 90 general programmable I/O ports (GPIO) with pull-high/low control
- Power management
- 1.2V DC2DC Feedback reference voltage out for core logic
- 3.3V to 2.8V~1.8V regulator for sensor's power
- 3.3V to 2.5V~1.8V regulator for DDR memory
- Dedicated 3.3V to 3.0V LDO for audio ADC
- Dedicated 3.3V to 3.0V LDO for PLLs
- Low voltage reset
- RTC with independent power supply
- Power-down mode with low standby current, typically less than 10uA
- Two sets of programmable PLLs frequency from 144MHz to 1188MHz and 72MHz to 594MHz
- 16-bit stereo DAC (2-channel) for audio playback
- 16-bit ADC with MIC for audio recording
- 12-bit SAR ADC with 8 line-in channels and 800KMsps
- MIC with digital AGC (auto gain control)
- LQFP128 package

Item	Product number	Embedded DDR density
1	GP328520A	128Mb DDR memory

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTION

PKG No	Name	Group	Type	Normal Function Description
1	IOE15	GPIO	IO	IOE15
2	VSS	Digital Ground	P	Digital ground
3	RESETB	SYSTEM	I	External RESETB(Low active)
4	IOD15	SD	IO	SD DATA2
5	IOD12	SD	IO	SD DATA3
6	IOD10	SD	IO	SD CMD
7	IOD11	SD	IO	SD CLK
8	IOD13	SD	IO	SD DATA0
9	V12I	CORE PWR	P	1.2V Core Power
10	IOC6	MIPI	IO	MIPI0 DATA1N/CSI D8
11	IOC7	MIPI	IO	MIPI0 DATA1P/CSI D9
12	IOC8	MIPI	IO	MIPI0 CLKN/ CSI CLKI
13	IOC9	MIPI	IO	MIPI0 CLKP/ CSI CLKO
14	IOC10	MIPI	IO	MIPI0 DATA0N/CSI HSYNC
15	IOC11	MIPI	IO	MIPI0 DATA0P/CSI VSYNC
16	IOE14	GPIO	IO	IOE14
17	VSS	Digital Ground	P	Digital ground
18	V33I	IO PWR	P	3.3V IO Power
19	PLL_V30O	PLL	P	3.0V PLL power
20	X12MI_SINGLE	PLL	AI	X'tal 12MHz input
21	IOD14	SD	IO	SD DATA1
22	IOA8	GPIO	IO	IOA8
23	IOA9	GPIO	IO	IOA9
24	IOA10	GPIO	IO	IOA10
25	IOA11	GPIO	IO	IOA11
26	IOA12	GPIO	IO	IOA12
27	IOA13	GPIO	IO	IOA13
28	IOA14	GPIO	IO	IOA14
29	IOA15	GPIO	IO	IOA15
30	IOB0	TFT	IO	TFT DE
31	IOB1	TFT	IO	TFT HSYNC
32	IOB2	TFT	IO	TFT VSYNC
33	IOB3	TFT	IO	TFT CLK
34	IOB8	NAND	IO	NAND FLASH Data bit 0
35	IOB9	NAND	IO	NAND FLASH Data bit 1
36	IOB10	NAND	IO	NAND FLASH Data bit 2
37	IOB11	NAND	IO	NAND FLASH Data bit 3
38	IOB12	NAND	IO	NAND FLASH Data bit 4
39	IOB13	NAND	IO	NAND FLASH Data bit 5
40	IOB14	NAND	IO	NAND FLASH Data bit 6
41	IOB15	NAND	IO	NAND FLASH Data bit 7
42	USB_V33	USB	P	3.3V USB Power
43	DM	USB	AIO	USB DM
44	DP	USB	AIO	USB DP

PKG No	Name	Group	Type	Normal Function Description
45	DDR_V25I	DDR	P	DDR SSTL2 power input
46	DDR_GND	DDR	P	DDR SSTL2 Ground
47	DDR_V25I	DDR	P	DDR SSTL2 power input
48	V12I	CORE PWR	P	1.2V Core Power input
49	IOB4	UART	IO	UART RX
50	IOB5	UART	IO	UART TX
51	IOB6	CSI	IO	CSI D0
52	IOB7	CSI	IO	CSI D1
53	IOF0	GPIO	IO	IOF0
54	IOF1	GPIO	IO	IOF1
55	IOF2	GPIO	IO	IOF2
56	IOF3	GPIO	IO	IOF3
57	IOF4	GPIO	IO	IOF4
58	IOF5	GPIO	IO	IOF5
59	IOF6	GPIO	IO	IOF6
60	IOF7	GPIO	IO	IOF7
61	IOF8	GPIO	IO	IOF8
62	IOF9	GPIO	IO	IOF9
63	IOC3	CSI	IO	CSI D5
64	IOC2	CSI	IO	CSI_D4
65	IOC1	CSI	IO	CSI D3
66	IOC0	CSI	IO	CSI D2
67	IOC4	CSI	IO	CSI D7
68	IOC5	CSI	IO	CSI D6
69	IOE4	GPIO	IO	IOE4
70	IOE5	GPIO	IO	IOE5
71	IOE6	GPIO	IO	IOE6
72	IOE7	GPIO	IO	IOE7
73	IOD6	SPI	IO	SPI CSI
74	IOD7	SPI	IO	SPI CLK
75	IOD8	SPI	IO	SPI TX
76	IOD9	SP	IO	SPI RX
77	V33I	IO PWR	P	3.3V IO Power
78	IOE3	GPIO	IO	IOE3
79	IOE2	GPIO	IO	IOE2
80	IOE1	GPIO	IO	IOE1
81	IOE0	GPIO	IO	IOE0
82	IOC15	ICE	IO	JTAG TMS
83	V12I	CORE PWR	P	1.2V Core Power input
84	VSS	Digital Ground	P	Digital ground
85	IOC14	ICE	IO	JTAG TCK
86	IOC13	ICE	IO	JTAG TDO
87	IOC12	ICE	IO	JTAG TDI
88	LINEIN5_PAD	SAR ADC	AI	SAR ADC LINEIN5
89	LINEIN4_PAD	SAR ADC	AI	SAR ADC LINEIN4

PKG No	Name	Group	Type	Normal Function Description
90	IOD0	SPIF	IO	SPI FLASH CSB
91	IOD1	SPIF	IO	SPI FLASH CLK
92	IOD2	SPIF	IO	SPI FLASH RX0
93	IOD3	SPIF	IO	SPI FLASH RX1
94	IOD4	SPIF	IO	SPI FLASH RX2
95	IOD5	SPIF	IO	SPI FLASH RX3
96	IOA0	TFT	IO	TFT D0
97	IOA1	TFT	IO	TFT D1
98	IOA2	TFT	IO	TFT D2
99	IOA3	TFT	IO	TFT D3
100	IOA4	TFT	IO	TFT D4
101	IOA5	TFT	IO	TFT D5
102	IOA6	TFT	IO	TFT D6
103	IOA7	TFT	IO	TFT D7
104	LINEIN3_PAD	SAR ADC	AI	SAR ADC LINEIN3
105	LINEIN2_PAD	SAR ADC	AI	SAR ADC LINEIN2
106	LINEIN1_PAD	SAR ADC	AI	SAR ADC LINEIN1
107	LINEIN0_PAD	SAR ADC	AI	SAR ADC LINEIN0
108	VOL	AuDAC	AO	Audio DAC left channel output
109	DAC_V33I	AuDAC	P	3.3V Power for AuDAC/SAR ADC
110	VOR	SAR ADC	AO	Audio DAC right channel output
111	AGND	SAR ADC	P	Ground for AuDAC/ADC/SAR ADC
112	ADVCM	CODEC_ADC	AO	CODEC ADC VREF
113	CODEC_V30O	CODEC ADC	P	3.0V Power for CODEC ADC. #3
114	MICIN_PAD	CODEC ADC	AI	CODEC ADC microphone input
115	V12I	CORE PWR	P	1.2V Core Power input
116	VSS	Digital Ground	P	Digital ground
117	DDR_V25O	CORE PWR	P	DDR SSTL2 power output. #2
118	REG_V28O	SYSTEM	P	LDO 2.8V power output. #2
119	FB_ADJ	CORE PWR	P	0.6V feedback voltage for DC to DC power converter reference.
120	REG_V33I	SYSTEM	P	LDO power input for DDR_REG/REGV28/REGV18
121	PWR_ON0	SYSTEM	AI	Power on key input 0
122	PWR_ON1	SYSTEM	AI	Power on key input 1
123	PWR_ON2	SYSTEM	AI	Power on key input 2
124	DC2DC_EN	SYSTEM	AO	DC to DC enable output
125	X32KI	RTC	AI	X'tal 32768Hz input
126	X32KO	RTC	AO	X'tal 32768Hz output
127	RTC_V33	RTC	P	RTC power input
128	PWR_ON3	SYSTEM	AI	Power on key input 3

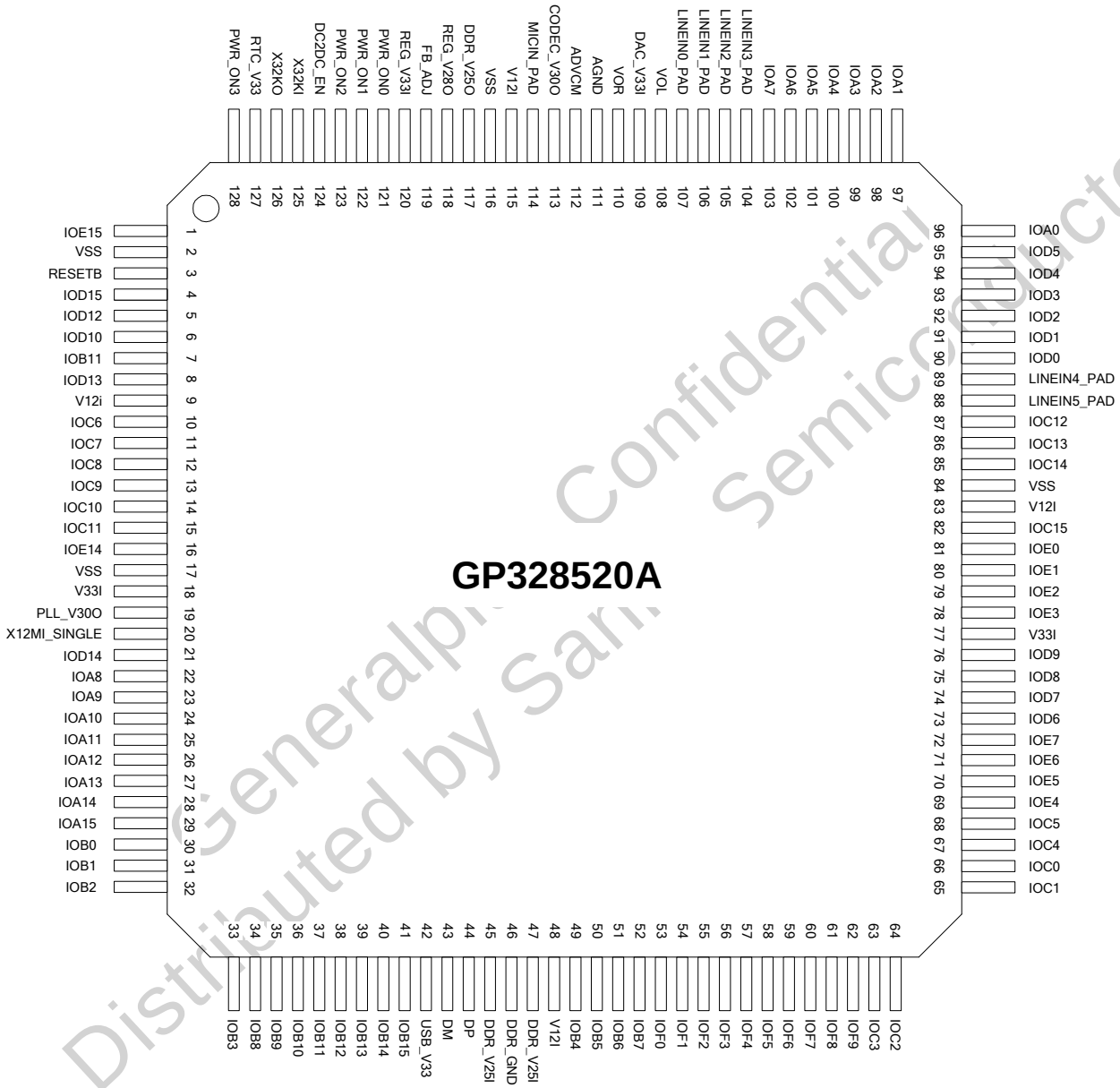
Note1: AO: Analog Output, AI: Analog Input

Note2: Power source REG33I

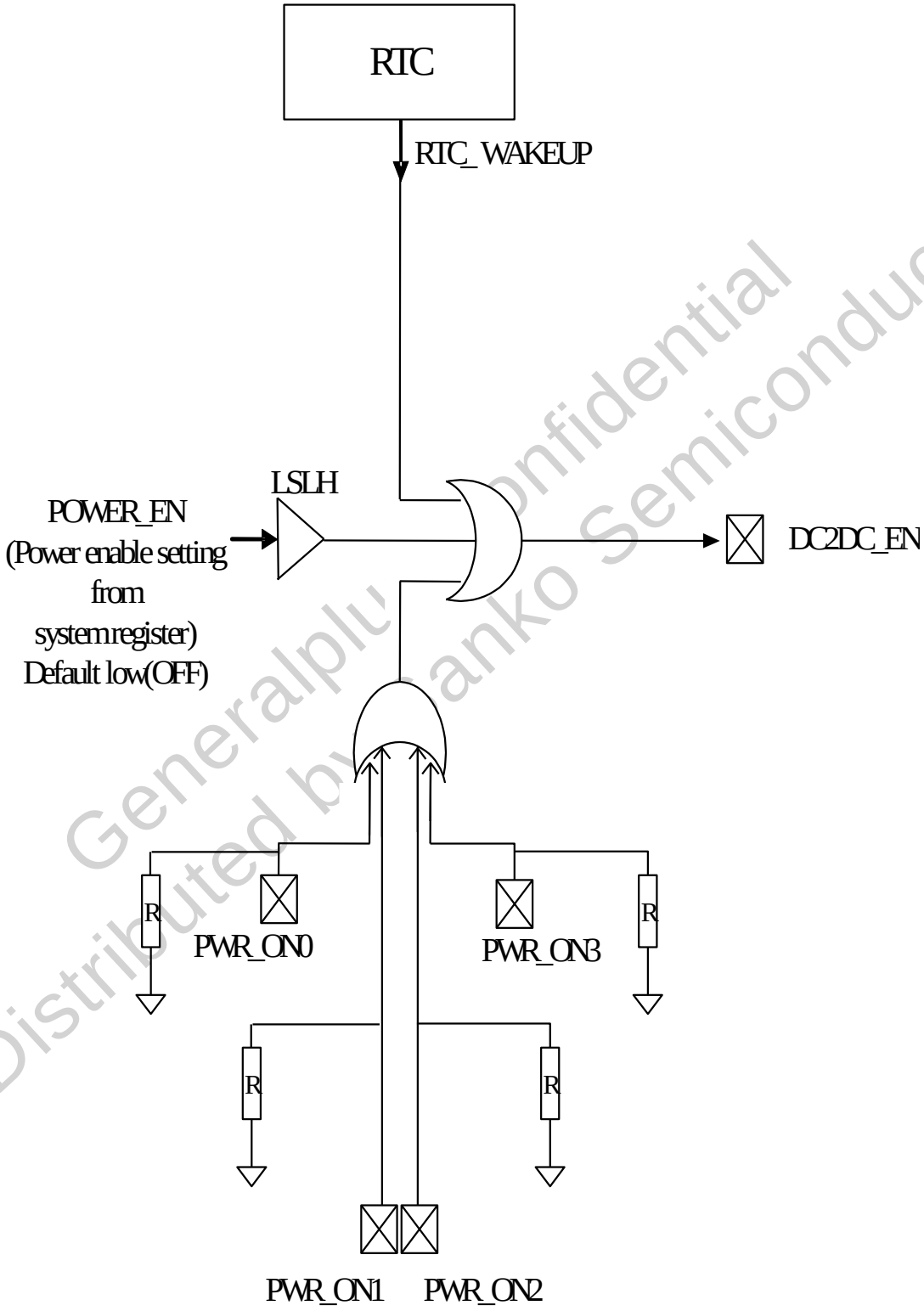
Note3: Power source DAC_V33I

4.1. Package Pin Sequence

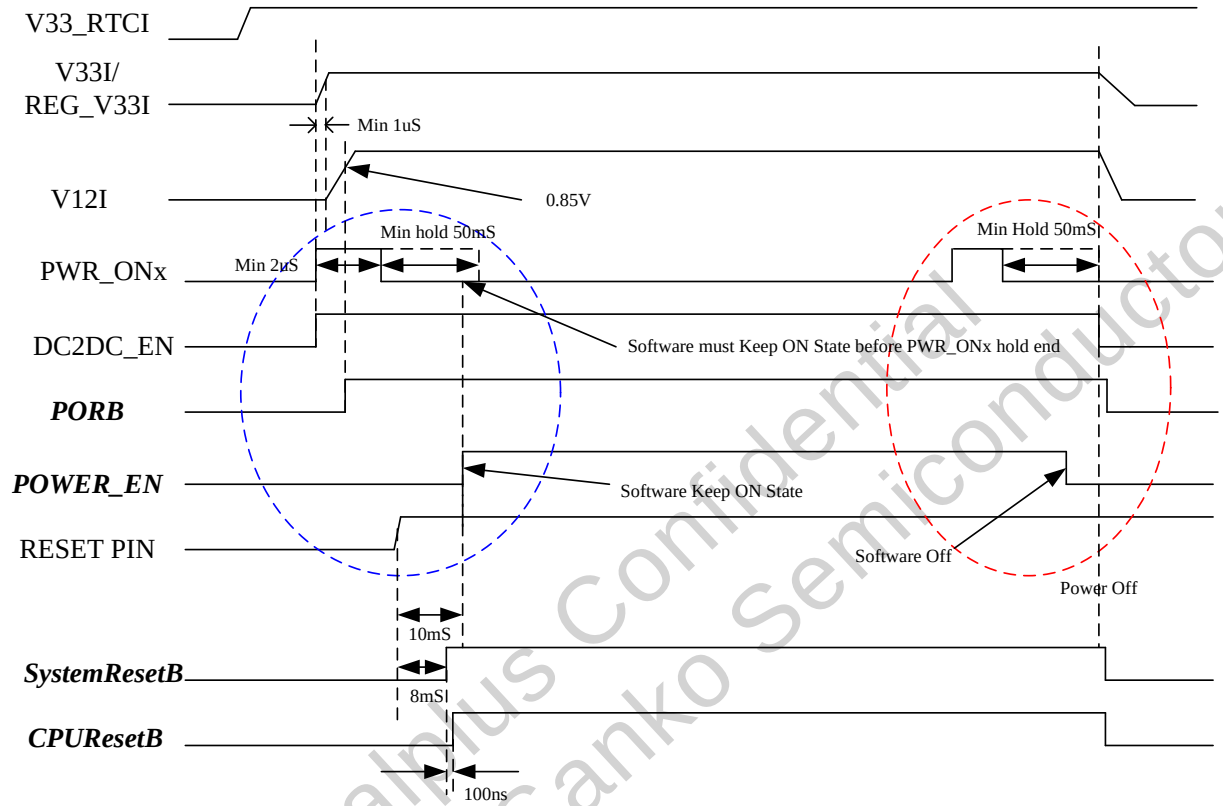
LQFP128 Package Top View



5. POWER MACRO FUNCTIONAL BLOCK



6. POWER SEQUENCE



Note 1. Word in ***Bold and Italic*** means IC internal signal

Note 2. In fast shutdown mode, PWR_Onx min hold time is 3mS

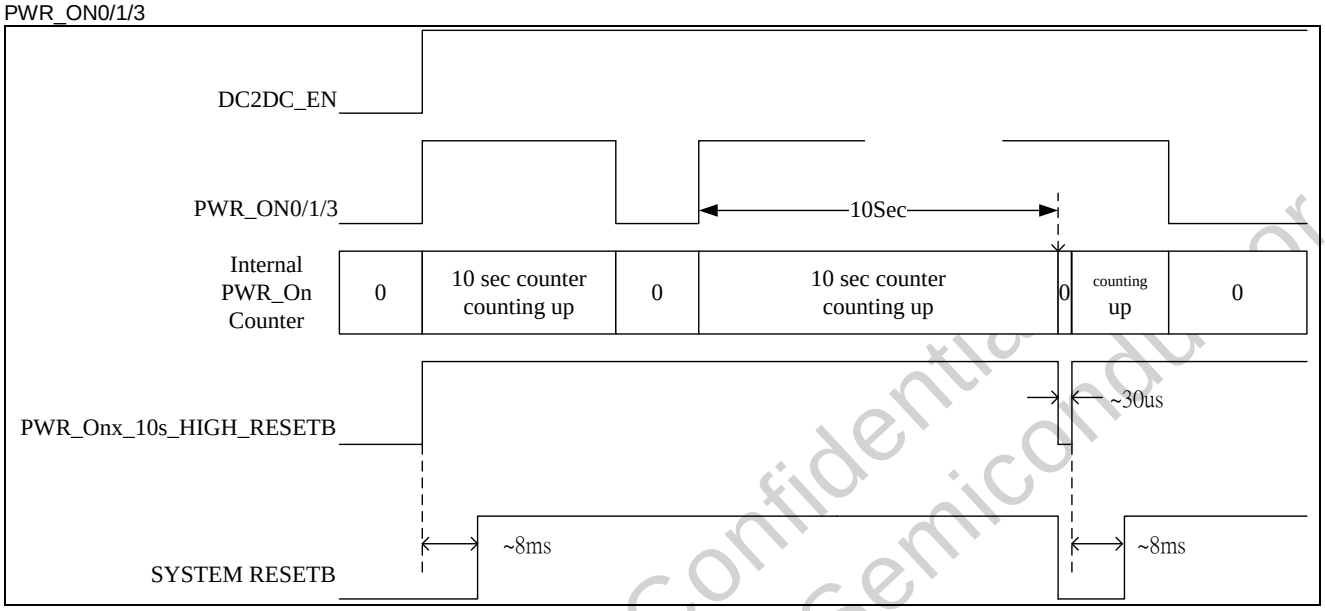
Note 3. PORB will be released after power satisfy all of following conditions,

1. V12I reach 0.85V
2. 2 mS late after REG_V33I reach 1.6V.
3. If user enable LVR and REG_V33I reach selected voltage level.

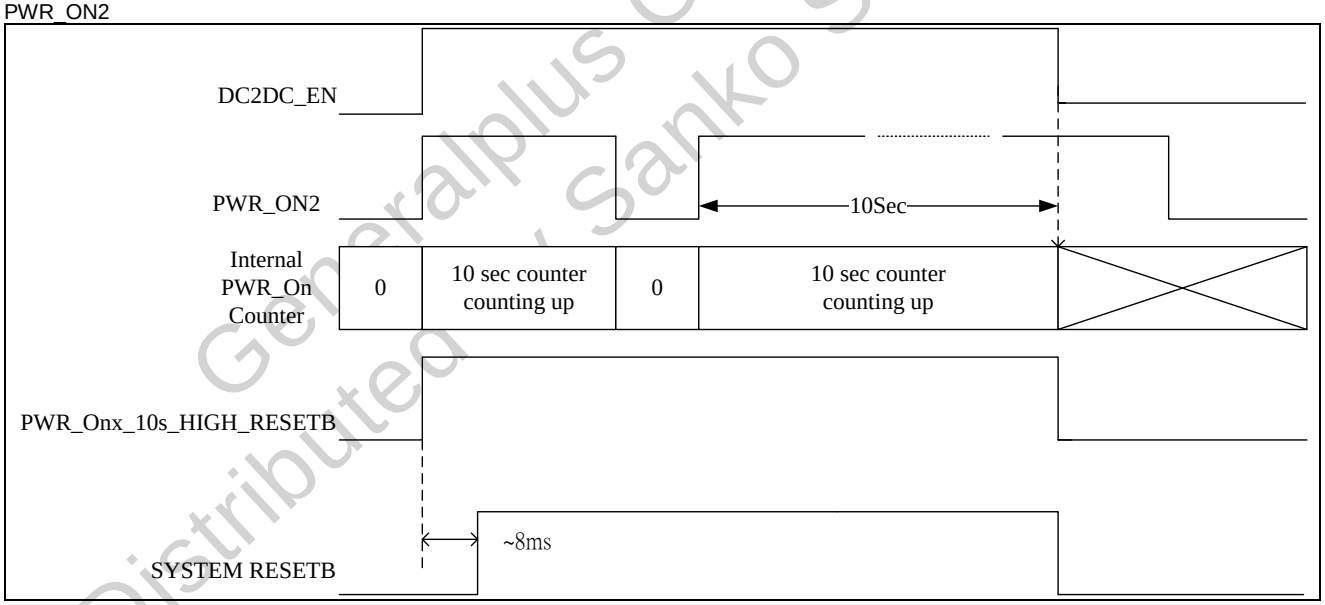
Note 4. During the entire power-on period, V33I must be higher than V12I.

7. POWER-ON KEY LONG PRESS RESET

PWR_ON0/1/3



PWR_ON2



Key No.	Default 10 Sec reset	Wake up system after 1st time power up	High Level active	Rising Edge active
NO0	ON	YES	YES	NO
NO1	OFF	NO	YES	NO
NO2	OFF	YES	NO	YES*1
NO3	OFF	YES	YES	NO

Note: PWR_ON0/1/2 includes a 5us deglitch circuit; PWR_ON2 shall be kept at last 5us for the rising edge detection.

8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage 1	REG_V33I	-0.3 to 3.6	V
Supply Voltage 2	RTC_V33I	-0.3 to 3.6	V
Supply Voltage 3	V33I	-0.3 to 3.6	V
Supply Voltage 4	PLL_V30O	-0.3 to 3.6	V
Supply Voltage 5	USB_V33	-0.3 to 3.6	V
Supply Voltage 6	DAC_V33I	-0.3 to 3.6	V
Supply Voltage 7	CODEC_V30O	-0.3 to 3.6	V
Supply Voltage 8	REG_V28O	-0.3 to 3.6	V
Supply Voltage 9	DDR_V25I	-0.3 to 3.6	V
Supply Voltage 10	DDR_V25O	-0.3 to 3.6	V
Supply Voltage 11	V12I	-0.3 to 1.4	V
Input Voltage	V_{IN}	-0.3 to 3.6	V
Operating Temperature	T_A	-20~70	℃
Storage Temperature	T_{STG}	-40 to +150	℃

8.2. DC Characteristics

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Supply Voltage 1	REG_V33I	2.7	3.3	3.6	V	-
Supply Voltage 2	RTC_V33I	2.2	3.3	3.6	V	-
Supply Voltage 3	V33I	2.7	3.3	3.6	V	-
Supply Voltage 4	PLL_V30O	2.7	3.3	3.6	V	-
Supply Voltage 5	USB_V33	3.0	3.3	3.6	V	
Supply Voltage 6	DAC_V33I	2.7	3.3	3.6	V	-
Supply Voltage 7	CODEC_V30O	2.7	3.0	3.6	V	-
Supply Voltage 8	REG_V28O	1.35	2.8	3.3	V	-
Supply Voltage 9	DDR_V25I	2.25	2.5	2.75	V	-
Supply Voltage 10	DDR_V25O	2.25	2.5	2.75	V	-
Supply Voltage 11	V12I	1.1	1.2	1.32	V	-
Operating Current Case 1	I_{OP1}	-	164	-	mA	Core power current@ System 171MHz, CPU 513MHz V33=3.3V, V12=1.2V , Sensor(CSI) +PPU+ TFT
Operating Current Case 2	I_{OP2}	-	60	-	mA	Core power current@ System 87MHz, CPU 87MHz, V33=3.3V, V12=1.2V , Sensor(CSI) +PPU+ TFT
Operating Current Case 3	I_{OP3}	-	25	-	mA	Core Power current@ System 24MHz CPU 48MHz V33=3.3V, V12=1.2V DAC decode MP3
Power Down Current	I_{PD}	-	10	-	μA	All power is off except RTC macro

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
						(RTC_V33=3.3V, the others = 0V) X'tal 32K on, IOSC32K off
High Input Voltage	V_{IH}	0.7V33	-	V33	V	-
Low Input Voltage	V_{IL}	VSS	-	0.3V33	V	-
Crystal Frequency 1	-	-	32768	-	Hz	-
Crystal Frequency 2	$F_{CRYSTAL}$	-	12	-	MHz	-
System Clock	F_{SYS}	5461Hz[1]	-	171	MHz	-

Note1: By setting clock divider and changing system clock to SLOW mode (32768Hz).

8.3. GPIO Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Input High Voltage(VIH)	0.55*V33	-	V33	V	-
Input Low Voltage(VIL)	0	-	0.45*V33	V	-
Output High Voltage(VOH)	0.8*V33	-	V33	V	-
Output Low Voltage(VOL)	0	-	0.2*V33	V	
IOA**,IOB***,IOC,IOD,IOE**** Output Driving Current(IOH)	-	15/20	-	mA	V33@3.3V, room temperature
IOA**,IOB***,IOC,IOD,IOE**** Output Sinking Current(IOL)	-	-15/-22	-	mA	V33@3.3V, room temperature
IOA[7:4], IOB[7:4], IOE[11:8], IOF Output Driving Current(IOH)	-	9/16	-	mA	V33@3.3V, room temperature
IOA[7:4], IOB[7:4], IOE[11:8], IOF Output Sinking Current(IOL)	-	-9/-17	-	mA	V33@3.3V, room temperature
Power On Pad0/1/3 High Pulse for Power Enable	5	-/-8	-	us	
Power On Pad2 High Pulse for Power Enable	1	-	-	us	
Power On Pad0/1 Input High Voltage(POVIH)	-	0.7*RTC_V33I	-	V	
Power On Pad2/3 Input High Voltage(POVIH)	1.5	-	-	V	
Power On Pad(PWR_ON0/1) Internal Pull-Down Resistor(POPRPD)	9K	18K	-	Ω	
Power On Pad(PWR_ON2/3) Internal Pull-Down Resistor(POPRPD)	100K	200K	-	Ω	
IOA,IOB,IOC,IOD,IOE,IOF Internal Pull-Up Resistor(RPU)*	40K*0.85	40K	40K*1.15	Ω	V33@3.3V, room temperature
IOA,IOB,IOC,IOD,IOE,IOF Internal Pull-Down Resistor(RPD)*	50K*0.85	50K	50K*1.15	Ω	V33@3.3V, room temperature

*GPIO pull resistor will vary with V33.

**IOA not including IOA[7:4]

***IOB not including IOB[7:4]

****IOE not including IOE[11:8]

8.4. Audio DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	16	16	16	Bit	Audio DAC digital input
Full Scale Output Voltage	0.55* DAC_V33I	0.6* DAC_V33I	-	Vp-p	-
THD+N (Fin = 0.997kHz)	0.15	0.10	-	%	Fin=0.997KHz output loading=32 ohm
Dynamic Range	75	79	-	dB	Fin=0.997KHz w/ -60dB output loading=32 ohm
Output Loading	32	-	-	ohm	-
Frequency Response	20	-	19200	Hz	-

8.5. CODEC ADC/MIC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	16	16	16	Bit	CODEC ADC digital output
Input Voltage Range	2.7	-	3.6	V	-
SNR	80	84	-	dB	Boost=0dB, PGA=0dB, filter: 20K LPF + A weighting@V33_DA16=3.3V
THD+N	70	72.8	-	dB	Boost=0dB, PGA=0dB, Fin=0.997KHz, Fs=48kHz @V33_DA16=3.3V
Dynamic Range	80	84.8	-	dB	Boost=0dB, PGA=0dB, filter: 20K LPF + A weighting @V33_DA16=3.3V
MICBIAS	CODEC_V30O * 0.75	2.25	-	V	MICBIAS= V33_AD * 0.75

8.6. SAR ADC Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SAR ADC Input Voltage Range	VIN_RANGE	2.7	-	3.6	V
Resolution of ADC	RESO	12	12	12	bit
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD (Note 1)	58	58.56	-	dB
Effective Number of Bit	ENOB (Note 2)	9.03	9.44	-	bit
Integral Non-Linearity of ADC	INL	-2	-	2	LSB (Note 3)
Differential Non-Linearity of ADC	DNL	-2	-	2	LSB
No Missing Code		10	11	12	bit
AD Conversion Rate=ADCCLK/20	F_{CONV}	-	534K	800K	Hz(Note4)

Note1: The SINAD testing condition at VINLp-p = 0.8 * DAC_V33I, F_{CONV} = 200KHz, Fin = 1.0KHz Sine waves at DAC_V33I = 3.0V from ADC input.

Note2: ENOB = (SINAD - 1.76) / 6.02.

Note3: LSB means Least Significant Bit (at 12-bit resolution).

Note4: @System CLK 171MHz, ADCCLK = SYSCLK/16.

8.7. DDR Regulator for DDR Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.7	-	3.6	V
Maximum Current Output	IREGO	-	-	100	mA
Output Voltage	VREGO	2.5*0.95	2.5(Note)	2.5*1.05	V
Standby Current	IREGS	-	-	2	uA

Note: The typical regulator output voltage is adjustable through register settings.

8.8. 3.3V-to-2.8V Regulator for Sensor Characteristics

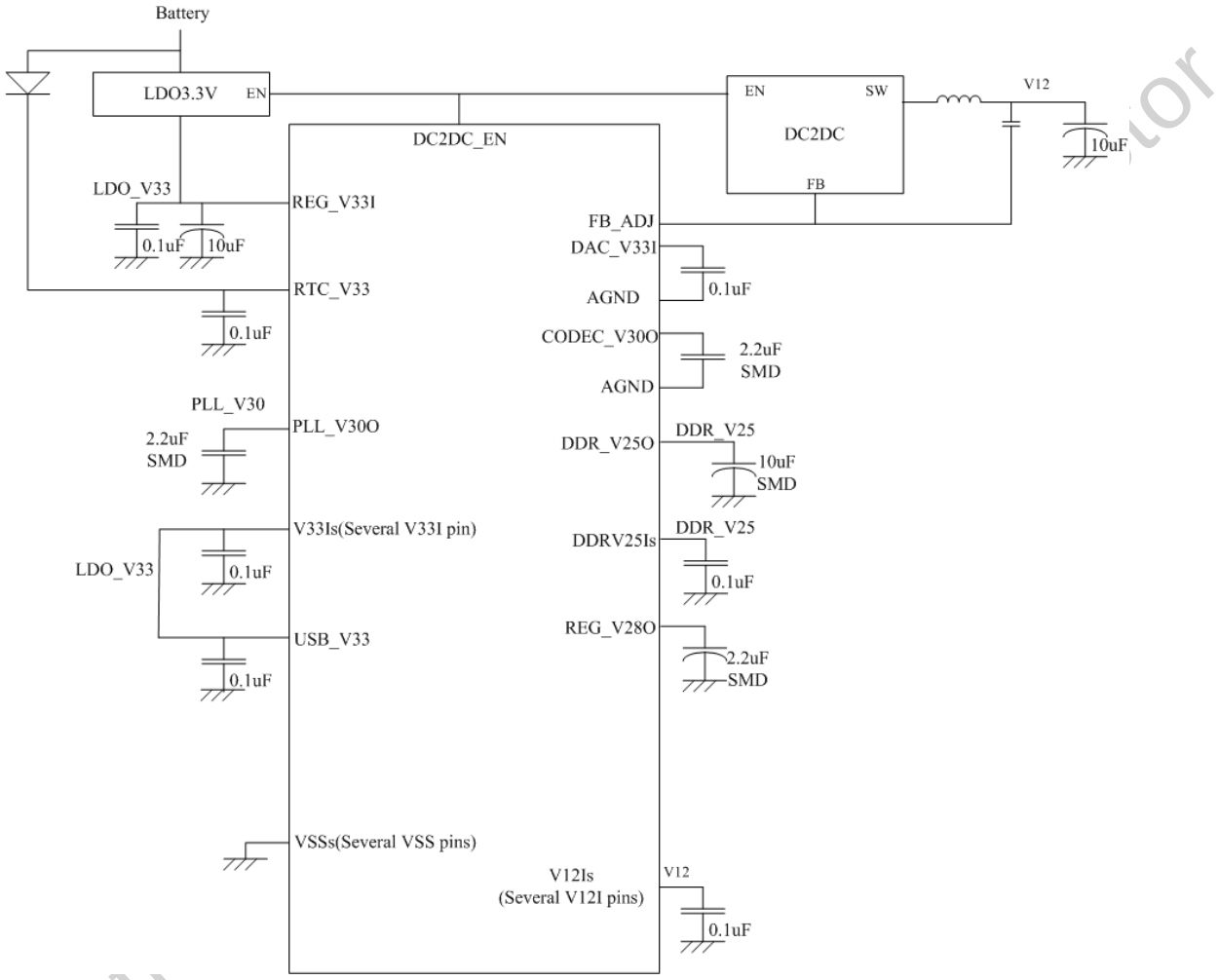
Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	3.0	-	3.6	V
Maximum Current Output	IREGO	-	-	60	mA
Output Voltage	VREGO	2.8*0.95	2.8(Note)	2.8*1.05	V
Standby Current	IREGS	-	-	2	uA

Note: The typical regulator output voltage is adjustable through register settings.

9. RECOMMENDED BOARD LAYOUT

9.1. Power and Ground

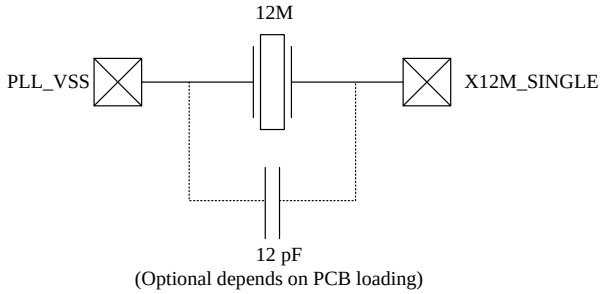
All power and ground pins are connected as in the following diagram for general application. The decoupling capacitor of 0.1μF, 10μF, and 47uF should be connected to each corresponding power pin of IC and 0.1uF capacitor must be as close as possible to the power pin. Each V33I/V12I requires one 0.1μF capacitor and must be as close as possible to the power pin.



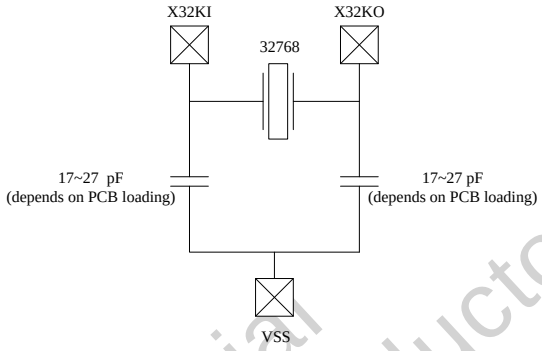
Note1: DC2DC should be located as close as possible to the main chip. If possible, the distance between DC2DC and main chip should be less than 1cm.
Note2: The wire width of FB_ADJ at least 2x wire width, if possible, please shading FB_ADJ
Note3: DC2DC feedback reference Voltage must be 0.6V because of FB_ADJ feedback 0.6V to DC2DC.

9.2. Crystal and PLL

When 12MHz crystal is applied in the system, please connect the crystal circuit as indicated in the following diagram.



Note*: Please refer to the crystal's application circuit.



A Crystal (32768Hz) may be used for applications that may involve with precise time clock requirement. See the above diagram for more details.

Note*: Please refer to the crystal's application circuit.

10. PACKAGE/PAD LOCATIONS

10.1. Ordering Information

Product Number	Package Type
GP328520A_XXXX-NnnV-QLM5x	Halogen Free Package

Note1: Code number is assigned for customer.

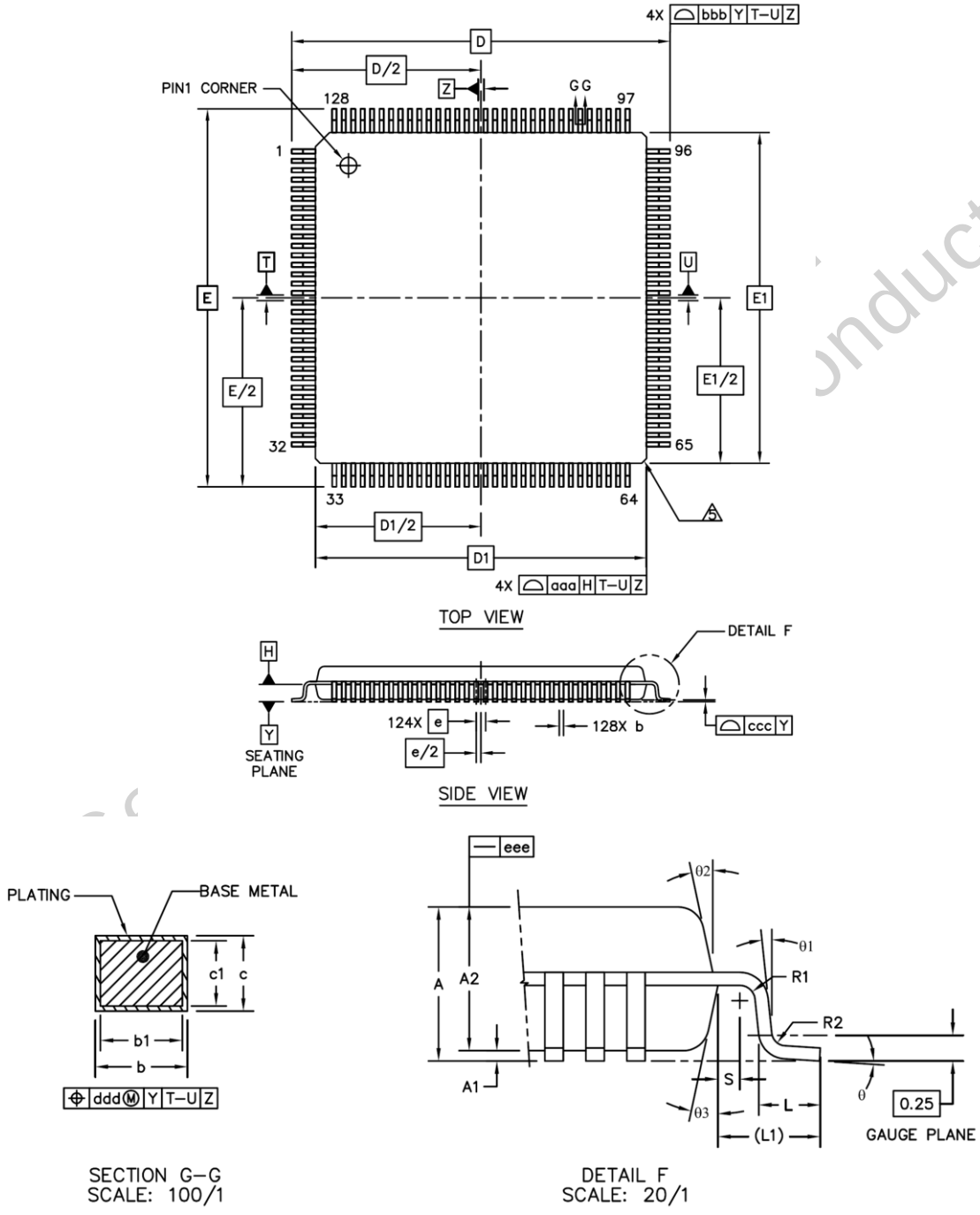
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

Note4: PartNumber_XXXX where "_XXXX" is a 4-digit code, managed by Generalplus, to indicate additional software algorithm(s) or royalty type(s) applied to the product. Same part numbers bearing different codes make no differences in hardware specification.

10.2. Package Information

LQFP 128



Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
b1	0.13	-	0.19
c	0.09	-	0.20

Symbol	Millimeter		
	Min.	Nom.	Max.
c1	0.09	-	0.16
D	16.00 BSC		
E	16.00 BSC		
D1	14.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°
θ1	0°	-	-°
θ2	11°	12°	13°
θ3	11°	12°	13°
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
aaa	0.10		
bbb	0.20		
ccc	0.08		
ddd	0.07		
eee	0.05		

11. DISCLAIMER

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12. REVISION HISTORY

Date	Revision #	Description	Page
Sep. 24, 2020	0.1	Preliminary version.	23