University Of Waterloo

ECE 429

Task 3
Register File and Execute Stage

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July 4, 2012

1 Register File Output

Listing 1: Bubble Sort Register File Output

```
# Initializing memory
# Initializing Fetch module
# opened file srec_files/BubbleSort.srec
#
# read in file
#
# Time: 1350, PC: 80020000, RS: 29, RT: 29, IR: 27bdffc8
# Time: 1360, PC: 80020004, RS: 29, RT: 31, IR: afbf0034
# Time: 1370, PC: 80020008, RS: 29, RT: 30, IR: afbe0030
# Time: 1380, PC: 8002000c, RS: 29, RT: 0, IR: 03a0f021
# Time: 1390, PC: 80020010, RS: 0, RT: 2, IR: 2402000c
# Time: 1400, PC: 80020014, RS: 30, RT: 2, IR: afc20010
# Time: 1410, PC: 80020018, RS: 0, RT: 2, IR: 24020009
# Time: 1420, PC: 8002001c, RS: 30, RT: 2, IR: afc20014
# Time: 1430, PC: 80020020, RS: 0, RT: 2, IR: 24020004
# Time: 1440, PC: 80020024, RS: 30, RT: 2, IR: afc20018
# Time: 1450, PC: 80020028, RS: 0, RT: 2, IR: 24020063
# Time: 1460, PC: 8002002c, RS: 30, RT: 2, IR: afc2001c
# Time: 1470, PC: 80020030, RS: 0, RT: 2, IR: 24020078
# Time: 1480, PC: 80020034, RS: 30, RT: 2, IR: afc20020
# Time: 1490, PC: 80020038, RS: 0, RT: 2, IR: 24020001
# Time: 1500, PC: 8002003c, RS: 30, RT: 2, IR: afc20024
# Time: 1510, PC: 80020040, RS: 0, RT: 2, IR: 24020003
# Time: 1520, PC: 80020044, RS: 30, RT: 2, IR: afc20028
# Time: 1530, PC: 80020048, RS: 0, RT: 2, IR: 2402000a
# Time: 1540, PC: 8002004c, RS: 30, RT: 2, IR: afc2002c
# Time: 1550, PC: 80020050, RS: 30, RT: 2, IR: 27c20010
# Time: 1560, PC: 80020054, RS: 2, RT: 0, IR: 00402021
# Time: 1570, PC: 80020058, RS: 0, RT: 5, IR: 24050008
# Time: 1580, PC: 8002005c, RS: 0, RT: 0, IR: 0c008020
# Time: 1590, PC: 80020060, RS: 0, RT: 0, IR: 00000000
# Time: 1600, PC: 80020064, RS: 0, RT: 0, IR: 00001021
# Time: 1610, PC: 80020068, RS: 30, RT: 0, IR: 03c0e821
# Time: 1620, PC: 8002006c, RS: 29, RT: 31, IR: 8fbf0034
# Time: 1630, PC: 80020070, RS: 29, RT: 30, IR: 8fbe0030
# Time: 1640, PC: 80020074, RS: 29, RT: 29, IR: 27bd0038
# Time: 1650, PC: 80020078, RS: 31, RT: 0, IR: 03e00008
# Time: 1660, PC: 8002007c, RS: 0, RT: 0, IR: 00000000
# Time: 1670, PC: 80020080, RS: 29, RT: 29, IR: 27bdffe8
# Time: 1680, PC: 80020084, RS: 29, RT: 30, IR: afbe0014
# Time: 1690, PC: 80020088, RS: 29, RT: 0, IR: 03a0f021
# Time: 1700, PC: 8002008c, RS: 30, RT: 4, IR: afc40018
# Time: 1710, PC: 80020090, RS: 30, RT: 5, IR: afc5001c
# Time: 1720, PC: 80020094, RS: 30, RT: 0, IR: afc00000
# Time: 1730, PC: 80020098, RS: 0, RT: 0, IR: 0800805f
# Time: 1740, PC: 8002009c, RS: 0, RT: 0, IR: 00000000
# Time: 1750, PC: 800200a0, RS: 0, RT: 2, IR: 24020001
# Time: 1760, PC: 800200a4, RS: 30, RT: 2, IR: afc20004
```

```
# Time: 1770, PC: 800200a8, RS: 0, RT: 0, IR: 08008055
# Time: 1780, PC: 800200ac, RS: 0, RT: 0, IR: 00000000
# Time: 1790, PC: 800200b0, RS: 30, RT: 2, IR: 8fc20004
# Time: 1800, PC: 800200b4, RS: 2, RT: 2, IR: 2442ffff
# Time: 1810, PC: 800200b8, RS: 0, RT: 2, IR: 00021080
# Time: 1820, PC: 800200bc, RS: 30, RT: 3, IR: 8fc30018
# Time: 1830, PC: 800200c0, RS: 3, RT: 2, IR: 00621021
# Time: 1840, PC: 800200c4, RS: 2, RT: 3, IR: 8c430000
# Time: 1850, PC: 800200c8, RS: 30, RT: 2, IR: 8fc20004
# Time: 1860, PC: 800200cc, RS: 0, RT: 2, IR: 00021080
# Time: 1870, PC: 800200d0, RS: 30, RT: 4, IR: 8fc40018
# Time: 1880, PC: 800200d4, RS: 4, RT: 2, IR: 00821021
# Time: 1890, PC: 800200d8, RS: 2, RT: 2, IR: 8c420000
# Time: 1900, PC: 800200dc, RS: 2, RT: 3, IR: 0043102a
# Time: 1910, PC: 800200e0, RS: 2, RT: 0, IR: 10400019
# Time: 1920, PC: 800200e4, RS: 0, RT: 0, IR: 00000000
# Time: 1930, PC: 800200e8, RS: 30, RT: 2, IR: 8fc20004
# Time: 1940, PC: 800200ec, RS: 2, RT: 2, IR: 2442ffff
# Time: 1950, PC: 800200f0, RS: 0, RT: 2, IR: 00021080
# Time: 1960, PC: 800200f4, RS: 30, RT: 3, IR: 8fc30018
# Time: 1970, PC: 800200f8, RS: 3, RT: 2, IR: 00621021
# Time: 1980, PC: 800200fc, RS: 2, RT: 2, IR: 8c420000
# Time: 1990, PC: 80020100, RS: 30, RT: 2, IR: afc20008
# Time: 2000, PC: 80020104, RS: 30, RT: 2, IR: 8fc20004
# Time: 2010, PC: 80020108, RS: 2, RT: 2, IR: 2442ffff
# Time: 2020, PC: 8002010c, RS: 0, RT: 2, IR: 00021080
# Time: 2030, PC: 80020110, RS: 30, RT: 3, IR: 8fc30018
# Time: 2040, PC: 80020114, RS: 3, RT: 2, IR: 00621021
# Time: 2050, PC: 80020118, RS: 30, RT: 3, IR: 8fc30004
# Time: 2060, PC: 8002011c, RS: 0, RT: 3, IR: 00031880
# Time: 2070, PC: 80020120, RS: 30, RT: 4, IR: 8fc40018
# Time: 2080, PC: 80020124, RS: 4, RT: 3, IR: 00831821
# Time: 2090, PC: 80020128, RS: 3, RT: 3, IR: 8c630000
# Time: 2100, PC: 8002012c, RS: 2, RT: 3, IR: ac430000
# Time: 2110, PC: 80020130, RS: 30, RT: 2, IR: 8fc20004
# Time: 2120, PC: 80020134, RS: 0, RT: 2, IR: 00021080
# Time: 2130, PC: 80020138, RS: 30, RT: 3, IR: 8fc30018
# Time: 2140, PC: 8002013c, RS: 3, RT: 2, IR: 00621021
# Time: 2150, PC: 80020140, RS: 30, RT: 3, IR: 8fc30008
# Time: 2160, PC: 80020144, RS: 2, RT: 3, IR: ac430000
# Time: 2170, PC: 80020148, RS: 30, RT: 2, IR: 8fc20004
# Time: 2180, PC: 8002014c, RS: 2, RT: 2, IR: 24420001
# Time: 2190, PC: 80020150, RS: 30, RT: 2, IR: afc20004
# Time: 2200, PC: 80020154, RS: 30, RT: 3, IR: 8fc3001c
# Time: 2210, PC: 80020158, RS: 30, RT: 2, IR: 8fc20000
# Time: 2220, PC: 8002015c, RS: 3, RT: 2, IR: 00621823
# Time: 2230, PC: 80020160, RS: 30, RT: 2, IR: 8fc20004
# Time: 2240, PC: 80020164, RS: 2, RT: 3, IR: 0043102a
# Time: 2250, PC: 80020168, RS: 2, RT: 0, IR: 1440ffd1
# Time: 2260, PC: 8002016c, RS: 0, RT: 0, IR: 00000000
# Time: 2270, PC: 80020170, RS: 30, RT: 2, IR: 8fc20000
```

```
# Time: 2280, PC: 80020174, RS: 2, RT: 2, IR: 24420001
# Time: 2290, PC: 80020178, RS: 30, RT: 2, IR: afc20000
# Time: 2300, PC: 8002017c, RS: 30, RT: 3, IR: 8fc30000
# Time: 2310, PC: 80020180, RS: 30, RT: 2, IR: 8fc2001c
# Time: 2320, PC: 80020184, RS: 3, RT: 2, IR: 0062102a
# Time: 2330, PC: 80020188, RS: 2, RT: 0, IR: 1440ffc5
# Time: 2340, PC: 8002018c, RS: 0, RT: 0, IR: 00000000
# Time: 2350, PC: 80020190, RS: 30, RT: 0, IR: 03c0e821
# Time: 2360, PC: 80020194, RS: 29, RT: 30, IR: 8fbe0014
# Time: 2370, PC: 80020198, RS: 29, RT: 29, IR: 27bd0018
# Time: 2380, PC: 8002019c, RS: 31, RT: 0, IR: 03e00008
# Time: 2390, PC: 800201a0, RS: 0, RT: 0, IR: 00000000
# ** Note: $finish : reg_file_tb.v(106)
# Time: 2400 ns Iteration: 0 Instance: /reg_file_tb
```

Listing 2: Simple Add Register File Output

```
# Initializing memory
# Initializing Fetch module
# opened file srec_files/SimpleAdd.srec
#
# read in file
#
# Time: 260, PC: 80020000, RS: 29, RT: 29, IR: 27bdffe8
# Time: 270, PC: 80020004, RS: 29, RT: 30, IR: afbe0014
# Time: 280, PC: 80020008, RS: 29, RT: 0, IR: 03a0f021
# Time: 290, PC: 8002000c, RS: 0, RT: 2, IR: 24020003
# Time: 300, PC: 80020010, RS: 30, RT: 2, IR: afc20000
# Time: 310, PC: 80020014, RS: 0, RT: 2, IR: 24020002
# Time: 320, PC: 80020018, RS: 30, RT: 2, IR: afc20004
# Time: 330, PC: 8002001c, RS: 30, RT: 0, IR: afc00008
# Time: 340, PC: 80020020, RS: 30, RT: 3, IR: 8fc30000
# Time: 350, PC: 80020024, RS: 30, RT: 2, IR: 8fc20004
# Time: 360, PC: 80020028, RS: 3, RT: 2, IR: 00621021
# Time: 370, PC: 8002002c, RS: 30, RT: 2, IR: afc20008
# Time: 380, PC: 80020030, RS: 30, RT: 2, IR: 8fc20008
# Time: 390, PC: 80020034, RS: 30, RT: 0, IR: 03c0e821
# Time: 400, PC: 80020038, RS: 29, RT: 30, IR: 8fbe0014
# Time: 410, PC: 8002003c, RS: 29, RT: 29, IR: 27bd0018
# Time: 420, PC: 80020040, RS: 31, RT: 0, IR: 03e00008
# Time: 430, PC: 80020044, RS: 0, RT: 0, IR: 00000000
# ** Note: $finish : reg_file_tb.v(106)
# Time: 440 ns Iteration: 0 Instance: /reg_file_tb
```

Listing 3: Simple If Register File Output

```
# Initializing memory
# Initializing Fetch module
# opened file srec_files/SimpleIf.srec
#
# read in file
#
```

```
# Time: 430, PC: 80020000, RS: 29, RT: 29, IR: 27bdffe8
# Time: 440, PC: 80020004, RS: 29, RT: 30, IR: afbe0014
# Time: 450, PC: 80020008, RS: 29, RT: 0, IR: 03a0f021
# Time: 460, PC: 8002000c, RS: 0, RT: 2, IR: 24020003
# Time: 470, PC: 80020010, RS: 30, RT: 2, IR: afc20000
# Time: 480, PC: 80020014, RS: 0, RT: 2, IR: 24020002
# Time: 490, PC: 80020018, RS: 30, RT: 2, IR: afc20004
# Time: 500, PC: 8002001c, RS: 30, RT: 0, IR: afc00008
# Time: 510, PC: 80020020, RS: 30, RT: 2, IR: 8fc20000
# Time: 520, PC: 80020024, RS: 2, RT: 2, IR: 28420005
# Time: 530, PC: 80020028, RS: 2, RT: 0, IR: 10400007
# Time: 540, PC: 8002002c, RS: 0, RT: 0, IR: 00000000
# Time: 550, PC: 80020030, RS: 30, RT: 3, IR: 8fc30000
# Time: 560, PC: 80020034, RS: 30, RT: 2, IR: 8fc20004
# Time: 570, PC: 80020038, RS: 3, RT: 2, IR: 00621021
# Time: 580, PC: 8002003c, RS: 30, RT: 2, IR: afc20000
# Time: 590, PC: 80020040, RS: 0, RT: 0, IR: 08008016
# Time: 600, PC: 80020044, RS: 0, RT: 0, IR: 00000000
# Time: 610, PC: 80020048, RS: 30, RT: 3, IR: 8fc30000
# Time: 620, PC: 8002004c, RS: 30, RT: 2, IR: 8fc20004
# Time: 630, PC: 80020050, RS: 3, RT: 2, IR: 00621023
# Time: 640, PC: 80020054, RS: 30, RT: 2, IR: afc20000
# Time: 650, PC: 80020058, RS: 30, RT: 3, IR: 8fc30000
# Time: 660, PC: 8002005c, RS: 30, RT: 2, IR: 8fc20004
# Time: 670, PC: 80020060, RS: 3, RT: 2, IR: 00621021
# Time: 680, PC: 80020064, RS: 30, RT: 2, IR: afc20008
# Time: 690, PC: 80020068, RS: 30, RT: 2, IR: 8fc20008
# Time: 700, PC: 8002006c, RS: 30, RT: 0, IR: 03c0e821
# Time: 710, PC: 80020070, RS: 29, RT: 30, IR: 8fbe0014
# Time: 720, PC: 80020074, RS: 29, RT: 29, IR: 27bd0018
# Time: 730, PC: 80020078, RS: 31, RT: 0, IR: 03e00008
# Time: 740, PC: 8002007c, RS: 0, RT: 0, IR: 00000000
# ** Note: $finish : reg_file_tb.v(106)
# Time: 750 ns Iteration: 0 Instance: /reg_file_tb
```

Listing 4: Sum Array Register File Output

```
# Initializing memory
# Initializing Fetch module
# opened file srec_files/SumArray.srec
#
# read in file
#
# Time: 570, PC: 80020000, RS: 29, RT: 29, IR: 27bdffc8
# Time: 580, PC: 80020004, RS: 29, RT: 30, IR: afbe0034
# Time: 590, PC: 80020008, RS: 29, RT: 0, IR: 03a0f021
# Time: 600, PC: 8002000c, RS: 30, RT: 0, IR: afc00000
# Time: 610, PC: 80020010, RS: 30, RT: 0, IR: afc00004
# Time: 620, PC: 80020014, RS: 30, RT: 0, IR: afc00000
# Time: 630, PC: 80020018, RS: 0, RT: 0, IR: 08008010
# Time: 640, PC: 8002001c, RS: 0, RT: 0, IR: 00000000
# Time: 650, PC: 80020020, RS: 30, RT: 2, IR: 8fc20000
```

```
# Time: 660, PC: 80020024, RS: 0, RT: 2, IR: 00021080
# Time: 670, PC: 80020028, RS: 30, RT: 2, IR: 03c21021
# Time: 680, PC: 8002002c, RS: 30, RT: 3, IR: 8fc30000
# Time: 690, PC: 80020030, RS: 2, RT: 3, IR: ac430008
# Time: 700, PC: 80020034, RS: 30, RT: 2, IR: 8fc20000
# Time: 710, PC: 80020038, RS: 2, RT: 2, IR: 24420001
# Time: 720, PC: 8002003c, RS: 30, RT: 2, IR: afc20000
# Time: 730, PC: 80020040, RS: 30, RT: 2, IR: 8fc20000
# Time: 740, PC: 80020044, RS: 2, RT: 2, IR: 2842000a
# Time: 750, PC: 80020048, RS: 2, RT: 0, IR: 1440fff5
# Time: 760, PC: 8002004c, RS: 0, RT: 0, IR: 00000000
# Time: 770, PC: 80020050, RS: 30, RT: 0, IR: afc00000
# Time: 780, PC: 80020054, RS: 0, RT: 0, IR: 08008021
# Time: 790, PC: 80020058, RS: 0, RT: 0, IR: 00000000
# Time: 800, PC: 8002005c, RS: 30, RT: 2, IR: 8fc20000
# Time: 810, PC: 80020060, RS: 0, RT: 2, IR: 00021080
# Time: 820, PC: 80020064, RS: 30, RT: 2, IR: 03c21021
# Time: 830, PC: 80020068, RS: 2, RT: 2, IR: 8c420008
# Time: 840, PC: 8002006c, RS: 30, RT: 3, IR: 8fc30004
# Time: 850, PC: 80020070, RS: 3, RT: 2, IR: 00621021
# Time: 860, PC: 80020074, RS: 30, RT: 2, IR: afc20004
# Time: 870, PC: 80020078, RS: 30, RT: 2, IR: 8fc20000
# Time: 880, PC: 8002007c, RS: 2, RT: 2, IR: 24420001
# Time: 890, PC: 80020080, RS: 30, RT: 2, IR: afc20000
# Time: 900, PC: 80020084, RS: 30, RT: 2, IR: 8fc20000
# Time: 910, PC: 80020088, RS: 2, RT: 2, IR: 2842000a
# Time: 920, PC: 8002008c, RS: 2, RT: 0, IR: 1440fff3
# Time: 930, PC: 80020090, RS: 0, RT: 0, IR: 00000000
# Time: 940, PC: 80020094, RS: 30, RT: 2, IR: 8fc20004
# Time: 950, PC: 80020098, RS: 30, RT: 0, IR: 03c0e821
# Time: 960, PC: 8002009c, RS: 29, RT: 30, IR: 8fbe0034
# Time: 970, PC: 800200a0, RS: 29, RT: 29, IR: 27bd0038
# Time: 980, PC: 800200a4, RS: 31, RT: 0, IR: 03e00008
# Time: 990, PC: 800200a8, RS: 0, RT: 0, IR: 00000000
# ** Note: $finish : reg_file_tb.v(106)
# Time: 1 us Iteration: 0 Instance: /reg_file_tb
```

2 Register File Source Code

Listing 5: Register File

```
//
// reg_file.v
//
// Register File
//
//
// Register outputs are the values stored in the regs
// Register inputs are pointers for the specific reg to use
//
```

```
module reg_file (
    clock,
    rsOut,
    rtOut,
    rsIn,
    rtIn,
    rdIn,
    regWriteEnable,
    writeBackData
);

    parameter REG_WIDTH = 32;
    parameter NUM_REGS = 32;

    input wire clock;
    input wire[4:0] rdIn;
    input wire[0:31] writeBackData;

    output reg[0:31] rsOut;
    output reg[0:31] rtOut;

    input wire[4:0] rsIn;
    input wire[4:0] rtIn;
    input wire regWriteEnable;

    reg[0:REG_WIDTH-1] registers[0:NUM_REGS-1];

    integer i;

    // Zero out all of the registers.
    initial
    begin
        for (i = 0; i < NUM_REGS; i = i + 1) begin
            registers[i] = i;
        end // for ()
    end // initial

    always @(posedge clock)
    begin
        fork
            rsOut <= registers[rsIn];
            rtOut <= registers[rtIn];
            //$display("time: %d Rs %d, RT: %d", $time, registers[rsIn], registers[rtIn]);
        join
        registers[rdIn] = writeBackData;
    end // always @(posedge clock)

endmodule
```

Listing 6: Register File Unit Test Bench

```
//
// reg_file_tb.v
//
// Register File Unit Test Bench
//

module reg_file_unit_tb();

reg clock;

reg[0:31] inst;
reg[0:31] data;
reg[0:31] pc;
reg[0:31] writeBackData;
reg[0:4] rdIn;

wire[0:31] rsOut;
wire[0:31] rtOut;
wire[0:31] pcOut;
wire[0:31] irOut;


reg_file U0(
    .clock (clock),
    .rsOut (rsOut),
    .rtOut (rtOut),
    .rdIn (rdIn),
    .writeBackData (writeBackData),
    .pcIn (pc),
    .pcOut (pcOut),
    .irIn (inst),
    .irOut (irOut)
);

initial begin
    clock = 1;
    inst = 0;
    data = 0;
    pc = 0;
    writeBackData = 0;
end

initial begin
    $display("\t\ttime,\tclock,\tpcIn,\tpcOut,\tirIn,\tirOut,\trsOut,\trtOut,\twriteBackData")
        ;
    $monitor("%d,\t%b,\t%h,\t%h,\t%h,\t%h,\t%h,\t%h,\t%h",
            $time, clock, pc, pcOut, inst, irOut, rsOut, rtOut, writeBackData);
end


always begin
```

```
    #5 clock = !clock;
end

initial
begin
    pc = 32'hdead_beef;
    inst = 32'h0000_0000;
    rdIn = 5'b0_0000; // $r0
    writeBackData = 32'hdeed_deed;
    @ (posedge clock);
    pc = 32'hffff_eeee;
    inst = 32'h0000_0000;
    rdIn = 5'b0_0001; // $r1
    writeBackData = 32'hbeaf_dead;
    @ (posedge clock);
    inst = 32'b000000_00000_00001_00010_00000_100000;
    rdIn = 5'b0_0100; // $r4
    writeBackData = 32'hbeef_deed;
    @ (posedge clock);
end

initial
    #100 $finish;

endmodule
```

Listing 7: Register File Test Bench

```
//
// fetch_tb.v
//
// Fetch test bench
//

module reg_file_tb;
    reg clock;

    wire[0:31] address;
    wire wren;
    wire[0:31] data_in;
    wire[0:31] data_out;

    wire[0:31] fetch_address;
    wire fetch_wren;
    wire[0:31] fetch_data_in;
    wire[0:31] fetch_data_out;

    wire[0:31] fetch_insn_decode;
    wire[0:31] fetch_pc;
    reg fetch_stall;

    wire[0:31] decode_rs_data;
```

```
wire[0:31] decode_rt_data;
wire[4:0] decode_rd_in;
wire[0:31] decode_pc_out;
wire[0:31] decode_ir_out;
wire[0:31] decode_write_back_data;
wire decode_reg_write_enable;
wire[0:`CONTROL_REG_SIZE-1] decode_control;

wire[0:31] srec_address;
wire srec_wren;
wire[0:31] srec_data_in;
wire[0:31] srec_data_out;

wire srec_done;

reg[0:31] tb_address;
reg tb_wren;
reg[0:31] tb_data_in;
wire[0:31] tb_data_out;

wire[0:31] bytes_read;
integer byte_count;
integer read_word;
reg[0:31] fetch_word;
reg instruction_valid;

mem_controller mcu(
    .clock (clock),
    .address (address),
    .wren (wren),
    .data_in (data_in),
    .data_out (data_out)
);

fetch DUT(
    .clock (clock),
    .address (fetch_address),
    .insn (fetch_data_in),
    .insn_decode (fetch_data_out),
    .pc (fetch_pc),
    .wren (fetch_wren),
    .stall (fetch_stall)
);

srec_parser #("srec_files/SimpleIf.srec") U0(
    .clock (clock),
    .mem_address (srec_address),
    .mem_wren (srec_wren),
    .mem_data_in (srec_data_in),
    .mem_data_out (srec_data_out),
    .done (srec_done),
```

```
    .bytes_read(bytes_read)
);

decode U1(
    .clock (clock),
    .insn (fetch_data_out),
        .insn_valid (instruction_valid),
    .pc (fetch_address),
    .rsData (decode_rs_data),
    .rtData (decode_rt_data),
    .rdIn (decode_rd_in),
    .pcOut (decode_pc_out),
    .irOut (decode_ir_out),
    .writeBackData (decode_write_back_data),
    .regWriteEnable (decode_reg_write_enable),
    .control (decode_control)
);

assign address = srec_done ? (fetch_stall ? tb_address : fetch_address) : srec_address;
assign wren = srec_done ? (fetch_stall ? tb_wren : fetch_wren) : srec_wren;
assign tb_data_out = data_out;
assign fetch_data_in = data_out;
assign data_in = srec_done ? (fetch_stall ? tb_data_in : fetch_data_in) : srec_data_in;

// Specify when to stop the simulation
event terminate_sim;
initial begin
    @ (terminate_sim);
    #10 $finish;
end

initial begin
    clock = 1;
    fetch_stall = 1;
    instruction_valid = 1'b0;
end

always begin
    #5 clock = !clock;
end

initial begin
    $dumpfile("reg_file_tb.vcd");
    $dumpvars;
end

initial begin
    @(posedge srec_done);
    @(posedge clock);
    byte_count = bytes_read+4;
    tb_address = 32'h8002_0000;
```

```
        tb_wren = 1'b0;
        instruction_valid = 1'b0;
        fetch_stall = 0;
        while (byte_count > 0) begin
            @(posedge clock);
            if ((fetch_address - 4) < 32'h8002_0000) begin
                instruction_valid = 1'b0;
            end else begin
                instruction_valid = 1'b1;
            end
                read_word = tb_data_out;
            fetch_word = fetch_data_out;

            $display("Time: %d, PC: %X, RS:%d, RT:%d, IR: %X", $time,
                   decode_pc_out, decode_rs_data, decode_rt_data, decode_ir_out);
            tb_address = tb_address + 4;
            byte_count = byte_count - 4;
        end

        // The decode runs one clock cycle behind the fetch
        @(posedge clock);
        $display("Time: %d, PC: %X, RS:%d, RT:%d, IR: %X", $time,
                 decode_pc_out, decode_rs_data, decode_rt_data, decode_ir_out);
        tb_address = tb_address + 4;

        instruction_valid = 1'b0;

        ->terminate_sim;
    end

endmodule
```