University Of Waterloo

ECE 429

Task 3
Register File and Execute Stage

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1 Register File Output

Listing 1: Bubble Sort Register File Output

```
# Initializing memory
# Initializing Fetch module
# opened file srec_files/BubbleSort.srec
#
# read in file
#
# Time: 1350, PC: 80020000, RS: 29, RT: 29, IR: 27bdffc8
# Time: 1360, PC: 80020004, RS: 29, RT: 31, IR: afbf0034
# Time: 1370, PC: 80020008, RS: 29, RT: 30, IR: afbe0030
# Time: 1380, PC: 8002000c, RS: 29, RT: 0, IR: 03a0f021
# Time: 1390, PC: 80020010, RS: 0, RT: 2, IR: 2402000c
# Time: 1400, PC: 80020014, RS: 30, RT: 2, IR: afc20010
# Time: 1410, PC: 80020018, RS: 0, RT: 2, IR: 24020009
# Time: 1420, PC: 8002001c, RS: 30, RT: 2, IR: afc20014
# Time: 1430, PC: 80020020, RS: 0, RT: 2, IR: 24020004
# Time: 1440, PC: 80020024, RS: 30, RT: 2, IR: afc20018
# Time: 1450, PC: 80020028, RS: 0, RT: 2, IR: 24020063
# Time: 1460, PC: 8002002c, RS: 30, RT: 2, IR: afc2001c
# Time: 1470, PC: 80020030, RS: 0, RT: 2, IR: 24020078
# Time: 1480, PC: 80020034, RS: 30, RT: 2, IR: afc20020
# Time: 1490, PC: 80020038, RS: 0, RT: 2, IR: 24020001
# Time: 1500, PC: 8002003c, RS: 30, RT: 2, IR: afc20024
# Time: 1510, PC: 80020040, RS: 0, RT: 2, IR: 24020003
# Time: 1520, PC: 80020044, RS: 30, RT: 2, IR: afc20028
# Time: 1530, PC: 80020048, RS: 0, RT: 2, IR: 2402000a
# Time: 1540, PC: 8002004c, RS: 30, RT: 2, IR: afc2002c
# Time: 1550, PC: 80020050, RS: 30, RT: 2, IR: 27c20010
# Time: 1560, PC: 80020054, RS: 2, RT: 0, IR: 00402021
# Time: 1570, PC: 80020058, RS: 0, RT: 5, IR: 24050008
# Time: 1580, PC: 8002005c, RS: 0, RT: 0, IR: 0c008020
# Time: 1590, PC: 80020060, RS: 0, RT: 0, IR: 00000000
# Time: 1600, PC: 80020064, RS: 0, RT: 0, IR: 00001021
# Time: 1610, PC: 80020068, RS: 30, RT: 0, IR: 03c0e821
# Time: 1620, PC: 8002006c, RS: 29, RT: 31, IR: 8fbf0034
# Time: 1630, PC: 80020070, RS: 29, RT: 30, IR: 8fbe0030
# Time: 1640, PC: 80020074, RS: 29, RT: 29, IR: 27bd0038
# Time: 1650, PC: 80020078, RS: 31, RT: 0, IR: 03e00008
# Time: 1660, PC: 8002007c, RS: 0, RT: 0, IR: 00000000
# Time: 1670, PC: 80020080, RS: 29, RT: 29, IR: 27bdffe8
# Time: 1680, PC: 80020084, RS: 29, RT: 30, IR: afbe0014
# Time: 1690, PC: 80020088, RS: 29, RT: 0, IR: 03a0f021
# Time: 1700, PC: 8002008c, RS: 30, RT: 4, IR: afc40018
# Time: 1710, PC: 80020090, RS: 30, RT: 5, IR: afc5001c
# Time: 1720, PC: 80020094, RS: 30, RT: 0, IR: afc00000
# Time: 1730, PC: 80020098, RS: 0, RT: 0, IR: 0800805f
# Time: 1740, PC: 8002009c, RS: 0, RT: 0, IR: 00000000
# Time: 1750, PC: 800200a0, RS: 0, RT: 2, IR: 24020001
# Time: 1760, PC: 800200a4, RS: 30, RT: 2, IR: afc20004
```

```
# Time: 1770, PC: 800200a8, RS: 0, RT: 0, IR: 08008055
# Time: 1780, PC: 800200ac, RS: 0, RT: 0, IR: 00000000
# Time: 1790, PC: 800200b0, RS: 30, RT: 2, IR: 8fc20004
# Time: 1800, PC: 800200b4, RS: 2, RT: 2, IR: 2442ffff
# Time: 1810, PC: 800200b8, RS: 0, RT: 2, IR: 00021080
# Time: 1820, PC: 800200bc, RS: 30, RT: 3, IR: 8fc30018
# Time: 1830, PC: 800200c0, RS: 3, RT: 2, IR: 00621021
# Time: 1840, PC: 800200c4, RS: 2, RT: 3, IR: 8c430000
# Time: 1850, PC: 800200c8, RS: 30, RT: 2, IR: 8fc20004
# Time: 1860, PC: 800200cc, RS: 0, RT: 2, IR: 00021080
# Time: 1870, PC: 800200d0, RS: 30, RT: 4, IR: 8fc40018
# Time: 1880, PC: 800200d4, RS: 4, RT: 2, IR: 00821021
# Time: 1890, PC: 800200d8, RS: 2, RT: 2, IR: 8c420000
# Time: 1900, PC: 800200dc, RS: 2, RT: 3, IR: 0043102a
# Time: 1910, PC: 800200e0, RS: 2, RT: 0, IR: 10400019
# Time: 1920, PC: 800200e4, RS: 0, RT: 0, IR: 00000000
# Time: 1930, PC: 800200e8, RS: 30, RT: 2, IR: 8fc20004
# Time: 1940, PC: 800200ec, RS: 2, RT: 2, IR: 2442ffff
# Time: 1950, PC: 800200f0, RS: 0, RT: 2, IR: 00021080
# Time: 1960, PC: 800200f4, RS: 30, RT: 3, IR: 8fc30018
# Time: 1970, PC: 800200f8, RS: 3, RT: 2, IR: 00621021
# Time: 1980, PC: 800200fc, RS: 2, RT: 2, IR: 8c420000
# Time: 1990, PC: 80020100, RS: 30, RT: 2, IR: afc20008
# Time: 2000, PC: 80020104, RS: 30, RT: 2, IR: 8fc20004
# Time: 2010, PC: 80020108, RS: 2, RT: 2, IR: 2442ffff
# Time: 2020, PC: 8002010c, RS: 0, RT: 2, IR: 00021080
# Time: 2030, PC: 80020110, RS: 30, RT: 3, IR: 8fc30018
# Time: 2040, PC: 80020114, RS: 3, RT: 2, IR: 00621021
# Time: 2050, PC: 80020118, RS: 30, RT: 3, IR: 8fc30004
# Time: 2060, PC: 8002011c, RS: 0, RT: 3, IR: 00031880
# Time: 2070, PC: 80020120, RS: 30, RT: 4, IR: 8fc40018
# Time: 2080, PC: 80020124, RS: 4, RT: 3, IR: 00831821
# Time: 2090, PC: 80020128, RS: 3, RT: 3, IR: 8c630000
# Time: 2100, PC: 8002012c, RS: 2, RT: 3, IR: ac430000
# Time: 2110, PC: 80020130, RS: 30, RT: 2, IR: 8fc20004
# Time: 2120, PC: 80020134, RS: 0, RT: 2, IR: 00021080
# Time: 2130, PC: 80020138, RS: 30, RT: 3, IR: 8fc30018
# Time: 2140, PC: 8002013c, RS: 3, RT: 2, IR: 00621021
# Time: 2150, PC: 80020140, RS: 30, RT: 3, IR: 8fc30008
# Time: 2160, PC: 80020144, RS: 2, RT: 3, IR: ac430000
# Time: 2170, PC: 80020148, RS: 30, RT: 2, IR: 8fc20004
# Time: 2180, PC: 8002014c, RS: 2, RT: 2, IR: 24420001
# Time: 2190, PC: 80020150, RS: 30, RT: 2, IR: afc20004
# Time: 2200, PC: 80020154, RS: 30, RT: 3, IR: 8fc3001c
# Time: 2210, PC: 80020158, RS: 30, RT: 2, IR: 8fc20000
# Time: 2220, PC: 8002015c, RS: 3, RT: 2, IR: 00621823
# Time: 2230, PC: 80020160, RS: 30, RT: 2, IR: 8fc20004
# Time: 2240, PC: 80020164, RS: 2, RT: 3, IR: 0043102a
# Time: 2250, PC: 80020168, RS: 2, RT: 0, IR: 1440ffd1
# Time: 2260, PC: 8002016c, RS: 0, RT: 0, IR: 00000000
# Time: 2270, PC: 80020170, RS: 30, RT: 2, IR: 8fc20000
```

```
# Time: 2280, PC: 80020174, RS: 2, RT: 2, IR: 24420001
# Time: 2290, PC: 80020178, RS: 30, RT: 2, IR: afc20000
# Time: 2300, PC: 8002017c, RS: 30, RT: 3, IR: 8fc30000
# Time: 2310, PC: 80020180, RS: 30, RT: 2, IR: 8fc2001c
# Time: 2320, PC: 80020184, RS: 3, RT: 2, IR: 0062102a
# Time: 2330, PC: 80020188, RS: 2, RT: 0, IR: 1440ffc5
# Time: 2340, PC: 8002018c, RS: 0, RT: 0, IR: 00000000
# Time: 2350, PC: 80020190, RS: 30, RT: 0, IR: 03c0e821
# Time: 2360, PC: 80020194, RS: 29, RT: 30, IR: 8fbe0014
# Time: 2370, PC: 80020198, RS: 29, RT: 29, IR: 27bd0018
# Time: 2380, PC: 8002019c, RS: 31, RT: 0, IR: 03e00008
# Time: 2390, PC: 800201a0, RS: 0, RT: 0, IR: 00000000
# ** Note: $finish : reg_file_tb.v(106)
# Time: 2400 ns Iteration: 0 Instance: /reg_file_tb
```

Listing 2: Simple Add Register File Output

```
# Initializing memory
# Initializing Fetch module
# opened file srec_files/SimpleAdd.srec
#
# read in file
#
# Time: 260, PC: 80020000, RS: 29, RT: 29, IR: 27bdffe8
# Time: 270, PC: 80020004, RS: 29, RT: 30, IR: afbe0014
# Time: 280, PC: 80020008, RS: 29, RT: 0, IR: 03a0f021
# Time: 290, PC: 8002000c, RS: 0, RT: 2, IR: 24020003
# Time: 300, PC: 80020010, RS: 30, RT: 2, IR: afc20000
# Time: 310, PC: 80020014, RS: 0, RT: 2, IR: 24020002
# Time: 320, PC: 80020018, RS: 30, RT: 2, IR: afc20004
# Time: 330, PC: 8002001c, RS: 30, RT: 0, IR: afc00008
# Time: 340, PC: 80020020, RS: 30, RT: 3, IR: 8fc30000
# Time: 350, PC: 80020024, RS: 30, RT: 2, IR: 8fc20004
# Time: 360, PC: 80020028, RS: 3, RT: 2, IR: 00621021
# Time: 370, PC: 8002002c, RS: 30, RT: 2, IR: afc20008
# Time: 380, PC: 80020030, RS: 30, RT: 2, IR: 8fc20008
# Time: 390, PC: 80020034, RS: 30, RT: 0, IR: 03c0e821
# Time: 400, PC: 80020038, RS: 29, RT: 30, IR: 8fbe0014
# Time: 410, PC: 8002003c, RS: 29, RT: 29, IR: 27bd0018
# Time: 420, PC: 80020040, RS: 31, RT: 0, IR: 03e00008
# Time: 430, PC: 80020044, RS: 0, RT: 0, IR: 00000000
# ** Note: $finish : reg_file_tb.v(106)
# Time: 440 ns Iteration: 0 Instance: /reg_file_tb
```

Listing 3: Simple If Register File Output

```
# Initializing memory
# Initializing Fetch module
# opened file srec_files/SimpleIf.srec
#
# read in file
#
```

```
# Time: 430, PC: 80020000, RS: 29, RT: 29, IR: 27bdffe8
# Time: 440, PC: 80020004, RS: 29, RT: 30, IR: afbe0014
# Time: 450, PC: 80020008, RS: 29, RT: 0, IR: 03a0f021
# Time: 460, PC: 8002000c, RS: 0, RT: 2, IR: 24020003
# Time: 470, PC: 80020010, RS: 30, RT: 2, IR: afc20000
# Time: 480, PC: 80020014, RS: 0, RT: 2, IR: 24020002
# Time: 490, PC: 80020018, RS: 30, RT: 2, IR: afc20004
# Time: 500, PC: 8002001c, RS: 30, RT: 0, IR: afc00008
# Time: 510, PC: 80020020, RS: 30, RT: 2, IR: 8fc20000
# Time: 520, PC: 80020024, RS: 2, RT: 2, IR: 28420005
# Time: 530, PC: 80020028, RS: 2, RT: 0, IR: 10400007
# Time: 540, PC: 8002002c, RS: 0, RT: 0, IR: 00000000
# Time: 550, PC: 80020030, RS: 30, RT: 3, IR: 8fc30000
# Time: 560, PC: 80020034, RS: 30, RT: 2, IR: 8fc20004
# Time: 570, PC: 80020038, RS: 3, RT: 2, IR: 00621021
# Time: 580, PC: 8002003c, RS: 30, RT: 2, IR: afc20000
# Time: 590, PC: 80020040, RS: 0, RT: 0, IR: 08008016
# Time: 600, PC: 80020044, RS: 0, RT: 0, IR: 00000000
# Time: 610, PC: 80020048, RS: 30, RT: 3, IR: 8fc30000
# Time: 620, PC: 8002004c, RS: 30, RT: 2, IR: 8fc20004
# Time: 630, PC: 80020050, RS: 3, RT: 2, IR: 00621023
# Time: 640, PC: 80020054, RS: 30, RT: 2, IR: afc20000
# Time: 650, PC: 80020058, RS: 30, RT: 3, IR: 8fc30000
# Time: 660, PC: 8002005c, RS: 30, RT: 2, IR: 8fc20004
# Time: 670, PC: 80020060, RS: 3, RT: 2, IR: 00621021
# Time: 680, PC: 80020064, RS: 30, RT: 2, IR: afc20008
# Time: 690, PC: 80020068, RS: 30, RT: 2, IR: 8fc20008
# Time: 700, PC: 8002006c, RS: 30, RT: 0, IR: 03c0e821
# Time: 710, PC: 80020070, RS: 29, RT: 30, IR: 8fbe0014
# Time: 720, PC: 80020074, RS: 29, RT: 29, IR: 27bd0018
# Time: 730, PC: 80020078, RS: 31, RT: 0, IR: 03e00008
# Time: 740, PC: 8002007c, RS: 0, RT: 0, IR: 00000000
# ** Note: $finish : reg_file_tb.v(106)
# Time: 750 ns Iteration: 0 Instance: /reg_file_tb
```

Listing 4: Sum Array Register File Output

```
# Initializing memory
# Initializing Fetch module
# opened file srec_files/SumArray.srec
#
# read in file
#
# Time: 570, PC: 80020000, RS: 29, RT: 29, IR: 27bdffc8
# Time: 580, PC: 80020004, RS: 29, RT: 30, IR: afbe0034
# Time: 590, PC: 80020008, RS: 29, RT: 0, IR: 03a0f021
# Time: 600, PC: 8002000c, RS: 30, RT: 0, IR: afc00000
# Time: 610, PC: 80020010, RS: 30, RT: 0, IR: afc00004
# Time: 620, PC: 80020014, RS: 30, RT: 0, IR: afc00000
# Time: 630, PC: 80020018, RS: 0, RT: 0, IR: 08008010
# Time: 640, PC: 8002001c, RS: 0, RT: 0, IR: 00000000
# Time: 650, PC: 80020020, RS: 30, RT: 2, IR: 8fc20000
```

```
# Time: 660, PC: 80020024, RS: 0, RT: 2, IR: 00021080
# Time: 670, PC: 80020028, RS: 30, RT: 2, IR: 03c21021
# Time: 680, PC: 8002002c, RS: 30, RT: 3, IR: 8fc30000
# Time: 690, PC: 80020030, RS: 2, RT: 3, IR: ac430008
# Time: 700, PC: 80020034, RS: 30, RT: 2, IR: 8fc20000
# Time: 710, PC: 80020038, RS: 2, RT: 2, IR: 24420001
# Time: 720, PC: 8002003c, RS: 30, RT: 2, IR: afc20000
# Time: 730, PC: 80020040, RS: 30, RT: 2, IR: 8fc20000
# Time: 740, PC: 80020044, RS: 2, RT: 2, IR: 2842000a
# Time: 750, PC: 80020048, RS: 2, RT: 0, IR: 1440fff5
# Time: 760, PC: 8002004c, RS: 0, RT: 0, IR: 00000000
# Time: 770, PC: 80020050, RS: 30, RT: 0, IR: afc00000
# Time: 780, PC: 80020054, RS: 0, RT: 0, IR: 08008021
# Time: 790, PC: 80020058, RS: 0, RT: 0, IR: 00000000
# Time: 800, PC: 8002005c, RS: 30, RT: 2, IR: 8fc20000
# Time: 810, PC: 80020060, RS: 0, RT: 2, IR: 00021080
# Time: 820, PC: 80020064, RS: 30, RT: 2, IR: 03c21021
# Time: 830, PC: 80020068, RS: 2, RT: 2, IR: 8c420008
# Time: 840, PC: 8002006c, RS: 30, RT: 3, IR: 8fc30004
# Time: 850, PC: 80020070, RS: 3, RT: 2, IR: 00621021
# Time: 860, PC: 80020074, RS: 30, RT: 2, IR: afc20004
# Time: 870, PC: 80020078, RS: 30, RT: 2, IR: 8fc20000
# Time: 880, PC: 8002007c, RS: 2, RT: 2, IR: 24420001
# Time: 890, PC: 80020080, RS: 30, RT: 2, IR: afc20000
# Time: 900, PC: 80020084, RS: 30, RT: 2, IR: 8fc20000
# Time: 910, PC: 80020088, RS: 2, RT: 2, IR: 2842000a
# Time: 920, PC: 8002008c, RS: 2, RT: 0, IR: 1440fff3
# Time: 930, PC: 80020090, RS: 0, RT: 0, IR: 00000000
# Time: 940, PC: 80020094, RS: 30, RT: 2, IR: 8fc20004
# Time: 950, PC: 80020098, RS: 30, RT: 0, IR: 03c0e821
# Time: 960, PC: 8002009c, RS: 29, RT: 30, IR: 8fbe0034
# Time: 970, PC: 800200a0, RS: 29, RT: 29, IR: 27bd0038
# Time: 980, PC: 800200a4, RS: 31, RT: 0, IR: 03e00008
# Time: 990, PC: 800200a8, RS: 0, RT: 0, IR: 00000000
# ** Note: $finish : reg_file_tb.v(106)
# Time: 1 us Iteration: 0 Instance: /reg_file_tb
```

2 Register File Source Code

Listing 5: Register File

```
//
// reg_file.v
//
// Register File
//
//
// Register outputs are the values stored in the regs
// Register inputs are pointers for the specific reg to use
//
```

```
module reg_file (
    clock,
    rsOut,
    rtOut,
    rsIn,
    rtIn,
    rdIn,
    regWriteEnable,
    writeBackData
);

    parameter REG_WIDTH = 32;
    parameter NUM_REGS = 32;

    input wire clock;
    input wire[4:0] rdIn;
    input wire[0:31] writeBackData;

    output reg[0:31] rsOut;
    output reg[0:31] rtOut;

    input wire[4:0] rsIn;
    input wire[4:0] rtIn;
    input wire regWriteEnable;

    reg[0:REG_WIDTH-1] registers[0:NUM_REGS-1];

    integer i;

    // Zero out all of the registers.
    initial
    begin
        for (i = 0; i  NUM_REGS; i = i + 1) begin
            registers[i] = i;
        end // for ()
    end // initial

    always @(posedge clock)
    begin
        fork
            rsOut = registers[rsIn];
            rtOut = registers[rtIn];
            //$display("time: %d Rs %d, RT: %d", $time, registers[rsIn], registers[rtIn]);
        join
        registers[rdIn] = writeBackData;
    end // always @(posedge clock)

endmodule
```

Listing 6: Register File Unit Test Bench

```
//
// reg_file_tb.v
//
// Register File Unit Test Bench
//

module reg_file_unit_tb();

reg clock;

reg[0:31] inst;
reg[0:31] data;
reg[0:31] pc;
reg[0:31] writeBackData;
reg[0:4] rdIn;

wire[0:31] rsOut;
wire[0:31] rtOut;
wire[0:31] pcOut;
wire[0:31] irOut;


reg_file U0(
    .clock (clock),
    .rsOut (rsOut),
    .rtOut (rtOut),
    .rdIn (rdIn),
    .writeBackData (writeBackData),
    .pcIn (pc),
    .pcOut (pcOut),
    .irIn (inst),
    .irOut (irOut)
);

initial begin
    clock = 1;
    inst = 0;
    data = 0;
    pc = 0;
    writeBackData = 0;
end

initial begin
    $display("\t\ttime,\tclock,\tpcIn,\tpcOut,\tirIn,\tirOut,\trsOut,\trtOut,\twriteBackData")
        ;
    $monitor("%d,\t%b,\t%h,\t%h,\t%h,\t%h,\t%h,\t%h,\t%h",
            $time, clock, pc, pcOut, inst, irOut, rsOut, rtOut, writeBackData);
end


always begin
```

```
    #5 clock = !clock;
end

initial
begin
    pc = 32'hdead_beef;
    inst = 32'h0000_0000;
    rdIn = 5'b0_0000; // $r0
    writeBackData = 32'hdeed_deed;
    @ (posedge clock);
    pc = 32'hffff_eeee;
    inst = 32'h0000_0000;
    rdIn = 5'b0_0001; // $r1
    writeBackData = 32'hbeaf_dead;
    @ (posedge clock);
    inst = 32'b000000_00000_00001_00010_00000_100000;
    rdIn = 5'b0_0100; // $r4
    writeBackData = 32'hbeef_deed;
    @ (posedge clock);
end

initial
    #100 $finish;

endmodule
```

Listing 7: Register File Test Bench

```
//
// fetch_tb.v
//
// Fetch test bench
//

module reg_file_tb;
    reg clock;

    wire[0:31] address;
    wire wren;
    wire[0:31] data_in;
    wire[0:31] data_out;

    wire[0:31] fetch_address;
    wire fetch_wren;
    wire[0:31] fetch_data_in;
    wire[0:31] fetch_data_out;

    wire[0:31] fetch_insn_decode;
    wire[0:31] fetch_pc;
    reg fetch_stall;

    wire[0:31] decode_rs_data;
```

```
wire[0:31] decode_rt_data;
wire[4:0] decode_rd_in;
wire[0:31] decode_pc_out;
wire[0:31] decode_ir_out;
wire[0:31] decode_write_back_data;
wire decode_reg_write_enable;
wire[0:`CONTROL_REG_SIZE-1] decode_control;

wire[0:31] srec_address;
wire srec_wren;
wire[0:31] srec_data_in;
wire[0:31] srec_data_out;

wire srec_done;

reg[0:31] tb_address;
reg tb_wren;
reg[0:31] tb_data_in;
wire[0:31] tb_data_out;

wire[0:31] bytes_read;
integer byte_count;
integer read_word;
reg[0:31] fetch_word;
reg instruction_valid;

mem_controller mcu(
    .clock (clock),
    .address (address),
    .wren (wren),
    .data_in (data_in),
    .data_out (data_out)
);

fetch DUT(
    .clock (clock),
    .address (fetch_address),
    .insn (fetch_data_in),
    .insn_decode (fetch_data_out),
    .pc (fetch_pc),
    .wren (fetch_wren),
    .stall (fetch_stall)
);

srec_parser #("srec_files/SimpleIf.srec") U0(
    .clock (clock),
    .mem_address (srec_address),
    .mem_wren (srec_wren),
    .mem_data_in (srec_data_in),
    .mem_data_out (srec_data_out),
    .done (srec_done),
```

```
    .bytes_read(bytes_read)
);

decode U1(
    .clock (clock),
    .insn (fetch_data_out),
        .insn_valid (instruction_valid),
    .pc (fetch_address),
    .rsData (decode_rs_data),
    .rtData (decode_rt_data),
    .rdIn (decode_rd_in),
    .pcOut (decode_pc_out),
    .irOut (decode_ir_out),
    .writeBackData (decode_write_back_data),
    .regWriteEnable (decode_reg_write_enable),
    .control (decode_control)
);

assign address = srec_done ? (fetch_stall ? tb_address : fetch_address) : srec_address;
assign wren = srec_done ? (fetch_stall ? tb_wren : fetch_wren) : srec_wren;
assign tb_data_out = data_out;
assign fetch_data_in = data_out;
assign data_in = srec_done ? (fetch_stall ? tb_data_in : fetch_data_in) : srec_data_in;

// Specify when to stop the simulation
event terminate_sim;
initial begin
    @ (terminate_sim);
    #10 $finish;
end

initial begin
    clock = 1;
    fetch_stall = 1;
    instruction_valid = 1'b0;
end

always begin
    #5 clock = !clock;
end

initial begin
    $dumpfile("reg_file_tb.vcd");
    $dumpvars;
end

initial begin
    @(posedge srec_done);
    @(posedge clock);
    byte_count = bytes_read+4;
    tb_address = 32'h8002_0000;
```

```
        tb_wren = 1'b0;
        instruction_valid = 1'b0;
        fetch_stall = 0;
        while (byte_count  0) begin
            @(posedge clock);
            if ((fetch_address - 4)  32'h8002_0000) begin
                instruction_valid = 1'b0;
            end else begin
                instruction_valid = 1'b1;
            end
                read_word = tb_data_out;
            fetch_word = fetch_data_out;

            $display("Time: %d, PC: %X, RS:%d, RT:%d, IR: %X", $time,
                   decode_pc_out, decode_rs_data, decode_rt_data, decode_ir_out);
            tb_address = tb_address + 4;
            byte_count = byte_count - 4;
        end

        // The decode runs one clock cycle behind the fetch
        @(posedge clock);
        $display("Time: %d, PC: %X, RS:%d, RT:%d, IR: %X", $time,
                 decode_pc_out, decode_rs_data, decode_rt_data, decode_ir_out);
        tb_address = tb_address + 4;

        instruction_valid = 1'b0;

        -terminate_sim;
    end

endmodule
```

3 ALU Output

Listing 8: Bubble Sort Register File Output - ALU

```
# Initializing memory
# Initializing Fetch module
# opened file srec_files/BubbleSort.srec
#
# read in file
#
# Time: 1360, Input insn: 27bdffc8, Input PC: 80020000, Input RS: 29, Input RT: 29,
    ALU_RESULT: 65509
# Time: 1370, Input insn: afbf0034, Input PC: 80020004, Input RS: 29, Input RT: 31,
    ALU_RESULT: 65509
# Time: 1380, Input insn: afbe0030, Input PC: 80020008, Input RS: 29, Input RT: 30,
    ALU_RESULT: 65509
# Time: 1390, Input insn: 03a0f021, Input PC: 8002000c, Input RS: 29, Input RT: 0, ALU_RESULT
    : 29
```

```
# Time: 1400, Input insn: 2402000c, Input PC: 80020010, Input RS: 0, Input RT: 2, ALU_RESULT:
     12
# Time: 1410, Input insn: afc20010, Input PC: 80020014, Input RS: 30, Input RT: 2, ALU_RESULT
    : 12
# Time: 1420, Input insn: 24020009, Input PC: 80020018, Input RS: 0, Input RT: 2, ALU_RESULT:
     9
# Time: 1430, Input insn: afc20014, Input PC: 8002001c, Input RS: 30, Input RT: 2, ALU_RESULT
    : 9
# Time: 1440, Input insn: 24020004, Input PC: 80020020, Input RS: 0, Input RT: 2, ALU_RESULT:
     4
# Time: 1450, Input insn: afc20018, Input PC: 80020024, Input RS: 30, Input RT: 2, ALU_RESULT
    : 4
# Time: 1460, Input insn: 24020063, Input PC: 80020028, Input RS: 0, Input RT: 2, ALU_RESULT:
     99
# Time: 1470, Input insn: afc2001c, Input PC: 8002002c, Input RS: 30, Input RT: 2, ALU_RESULT
    : 99
# Time: 1480, Input insn: 24020078, Input PC: 80020030, Input RS: 0, Input RT: 2, ALU_RESULT:
     120
# Time: 1490, Input insn: afc20020, Input PC: 80020034, Input RS: 30, Input RT: 2, ALU_RESULT
    : 120
# Time: 1500, Input insn: 24020001, Input PC: 80020038, Input RS: 0, Input RT: 2, ALU_RESULT:
     1
# Time: 1510, Input insn: afc20024, Input PC: 8002003c, Input RS: 30, Input RT: 2, ALU_RESULT
    : 1
# Time: 1520, Input insn: 24020003, Input PC: 80020040, Input RS: 0, Input RT: 2, ALU_RESULT:
     3
# Time: 1530, Input insn: afc20028, Input PC: 80020044, Input RS: 30, Input RT: 2, ALU_RESULT
    : 3
# Time: 1540, Input insn: 2402000a, Input PC: 80020048, Input RS: 0, Input RT: 2, ALU_RESULT:
     10
# Time: 1550, Input insn: afc2002c, Input PC: 8002004c, Input RS: 30, Input RT: 2, ALU_RESULT
    : 10
# Time: 1560, Input insn: 27c20010, Input PC: 80020050, Input RS: 30, Input RT: 2, ALU_RESULT
    : 46
# Time: 1570, Input insn: 00402021, Input PC: 80020054, Input RS: 2, Input RT: 0, ALU_RESULT:
     2
# Time: 1580, Input insn: 24050008, Input PC: 80020058, Input RS: 0, Input RT: 5, ALU_RESULT:
     8
# Time: 1590, Input insn: 0c008020, Input PC: 8002005c, Input RS: 0, Input RT: 0, ALU_RESULT:
     8
# Time: 1600, Input insn: 00000000, Input PC: 80020060, Input RS: 0, Input RT: 0, ALU_RESULT:
     0
# Time: 1610, Input insn: 00001021, Input PC: 80020064, Input RS: 0, Input RT: 0, ALU_RESULT:
     0
# Time: 1620, Input insn: 03c0e821, Input PC: 80020068, Input RS: 30, Input RT: 0, ALU_RESULT
    : 30
# Time: 1630, Input insn: 8fbf0034, Input PC: 8002006c, Input RS: 29, Input RT: 31,
    ALU_RESULT: 30
# Time: 1640, Input insn: 8fbe0030, Input PC: 80020070, Input RS: 29, Input RT: 30,
    ALU_RESULT: 30
```

```
# Time: 1650, Input insn: 27bd0038, Input PC: 80020074, Input RS: 29, Input RT: 29,
    ALU_RESULT: 85
# Time: 1660, Input insn: 03e00008, Input PC: 80020078, Input RS: 31, Input RT: 0, ALU_RESULT
    : 85
# Time: 1670, Input insn: 00000000, Input PC: 8002007c, Input RS: 0, Input RT: 0, ALU_RESULT:
     0
# Time: 1680, Input insn: 27bdffe8, Input PC: 80020080, Input RS: 29, Input RT: 29,
    ALU_RESULT: 65541
# Time: 1690, Input insn: afbe0014, Input PC: 80020084, Input RS: 29, Input RT: 30,
    ALU_RESULT: 65541
# Time: 1700, Input insn: 03a0f021, Input PC: 80020088, Input RS: 29, Input RT: 0, ALU_RESULT
    : 29
# Time: 1710, Input insn: afc40018, Input PC: 8002008c, Input RS: 30, Input RT: 4, ALU_RESULT
    : 29
# Time: 1720, Input insn: afc5001c, Input PC: 80020090, Input RS: 30, Input RT: 5, ALU_RESULT
    : 29
# Time: 1730, Input insn: afc00000, Input PC: 80020094, Input RS: 30, Input RT: 0, ALU_RESULT
    : 29
# Time: 1740, Input insn: 0800805f, Input PC: 80020098, Input RS: 0, Input RT: 0, ALU_RESULT:
     29
# Time: 1750, Input insn: 00000000, Input PC: 8002009c, Input RS: 0, Input RT: 0, ALU_RESULT:
     0
# Time: 1760, Input insn: 24020001, Input PC: 800200a0, Input RS: 0, Input RT: 2, ALU_RESULT:
     1
# Time: 1770, Input insn: afc20004, Input PC: 800200a4, Input RS: 30, Input RT: 2, ALU_RESULT
    : 1
# Time: 1780, Input insn: 08008055, Input PC: 800200a8, Input RS: 0, Input RT: 0, ALU_RESULT:
     1
# Time: 1790, Input insn: 00000000, Input PC: 800200ac, Input RS: 0, Input RT: 0, ALU_RESULT:
     0
# Time: 1800, Input insn: 8fc20004, Input PC: 800200b0, Input RS: 30, Input RT: 2, ALU_RESULT
    : 0
# Time: 1810, Input insn: 2442ffff, Input PC: 800200b4, Input RS: 2, Input RT: 2, ALU_RESULT:
     65537
# Time: 1820, Input insn: 00021080, Input PC: 800200b8, Input RS: 0, Input RT: 2, ALU_RESULT:
     8
# Time: 1830, Input insn: 8fc30018, Input PC: 800200bc, Input RS: 30, Input RT: 3, ALU_RESULT
    : 8
# Time: 1840, Input insn: 00621021, Input PC: 800200c0, Input RS: 3, Input RT: 2, ALU_RESULT:
     5
# Time: 1850, Input insn: 8c430000, Input PC: 800200c4, Input RS: 2, Input RT: 3, ALU_RESULT:
     5
# Time: 1860, Input insn: 8fc20004, Input PC: 800200c8, Input RS: 30, Input RT: 2, ALU_RESULT
    : 5
# Time: 1870, Input insn: 00021080, Input PC: 800200cc, Input RS: 0, Input RT: 2, ALU_RESULT:
     8
# Time: 1880, Input insn: 8fc40018, Input PC: 800200d0, Input RS: 30, Input RT: 4, ALU_RESULT
    : 8
# Time: 1890, Input insn: 00821021, Input PC: 800200d4, Input RS: 4, Input RT: 2, ALU_RESULT:
     6
```

```
# Time: 1900, Input insn: 8c420000, Input PC: 800200d8, Input RS: 2, Input RT: 2, ALU_RESULT:
     6
# Time: 1910, Input insn: 0043102a, Input PC: 800200dc, Input RS: 2, Input RT: 3, ALU_RESULT:
     1
# Time: 1920, Input insn: 10400019, Input PC: 800200e0, Input RS: 2, Input RT: 0, ALU_RESULT:
     1
# Time: 1930, Input insn: 00000000, Input PC: 800200e4, Input RS: 0, Input RT: 0, ALU_RESULT:
     0
# Time: 1940, Input insn: 8fc20004, Input PC: 800200e8, Input RS: 30, Input RT: 2, ALU_RESULT
    : 0
# Time: 1950, Input insn: 2442ffff, Input PC: 800200ec, Input RS: 2, Input RT: 2, ALU_RESULT:
     65537
# Time: 1960, Input insn: 00021080, Input PC: 800200f0, Input RS: 0, Input RT: 2, ALU_RESULT:
     8
# Time: 1970, Input insn: 8fc30018, Input PC: 800200f4, Input RS: 30, Input RT: 3, ALU_RESULT
    : 8
# Time: 1980, Input insn: 00621021, Input PC: 800200f8, Input RS: 3, Input RT: 2, ALU_RESULT:
     5
# Time: 1990, Input insn: 8c420000, Input PC: 800200fc, Input RS: 2, Input RT: 2, ALU_RESULT:
     5
# Time: 2000, Input insn: afc20008, Input PC: 80020100, Input RS: 30, Input RT: 2, ALU_RESULT
    : 5
# Time: 2010, Input insn: 8fc20004, Input PC: 80020104, Input RS: 30, Input RT: 2, ALU_RESULT
    : 5
# Time: 2020, Input insn: 2442ffff, Input PC: 80020108, Input RS: 2, Input RT: 2, ALU_RESULT:
     65537
# Time: 2030, Input insn: 00021080, Input PC: 8002010c, Input RS: 0, Input RT: 2, ALU_RESULT:
     8
# Time: 2040, Input insn: 8fc30018, Input PC: 80020110, Input RS: 30, Input RT: 3, ALU_RESULT
    : 8
# Time: 2050, Input insn: 00621021, Input PC: 80020114, Input RS: 3, Input RT: 2, ALU_RESULT:
     5
# Time: 2060, Input insn: 8fc30004, Input PC: 80020118, Input RS: 30, Input RT: 3, ALU_RESULT
    : 5
# Time: 2070, Input insn: 00031880, Input PC: 8002011c, Input RS: 0, Input RT: 3, ALU_RESULT:
     0
# Time: 2080, Input insn: 8fc40018, Input PC: 80020120, Input RS: 30, Input RT: 4, ALU_RESULT
    : 0
# Time: 2090, Input insn: 00831821, Input PC: 80020124, Input RS: 4, Input RT: 3, ALU_RESULT:
     7
# Time: 2100, Input insn: 8c630000, Input PC: 80020128, Input RS: 3, Input RT: 3, ALU_RESULT:
     7
# Time: 2110, Input insn: ac430000, Input PC: 8002012c, Input RS: 2, Input RT: 3, ALU_RESULT:
     7
# Time: 2120, Input insn: 8fc20004, Input PC: 80020130, Input RS: 30, Input RT: 2, ALU_RESULT
    : 7
# Time: 2130, Input insn: 00021080, Input PC: 80020134, Input RS: 0, Input RT: 2, ALU_RESULT:
     8
# Time: 2140, Input insn: 8fc30018, Input PC: 80020138, Input RS: 30, Input RT: 3, ALU_RESULT
    : 8
```

```
# Time: 2150, Input insn: 00621021, Input PC: 8002013c, Input RS: 3, Input RT: 2, ALU_RESULT:
     5
# Time: 2160, Input insn: 8fc30008, Input PC: 80020140, Input RS: 30, Input RT: 3, ALU_RESULT
    : 5
# Time: 2170, Input insn: ac430000, Input PC: 80020144, Input RS: 2, Input RT: 3, ALU_RESULT:
     5
# Time: 2180, Input insn: 8fc20004, Input PC: 80020148, Input RS: 30, Input RT: 2, ALU_RESULT
    : 5
# Time: 2190, Input insn: 24420001, Input PC: 8002014c, Input RS: 2, Input RT: 2, ALU_RESULT:
     3
# Time: 2200, Input insn: afc20004, Input PC: 80020150, Input RS: 30, Input RT: 2, ALU_RESULT
    : 3
# Time: 2210, Input insn: 8fc3001c, Input PC: 80020154, Input RS: 30, Input RT: 3, ALU_RESULT
    : 3
# Time: 2220, Input insn: 8fc20000, Input PC: 80020158, Input RS: 30, Input RT: 2, ALU_RESULT
    : 3
# Time: 2230, Input insn: 00621823, Input PC: 8002015c, Input RS: 3, Input RT: 2, ALU_RESULT:
     1
# Time: 2240, Input insn: 8fc20004, Input PC: 80020160, Input RS: 30, Input RT: 2, ALU_RESULT
    : 1
# Time: 2250, Input insn: 0043102a, Input PC: 80020164, Input RS: 2, Input RT: 3, ALU_RESULT:
     1
# Time: 2260, Input insn: 1440ffd1, Input PC: 80020168, Input RS: 2, Input RT: 0, ALU_RESULT:
     2147877036
# Time: 2270, Input insn: 00000000, Input PC: 8002016c, Input RS: 0, Input RT: 0, ALU_RESULT:
     0
# Time: 2280, Input insn: 8fc20000, Input PC: 80020170, Input RS: 30, Input RT: 2, ALU_RESULT
    : 0
# Time: 2290, Input insn: 24420001, Input PC: 80020174, Input RS: 2, Input RT: 2, ALU_RESULT:
     3
# Time: 2300, Input insn: afc20000, Input PC: 80020178, Input RS: 30, Input RT: 2, ALU_RESULT
    : 3
# Time: 2310, Input insn: 8fc30000, Input PC: 8002017c, Input RS: 30, Input RT: 3, ALU_RESULT
    : 3
# Time: 2320, Input insn: 8fc2001c, Input PC: 80020180, Input RS: 30, Input RT: 2, ALU_RESULT
    : 3
# Time: 2330, Input insn: 0062102a, Input PC: 80020184, Input RS: 3, Input RT: 2, ALU_RESULT:
     0
# Time: 2340, Input insn: 1440ffc5, Input PC: 80020188, Input RS: 2, Input RT: 0, ALU_RESULT:
     2147877020
# Time: 2350, Input insn: 00000000, Input PC: 8002018c, Input RS: 0, Input RT: 0, ALU_RESULT:
     0
# Time: 2360, Input insn: 03c0e821, Input PC: 80020190, Input RS: 30, Input RT: 0, ALU_RESULT
    : 30
# Time: 2370, Input insn: 8fbe0014, Input PC: 80020194, Input RS: 29, Input RT: 30,
    ALU_RESULT: 30
# Time: 2380, Input insn: 27bd0018, Input PC: 80020198, Input RS: 29, Input RT: 29,
    ALU_RESULT: 53
# Time: 2400, Input insn: 00000000, Input PC: 800201a0, Input RS: 0, Input RT: 0, ALU_RESULT:
     0
# ** Note: $finish : exec_stage_tb.v(129)
```

```
# Time: 2420 ns Iteration: 0 Instance: /exec_stage_tb
```

Listing 9: Simple Add Register File Output - ALU

```
# Initializing memory
# Initializing Fetch module
# opened file srec_files/SimpleAdd.srec
#
# read in file
#
# Time: 270, Input insn: 27bdffe8, Input PC: 80020000, Input RS: 29, Input RT: 29, ALU_RESULT
    : 65541
# Time: 280, Input insn: afbe0014, Input PC: 80020004, Input RS: 29, Input RT: 30, ALU_RESULT
    : 65541
# Time: 290, Input insn: 03a0f021, Input PC: 80020008, Input RS: 29, Input RT: 0, ALU_RESULT:
     29
# Time: 300, Input insn: 24020003, Input PC: 8002000c, Input RS: 0, Input RT: 2, ALU_RESULT:
    3
# Time: 310, Input insn: afc20000, Input PC: 80020010, Input RS: 30, Input RT: 2, ALU_RESULT:
     3
# Time: 320, Input insn: 24020002, Input PC: 80020014, Input RS: 0, Input RT: 2, ALU_RESULT:
    2
# Time: 330, Input insn: afc20004, Input PC: 80020018, Input RS: 30, Input RT: 2, ALU_RESULT:
     2
# Time: 340, Input insn: afc00008, Input PC: 8002001c, Input RS: 30, Input RT: 0, ALU_RESULT:
     2
# Time: 350, Input insn: 8fc30000, Input PC: 80020020, Input RS: 30, Input RT: 3, ALU_RESULT:
     2
# Time: 360, Input insn: 8fc20004, Input PC: 80020024, Input RS: 30, Input RT: 2, ALU_RESULT:
     2
# Time: 370, Input insn: 00621021, Input PC: 80020028, Input RS: 3, Input RT: 2, ALU_RESULT:
    5
# Time: 380, Input insn: afc20008, Input PC: 8002002c, Input RS: 30, Input RT: 2, ALU_RESULT:
     5
# Time: 390, Input insn: 8fc20008, Input PC: 80020030, Input RS: 30, Input RT: 2, ALU_RESULT:
     5
# Time: 400, Input insn: 03c0e821, Input PC: 80020034, Input RS: 30, Input RT: 0, ALU_RESULT:
     30
# Time: 410, Input insn: 8fbe0014, Input PC: 80020038, Input RS: 29, Input RT: 30, ALU_RESULT
    : 30
# Time: 420, Input insn: 27bd0018, Input PC: 8002003c, Input RS: 29, Input RT: 29, ALU_RESULT
    : 53
# Time: 430, Input insn: 03e00008, Input PC: 80020040, Input RS: 31, Input RT: 0, ALU_RESULT:
     53
# Time: 450, Input insn: 00000000, Input PC: 80020048, Input RS: 0, Input RT: 0, ALU_RESULT:
    0
# ** Note: $finish : exec_stage_tb.v(129)
# Time: 460 ns Iteration: 0 Instance: /exec_stage_tb
```

Listing 10: Simple If Register File Output - ALU

```
# Initializing memory
```

```
# Initializing Fetch module
# opened file srec_files/SimpleIf.srec
#
# read in file
#
# Time: 440, Input insn: 27bdffe8, Input PC: 80020000, Input RS: 29, Input RT: 29, ALU_RESULT
    : 65541
# Time: 450, Input insn: afbe0014, Input PC: 80020004, Input RS: 29, Input RT: 30, ALU_RESULT
    : 65541
# Time: 460, Input insn: 03a0f021, Input PC: 80020008, Input RS: 29, Input RT: 0, ALU_RESULT:
     29
# Time: 470, Input insn: 24020003, Input PC: 8002000c, Input RS: 0, Input RT: 2, ALU_RESULT:
    3
# Time: 480, Input insn: afc20000, Input PC: 80020010, Input RS: 30, Input RT: 2, ALU_RESULT:
     3
# Time: 490, Input insn: 24020002, Input PC: 80020014, Input RS: 0, Input RT: 2, ALU_RESULT:
    2
# Time: 500, Input insn: afc20004, Input PC: 80020018, Input RS: 30, Input RT: 2, ALU_RESULT:
     2
# Time: 510, Input insn: afc00008, Input PC: 8002001c, Input RS: 30, Input RT: 0, ALU_RESULT:
     2
# Time: 520, Input insn: 8fc20000, Input PC: 80020020, Input RS: 30, Input RT: 2, ALU_RESULT:
     2
# Time: 530, Input insn: 28420005, Input PC: 80020024, Input RS: 2, Input RT: 2, ALU_RESULT:
    1
# Time: 540, Input insn: 10400007, Input PC: 80020028, Input RS: 2, Input RT: 0, ALU_RESULT:
    1
# Time: 550, Input insn: 00000000, Input PC: 8002002c, Input RS: 0, Input RT: 0, ALU_RESULT:
    0
# Time: 560, Input insn: 8fc30000, Input PC: 80020030, Input RS: 30, Input RT: 3, ALU_RESULT:
     0
# Time: 570, Input insn: 8fc20004, Input PC: 80020034, Input RS: 30, Input RT: 2, ALU_RESULT:
     0
# Time: 580, Input insn: 00621021, Input PC: 80020038, Input RS: 3, Input RT: 2, ALU_RESULT:
    5
# Time: 590, Input insn: afc20000, Input PC: 8002003c, Input RS: 30, Input RT: 2, ALU_RESULT:
     5
# Time: 600, Input insn: 08008016, Input PC: 80020040, Input RS: 0, Input RT: 0, ALU_RESULT:
    5
# Time: 610, Input insn: 00000000, Input PC: 80020044, Input RS: 0, Input RT: 0, ALU_RESULT:
    0
# Time: 620, Input insn: 8fc30000, Input PC: 80020048, Input RS: 30, Input RT: 3, ALU_RESULT:
     0
# Time: 630, Input insn: 8fc20004, Input PC: 8002004c, Input RS: 30, Input RT: 2, ALU_RESULT:
     0
# Time: 640, Input insn: 00621023, Input PC: 80020050, Input RS: 3, Input RT: 2, ALU_RESULT:
    1
# Time: 650, Input insn: afc20000, Input PC: 80020054, Input RS: 30, Input RT: 2, ALU_RESULT:
     1
# Time: 660, Input insn: 8fc30000, Input PC: 80020058, Input RS: 30, Input RT: 3, ALU_RESULT:
     1
```

```
# Time: 670, Input insn: 8fc20004, Input PC: 8002005c, Input RS: 30, Input RT: 2, ALU_RESULT:
     1
# Time: 680, Input insn: 00621021, Input PC: 80020060, Input RS: 3, Input RT: 2, ALU_RESULT:
    5
# Time: 690, Input insn: afc20008, Input PC: 80020064, Input RS: 30, Input RT: 2, ALU_RESULT:
     5
# Time: 700, Input insn: 8fc20008, Input PC: 80020068, Input RS: 30, Input RT: 2, ALU_RESULT:
     5
# Time: 710, Input insn: 03c0e821, Input PC: 8002006c, Input RS: 30, Input RT: 0, ALU_RESULT:
     30
# Time: 720, Input insn: 8fbe0014, Input PC: 80020070, Input RS: 29, Input RT: 30, ALU_RESULT
    : 30
# Time: 730, Input insn: 27bd0018, Input PC: 80020074, Input RS: 29, Input RT: 29, ALU_RESULT
    : 53
# Time: 740, Input insn: 03e00008, Input PC: 80020078, Input RS: 31, Input RT: 0, ALU_RESULT:
     53
# Time: 760, Input insn: 00000000, Input PC: 80020080, Input RS: 0, Input RT: 0, ALU_RESULT:
    0
# ** Note: $finish : exec_stage_tb.v(129)
# Time: 770 ns Iteration: 0 Instance: /exec_stage_tb
```

Listing 11: Sum Array Register File Output - ALU

```
# Initializing memory
# Initializing Fetch module
# opened file srec_files/SumArray.srec
#
# read in file
#
# Time: 580, Input insn: 27bdffc8, Input PC: 80020000, Input RS: 29, Input RT: 29, ALU_RESULT
    : 65509
# Time: 590, Input insn: afbe0034, Input PC: 80020004, Input RS: 29, Input RT: 30, ALU_RESULT
    : 65509
# Time: 600, Input insn: 03a0f021, Input PC: 80020008, Input RS: 29, Input RT: 0, ALU_RESULT:
     29
# Time: 610, Input insn: afc00000, Input PC: 8002000c, Input RS: 30, Input RT: 0, ALU_RESULT:
     29
# Time: 620, Input insn: afc00004, Input PC: 80020010, Input RS: 30, Input RT: 0, ALU_RESULT:
     29
# Time: 630, Input insn: afc00000, Input PC: 80020014, Input RS: 30, Input RT: 0, ALU_RESULT:
     29
# Time: 640, Input insn: 08008010, Input PC: 80020018, Input RS: 0, Input RT: 0, ALU_RESULT:
    29
# Time: 650, Input insn: 00000000, Input PC: 8002001c, Input RS: 0, Input RT: 0, ALU_RESULT:
    0
# Time: 660, Input insn: 8fc20000, Input PC: 80020020, Input RS: 30, Input RT: 2, ALU_RESULT:
     0
# Time: 670, Input insn: 00021080, Input PC: 80020024, Input RS: 0, Input RT: 2, ALU_RESULT:
    8
# Time: 680, Input insn: 03c21021, Input PC: 80020028, Input RS: 30, Input RT: 2, ALU_RESULT:
     32
# Time: 690, Input insn: 8fc30000, Input PC: 8002002c, Input RS: 30, Input RT: 3, ALU_RESULT:
```

```
     32
# Time: 700, Input insn: ac430008, Input PC: 80020030, Input RS: 2, Input RT: 3, ALU_RESULT:
    32
# Time: 710, Input insn: 8fc20000, Input PC: 80020034, Input RS: 30, Input RT: 2, ALU_RESULT:
     32
# Time: 720, Input insn: 24420001, Input PC: 80020038, Input RS: 2, Input RT: 2, ALU_RESULT:
    3
# Time: 730, Input insn: afc20000, Input PC: 8002003c, Input RS: 30, Input RT: 2, ALU_RESULT:
     3
# Time: 740, Input insn: 8fc20000, Input PC: 80020040, Input RS: 30, Input RT: 2, ALU_RESULT:
     3
# Time: 750, Input insn: 2842000a, Input PC: 80020044, Input RS: 2, Input RT: 2, ALU_RESULT:
    1
# Time: 760, Input insn: 1440fff5, Input PC: 80020048, Input RS: 2, Input RT: 0, ALU_RESULT:
    2147876892
# Time: 770, Input insn: 00000000, Input PC: 8002004c, Input RS: 0, Input RT: 0, ALU_RESULT:
    0
# Time: 780, Input insn: afc00000, Input PC: 80020050, Input RS: 30, Input RT: 0, ALU_RESULT:
     0
# Time: 790, Input insn: 08008021, Input PC: 80020054, Input RS: 0, Input RT: 0, ALU_RESULT:
    0
# Time: 800, Input insn: 00000000, Input PC: 80020058, Input RS: 0, Input RT: 0, ALU_RESULT:
    0
# Time: 810, Input insn: 8fc20000, Input PC: 8002005c, Input RS: 30, Input RT: 2, ALU_RESULT:
     0
# Time: 820, Input insn: 00021080, Input PC: 80020060, Input RS: 0, Input RT: 2, ALU_RESULT:
    8
# Time: 830, Input insn: 03c21021, Input PC: 80020064, Input RS: 30, Input RT: 2, ALU_RESULT:
     32
# Time: 840, Input insn: 8c420008, Input PC: 80020068, Input RS: 2, Input RT: 2, ALU_RESULT:
    32
# Time: 850, Input insn: 8fc30004, Input PC: 8002006c, Input RS: 30, Input RT: 3, ALU_RESULT:
     32
# Time: 860, Input insn: 00621021, Input PC: 80020070, Input RS: 3, Input RT: 2, ALU_RESULT:
    5
# Time: 870, Input insn: afc20004, Input PC: 80020074, Input RS: 30, Input RT: 2, ALU_RESULT:
     5
# Time: 880, Input insn: 8fc20000, Input PC: 80020078, Input RS: 30, Input RT: 2, ALU_RESULT:
     5
# Time: 890, Input insn: 24420001, Input PC: 8002007c, Input RS: 2, Input RT: 2, ALU_RESULT:
    3
# Time: 900, Input insn: afc20000, Input PC: 80020080, Input RS: 30, Input RT: 2, ALU_RESULT:
     3
# Time: 910, Input insn: 8fc20000, Input PC: 80020084, Input RS: 30, Input RT: 2, ALU_RESULT:
     3
# Time: 920, Input insn: 2842000a, Input PC: 80020088, Input RS: 2, Input RT: 2, ALU_RESULT:
    1
# Time: 930, Input insn: 1440fff3, Input PC: 8002008c, Input RS: 2, Input RT: 0, ALU_RESULT:
    2147876952
# Time: 940, Input insn: 00000000, Input PC: 80020090, Input RS: 0, Input RT: 0, ALU_RESULT:
    0
```

```
# Time: 950, Input insn: 8fc20004, Input PC: 80020094, Input RS: 30, Input RT: 2, ALU_RESULT:
     0
# Time: 960, Input insn: 03c0e821, Input PC: 80020098, Input RS: 30, Input RT: 0, ALU_RESULT:
     30
# Time: 970, Input insn: 8fbe0034, Input PC: 8002009c, Input RS: 29, Input RT: 30, ALU_RESULT
    : 30
# Time: 980, Input insn: 27bd0038, Input PC: 800200a0, Input RS: 29, Input RT: 29, ALU_RESULT
    : 85
# Time: 1000, Input insn: 00000000, Input PC: 800200a8, Input RS: 0, Input RT: 0, ALU_RESULT:
     0
# ** Note: $finish : exec_stage_tb.v(129)
# Time: 1020 ns Iteration: 0 Instance: /exec_stage_tb
```

4 ALU Source Code

Listing 12: ALU

```
//
// alu.v
//
//

`include "control.vh"
`include "alu_func.vh"

module alu (
    clock,
    rsData,
    rtData,
    control,
    outData,
    bt,
    insn,
    pc
);

    input wire clock;
    input wire [0:31] rsData;
    input wire [0:31] rtData;

    input wire [0:`CONTROL_REG_SIZE-1] control;
    wire [0:5] opcode;
    wire [5:0] funct;
    wire [0:5] sa;
    wire [0:15] immediate;
    input wire [0:31] insn;
    wire [0:25] insn_index;
    input wire [0:31] pc;
    wire [0:17] offset;
    wire [0:4] rt;
```

```
output reg [0:31] outData;
output reg bt; //branch taken

assign opcode = insn[0:5];
assign rt = insn[11:15];
assign sa = insn[20:25];
assign funct = insn[26:31];
assign immediate = insn[16:31];
assign offset = insn[16:31];
assign insn_index = insn[6:31];

always @(posedge clock)
  begin
      bt = 0;

    if (control[`R_TYPE]) begin
    case(funct)
    `ADD:
      //rd - rs + rt
      outData = rsData + rtData;
    `ADDU:
      //todo: do we need to treat unsigned specially?
      outData = $unsigned(rsData) + $unsigned(rtData);
    `SUB:
      outData = rsData - rtData;
    `SUBU:
      //todo: correct way to do unsigned?
      outData = $unsigned(rsData) - $unsigned(rtData);
    `SLT: // rd - 1 if rs  rt; else rd - 0
      if ($signed(rsData)  $signed(rtData)) begin
          outData = 32'h00000001;
      end else begin
          outData = 32'h00000000;
      end
    `SLTU:
       if ($unsigned(rsData)  $unsigned(rtData)) begin
           outData = 32'h0000001;
       end else begin
           outData = 32'h00000000;
       end
    `SLL:
       outData = rtData  sa;
    `SRL:
       outData = rtData  sa;
    `SRA:
       outData = rtData  sa;
    `AND:
       outData = rsData & rtData;
    `OR:
```

```
  outData = rsData | rtData;
‘XOR:
  outData = rsData ^ rtData;
‘NOR:
  outData = ~(rsData | rtData);
endcase // case (funct)
end else if(control[‘I_TYPE]) begin
    case(opcode)
      ‘ADDIU:
        outData = rsData + $signed(immediate);
      ‘SLTI:
        if ($signed(rsData)  $signed(immediate)) begin
            outData = 32’h0000001;
        end else begin
            outData = 32’h0000000;
        end
      ‘LW:
        ;
      ‘SW:
        ;
      ‘LUI:
        outData = immediate  16;
      ‘ORI:
        outData = rsData | immediate;
    endcase // case (funct)
end else if (control[‘J_TYPE]) begin
case(opcode)
      ‘J:
        //outData = insn_index;
        bt = 1’b1;

      ‘BEQ:
        if (rsData == rtData) begin
            outData = pc + $signed(offset  2);
            bt = 1’b1;
        end else begin
            bt = 1’b0;
        end
      ‘BNE:
        if (rsData != rtData) begin
            outData = pc + $signed(offset  2);
            bt = 1’b1;
        end else begin
            bt = 1’b0;
        end
      ‘BGTZ:
        if ($signed(rsData)  1’b0) begin
            outData = pc + $signed(offset  2);
            bt = 1’b1;
        end else begin
            bt = 1’b0;
```

```
            end
          `BLEZ:
            if ($signed(rsData) = 1'b0) begin
                outData = pc + $signed(offset  2);
            end else begin
                bt = 1'b0;
            end

          `REGIMM:
            case(rt)
              `BLTZ:
                if ($signed(rsData)  1'b0) begin
                    outData = pc + $signed(offset  2);
                    bt = 1'b1;
                end else begin
                    bt = 1'b0;
                end
              `BGEZ:
                if ($signed(rsData) = 1'b0) begin
                    outData = pc + $signed(offset  2);
                    bt = 1'b1;
                end else begin
                    bt = 1'b0;
                end
            endcase // case (rtData)

        endcase // case (funct)

    end

  end



endmodule
```

Listing 13: ALU Unit Test Bench

```
//
// alu_tb.v
//
// ALU test bench
//

`include "control.vh"
`include "alu_func.vh"

module alu_tb;
    reg clock;
    reg[0:31] rsData;
    reg[0:31] rtData;
```

```
    reg[0:`CONTROL_REG_SIZE-1] control;
    reg[0:5] funct;
    reg[0:5] sa;
    reg[0:15] immediate;
    reg[0:31] insn;
    wire [0:31] aluOutput;
    wire bt;
    reg [0:31] pc;

    alu DUT(
        .clock (clock),
            .rsData (rsData),
        .rtData (rtData),
            .control (control),
            .outData (aluOutput),
            .bt (bt),
            .insn (insn),
            .pc (pc)
    );

initial begin
        clock = 1;
    end

    always begin
        #5 clock = !clock;
    end

    event terminate_sim;
    initial begin
        @ (terminate_sim);
        #10 $finish;
    end

    initial begin

        @ (posedge clock);
        control[`R_TYPE] = 1'b1;
        control[`I_TYPE] = 1'b0;
        pc = 0;
        rsData = 32'h00000005;
        rtData = 32'h00000002;

        //arithmetic function set to ADD
        insn = 32'h00000000 | `ADD;
        @ (posedge clock);
        @ (posedge clock);
        $display("ALU output for 5 + 2: %d", aluOutput);

        rsData = -32'h00000002;
        rtData = 32'h00000002;
```

```
//arithmetic function set to ADD
insn = 32'h00000000 | `ADD;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %d + %d : %d",$signed(rsData), rtData, aluOutput);

rsData = -32'h00000002;
rtData = 32'h00000001;
//arithmetic function set to ADDU
insn = 32'h00000000 | `ADDU;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %d + %d (unsigned): %d",rsData, rtData, aluOutput);

rsData = 32'h00000004;
rtData = 32'h00000002;
insn = 32'h00000000 | `SUB;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %d - %d : %d",rsData, rtData, aluOutput);

rsData = -32'h00000002;
rtData = 32'h00000007;
insn = 32'h00000000 | `SUBU;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %d - %d (unsigned): %d",rsData, rtData, aluOutput);

rsData = -32'h00000002;
rtData = 32'h00000007;
insn = 32'h00000000 | `SLT;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %d  %d : %d", $signed(rsData), rtData, aluOutput);

rsData = -32'h00000002;
rtData = 32'h00000007;
insn = 32'h00000000 | `SLTU;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %d  %d (unsigned): %d",rsData, rtData, aluOutput);

rsData = 32'h00000002;
rtData = 32'h00000002;
sa = 5'b00010;

insn = 32'h00000000 | `SLL | (5'b00010  6);
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %d  %d: %d", rtData, sa, aluOutput);
```

```
rsData = 32'h00000002;
rtData = 32'h00000002;
sa = 5'b00010;
insn = 32'h00000000 | `SRL | (5'b00010  6);
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %d  %d: %d", rtData, sa, aluOutput);

rsData = 32'h00000002;
rtData = 32'h00000001;
sa = 5'b00010;
insn = 32'h00000000 | `SRA | (5'b00010  6);
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %d  %d: %d", rtData, sa, aluOutput);

rsData = 32'h00040a02;
rtData = 32'hffffffff;
insn = 32'h00000000 | `AND;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %h AND %h: %h", rsData, rtData, aluOutput);

rsData = 32'h00040a02;
rtData = 32'hffff0000;
insn = 32'h00000000 | `OR;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %h OR %h: %h", rsData, rtData, aluOutput);

rsData = 32'h00040a02;
rtData = 32'hffffffff;
insn = 32'h00000000 | `XOR;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %h XOR %h: %h", rsData, rtData, aluOutput);

rsData = 32'h00040a02;
rtData = 32'hffffffff;
insn = 32'h00000000 | `NOR;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %h NOR %h: %h", rsData, rtData, aluOutput);

control[`I_TYPE] = 1'b1;
control[`R_TYPE] = 1'b0;

rsData = 32'h00000008;
immediate = 16'h0007;
insn = 32'h00000000 | (`ADDIU  26) | 16'h0007;
@ (posedge clock);
```

```
@ (posedge clock);
$display("ALU output for %d + %d: %d (immediate unsigned)", rsData, immediate,
    aluOutput);

rsData = 32'h00000008;
immediate = 16'h0007;
insn = 32'h00000000 | (`SLTI  26) | 16'h0007;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %d  %d: %d (immediate)", rsData, immediate, aluOutput);

rsData = 32'h00000007;
immediate = 16'h0008;
insn = 32'h00000000 | (`SLTI  26) | 16'h0008;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %d  %d: %d (immediate)", rsData, immediate, aluOutput);


immediate = 16'h0007;
insn = 32'h00000000 | (`LUI  26) | 16'h0007;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for load upper immediate: %h - %h ",immediate, aluOutput);

rsData = 32'h0000ffff;
immediate = 16'h0007;
insn = 32'h00000000 | (`ORI  26) | 16'h0007;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for %h ORI %h: %h (immediate)", rsData, immediate, aluOutput);

control[`I_TYPE] = 1'b0;
control[`R_TYPE] = 1'b0;
control[`J_TYPE] = 1'b1;

insn = 32'h00000000 | (`J  26) | 32'h000000ff;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for J %h", aluOutput);
$display("Branch taken: (1 = yes, 0 = no) %d", bt);

rsData = 32'h00000001;
rtData = 32'h00000001;
insn = 32'h00000000 | (`BEQ  26) | 32'h0000dead;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for BEQ %h", aluOutput);
$display("Branch taken: (1 = yes, 0 = no) %d", bt);

rsData = 32'h00000101;
```

```
rtData = 32'h00000001;
insn = 32'h00000000 | (`BEQ  26) | 32'h0000dead;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for BEQ %h", aluOutput);
$display("Branch taken: (1 = yes, 0 = no) %d", bt);

       rsData = 32'h00000001;
rtData = 32'h00000001;
insn = 32'h00000000 | (`BNE  26) | 32'h0000dead;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for BNE %h", aluOutput);
$display("Branch taken: (1 = yes, 0 = no) %d", bt);

rsData = 32'h00000101;
rtData = 32'h00000001;
insn = 32'h00000000 | (`BNE  26) | 32'h0000dead;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for BNE %h", aluOutput);
$display("Branch taken: (1 = yes, 0 = no) %d", bt);

rsData = 32'h00000101;
insn = 32'h00000000 | (`BGTZ  26) | 32'h0000beef;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for BGTZ %h (taken)", aluOutput);
$display("Branch taken: (1 = yes, 0 = no) %d", bt);

rsData = 32'h00000101;
insn = 32'h00000000 | (`BLEZ  26) | 32'h0000beef;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for BLEZ %h (not taken)", aluOutput);
$display("Branch taken: (1 = yes, 0 = no) %d", bt);


rsData = 32'h00000101;
insn = 32'h00000000 | (`REGIMM  26) | 32'h0000beef;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for BLTZ %h (not taken)", aluOutput);
$display("Branch taken: (1 = yes, 0 = no) %d", bt);

rsData = 32'h00000101;
insn = 32'h00000000 | (`REGIMM  26) | (`BGEZ  16) | 32'h0000beef;
@ (posedge clock);
@ (posedge clock);
$display("ALU output for BGEZ %h (taken)", aluOutput);
$display("Branch taken: (1 = yes, 0 = no) %d", bt);
```

```
        - terminate_sim;
    end


endmodule
```

Listing 14: Execute Stage Test Bench

```
//
// exec_stage_tb.v
//
// Testbench for the execute stage
// includes fetch, decode, and alu
//

module exec_stage_tb;
    reg clock;

    wire[0:31] address;
    wire wren;
    wire[0:31] data_in;
    wire[0:31] data_out;

    wire[0:31] fetch_address;
    wire fetch_wren;
    wire[0:31] fetch_data_in;
    wire[0:31] fetch_data_out;

    wire[0:31] fetch_insn_decode;
    wire[0:31] fetch_pc;
    reg fetch_stall;

    wire[0:31] decode_rs_data;
    wire[0:31] decode_rt_data;
    wire[4:0] decode_rd_in;
    wire[0:31] decode_pc_out;
    wire[0:31] decode_ir_out;
    wire[0:31] decode_write_back_data;
    wire decode_reg_write_enable;
    wire [0:`CONTROL_REG_SIZE-1] decode_control;

    wire[0:31] srec_address;
    wire srec_wren;
    wire[0:31] srec_data_in;
    wire[0:31] srec_data_out;

    wire srec_done;

    reg[0:31] tb_address;
```

```
reg tb_wren;
reg[0:31] tb_data_in;
wire[0:31] tb_data_out;

wire[0:31] bytes_read;
integer byte_count;
integer read_word;
reg[0:31] fetch_word;
reg instruction_valid;

// alu
reg[0:31] alu_rs_data_res;
reg[0:31] alu_rt_data_res;
reg[0:31] alu_insn;
reg[0:31] alu_insn_res;
wire [0:31] alu_output;
wire bt;
reg [0:31] alu_pc_res;
reg [0:`CONTROL_REG_SIZE-1] alu_control_res;

mem_controller mcu(
    .clock (clock),
    .address (address),
    .wren (wren),
    .data_in (data_in),
    .data_out (data_out)
);

fetch DUT(
    .clock (clock),
    .address (fetch_address),
    .insn (fetch_data_in),
    .insn_decode (fetch_data_out),
    .pc (fetch_pc),
    .wren (fetch_wren),
    .stall (fetch_stall)
);

srec_parser #("srec_files/BubbleSort.srec") U0(
    .clock (clock),
    .mem_address (srec_address),
    .mem_wren (srec_wren),
    .mem_data_in (srec_data_in),
    .mem_data_out (srec_data_out),
    .done (srec_done),
    .bytes_read(bytes_read)
);

decode U1(
    .clock (clock),
    .insn (fetch_data_out),
```

```
        .insn_valid (instruction_valid),
    .pc (fetch_address),
    .rsData (decode_rs_data),
    .rtData (decode_rt_data),
    .rdIn (decode_rd_in),
    .pcOut (decode_pc_out),
    .irOut (decode_ir_out),
    .writeBackData (decode_write_back_data),
    .regWriteEnable (decode_reg_write_enable),
    .control (decode_control)
);

alu alu(
    .clock (clock),
        .rsData (decode_rs_data),
    .rtData (decode_rt_data),
        .control (decode_control),
        .outData (alu_output),
        .bt (alu_bt),
        .insn (alu_insn),
        .pc (decode_pc_out)
);



assign address = srec_done ? (fetch_stall ? tb_address : fetch_address) : srec_address;
assign wren = srec_done ? (fetch_stall ? tb_wren : fetch_wren) : srec_wren;
assign tb_data_out = data_out;
assign fetch_data_in = data_out;
assign data_in = srec_done ? (fetch_stall ? tb_data_in : fetch_data_in) : srec_data_in;


// Specify when to stop the simulation
event terminate_sim;
initial begin
    @ (terminate_sim);
    #10 $finish;
end

initial begin
    clock = 1;
    fetch_stall = 1;
    instruction_valid = 1'b0;
end

always begin
    #5 clock = !clock;
end

initial begin
    $dumpfile("exec_stage_tb.vcd");
```

```
    $dumpvars;
end


always @(posedge clock) begin
    alu_insn = fetch_data_out;
    alu_insn_res = alu_insn;
    alu_control_res = decode_control;
    alu_pc_res = decode_pc_out;
    alu_rs_data_res = decode_rs_data;
    alu_rt_data_res = decode_rt_data;
end


initial begin
    @(posedge srec_done);
    @(posedge clock);
    byte_count = bytes_read+4;
    tb_address = 32'h8002_0000;
    tb_wren = 1'b0;
    instruction_valid = 1'b0;
    fetch_stall = 0;

    while (byte_count  0) begin
        @(posedge clock);
        if ((fetch_address - 4)  32'h8002_0000) begin
            instruction_valid = 1'b0;
        end else begin
            instruction_valid = 1'b1;
        end
            read_word = tb_data_out;
        fetch_word = fetch_data_out;

        tb_address = tb_address + 4;
        byte_count = byte_count - 4;
    end

    // The decode runs one clock cycle behind the fetch
    @(posedge clock);
    tb_address = tb_address + 4;
    instruction_valid = 1'b0;

    // allow the last alu op to run
    @(posedge clock);
    @(posedge clock);
    -terminate_sim;
end // initial begin

// ALU Process
initial begin
    @(posedge srec_done);
```

```
        @(posedge clock);

        while (byte_count  0) begin
            @(posedge clock);

            $display("Time: %d, Input insn: %X, Input PC: %X, Input RS: %d, Input RT: %d,
                ALU_RESULT: %d",
                    $time, alu_insn_res, alu_pc_res, alu_rs_data_res, alu_rt_data_res,
                        alu_output);

        end
        // allow the last decode to run
        @(posedge clock);
        @(posedge clock);
        $display("Time: %d, Input insn: %X, Input PC: %X, Input RS: %d, Input RT: %d,
            ALU_RESULT: %d",
                $time, alu_insn_res, alu_pc_res, alu_rs_data_res, alu_rt_data_res, alu_output)
                    ;
    end

endmodule
```