CS224

Lab 6

Section 6

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1)

No.	Cache Size KB	N way cache	Word Size in bits	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Word Block Offset Size in bits	Byte Offset Size in bits	Block Replacement Policy Needed (Yes/No)
1	128	1	32	4	2^{13}	15	13	2	2	No
2	128	4	32	16	2^{9}	17	9	4	2	Yes
4	128	Full	32	16	1	26	0	4	2	Yes
5	256	2	64	8	2^{11}	15	11	3	3	Yes
6	256	4	64	32	2^{8}	16	8	5	3	Yes
7	256	Full	16	16	1	27	0	4	1	Yes

2)

Memory Address Accessed (hex)	Set No.	Hit (yes/no)
00 00 20 24	0	no
00 00 20 42	0	no
00 00 20 68	1	no
00 00 20 04	0	no
00 00 20 0C	1	no
00 00 20 4C	1	no

3)

Memory Address Accessed (hex)	Set No.	Hit (yes/no)
00 00 20 2C	1	no
00 00 20 48	1	no
00 00 20 44	0	no
00 00 20 0C	1	no
00 00 20 04	0	no
00 00 20 0C	1	yes

4)

a) Physical address structure

Tag 25 bits	Set 1 bit	Block offset 5 bits	Byte offset 1 bit

b) Size of block

LRU bits = log_2(8) = 3

Data bits = word size (bytes) * block size (words) * 8 = 2 * 32 * 8 = 512

Size of a block in total = V + D + LRU + Tag + Data = 1 + 1 + 3 + 25 + 512 = 542 bits

V 1 bit	D (Dirty bit) 1 bit	LRU 3 bits	Tag 25 bits	Data 512 bits

c) Size of a set, total SRAM size

Size of a set = 8 * size of a block = 8 * 542 = 4336 bits

Total SRAM size = number of sets * size of a set = 2 * 4336 = 8672 bits

d) Random replacement

If we would use random replacement then we won't need 3 bits of LRU since it would be meaningless to store the least recently used block. Therefore, the size of a block would decrease by 3 and become 539 bits.

Size of a new set = 8 * 539 = 4312 bits

New total SRAM size = 2 * 4312 = 8624 bits

Difference = 8672 - 8624 = 48 bits

New SRAM would be 48 bits smaller than the first one.