Diagram, schematic

Description automatically generated

We have 8 cache blocks (squares, labelled 0-7) and 7 LRU bits (circles, labelled 0-6). Each bit can be 0 or 1, pointing to the left or the right respectively. Staring from the scenario on the top, where all LRU bits are 0, following the arrows, it can be determined that cache block #0 is the least recently accessed.

Then the bits on the arrow paths are flipped, leading to the bottom scenario. This time, cache block #4 is selected. This process continues, and the results are summarized in the table below.

x means don’t care.

|  |  |  |
| --- | --- | --- |
| current LRU bits [6:0] | replace block # | new LRU bits [6:0] |
| xxx0x00 | 0 | xxx1x11 |
| x0xx0x1 | 4 | x1xx1x0 |
| xx0xx10 | 2 | xx1xx01 |
| 0xxx1x1 | 6 | 1xxx0x0 |
| xxx1x00 | 1 | xxx0x11 |
| x1xx0x1 | 5 | x0xx1x0 |
| xx1xx10 | 3 | xx0xx01 |
| 1xxx1x1 | 7 | 0xxx0x0 |