

THE UNIVERSITY OF BRITISH COLUMBIA  
DEPARTMENT OF ELECTRICAL AND COMPUTER  
ENGINEERING

**ELEC 402 Assignment 3: The MOS  
Transistor / Cadence**

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## Question 1

### Circuit A

When  $V_{out} = V_{OL}$ ,  $V_{in}$  must be equal to  $V_{DD} = 1.2\text{ V}$ . Hence,  $V_{GS} - V_T > V_{DS}$ , NMOS is in the linear region. For small  $V_{OL}$ , we have

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{W}{L} \mu_n C_{ox} [(V_{DD} - V_{T0}) V_{OL}]$$

Substituting numbers in, we get  $W = 0.6\text{ }\mu\text{m}$ .

### Circuit B

The top transistor has

$$\begin{aligned}V_G &= V_{DD} \\V_S &= V_{DD} - V_{DS} \\V_{GS} &= V_{DD} - (V_{DD} - V_{DS}) = V_{DS}\end{aligned}$$

hence,  $V_{GS} - V_T < V_{DS}$ , it is always in saturation.

$$I_{sat}^{top} = \frac{1}{2} \mu_n C_{ox} (V_{DD} - V_{T0})^2 = 94.5 \times 10^{-6} \text{ A}$$

The bottom transistor has

$$V_{GS} = V_{DD} \quad V_{DS} = V_{OL}$$

hence,  $V_{GS} - V_T > V_{DS}$ , it is in linear region.

$$\begin{aligned}I_{sat}^{bottom} &= \mu_n C_{ox} [(V_{DD} - V_{T0}) V_{DS}] = \frac{W}{0.1\mu\text{m}} \times 21.6 \times 10^{-6} \text{ A} \\I_{sat}^{bottom} &= I_{sat}^{top}\end{aligned}$$

We have  $W = 0.438\text{ }\mu\text{m}$ .

### Circuit C

The top transistor is always in saturation, hence

$$I_{sat}^{top} = \frac{1}{2} \mu_n C_{ox} (V_{DD} - V_{T0})^2 = 148.5 \times 10^{-6} \text{ A}$$

$I_{sat}^{bottom}$  is the same as Circuit B, equating the two terms, we have  $W = 0.6875 \mu m$ .

## Observation

When the pull-up network becomes stronger, we need stronger pull-down network to battle it, hence, the transistor becomes wider.

## Question 2

a

When  $V_{in}$  goes high, the NMOS will pull  $V_{out}$  to  $V_{OH} = V_{DD} - V_{Tn}$ , at that point  $V_{GS} = V_{DD} - V_{DD} + V_{Tn} = V_{Tn}$ , any higher  $V_{out}$  will set the NMOS to cutoff. When  $V_{in}$  goes low, the PMOS will pull  $V_{out}$  to  $V_{OL} = -V_{Tp}$ , at that point  $V_{GS} = 0 - (-V_{Tp}) = V_{Tp}$ , any lower  $V_{out}$  will set the PMOS to cutoff. This is a buffer, the output swing is from  $V_{OL} = -V_{Tp}$  to  $V_{OH} = V_{DD} - V_{Tn}$ .

b

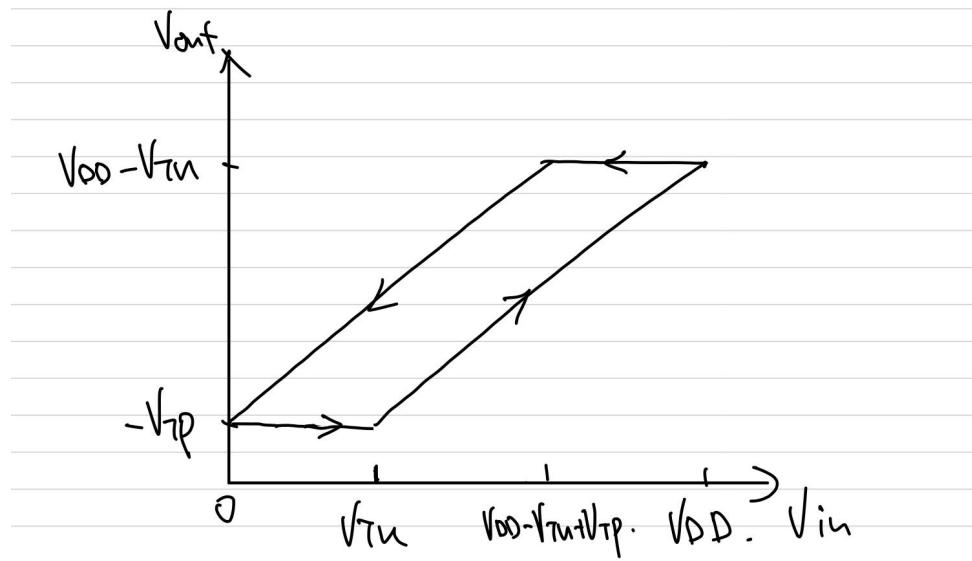


Figure 1: Plotted VTC of the buffer.

**c**

The gain of the circuit is  $\frac{V_{DD} - V_{Tn} + V_{Tp}}{V_{DD}}$ . This is not a valid gate. It does not have a high gain region between two low gain regions.

**d**

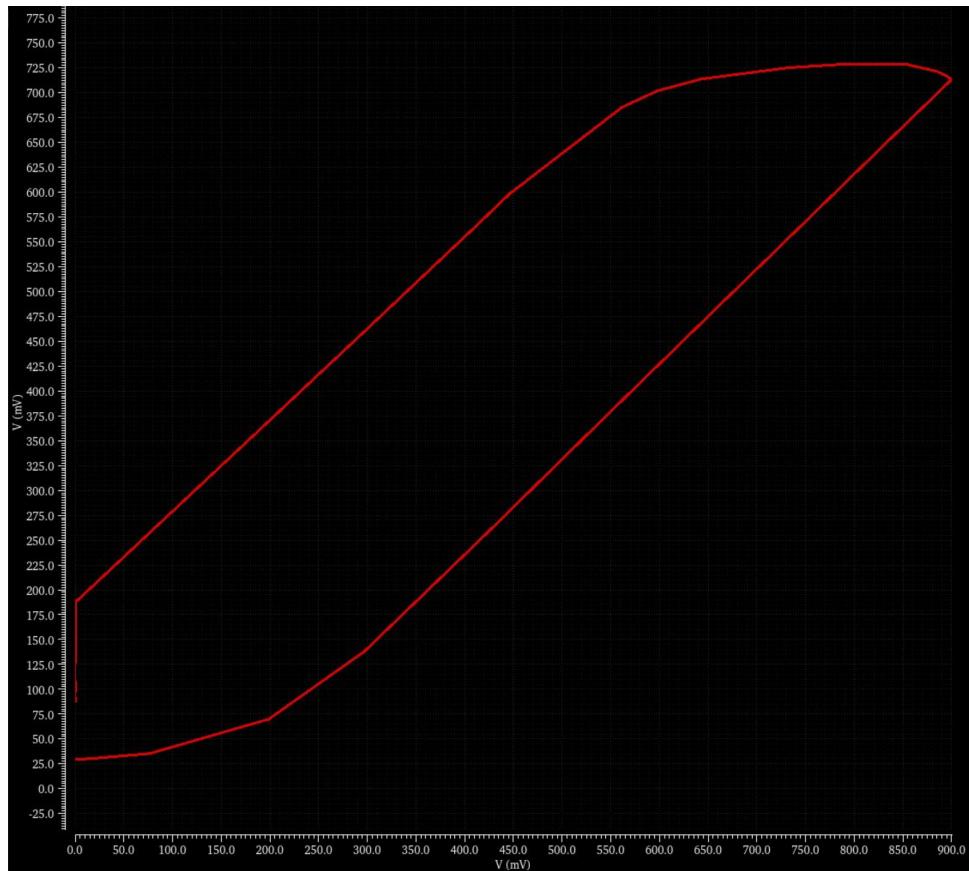


Figure 2: Simulated VTC of the buffer.

## Question 3

**Find  $V_{T0}$**

The circuit shown in Figure 3 is used to carry out a DC analysis where  $I_D$  is plotted versus a sweep of  $V_{GS}$ .  $V_{DS}$  is kept to be constant 1 V. The simulation waveform is shown in Figure 4.

When  $V_{DS}$  is 1 V, and  $V_{GS}$  is slightly higher than  $V_{T0}$ , the transistor is in the saturation region, we have

$$I_{DS} = \frac{W}{L} \mu C_{ox} (V_{GS} - V_T)(1 + \lambda V_{DS}) \quad (1)$$

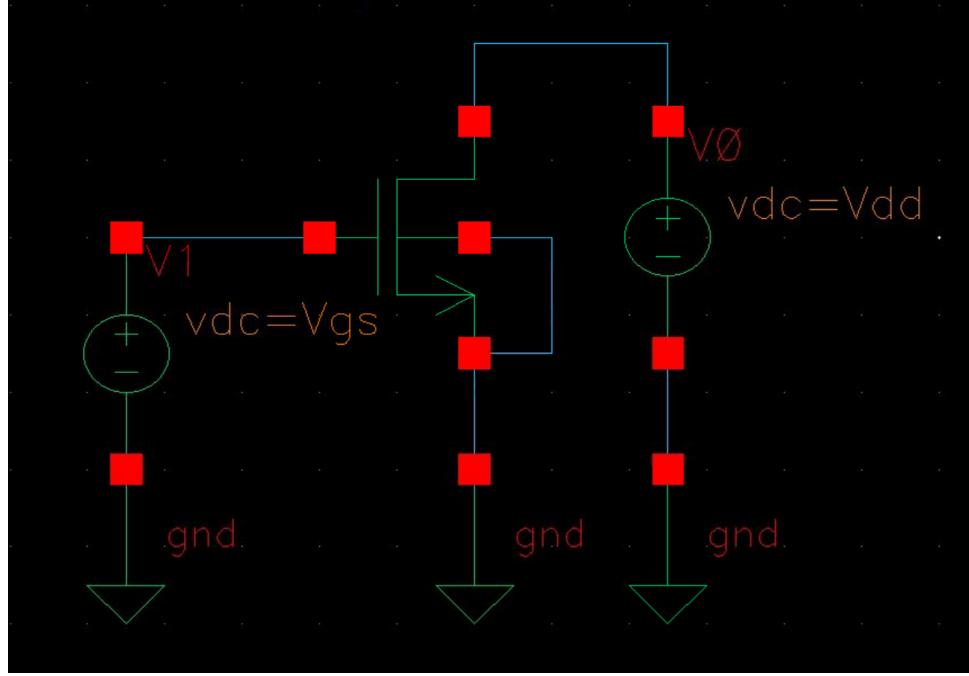


Figure 3: Circuit used to find  $V_{T0}$ .

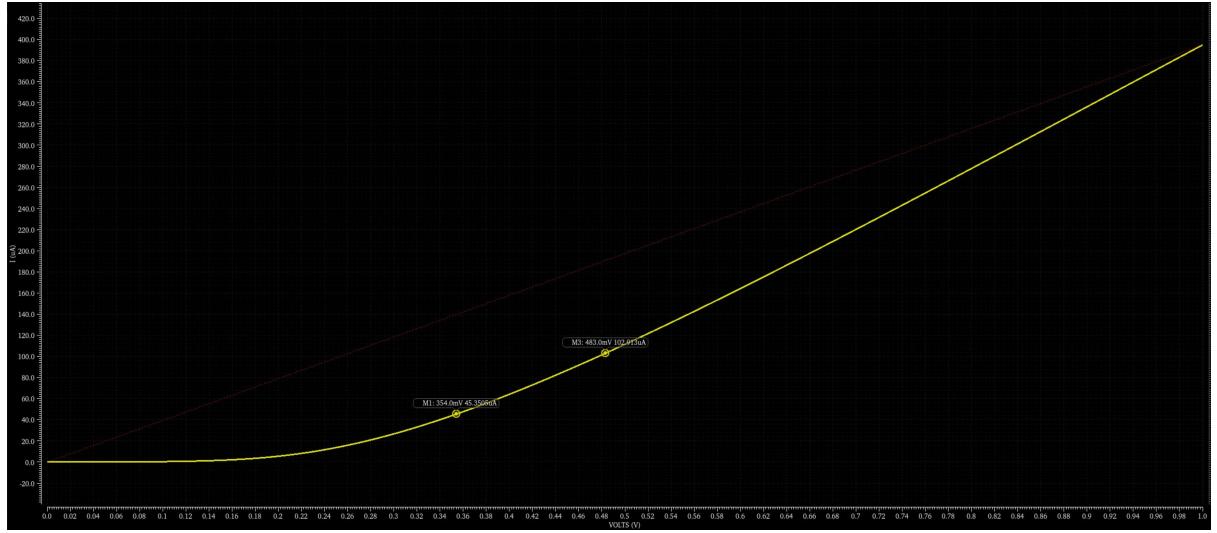


Figure 4: Simulation waveform of a DC  $V_{GS}$  sweep.  $I_{DS}$  is plotted on the y-axis and  $V_{GS}$  is plotted on the x-axis.  $V_{DS}$  is kept to be constant 1 V.

Here because  $V_{SB}$  is 0, we do not have any body effect, thus,  $V_T = V_{T0}$ . For two points on the  $I_{DS}$  vs  $V_{GS}$  plot with the same  $V_{DS}$ , we can derive the following

$$\frac{I_{DS}^1}{I_{DS}^2} = \frac{V_{GS}^1 - V_{T0}}{V_{GS}^2 - V_{T0}}$$

$$V_{T0} = \frac{I_{DS}^1 V_{GS}^2 - I_{DS}^2 V_{GS}^1}{I_{DS}^1 - I_{DS}^2}$$

From the curve shown in Figure 4, we marked two points where  $I_{DS}^1 = 45.4 \mu A$ ,

$V_{GS}^1 = 354 \text{ mV}$ ,  $I_{DS}^2 = 102.9 \mu\text{A}$ , and  $V_{GS}^2 = 483 \text{ mV}$ . Therefore,  $V_{T0} = 252 \text{ mV}$ .

## Find the body-effect coefficient $\gamma$

Circuit shown in Figure 5 is used to find the body-effect coefficient  $\gamma$ .  $V_D$  and  $V_S$  are fixed to 1 V and 0.1 V respectively, such that  $V_{DS} = 0.9 \text{ V}$  and  $V_{SB} = 0.1 \text{ V}$ . A DC sweep of  $V_{GS}$  is carried out again to find  $V_T$ . We have

$$V_T = V_{T0} + \gamma(\sqrt{V_{SB} + |2\Phi_F|} - \sqrt{|2\Phi_F|})$$

$V_{T0}$ ,  $V_{SB}$ , and  $|2\Phi_F|$  are known, hence, we can get  $\gamma$  once we have found  $V_T$ . Figure 6 shows the simulation waveform. Just like before, we extract two points and have found out that  $V_T = 262 \text{ mV}$  using Equation 1. Hence,  $\gamma = 0.193$ .

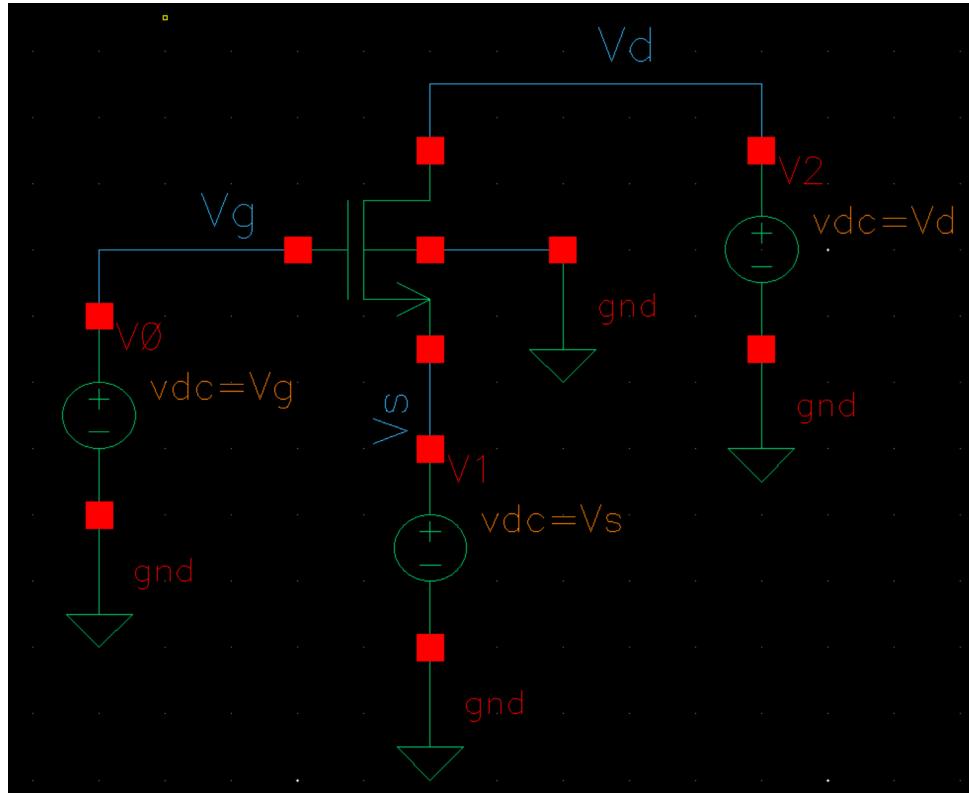


Figure 5: Circuit used to find  $\gamma$  and  $\lambda$ .

## Find the channel-length modulation parameter $\lambda$

Looking back at Equation 1, for constant  $V_{GS}$  and  $V_T$  (due to a constant  $V_{SB}$ ), if we plot  $I_{DS}$  over a sweep of  $V_{DS}$  (using the testbench in Figure 5) and extract two points in the

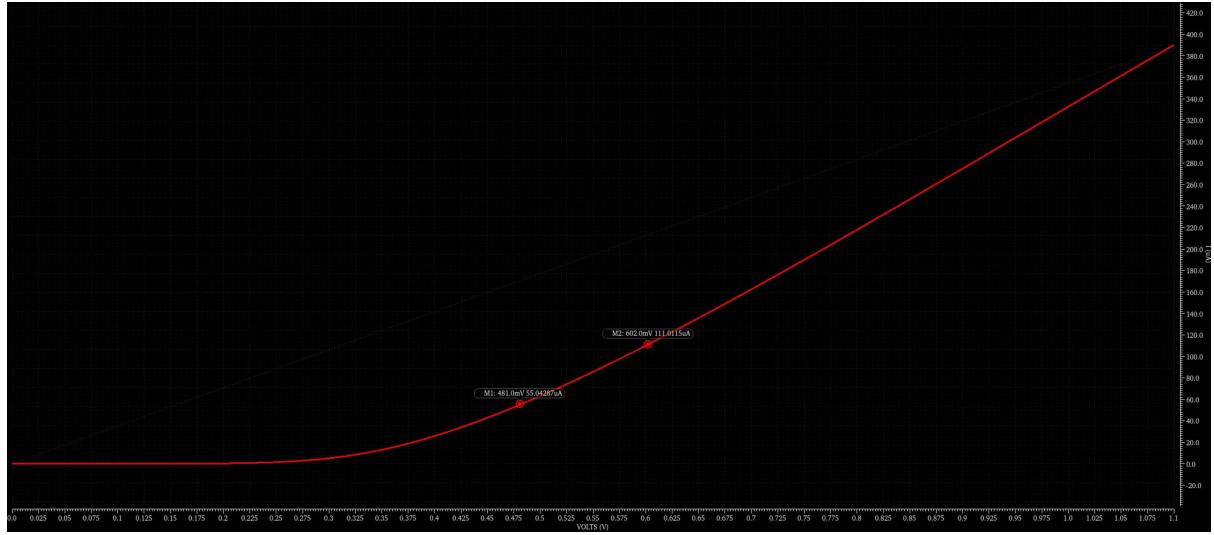


Figure 6: Simulation waveform of a DC  $V_{GS}$  sweep.  $I_{DS}$  is plotted on the y-axis and  $V_{GS}$  is plotted on the x-axis.  $V_{DS} = 0.9$  V and  $V_{SB} = 0.1$  V.

saturation region from the plot, we have

$$\frac{I_{DS}^1}{I_{DS}^2} = \frac{1 + \lambda V_{DS}^1}{1 + \lambda V_{DS}^2}$$

$$\lambda = \frac{I_{DS}^1 - I_{DS}^2}{I_{DS}^2 V_{DS}^1 - I_{DS}^1 V_{DS}^2}$$

Figure 7 shows the simulation waveform, after taking two points from the curve, we have found out that  $\lambda = 0.132$   $V^{-1}$ .

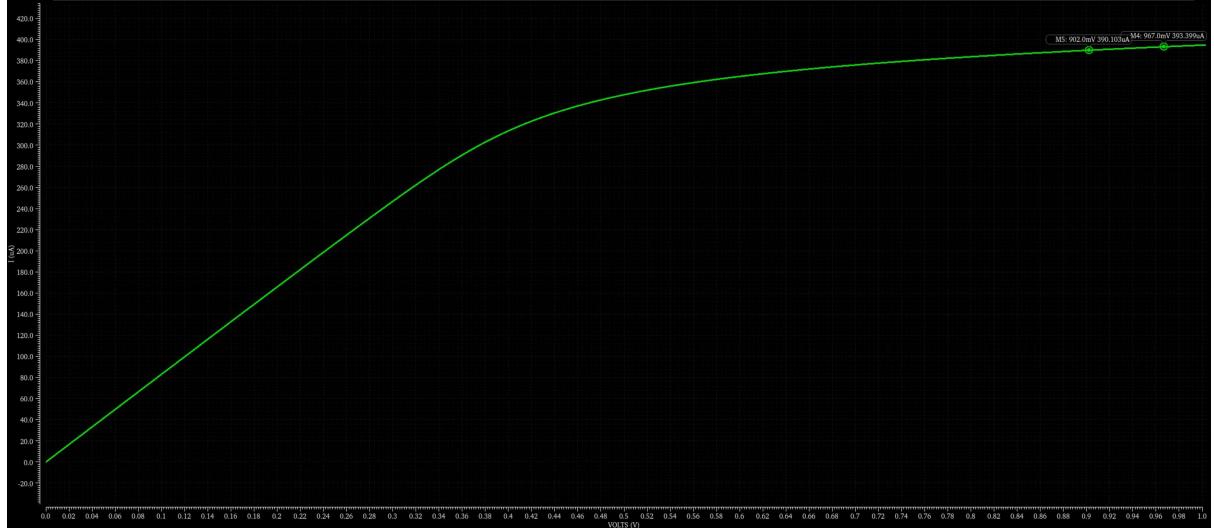


Figure 7: Simulation waveform of a DC  $V_{DS}$  sweep.  $I_{DS}$  is plotted on the y-axis and  $V_{DS}$  is plotted on the x-axis.  $V_{GS} = 1$  V and  $V_{SB} = 0$ .

## Question 4

**a**

Let  $\epsilon_{ox} = 3.45 \times 10^{-11} F/m$ , then

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 8.63 \times 10^{-3} F/m^2$$

$$C_g = C_{ox}L = 1.55 fF/\mu m$$

$$C_{overlap} = C_{ox}x_d = 0.19 fF/\mu m$$

The worst case  $C_G$  occurs when the transistor is in the cutoff or the linear region. Where  $C_G = C_gW + 2C_{overlap}W = 1.74 fF$ . The values of  $C_{GS}$ ,  $C_{GD}$ , and  $C_{GB}$  in different operation regions are summarized in Table 1.

Table 1: Different components of the channel capacitance of MOS transistor for different operation regions.

Operation region	$C_{GB} (fF)$	$C_{GS} (fF)$	$C_{GD} (fF)$
Cutoff	$C_gW = 1.40$	$C_{overlap}W = 0.17$	$C_{overlap}W = 0.17$
Linear	0	$C_gW/2 + C_{overlap}W = 0.87$	$C_gW/2 + C_{overlap}W = 0.87$
Saturation	0	$2C_gW/3 + C_{overlap}W = 1.10$	$C_{overlap}W = 0.17$

**b**

Assume the intrinsic carrier concentration of silicon  $n_i$  at  $298 K$  is  $1.45 \times 10^{10} cm^{-3}$  and the permittivity of silicon  $\epsilon_{Si}$  is  $1.04 \times 10^{-12} F/cm$ . Assume  $V_D = 0$  and  $m = 0.5$ . We have

$$\Phi_B = \frac{kT}{q} \ln \left| \frac{N_A N_D}{n_i^2} \right| = 0.927 V$$

$$C_{j0} = \sqrt{\frac{\epsilon_{Si} q}{2\Phi_B} \frac{N_A N_D}{N_A + N_D}} = 5.19 \times 10^{-4} F/m^2$$

$$C'_j = \frac{C_{j0}}{(1 - V_D/\Phi_B)^m} = 5.18 \times 10^{-4} F/m^2$$

$$C_J = W C_j = W C'_j (Y + x_j)$$

$$C_j = C'_j (Y + x_j) = 0.571 fF/\mu m$$

c

i

For a reverse-biased voltage of  $-1.8\text{ V}$ , we have

$$C'_j = \frac{C_{j0}}{(1 - V_D/\Phi_B)^m} = 3.03 \times 10^{-4} \text{ F/m}^2$$

$$C_J = WC'_j(Y + x_j) = 0.3 \text{ fF}$$

ii

$$C_J = WC_J = 0.5 \text{ fF}$$

## Question 5

### Find the average FO4 propagation delay

Figure 8 shows the circuit used to find the average FO4 propagation delay of a CMOS inverter. The inverter on the very left has a size of  $\frac{W_p}{W_n} = \frac{2}{1}$ , the one following it on the right has  $\frac{W_p}{W_n} = \frac{8}{4}$ , each inverter is 4 times sized than its previous one. For a transient analysis, an abrupt rising signal from 0 to 1 V was applied to the input on the left, it waited for a period long enough for the signal to propagate to the output on the right. Then, an abrupt falling signal from 1 V to 0 was applied on the input and it waited for transitions of all inverters to settle. Figure 9 shows the simulation waveform.

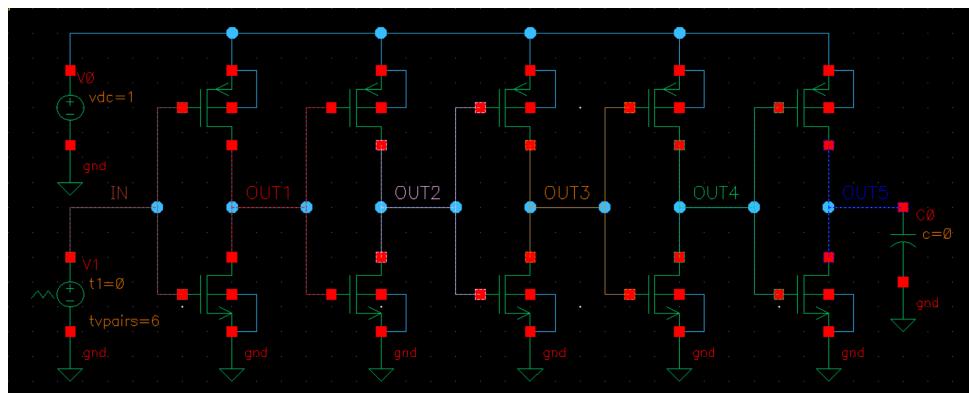


Figure 8: Circuit used to find the average FO4 propagation delay of a CMOS inverter. Each inverter is 4 times sized than its previous one.

$t_{PHL}$  and  $t_{PLH}$  of inverter number 2, 3, and 4, were extracted from Figure 9 and are summarized in Table 2. The FO4 propagation delay of inverter number 3 is calculated to be  $(3.34 + 2.37)/2 = 2.86\text{ ps}$ .

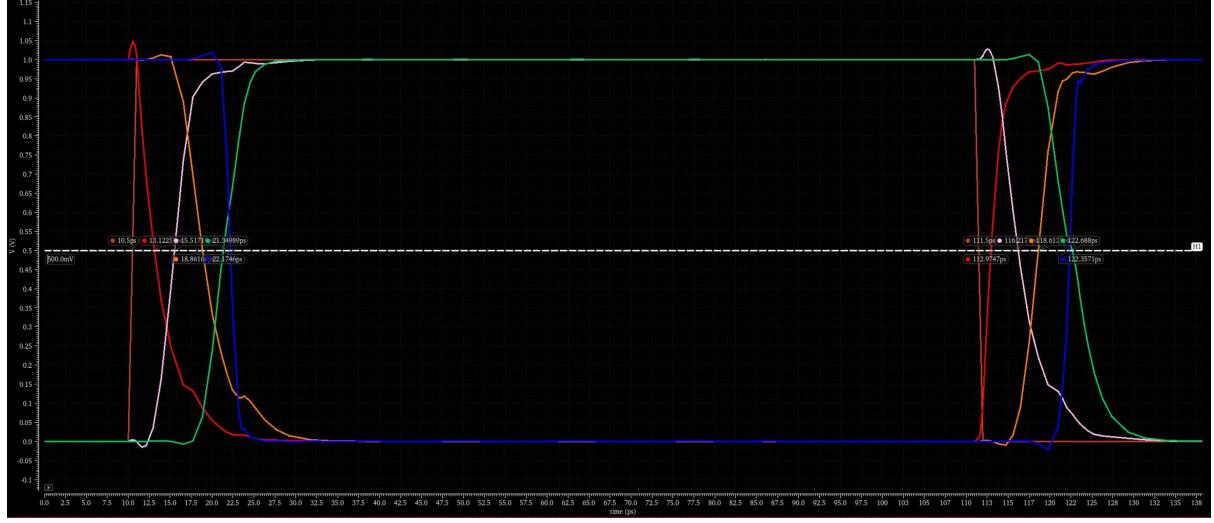


Figure 9: Transient analysis waveform of the circuit shown in Figure 8.

Table 2:  $t_{PHL}$  and  $t_{PLH}$  of inverter number 2, 3, and 4.

Inverter	$t_{PHL}$ (ps)	$t_{PLH}$ (ps)
2	3.27	2.39
3	3.34	2.37
4	4.11	2.49

## Find the gate capacitance $C_g$

We use the circuit shown in Figure 10 to find the gate capacitance  $C_g$  of our MOSFETs. To do this we add on the top a inverter sized the same as inverter number 3. This new inverter drives a capacitor with a capacitance  $C_{delay}$  instead of another inverter with fan-out of 4. By adjusting the capacitance of the capacitor, we aim to match the waveform of  $OUT\_CG$  and  $OUT3$  such that they have same propagation delay. We can then claim  $C_{delay}$  equals to the total gate capacitance  $C_G$  of the load (inverter number 4),  $C_g$ , which is the gate capacitance per unit width, can be then calculated by dividing  $C_{delay}$  by the width sizing of inverter number 4.

Figure 11 shows the simulation waveform. It is found that when  $C_{delay}$  equals to  $11.25 \text{ fF}$ , the propagation delay of the two inverters match with each other. Thus,  $C_G = C_{delay} = C_g W = 11.25 \text{ fF}$ . Considering the sizing of inverter number 4, its NMOS has 64 fins and its PMOS has 128 fins. Each fin accounts for  $68 \text{ nm}$ , then the total width  $W = (64 + 128) \times 68 \text{ nm} = 13 \mu\text{m}$ . Therefore,  $C_g = 11.25/13 = 0.865 \text{ fF}/\mu\text{m}$ .

## Find the effective parasitic capacitance $C_{eff}$

We have replaced inverter number 4 and 5 in Figure 10 with an NMOS with  $W = 40$  in Figure 12 in order to find the effective parasitic capacitance  $C_{eff}$ . Using the same method as when we were investigating  $C_g$ , we adjust the value of  $C_{delay}$  such that it

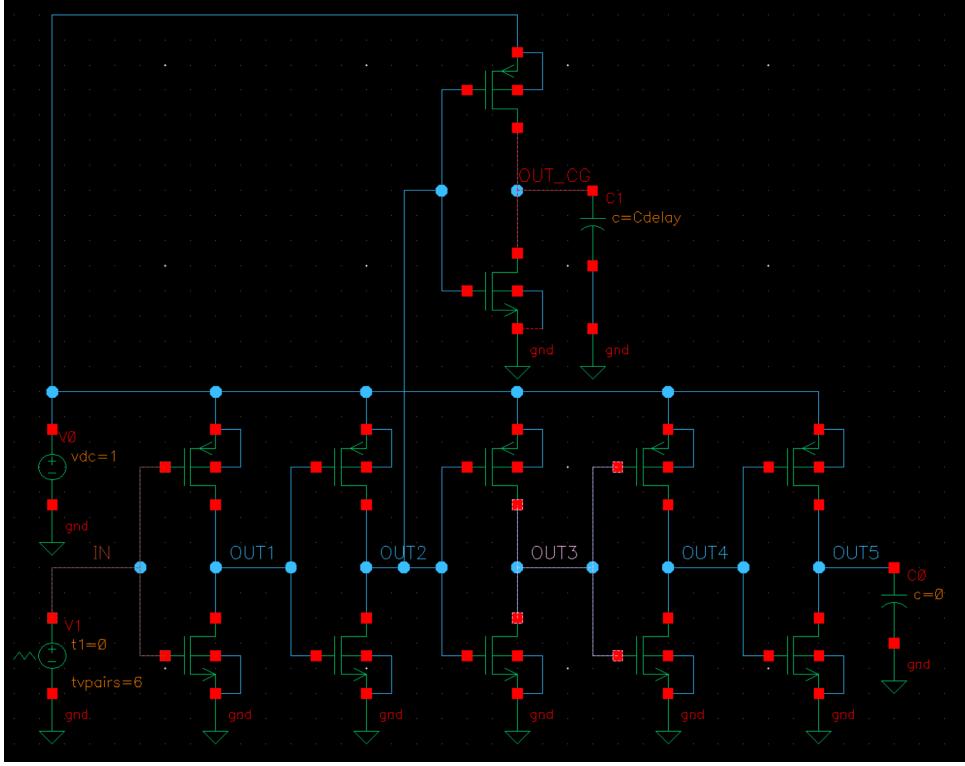


Figure 10: Circuit used to find the gate capacitance  $C_g$  of our MOSFETs.

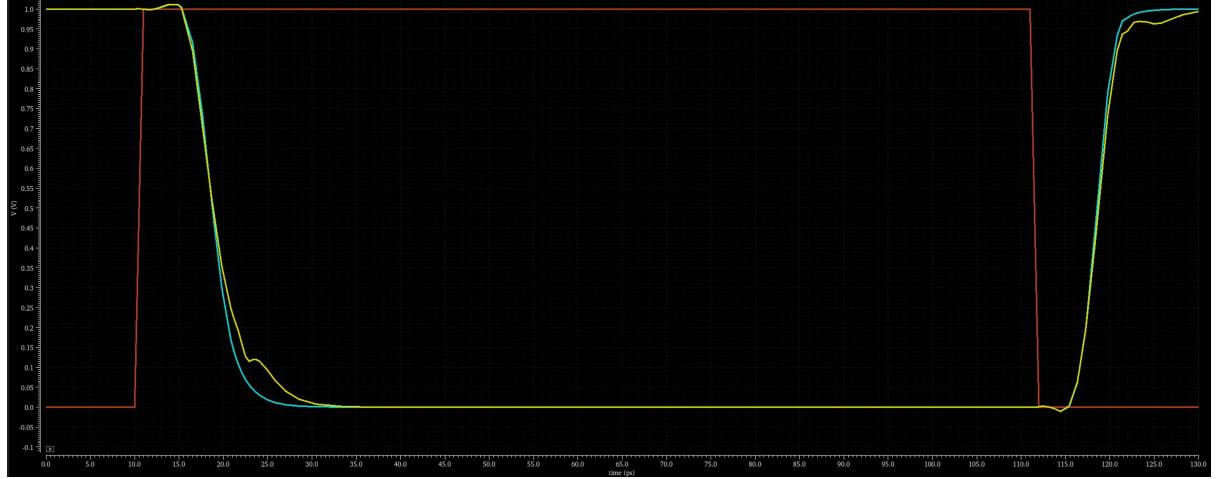


Figure 11: Transient analysis waveform of the circuit shown in Figure 10.  $OUT\_CG$  is the blue curve and  $OUT3$  is the yellow curve.

equals to  $C_{self} = C_{eff}W$  of the NMOS.

Figure 13 shows the simulation waveform. It is found that when  $C_{delay}$  equals to  $1 \text{ fF}$ , the propagation delay of the  $OUT3$  and  $OUT\_CG$  match with each other. Thus,  $C_{self} = C_{delay} = C_{eff}W = 1 \text{ fF}$ . Considering the sizing of the NMOS, it has 40 fins, then the total width  $W = 40 \times 68 \text{ nm} = 2.72 \mu\text{m}$ . Therefore,  $C_{eff} = 1/2.72 = 0.368 \text{ fF}/\mu\text{m}$ .

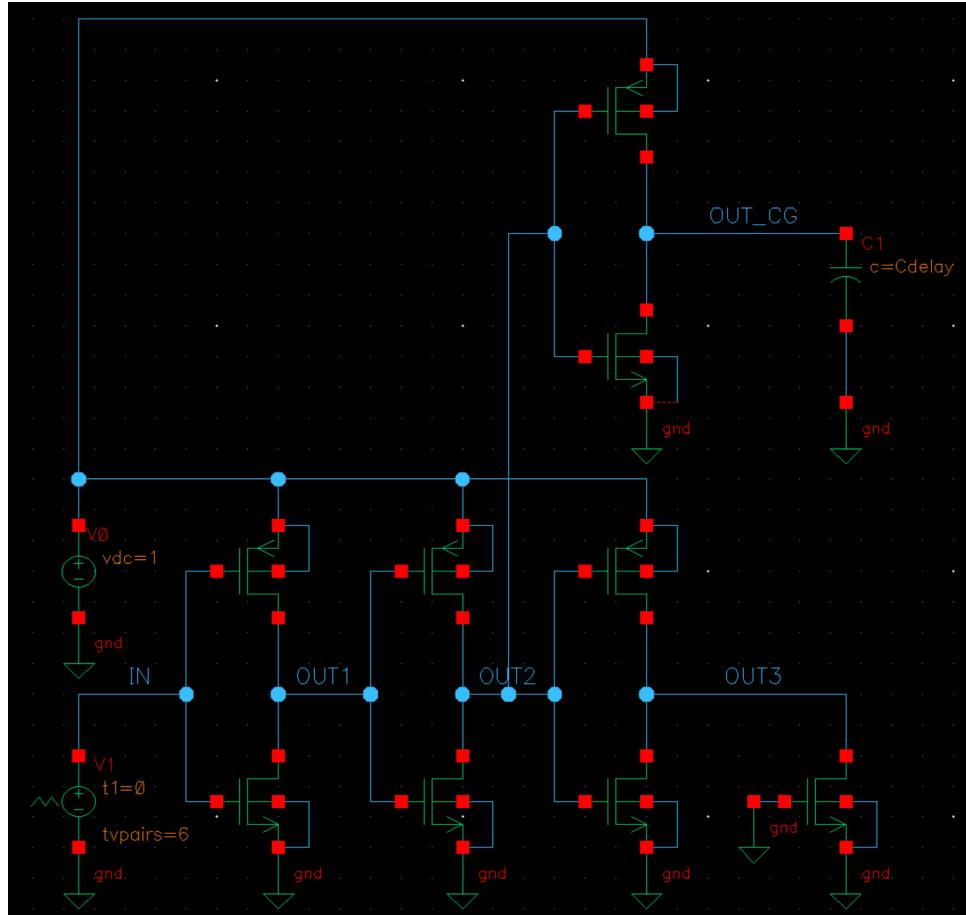


Figure 12: Circuit used to find the effective parasitic capacitance  $C_{eff}$  of our MOSFETs.



Figure 13: Transient analysis waveform of the circuit shown in Figure 12.  $OUT\_CG$  is the blue curve and  $OUT3$  is the yellow curve. They are close to overlapping with each other.

## Question 6

$$t_{pdr} = 0.5R_p(12C_g + 3C_{eff}) = 2.37 \text{ ps}$$

$$t_{pdr} = R_n(12C_g + 3C_{eff}) = 3.05 \text{ ps}$$

$$t_{pd} = (t_{pdr} + t_{pdr})\sqrt{2} = 2.71 \text{ ps}$$