Bruce Xi

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Education

The University of British Columbia **Vancouver, BC**

Master of Engineering in Electrical and Computer Engineering, GPA 4.0 *2021–Present*

- Relevant courses: Digital/Microcomputer System Design, Computer Architecture, VLSI, IC Testing and Reliability, DNN Accelerator, Machine Learning

Imperial College London **London, UK**

Bachelor of Engineering in Materials Science and Engineering, First-Class Honours Degree *2018–2021*

- Obtained Dean's List for three consecutive years (2018-2021)

Experience

Motorola Solutions **Vancouver, BC**

Design Validation Co-op *May-Dec. 2022*

- Conducted extensive surveillance camera tests, validating the cameras' electrical, mechanical, and optical performance
- Engineered Python-based software for test automation and data analysis, enhancing test efficiency with up to 90% automation
- Utilized FFmpeg for video processing and analysis
- Collaborated within a team using Git, GitHub, Confluence, and Jira to optimize workflow efficiency

Project

AXI Stream Header Insertion **Feb. 2024**

- Designed a Verilog RTL module for inserting headers into network packets, adhering to the AXI Stream protocol. The module receives headers and data packets from two master interfaces and sends them to one slave after processing and arbitration
- Implemented pipelining for both data and handshake signals, incorporating skid buffers to eliminate bubbles and efficiently manage backpressure

Computer Architecture Simulator **Sept.-Dec. 2023**

- Optimized matrix multiplication in C by leveraging tiling and loop reordering techniques, altering memory access patterns and increasing cache hit rate by a factor of 8
- Developed four cache replacement policies and two branch prediction algorithms in C++ in the ChampSim simulator

Microcomputer System Development **Jan.-Apr. 2023**

- Engineered key components of a microcomputer system including a 4-way set-associative cache and a DRAM controller using Verilog. The cache reduced the runtime of a benchmark by 43%
- Implemented the system on an Altera FPGA with a soft core provided by the course
- Developed software and firmware in C that interacted with hardware (Flash, EEPROM, and ADC/DAC) using SPI, IIC, and CAN protocol
- Utilized hardware timer interrupt and designed a snake game software that ran on the system and interact with the player using VGA

CPU Design and Assembly programming **June-Sept. 2022**

- Architected a 16-bit RISC CPU from the ground up using Verilog, integrating pivotal components such as FSM, datapath, RAM, and I/O interfaces. The CPU was implemented on an Altera FPGA
- The CPU supported 13 diverse instructions encompassing ALU operations, memory access, and branching mechanisms
- Implemented preemptive multitasking on an ARM core integrated on the FPGA using ARM Assembly

FPGA SoC Design **Jan.-Apr. 2022**

- Developed a comprehensive SoC on FPGA using Quartus, incorporating a Nios II soft processor, on-chip RAM, and custom IP cores, managed via an Avalon memory-mapped interface
- Designed and synthesized custom IP cores in Verilog for functionalities like image data processing, arithmetic acceleration and VGA output
- Created embedded software in C to perform system tasks such as performance benchmarking and control over VGA display

Skills

Hardware: Verilog, FPGA, ModelSim, Quartus, Cadence

Software: Python > C > ARM Assembly = C++, Linux

SoC design: Familiar with concepts of cache coherency, DVFS, DFT, ATPG, P&R from courses