Bruce (Shidi) Xi

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Education

The University of British Columbia **Vancouver, BC**
Master of Engineering in Electrical and Computer Engineering, GPA 4.0 *2021–2024*
- Relevant courses: Deep Learning, ML Hardware Accelerator, Computer Architecture, Digital System Design, Embedded System, VLSI, IC Testing and Reliability

Imperial College London **London, UK**
Bachelor of Engineering in Materials Science and Engineering *2018–2021*
- Graduated with First-Class Honours
- Obtained Dean's List for three consecutive years (2018-2021)

Experience

Motorola Solutions **Vancouver, BC**
Design Validation Co-op *May-Dec. 2022*
- Orchestrated a comprehensive range of camera tests, ensuring precision both in lab settings and office environments
- Developed Python-based software, realizing test automation and data analysis, resulting in a significant enhancement in test efficiency. Some tests achieved automation of up to 90%
- Collaborated effectively within a team framework, leveraging tools like Git, Confluence, and Jira for optimal workflow management

Project

Multi-agent Deep Reinforcement Learning for VLSI Routing **May-Oct. 2023**
- Demonstrated initiative by independently mastering DRL and VLSI global routing through exhaustive self-study and comprehensive literature review
- Successfully modeled and implemented the physical routing problem in Python
- Designed an innovative multi-agent DRL model to address the routing challenge, leveraging the sophisticated capabilities of Python libraries

Embedded System Design **Jan.-Apr. 2023**
- Designed key components of an embedded system including a 4-way set-associative cache controller and a DRAM controller using Verilog. The cache reduced the runtime of a benchmark by 43%
- Implemented the system on an FPGA with a provided soft microcontroller
- Developed software and firmware in C that interacted with hardware using SPI, IIC, and CAN protocol
- Utilized hardware timer interrupt and designed a snake game software that ran on the embedded system

CPU Architecture Design **June-Sept. 2022**
- Architected and crafted a 16-bit RISC CPU from the ground up using Verilog, integrating pivotal components such as FSM, datapath, RAM, and I/O interfaces
- The CPU supported 13 diverse instructions encompassing ALU operations, memory access, and branching mechanisms
- Successfully deployed the system onto an FPGA and validated the design's capabilities by executing a test program

FPGA SOC Study **Jan.-Apr. 2023**
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- yoyo

Skills

Hardware: Verilog, Assembly, FPGA, ModelSim, Quartus, Cadence

Software: Python, C, Linux, Deep Learning, Reinforcement Learning

DevOps Tools: Confluence, Jira, Git, GitHub