

Bruce Xi

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Education

The University of British Columbia

Vancouver, BC

Master of Engineering in Electrical and Computer Engineering, GPA 4.0

2021–Present

- Relevant courses: Digital/Microcomputer System Design, Computer Architecture, VLSI, High-speed Data Link, IC Testing and DFT, DNN Accelerator, Deep Learning

Imperial College London

London, UK

Bachelor of Engineering in Materials Science and Engineering, First-Class Honours Degree

2018–2021

- Obtained Dean's List for three consecutive years (2018–2021)

Project

AMBA AXI Stream Header Insertion Module Design and Verification

Feb.–Mar. 2024

- Designed an RTL module using Verilog to insert headers into network data packets. This module transfers data following the AXI Stream protocol, accepting data and headers from two master interfaces. It removes invalid bytes from both input signals based on the keep signal (packing), merges the remaining valid bytes, sends them to a slave interface, and outputs the corresponding keep and last signals.
- Used pipelining for data and handshake signals, and equipped skid buffers to handle backpressure, eliminate bubbles in the pipeline, and optimize throughput.
- Verified the module using constrained-random stimuli and SystemVerilog assertions to ensure data correctness.

Microcomputer System Development

Jan.–Apr. 2023

- Developed critical components for a microcomputer system capable of operating at 45 MHz on an Altera FPGA. Implemented an 8-way set associative cache using SRAM on the FPGA, and designed a segment of the cache controller featuring a Tree PLRU replacement policy using Verilog. Also designed components of a DRAM controller using Verilog.
- Wrote embedded C drivers to manage a soft Motorola 68000 microprocessor for communications via SPI protocol with a Flash, and via IIC protocol with a EEPROM and an ADC/DAC PCB.
- Leveraged hardware timer interrupts to create a snake game in C, which was playable on the system and utilized VGA for user interaction.

Design of a 10 Gbps Differential SerDes Data Link with TX FIR Equalization

Jan.–May 2024

- Designed a 10 Gbps differential SerDes data link using Cadence Virtuoso in 45 nm technology, incorporating a TX, a differential channel, and an RX. Performed circuit simulations using Spectre, achieving a power consumption of 9 mW, an eye-opening of 47 mV under the worst-case data pattern, and zero errors with both worst-case and PRBS7 input over 10,000 UIs.
- Characterized channel impulse and pulse responses using MATLAB, determining the worst-case data pattern and computing tap values for 2-tap FIR equalization.
- Developed the TX with a 4:1 serializer based on a 5-latch-2:1 multiplexer topology with half-rate clocking, requiring 5 GHz clock frequency at max. Pre-drivers are designed as inverter chains optimized using logical effort. Implemented a high-swing, voltage-mode driver segmented into 10 parts to provide a tunable impedance of $50\Omega \pm 30\%$ and configured to pre-emphasize the signal, functioning as an FIR equalizer to suppress ISI.
- Implemented the RX with 1:4 deserialization at 2.5 GHz using four slicers followed by synchronizers. Each slicer integrates a track-and-hold switch executed as a transmission gate, a StrongArm latch, and an SR latch.

FPGA SoC Design

Jan.–Apr. 2022

- Developed a comprehensive SoC using Quartus, incorporating a Nios II soft processor, on-chip RAM, and custom IP cores, managed via Avalon memory-mapped interface. Simulated and verified the SoC and emulated it on an Altera FPGA.
- Designed and synthesized custom IP blocks in Verilog for functionalities like image data processing, arithmetic acceleration and VGA output, integrated IP blocks into the system.
- Created software in C to perform system tasks such as performance benchmarking and control over VGA display.

Work Experience

Motorola Solutions

Vancouver, BC

Design Validation Co-op

May–Dec. 2022

- Conducted extensive electrical, mechanical, and optical tests on surveillance cameras.
- Proposed reflections and innovations on existing testing processes, self-taught Python programming, and wrote software for test automation and data analysis. Reduced repetitive manual labor within the team, improving work efficiency. Automation of some tests reached up to 90%.
- Collaborated within a team using Git, GitHub, Confluence, and Jira to optimize workflow efficiency.

Skills

Hardware: Verilog, SystemVerilog, Altera FPGA, ModelSim, Quartus, Cadence Virtuoso

Software: Python > C > ARM Assembly = C++, Linux, MATLAB