Bruce Xi

(236)-777-8218 • brucexi99@outlook.com • bruce-shidi-xi • brucexi999

Education

The University of British Columbia **Vancouver, BC**

Master of Engineering in Electrical and Computer Engineering, GPA 4.0 *2021–2024*

- Relevant courses: Digital/Microcomputer System Design, Computer Architecture, VLSI, High-speed Data Link, IC Testing and DFT, DNN Accelerator, Signals and Systems, Circuit Analysis, Deep Learning

Imperial College London **London, UK**

Bachelor of Engineering in Materials Science and Engineering, First-Class Honours Degree *2018–2021*

- Obtained Dean's List for three consecutive years (2018-2021)

Work Experience

Motorola Solutions **Vancouver, BC**

Design Validation Co-op *May-Dec. 2022*

- Conducted electrical and optical testing on surveillance cameras by following a standard workflow, documented results, and managed issues using Confluence and Jira.
- Analyzed test results to identify performance trends and quality issues, showcasing strong analytical skills and meticulous attention to detail, leading to early detection of potential defects and reducing post-production errors.
- Proposed improvements and innovations in existing testing procedures, self-taught Python programming to develop software for test automation and data analysis, utilizing OOP to create modular, reusable scripts. Successfully reduced repetitive manual tasks, increasing team efficiency by automating tests up to 90%, demonstrating strong problem-solving and debugging skills.
- Collaborated with electrical and firmware teams to identify and resolve hardware and software issues, showcasing teamwork and communication skills.

Projects

AMBA AXI Stream Header Insertion IP Design and Verification **Feb.-Apr. 2024**

- Designed an RTL IP using Verilog to insert headers into network data packets. This IP transfers data following the AXI Stream protocol, accepting packets and headers from two input interfaces. It removes invalid bytes from both input data based on the keep signals (packing), merges the remaining valid bytes, sends the processed data to the output ports, and outputs the corresponding keep and last signals.
- Used pipelining for data and handshake signals, and equipped skid buffers to handle backpressure, eliminate bubbles in the pipeline, and optimize throughput.
- Verified the IP using constrained-random testing in SystemVerilog to ensure data correctness.

Design of a 10 Gbps Differential SerDes Data Link with TX FIR Equalization **Jan.-May 2024**

- Designed a 10 Gbps differential SerDes data link using Cadence Virtuoso in 45 nm technology, including a TX, differential channel, and RX. Achieved 9 mW power consumption, 47 mV eye-opening under worst-case data pattern, and zero errors with both worst-case and PRBS7 input over 10,000 UIs.
- Characterized channel responses using MATLAB, determined worst-case data pattern and the tap values for 2-tap FIR equalization.
- Developed a 4:1 serializer TX with a 5 GHz clock, featuring a high-swing, voltage-mode driver with tunable impedance and pre-emphasis FIR equalization for transmission line impedance matching and ISI suppression respectively.
- Implemented a 1:4 deserialization RX at 2.5 GHz using slicers with track-and-hold switches, StrongArm latches, and SR latches.

Microcomputer System Development **Jan.-Apr. 2023**

- Developed critical components for a microcomputer system capable of operating at 45 MHz on an Altera FPGA. Implemented an 8-way set associative cache using SRAM on the FPGA, and designed a segment of the cache controller featuring a Tree PLRU replacement policy using Verilog. Also designed components of a DRAM controller using Verilog.
- Wrote embedded C drivers to manage a soft Motorola 68000 microprocessor for communications via SPI protocol with a Flash, and via IIC protocol with a EEPROM and an ADC/DAC PCB.
- Leveraged hardware timer interrupts to create a snake game in C, which was playable on the system.

FPGA SoC Design **Jan.-Apr. 2022**

- Developed a System-on-Chip running at 50 MHz on an Altera FPGA using Quartus IP and Verilog, integrating a Nios II soft processor, on-chip RAM, VGA core, JTAG UART core for host PC communication, and custom IPs. Utilized the Avalon Memory-Mapped Interface for module communication.
- Designed and implemented custom IPs, including counters, state machines, and Avalon interfaces. Conducted simulations of individual IPs and the complete system using ModelSim to verify functionality.
- Created embedded software in C to interact with system modules via memory-mapped addresses, enabling data read/write operations with IPs and performing arithmetic operations on the CPU.

Skills

Hardware: Verilog, SystemVerilog, Altera FPGA, ModelSim, Quartus, Cadence Virtuoso

Software: Python, OOP, C, ARM Assembly, Linux, MATLAB