The Cell Processor Computer Vision Project

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The Cell Broadband Engine Processor Overview

- The CBEA extends the 64-bit PowerPC Architecture
- The PPE contains a 64-bit dual-thread PowerPC Architecture RISC core
- The eight SPE are single-instruction, multiple-data processor elements, with their own Local Storage
- The Element Interconnect Bus connects PPE and SPES and consists of four 16byte-wide data rings

PPE - PowerPC Processor Element

- General-purpose, dual-threaded 64-bit RISC processor conforming to the PowerPC Architecture, version 2.02
- Vector/SIMD multimedia extension instructions
- Vector/SIMD Multimedia Extension C/C++ Language Intrinsics
- Specialized for running 32-bit and 64-bit operating systems

SPE - Synergistic Processor Elements

- SIMD istruction set
- Each SPE is a 128-bit RISC processor
- specialized (optimized) for data-rich, compute-intensive SIMD and scalar applications

Synergistic Processor Unit

- 256 KB Local Store with unified instructions and data
- independent processor element with its own program counter
- SPU fills the Local Storage with DMA transfers from its MFC
- SPU fetches and executes instructions from its LS

Memory Flow Controller

- Each SPU has its own MFC
- SPE communicates with main memory, PPE and other SPEs through its channels
- Channels are message-passing interfaces
- Mailboxes and Signalling
- MFC Commands and Command Queues

The Project

- C/C++ computer vision project
- parallel elaboration of image sequences, either acquired in real time by some dedicated hardware or by reading disk files
- thought for the STI Cell Processor
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Project Architecture

- The PPE splits the input images in vertical bands
- Each subimage is then mapped onto the SPE Synergistic Processing Elements' embedded SRAM through opportune MFC Memory Flow Controller commands
- Each SPE analyzes with computer vision algorithms its own subimage
- The SPEs work in parallel on the subimages and return to the PPE a list of bounding boxes (regions of interest)
- The processed output subimages modified by the SPEs are mapped back to the main memory
- Subimages are joined into a single output image by the PPE
- The PPE collects also the list of boxes and tracks over time their output image location evolution

The speedup

- For each Cell core there are eight physical SPEs
- for compute-intensive computer vision algorithms, a speedup is obtained
- The so achieved parallelism can reduce sensibly the total time of an image elaboration
- statistical measure of the speedup

CellCV Project Requirements

- A computer mounting the Cell Processor (i.e. Sony PlayStation3)
- An installed Linux distribution (i.e. YellowDog 5.0 for PS3)
- Cell SDK at least 2.0

CellCV Components

- The subimage module for splitting and joining images
- The main loop module
- The profiler module for statistical timing observations
- The libpng wrapper module
- The ImageAcquisition module
- The GlutWindow class
- The SPU CV algorithm module

CellCV Project Conclusions

- The Cell Architecture grew from a challenge posed by Sony and Toshiba and IBM
- Power-efficient and cost-effective high-performance processing for a wide range of applications
- Innovative solution whose design was based on the analysis of a broad range of workloads in areas such as cryptography, graphics transform and lighting, physics, fast-Fourier transforms (FFT), matrix operations, and scientific workloads
- CBEA is ideal for compute-intensive computer vision algorithms