

1. Description

1.1. Project

Project Name	VCU
Board Name	NUCLEO-F401RE
Generated with:	STM32CubeMX 6.14.0
Date	04/25/2025

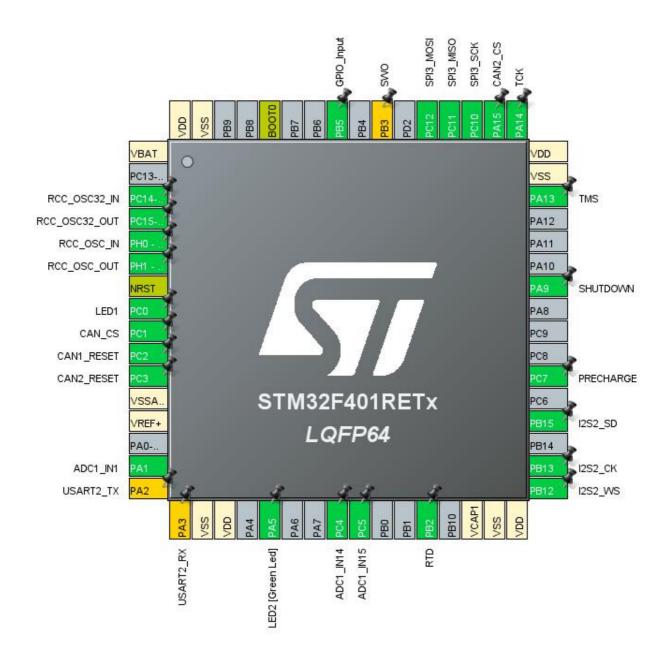
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F401
MCU name	STM32F401RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

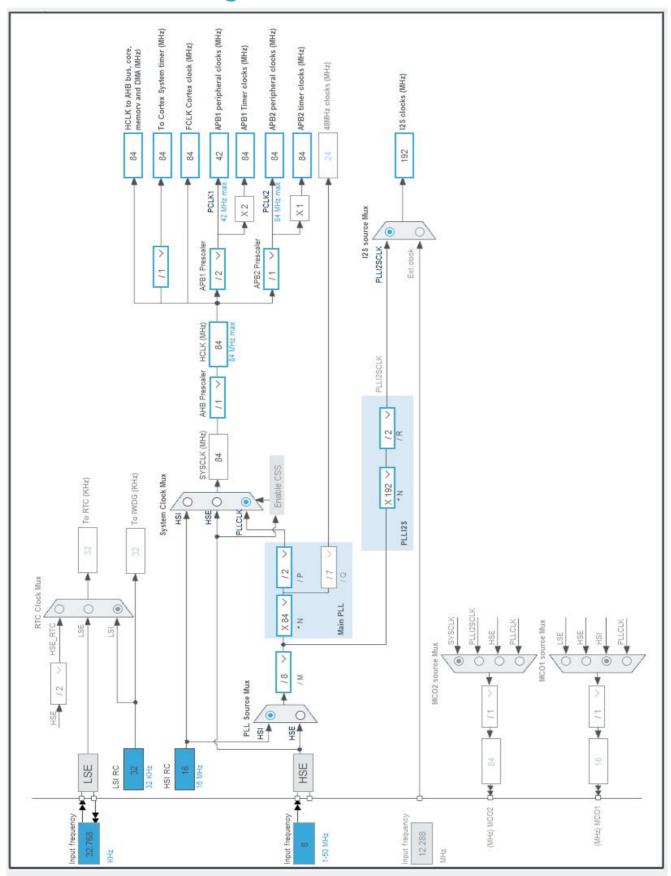
Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP64	(function after		Function(s)	
	reset)			
1	VBAT	Power		
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Output	LED1
9	PC1 *	I/O	GPIO_Output	CAN_CS
10	PC2 *	I/O	GPIO_Output	CAN1_RESET
11	PC3 *	I/O	GPIO_Output	CAN2_RESET
12	VSSA/VREF-	Power		
13	VREF+	Power		
15	PA1	I/O	ADC1_IN1	
16	PA2 **	I/O	USART2_TX	
17	PA3 **	I/O	USART2_RX	
18	VSS	Power		
19	VDD	Power		
21	PA5 *	I/O	GPIO_Output	LED2 [Green Led]
24	PC4	I/O	ADC1_IN14	
25	PC5	I/O	ADC1_IN15	
28	PB2 *	I/O	GPIO_Input	RTD
30	VCAP1	Power		
31	VSS	Power		
32	VDD	Power		
33	PB12	I/O	12S2_WS	
34	PB13	I/O	12S2_CK	
36	PB15	I/O	12S2_SD	
38	PC7 *	I/O	GPIO_Input	PRECHARGE
42	PA9 *	I/O	GPIO_Input	SHUTDOWN
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
50	PA15 *	I/O	GPIO_Output	CAN2_CS
51	PC10	I/O	SPI3_SCK	
52	PC11	I/O	SPI3_MISO	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
53	PC12	I/O	SPI3_MOSI	
55	PB3 **	I/O	SYS_JTDO-SWO	SWO
57	PB5 *	I/O	GPIO_Input	
60	воото	Boot		
63	VSS	Power		
64	VDD	Power		

^{*} The pin is affected with an I/O function

^{**} The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



Page 5

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F401
MCU	STM32F401RETx
Datasheet	DS10086_Rev3

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

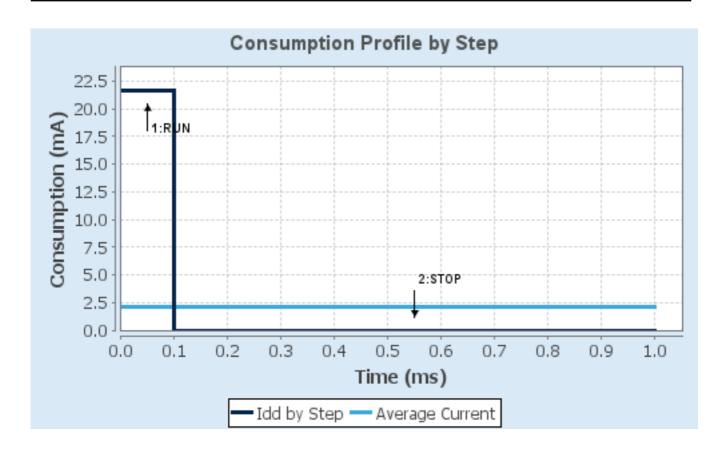
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale2-Medium	No Scale
Fetch Type	FLASH/ART/PREFETCH	n/a
CPU Frequency	84 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash- PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	21.6 mA	10 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	105.0	0.0
Ta Max	101.44	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	2.17 mA
Battery Life	2 months, 4 days,	Average DMIPS	105.0 DMIPS
	8 hours	_	

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	VCU
Project Folder	C:\Users\antho\STM32CubeIDE\workspace_1.17.0\VCU
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_TIM3_Init	TIM3
6	MX_SPI3_Init	SPI3
7	MX_I2S2_Init	12\$2

3. Peripherals and Middlewares Configuration

3.1. ADC1 mode: IN1 mode: IN14 mode: IN15

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment

Scan Conversion Mode

Continuous Conversion Mode

Disabled

Discontinuous Conversion Mode

Disabled

DMA Continuous Requests

Disabled

End Of Conversion Selection EOC flag at the end of all conversions *

ADC_Regular_ConversionMode:

Number Of Conversion 3 *

External Trigger Conversion Source Timer 3 Trigger Out event *

External Trigger Conversion Edge Trigger detection on the rising edge

Rank 1

Channel Channel 1

Sampling Time 480 Cycles *

<u>Rank</u> **2** *

Channel 14 *
Sampling Time 480 Cycles *

<u>Rank</u> 3 *

Channel 15 *
Sampling Time 480 Cycles *

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

3.2. I2S2

Mode: Half-Duplex Master

3.2.1. Parameter Settings:

Generic Parameters:

Transmission Mode Master Transmit

Communication Standard I2S Philips

Data and Frame Format 16 Bits Data on 16 Bits Frame

Selected Audio Frequency 44 KHz *

Real Audio Frequency 44.117 KHz *

Error between Selected and Real 0.26 % *

Clock Parameters:

Clock Source I2S PLL Clock

Clock Polarity Low

3.3. RCC

High Speed Clock (HSE): BYPASS Clock Source Low Speed Clock (LSE): Crystal/Ceramic Resonator

3.3.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 2

3.4. SPI3

Mode: Full-Duplex Master

3.4.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 8 *

Clock Polarity (CPOL) Low

Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled
NSS Signal Type Software

3.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

3.6. TIM3

Clock Source: Internal Clock

3.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 4 *
Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 10001 *

Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Enable (Trigger delayed for master/slaves simultaneous start)

*

Trigger Event Selection Update Event *

* User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
7.50	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	
12\$2	PB12	12S2_WS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	I2S2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	12S2_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	TCK
Single Mapped	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
Signals	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB3	SYS_JTDO- SWO	n/a	n/a	n/a	SWO
GPIO	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PC1	GPIO_Output	Output Push Pull	Pull-up *	Very High *	CAN_CS
	PC2	GPIO_Output	Output Push Pull	Pull-up *	Low	CAN1_RESET
	PC3	GPIO_Output	Output Push Pull	Pull-up *	Low	CAN2_RESET

VCU Project Configuration Report

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2 [Green Led]
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	RTD
	PC7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PRECHARGE
	PA9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SHUTDOWN
	PA15	GPIO_Output	Output Push Pull	Pull-up *	Very High	CAN2_CS
					*	
	PB5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

4.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Very High *
SPI2_TX	DMA1_Stream4	Memory To Peripheral	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Word *
Memory Data Width: Word *

SPI2_TX: DMA1_Stream4 DMA request Settings:

Mode: Normal

Use fifo: Enable *

FIFO Threshold: Half Full *

Peripheral Increment: Disable

Memory Increment: Enable *

Peripheral Data Width: Half Word *

Memory Data Width: Half Word *

Peripheral Burst Size: Single Memory Burst Size: Single

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
DMA1 stream4 global interrupt	true	0	0	
ADC1 global interrupt	true	0	0	
TIM3 global interrupt	true	0	0	
DMA2 stream0 global interrupt	true	0	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
SPI2 global interrupt		unused		
SPI3 global interrupt	unused			
FPU global interrupt	unused			

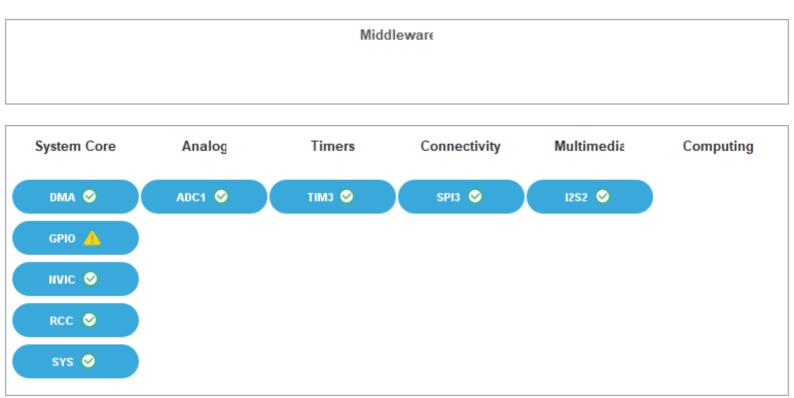
4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream4 global interrupt	false	true	true
ADC1 global interrupt	false	true	true
TIM3 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true

* User modified value

5. System Views

- 5.1. Category view
- 5.1.1. Current



6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f401_bsdl.zip https://www.st.com/resource/en/ibis_model/stm32f401_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f4-svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_embedded_software_solutions.pdf

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tools_portfolio.pdf

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onal-safety-packages.pdf

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guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf

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microcontroller-system-memory-boot-mode-stmicroelectronics.pdf

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stm32-mcus-a-consistent-832bit-product-line-for-painless-migration-

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Application Notes https://www.st.com/resource/en/application_note/an3070-managing-the-

- driver-enable-signal-for-rs485-and-iolink-communications-with-the-stm32s-usart-stmicroelectronics.pdf
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- interconnections-on-stm32f401-and-stm32f411-linesstmicroelectronics.pdf
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