Coding- and Energy-Efficient FME Hardware Design

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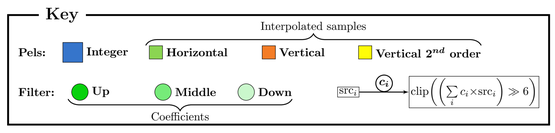
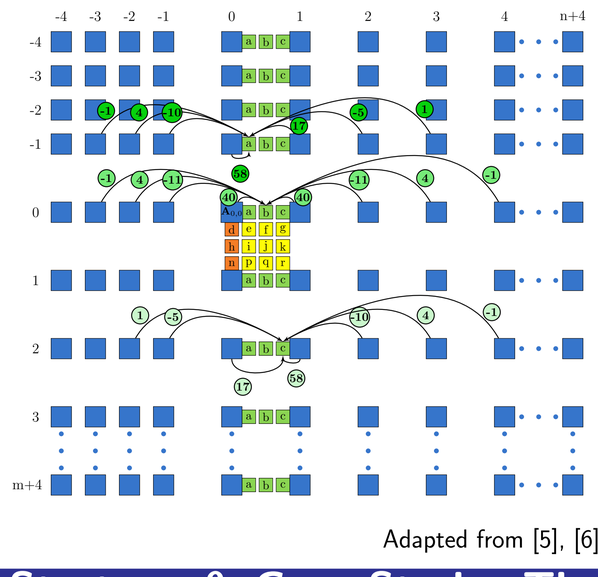
1. Introduction & Definitions

- In 2016, 73% of all Internet traffic was video [1]
- Thus there is a need for ever higher compression
- High Efficiency Video Coding (HEVC) [2] improves ∼50% the coding efficiency over its predecessor
  - But at a huge cost in computational complexity [3]
- Fractional Motion Estimation (FME) is responsible for up to $\mathbf{33.88\%}$ of inter prediction time in HEVC Model [4]
  - $\mathbf{46.9\%}$ of FME time is spent interpolating pixels
  - $\mathbf{53.1\%}$ is spent doing block matching





Adapted from [5], [6].

- Block Matching Algorithm (BMA) [7]:

$$\boldsymbol{B}^{\text{ref}} = \underset{\boldsymbol{B}^{\text{can}} \in \boldsymbol{S}}{\arg\min}\, \boldsymbol{cost}_{m\times n}(\boldsymbol{B}^{\text{ori}}, \boldsymbol{B}^{\text{can}}) \quad (1)$$

- Rate-Distortion Optimization (RDO): Lagrangian rate-distortion cost (j_{cost}) [8] as $\boldsymbol{cost}$:

$$j_{\text{cost}}(\boldsymbol{B}^{\text{ori}}, \boldsymbol{B}^{\text{can}}) = \boldsymbol{distortion}(\boldsymbol{B}^{\text{ori}}, \boldsymbol{B}^{\text{can}}) + \boldsymbol{\lambda} \times \boldsymbol{rate}(\boldsymbol{B}^{\text{ori}}, \boldsymbol{B}^{\text{can}}) \quad (2)$$

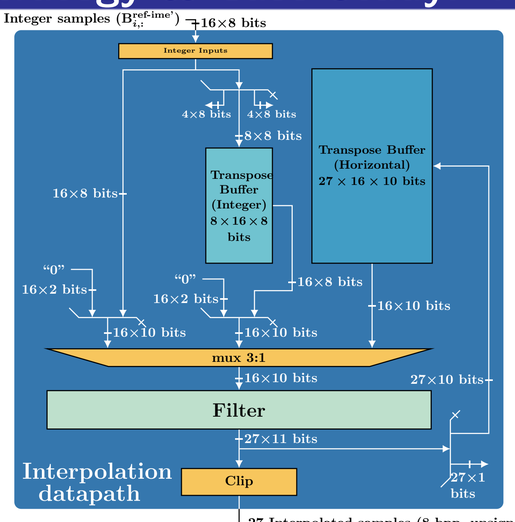
$$\text{sad}_{m\times n}(\boldsymbol{B}^{\text{ori}}, \boldsymbol{B}^{\text{can}}) = \sum_{i=0}^{m-1}\sum_{j=0}^{n-1} |\boldsymbol{d}_{i,j}| \quad (3)$$

2. Proposed Design Strategy & Case Study: The HEVC 8×8 FME

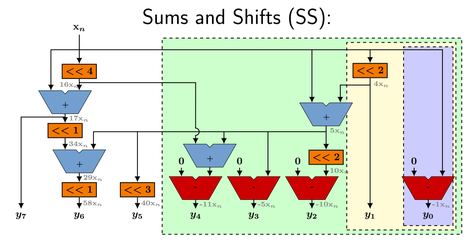
Contributions

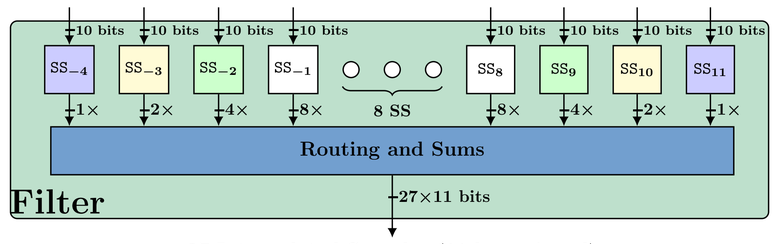
- **Main: Design Strategy!**
  - **Coding-efficient**
  - **Energy-efficient**
- Secondary:
  - Area and Power/Energy Breakdown
- More details in our paper
  - Enjoy open-preview:

- **Memory-Aware**
  - Loads all the required pixels only once
  - Keeps data internally
  - Does transposition internally

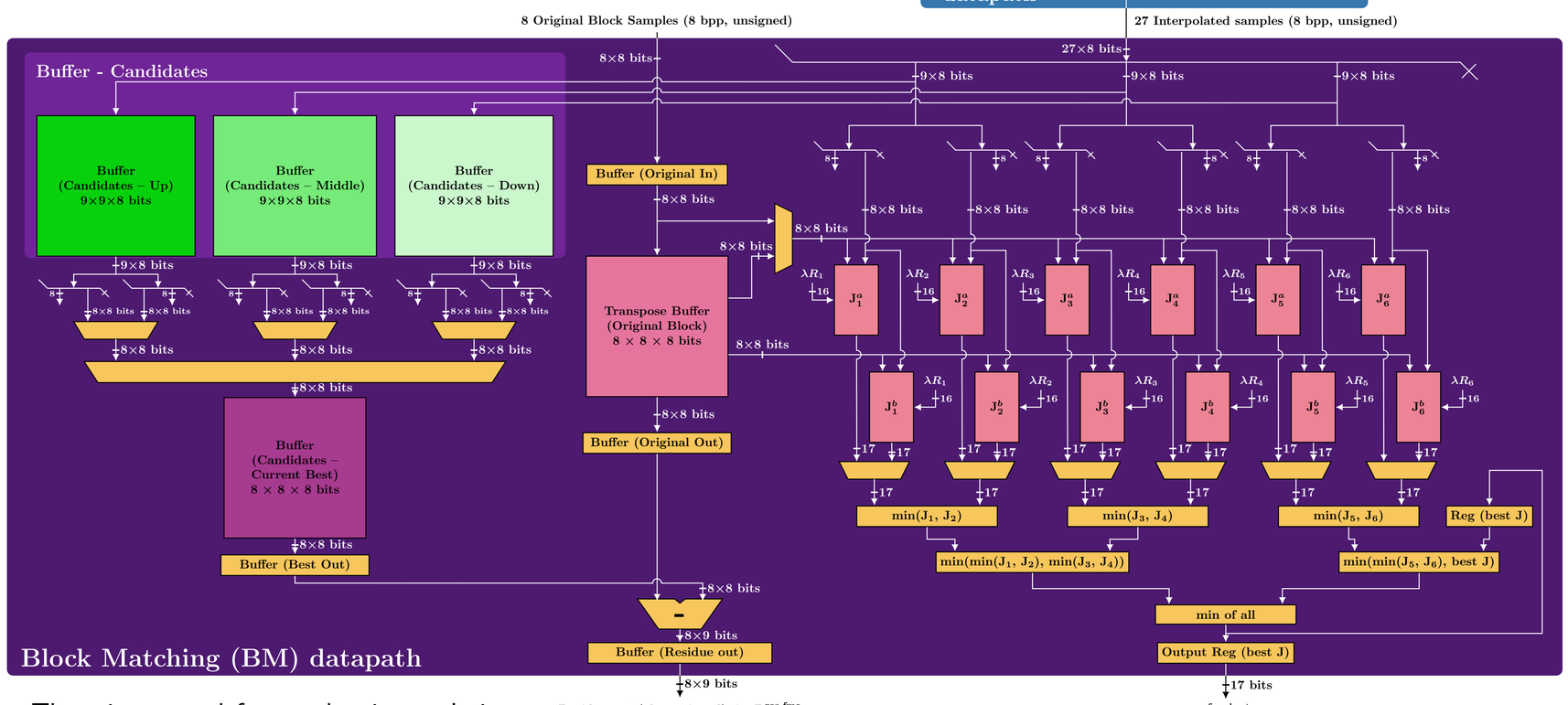


- Using Multiplierless Constant Multiplication (MCM)
- No redundant operations
  - Exploring common sub-expressions





- **Interpolation** and **BMA** integrated in the same hardware
- Using data as soon as possible



- Searching all 48 FME candidates

$$\mathbf{6 + 6 + 3 \times 12}$$

Horizontals+Verticals+Verticals 2^{nd} order

- Leads to a regular dataflow
  - Allows to explore data-level parallelism
- BD-Rate:
  - **-0.37%** (RA)
  - **-0.77%** (LD)

- Using $\boldsymbol{\lambda} \times$ rate (j_{cost})
  - **-1.43%** (RA)
  - **-0.86%** (LD)

- There is no need for another interpolation:

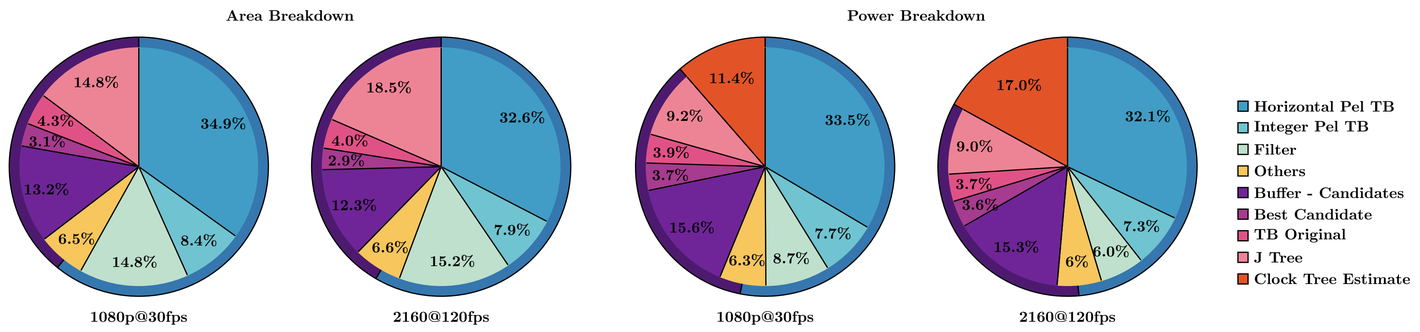
3. Area and Power Evaluation

- The case study architecture was synthesized with Synopsys® Design Compiler (DC®) [9]

Synthesis results for TSMC 45 nm @ 0.9 V standard cell library [10]

Target	1080@30fps	2160@30fps	2160@60fps	2160@120fps*
Period (ns)	20	5	2.5	1.25
Area (μm^2)	93738.3	93826.5	94439.1	100733.4
Dynamic (mW)	3.05	10.78	21.21	44.04
Static (mW)	0.91	0.91	0.92	1.04
Total (mW)	3.96	11.69	22.13	45.07

* 2160@120fps is equivalent in terms of throughput to 4320@30fps.



- For a fair power comparison with [6], we disregarded the power share of the blocks that are exclusive to our design:
  - Our design consumes **6.4%** and **46.5%** less power than theirs for 2160@60fps and 1080@30fps, respectively
- The work in [6] reports lower power than those in [11]–[14]

4. Conclusions

- The case study hardware architecture is more energy-efficient than state-of-the-art similar ones
- The obtained power and area breakdowns show that buffers are responsible for up to 64% of both area and power
  - The largest one (more than 30% of area and power) is intrinsic of any memory-aware parallel FME architecture
- Future work may address power optimization of buffers through low-power techniques using slower cells.

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