Brunda Marpadaga

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Education

Portland State University, Portland, OR Jan 2024 – Dec 2025 (Ongoing)
Masters in Electrical and Computer Engineering ***GPA: 3.88/4***

- Coursework : Microprocessor System Design, Introduction to SystemVerilog, Computer Architecture, Pre-Silicon Validation, Introduction to Python Scripting, SOC Design with FPGA's, Assertion Based Verification, Embedded Design with FPGA's, Formal Verification of Hw/Sw systems, Emulation And Functional Specification Verification, Post-Silicon Validation

Vasavi College of Engineering, Hyderabad,TS,India Oct. 2020 – Jun 2023
Bachelor of Engineering in Electronics and Communications ***GPA: 3.37/4***

Government Institute of Electronics, Hyderabad,TS,India Jun 2016 – Dec 2019
Special Diploma in Embedded Systems ***GPA: 3.7/4***

Technical Skills

Languages & Scripting: SystemVerilog, C/C++, Python, TCL, Matlab
Assembly Languages: x86, RISC-V, MIPS **Methodologies**: UVM, Agile
Protocols: I2C, Wishbone, UART, SPI
Concepts: Data Structures, Digital Logic Design, System Verilog Assertions, Randomization and Constraints, Environment-based Verification, Coverage-Driven Verification, Code/ Functional Coverage, Scoreboards, OOPS, Static Timing Analysis, DDR Memory, Caches, Cache Coherence, Virtual Memory, MESI, MESIF, Pipelining, Scheduling, Branch Prediction, Formal Verification, XRTL, TBX SCEMI pipes
Tools & EDAs: Questasim, Vivado, MentorGraphics Tanner EDA, Multisim, Keil uVision, PSpice, Siemens Veloce Emulator and Synopsys VCFormal

Projects

Design and Formal Verification of a Sequence Detector FSM for Enhanced Security Applications | *SystemVerilog,*

- Engineered an advanced FSM for binary sequence detection in security systems, ensuring high precision and reliability.
- Utilized Synopsys VC Formal for exhaustive property checking and X-propagation analysis to guarantee correctness across all input sequences.
- Developed and validated a noise-resistant design for enhanced detection accuracy in high-security applications.

Smart Environmental Control System | *C, FreeRTOS* Feb 2025

- Board Bring-up on the Nexys A7 FPGA using MicroBlaze based system. Made use of temperature and humidity (bme280) sensor and light sensor (tsl2561) to monitor and provide feedback through PID control loop so that the outputs (LEDs & Fans) can be controlled to maintain desirable environmental conditions.

TinyALU Testbench Conversion for Siemens Veloce Emulator | *SystemVerilog* Apr 2025 – Jun 2025

- Converted a conventional testbench into an emulator-compatible setup on Veloce, significantly accelerating verification by leveraging parallel hardware emulation using SCEMI pipes, DPI calls & HDL-HVL interfaces.

Design of Pipelined processor for MIPS architecture | *SystemVerilog* Apr 2024 - Jun 2024

- Designed & implemented a 5-stage pipelined processor simulator to model instruction execution using forwarding logic, reducing stall penalties by 90% and optimized execution time through efficient hazard resolution strategies.

Experience

Associate Software Engineer - Prodapt, Hyderabad Jul 2023 – Dec 2023

- Skills : SpringBoot, MongoDB, SQL, OOP, AngularJS, Git, Docker, Agile, Jira, PostMan
- Developed a full-stack web application "Analytics-Dashboard (Telecommunication)" using SpringBoot and MongoDB that presents real-time updation of data being collected in the MongoDB.

Failure Analysis Intern - ECIL, Hyderabad, India May 2019 – Dec 2019

- Collaborated with the manufacturing team to identify failures, analyze schematics, implement corrective actions, and enhance yield rates.The assigned responsibilities covered multiple stages of production line.