Brunda Marpadaga

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Summary

Embedded Firmware Engineer with a strong foundation in real-time systems, bare-metal firmware, and digital hardware design. Skilled in C/C++, RTOS, SystemVerilog, and embedded system design. Passionate about working on low-level systems that push the boundaries of hardware/software co-design.

Education

Portland State University, Portland, OR Jan 2024 – Dec 2025 (Ongoing)
Masters in Electrical and Computer Engineering ***GPA: 3.88/4***

- Coursework : Microprocessor System Design, Introduction to SystemVerilog, Computer Architecture, Pre-Silicon Validation, Introduction to Python Scripting, SOC Design with FPGAs, Assertion Based Verification, Embedded Design with FPGAs, Formal Verification of Hw/Sw systems, Emulation And Functional Specification Verification, Post-Silicon Validation

Vasavi College of Engineering, Hyderabad,TS,India Oct. 2020 – Jun 2023
Bachelor of Engineering in Electronics and Communications ***GPA: 3.37/4***

Government Institute of Electronics, Hyderabad,TS,India Jun 2016 – Dec 2019
Special Diploma in Embedded Systems ***GPA: 3.7/4***

Technical Skills

Languages: SystemVerilog, C/C++, Python, TCL, MATLAB **Methodologies**: UVM, Agile
Architectures & Protocols: RISC-V, MIPS, I2C, Wishbone, UART, SPI **Operating systems**: Linux, freeRTOS
Hardware: Nexys A7-100t, Zynq-7000, Arduino, STM32 **Test Equipment**: Oscilloscope, Logic Analyzer, Multimeter
Development Tools & EDAs: Questasim, Vivado & Vitis, Multisim, Keil uVision, Segger and VCFormal

Projects

Smart Environmental Control System | *C, FreeRTOS* Feb 2025

- Built with MicroBlaze based system on the Nexys A7 FPGA using freeRTOS. Created drivers for temperature & humidity (bme280) sensor & light sensor (tsl2561) to monitor and provide feedback through PID control loop so that the actuator and outputs could be PWM-controlled to maintain desirable environmental conditions.

Design of Pipelined processor for MIPS architecture | *SystemVerilog*

- Designed & implemented a 5-stage pipelined processor simulator to model instruction execution using forwarding logic, reducing stall penalties by 90% and optimized execution time through efficient hazard resolution strategies.

Tiny-ALU Testbench Conversion for Siemens Veloce Emulator | *SystemVerilog*

- Converted a conventional testbench into an FPGA-compatible setup on Veloce, significantly accelerating verification by leveraging parallel hardware emulation using SCEMI pipes, DPI calls & HDL-HVL interfaces.

Remote Monitoring System for Infants | *Arduino C++, Python, MQTT, Git*

- Developed an IOT based Cradle system that measures vitals of a baby through sensors and sends them over ThingSpeak cloud and made use of event-driven firmware to notify parents if the vitals don't look good. Data collected in ThingsSpeak cloud used to present the sensor data collected through the cloud's APIs.

Experience

Associate Software Engineer - Prodapt, Hyderabad Jul 2023 – Dec 2023

- Skills : SpringBoot, MongoDB, SQL, AngularJS, Git, Docker, Agile, Jira, PostMan
- Developed a full-stack web application "Analytics-Dashboard (Telecommunication)" using SpringBoot and MongoDB that presents real-time updation of data being collected in the MongoDB.

Failure Analysis Intern - ECIL, Hyderabad, India May 2019 – Dec 2019

- Collaborated with the manufacturing team to identify failures, analyze schematics, implement corrective actions on embedded boards through debugging and IC component replacements & enhance yield rates. The assigned responsibilities covered multiple stages of production line, including Visual-Inspection, Troubleshooting, Functional Testing, In-Circuit Testing, and Calibration of Energy Meters.