Khushboo Khairkar

Validation & Verification Engineer

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Work Experience

L&T Technology Services Ltd   **Position: Validation & Verification Engineer**
Location: Mysore
Client: Volvo Car Corporation, Sweden.

❖ **Oct 2021 – Dec 2022**
Project Name: Hilding.
Description: Verification and Validation of EV Battery Module ECU Software with Hilding testbench.
- Automotive embedded software testing/verification & validation using python scripting language in HIL environment for high voltage battery management (HVBM) ECU.
- Issue finding, issue tracking and retesting and issue reporting through JIRA.
- Responsible for testing process starting from Requirement Analysis, Test Case Development, Testing, Reporting Defects and Automation of Test Cases.
- In addition to testing, also playing the role of Test Script Reviewer and experienced in handling a team in Agile Framework.

Skills: Python scripting, Test Automation, UDS (Unified Diagnostic Services), Off-Board Diagnostic, Communication Protocols (CAN, LIN, MOST, Ethernet), VS Code (IDE), Pycharm (IDE), GIT, JIRA, Confluence, Software Testing, Agile.

❖ **Jan 2023 – Present**
Project Name: BSW Test Automation.
Description: Hardware in Loop (HIL) validation for EV Battery Module (HVBM) using dSPACE HIL Simulator.
- Automotive embedded DTC testing/verification & validation in HIL environment for high voltage battery management (HVBM) ECU.
- Responsible for Test Procedure & Test Script development for HIL Testing.
- Performing manual test using Control Desk to check the behavior of DTCs.
- Injecting fault to trigger DTCs, then validating script using ReadDTCInformation (19 hex) Service.
- Generating testcase report and analyzing it to check the expected behavior of DTC.

Skills: Python scripting, Test Automation, HIL Testing, dSpace AutomationDesk, ControlDesk, Cygwin, DSA, Gerrit, JIRA.

Semi-Conductor Laboratory, Department of Space,
Government of India   **Position: Design Engineer - Trainee**
Dec 2020 - Jul 2021
Description: Design and simulation of custom FPGA was done to reduce dependencies of market FPGA'S.
Skills: Design, Simulation
Tools and Technology: LTspice®, Verilog to routing (VTR)

Education

Year	Degree	University/School	Percentage/CGPA
2019-21	M. Tech. VLSI and Embedded System	MIT - WPU	9.51
2014-18	B.E. (ETC) - RTMNU	S. B. Jain	68.2%
2014	HSC - CBSE	Kendriya Vidalaya, VSN	65.0%
2012	SSC - CBSE	SGHPS	8.40

Major Projects

MTech dissertation
Design of FPGA Building Blocks Using LTspice®

Design and simulation of custom FPGA was done intending to design own FPGA by first designing basic building blocks of Spartan-3 FPGA family at 180 nm technology in LTspice®. After which we can place and route them together to realize own FPGA resulting in reduced dependencies of market FPGAS. The circuits were built of Spartan-3 FPGA family using 180 nm technology. Successful simulation and design of individual blocks was achieved using LTspice®.

BTech dissertation
Script To Speech Multilingual Translator

Script to speech multilingual translator (using Raspberry Pi) is a device which can be used to scan the printed text by camera, translate the text to desired language and convert it to audio output through headphones with a single press of push button.

Programming Languages

- Python
- C (Basic)
- C++ (Basic)

Achievements

- Secured 1st position in Embedded BU (L & T Technology Services) in quality testing exam.
- Secured 1st position in a national level project competition at YCCE 2018.
- Secured 2nd position in a national level project competition at PRIYADARSHANI 2018.

Extra-Curricular Activities

- IIT BOMBAY WORKSHOP, Coordinator (2019), Reinforced group of 12 members as a technical coordinator (Arduino board).
- Department of Electronics and Telecommunication, Teaching Assistant, Mentored and guided 5 B.E. F.Y. students in Mathematics-1 course.
- IETE, Coordinator (2015-2018), Planned meetups and organized various events.
- FEETA SRC, INR (2016-2017), worked as public relation officer. Gained experience at writing skills, finance and management. Discovered WhatsApp as a platform to edit texts and attract customers.
- Coordinator in IEEE PUNECON 2019 2nd International Conference.
- Anchored Technoutsav- 2k17.
- Member of rotary club.

Publications

Design of FPGA Building Blocks Using LTspice® | IEEE Conference Publication | IEEE Xplore

About Me

Experienced Embedded Test Engineer with a 2+ years of demonstrated history of working in the automotive industry. Skilled in Python scripting, Automation Testing, Diagnostics over CAN (Do CAN) and well versed in all phases of Software Testing Life Cycle (STLC).

Have good hands-on experience in validation of diagnostics in HIL simulation environment and scripting language like Python.

Languages Known: English, Marathi and Hindi.

Strengths: Eager to learn and adopt new technologies, Quick learner, Good managerial skills, self-motivated, enthusiastic individual with leadership skills. Strong interpersonal organizational skills. Resourceful, energetic, multitasker and result-oriented. Communication skills and problem-solving abilities.

Hobbies: Reading books, writing, painting.

Nationality: Indian