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1. GENERAL

1.1 Architecture

The P/15 electronics are located mostly on a single board. This board contains all circuitry except for bus interface buffering and main RAM which is located on a piggyback board connected back-to-back with the main board. The basic architecture of the system is shown in Figure 1. and has two internal 68000 buses. In addition, there is interface circuitry existing for two additional buses which are external to the main board; the Multibus and the SCSI bus. There are two processors in the design. Both of these are 68010's and are designated the Job processor and DMA processor. Both processor's are masters on their respective buses as are the external bus interfaces. The Job processor has on its bus the Multibus interface (a bus master) and the DMA processor has the SCSI interface (also a master). These buses are interconnected via a switchyard and arbitration circuit. Arbitration for the RAM as well as each of the two internal buses is accomplished by this single arbiter. The two interfaces to the external buses are limited gateways. All of the external bus arbitration protocols are handled by the interface and not exposed to the two internal buses.

There are two additional communications paths associated with the internal buses. The first provides the Job processor access to the DMA processor's bus but not the opposite. Second, the Job processor is provided access to the map registers but the DMA processor is not. Other occupants of the buses live on the DMA processor's bus. These include static RAM, PROM, non-volatile clock RAM, control regusters, and the serial channel controllers.

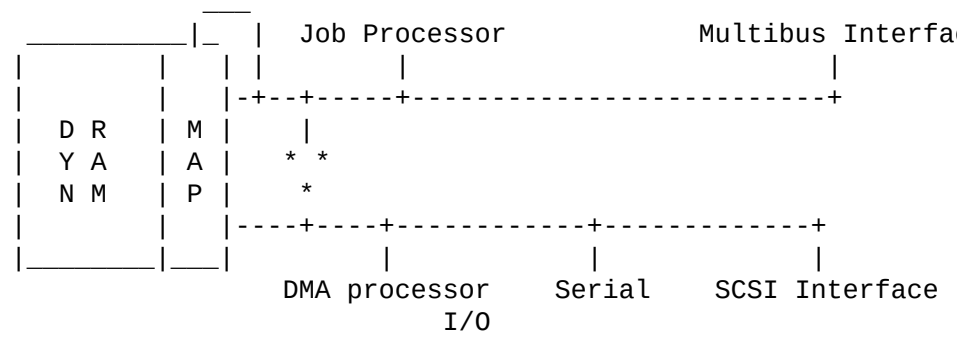

Figure 1. System Block Diagram

1.2 Address Spaces

The various address spaces for the processors are shown in appendix C. Since the memory mapping is performed at the RAM of the system, the addresses which are defined are virtual and apply across the system. The exceptions to the virtual mapping are the static RAM, USART control, SCSI interface control, PROM's, non-volatile clock RAM, clock control ports, and RAM map registers. A different exception to this is that the map can be disabled. This disables address translation, page protection, and disables the ability to access RAM in user mode.

2. JOB BUS ENVIRONMENT

2.1 Main RAM Access

Main RAM is accessed through the bus switchyard. The data path is 16 bits wide and the address is 24 bits wide. Parity is checked for each byte. The Multibus interface requests and arbitrates for main RAM when needed. The Job processor, however, issues a request for main RAM only when no other master owns it and is then guaranteed zero wait states (for either 10 or 12.5 MHz processors).

Should a parity error occur, both processors are given a level 7 interrupt. Also this occurrance causes a number of latches to store the data at their inputs. The information stored includes the states of the following lines:

memory address bits 9, 16-21 (bank select)

memory write line

parity indicator (high/low byte)

which bus master was on a bus

map disable line

processor halt and reset lines

ups power fail line

over temperature line

power fail line (generated by the power supply)

Multibus request lines

Multibus busy line

SCSI busy line

bus error lines for both buses

2.2 Multibus Interface

The Multibus interface is a gateway between the Multibus and the Job processor's bus on the P/15/20 main board. Any access for read or write purposes to a Multibus specific address will result in action on the part of this interface. The interface translates the address received to one appropriate to the Multibus and arbitrates for Multibus mastership transparent to the JOB processor. As shown in Appendix C, a Job processor bus address of B00000-BFFFFF is decoded by this interface. These addresses are translated into two kinds of Multibus addresses. The first of these is B00000 to B7FFFF in the Job processor address space and transfers to 0000 to 7FFFF in the Multibus I/O address space. The second of these is B80000 to BFFFFF in the Job processor address space and translates to 0000 to 7FFFF in the Multibus memory address space.

For transfers which are initiated by Multibus modules, the addresses decoded by this interface result in allowing the access to the P/15 main board if the memory address appearing on the Multibus is greater than or equal to 80000. If an address in this range is decoded, it is passed to the Job processor bus and translated to addresses beginning at 780000. Arbitration on the Job processor bus is handled by the interface and is transparent to the Multibus module initiating the transfer.

In the event that the Job processor is master of its bus and is accessing an address located out on the Multibus, and there is a simultaneous access by a Multibus module to an address which is located on the P/15 main board requiring the Multibus interface to arbitrate for the Job processor bus, a collision occurs. The action performed when this occurs is to generate a bus error for the Job processor causing it to back down, release the bus, and retry the cycle. Upon this release, the Multibus interface gains mastership of the Job proccssor bus and performs its transfer. Upon completion of the transfer the bus is released and the Job processor can acquire mastership. Thus a potential deadlock is averted. The type of bus error given the JOB processor is transparent to software.

2.2.1 Multibus Conventions The standard bus is used in Plexus systems in the following way. The first convention is a priority encode for bus requests. Four bus request lines are used on the backplane, each associated with a physical slot. Each of these request lines goes to a priority encoder. A hardwired priority relationship among the slots is adhered to allowing bus mastership to the highest priority requester.

The second convention is the use of the address space. All addresses on the bus are decoded as I/O or memory space addresses depending upon the appropriate control signals. Those memory access addresses which are greater than 80000 are for cpu module destinations. Those which are less than 80000 are reserved for other Multibus modules. Those addresses which are I/O addresses, are not responded to by the CPU.

2.2.2 Loopback Function The Multibus interface may be tested with or without backplane or Multibus modules connected. The method allows an access to be mirrored back into the logic board transparent to the processor. This is invoked by setting a diagnostic bit and making an

access to Multibus address space in the range of B80000-BFFFFF which is decoded by the interface as an access to the logic board beginning at address 780000. This access then appears on the JOB processor bus as an access from the Multibus to main memory.

3. DMA BUS ENVIRONMENT

3.1 Main RAM Access

The DMA bus owner accesses main memory by arbitrating for it with the job processor. The map translates dma addresses just as it does job addresses. If the dma bus tries to go to main memory while the job processor tries to talk to the DMA bus a collision occurs, requiring the job processor to rerun its bus cycle the same way it does for a collision with multibus.

3.2 SCSI Interface

This circuitry is a master on the DMA processor’s bus. It supports one address pointer/byte count of any SCSI type. If the SCSI bus uses a pointer of a type different than the pointer in the interface, a pointer interrupt is generated to the DMA processor to allow it to update the interface with the proper pointer. Additional logic is included to support SCSI selection and reselection. The SCSI specific commands are shown in appendix A.

Selection of a device controller on the SCSI bus is expained by the following:

How To Select a SCSI Controller

Assumptions: You are trying to select ONLY ONE controller at a time. Other controllers that have been previously selected may still be active and even connected. If you need to select to controllers the Arbitrate Flag will have to be set a second time after the completion of step 12 to cause a second SINT.

1. Set Arbitration Flag (bit 8)
2. Wait for SINT (timeout only after many seconds)
3. Put Selection code into SCSI Output Registers.
4. Clear I/OPTR (bit 15)
5. Set BSY and SEL (bits 9 and 10) -- Diagnostics might want to set I/O (bit 4) here to test Reselection.
6. Wait 1 usec.
7. Clear BSY (bit 9)
8. Wait 1 usec.
9. Wait for BSY active (timeout only after 250 msec.)
10. Set ATN (bit 2) if desired. -- Diagnostics testing Reselection might want to set BSY (bit 9).
11. Clear SEL (bit 10) -- Diagnostics should clear I/O (bit 4) also.
12. Initialize Pointers (Command pointer ?)
13. Set Auto Enable (BIT 0)

The data transmissions through the SCSI interface are handled by a block mover function. The SCSI bus does not pass addresses. Each device on the bus is ignorant of the destination internal to the device to which information is being sent.

The SCSI bus transfers blocks of data, not words like the processor bus or the Multibus. After a SCSI device arbitrates for the bus, it will usually transfer an entire block of something (command, status, data) before releasing control of the bus. However, the controller never never has any control over the addresses used. Controller's request to send or receive bytes of information while simply counting the number of bytes until the transfer is complete. The main logic board must also count bytes but add the addresses for memory reference on its own. Registers in the interface are used to perform the byte count and address increment for these transfers.

3.3 Other Bus Residents

3.3.1 Clock The clock is the MC146818 calendar/clock chip. There is a 50 byte RAM internal to the chip which is backed up by a rechargeable battery on the logic board. The interface to the clock circuit is shown in appendix G.

3.3.2 Static RAM The static memory is a single contiguous space from C00000 to C03FFF. The DMA processor accesses static ram with no wait states.

4. EXTERNAL INTERFACE

4.1 Serial Port Connection

The serial port connectors are of the 9 or 25 pin "D" style. Six ports use the 9 pin and two the 25 pin connectors. The pinouts are given in appendix D. Ports 0-3 support only tty (no hardware handshake), ports 4-5 support tty plus asynchronous modems (hardware handshake included), and ports 6-7 support the above plus synchronous modems (clock lines included).

4.2 Test Connector

In addition to the eight serial ports exposed through the back panel, there is a connector for access to the electronics for test purposes. This port provides access to internal registers in a read only mode as well as various single bit control signals for such things as power down and system reset. The definitions for these signals are given in appendix B.

4.3 SCSI Connector

Plexus part number 04-000235 is used. The pinout is in appendix E.

4.4 Multibus Connection

A standard multibus connector is not used. Rather, the main board connects with the backplane via a special edge connector. The pinout for this is in Appendix F.

5. REGISTERS

Various registers latch signals applied to their inputs upon the occurance of different hardware events. They are divided into two classes, those being input and output. These designations are based upon how the processors use them. The decoding of these registers is as follows:

5.1 Input Registers

Address	High byte	Low byte
E00000	15 = spare 14 = spare 13 = PEH 12 = PEL 11 = EN.BLK 10 = EN.MBUS 9 = EN.DMA 8 = EN.JOB All 16 bits are latched on PELATCH	7 = MWT 6 = MA9 5-0 = MA21 - MA16
E00002	15 = DIS.MAP 14 = RES.DMA- 13 = HALT.DMA- 12 = RES.JOB- 11 = HALT.JOB- 10 = UPS 9 = TEMP 8 = PFW All 16 bits are latched on PELATCH	7 = BREQ3* 6 = BREQ2* 5 = BREQ1* 4 = BREQ- 3 = BUSY 2 = SCSIBSY 1 = BERR.JOB- 0 = BERR.DMA-
E00004	Not used All 8 bits are latched on MBERR	7 = A.JOB18 6 = A.JOB17 5 = A.JOB16 4 = A.JOB15 3 = A.JOB14 2 = A.JOB13 1 = A.JOB12 0 = READ.JOB
E00006	Not used	7-4 Not used 3-0 SCSI byte count 19 - 16
E00008	SCSI byte count 15 - 8	SCSI byte count 7 - 0
E0000A	Not used	7-4 Not used 3-0 SCSI pointer 19 - 16
E0000C	SCSI pointer 15 - 8	SCSI pointer 7 - 0
E0000E	15 = ARBR- 14 = SCZERO 13 = SCPERR- 12 = SCBERR- 11 = STIME 10 = SEL 9 = BSY 8 = MYBIT	7 = REQ 6 = MSG 5 = SCRST 4 = I/O 3 = C/D 2 = ATN 1 = ACK 0 = DATEN

```
E00010      Not used                        Not used

E00012      Not used                        Not used

E00014        15 = AS26                       7 = AERR.JOB
              14 = S.OOPS                     6 = DERR.JOB
              13 =                            5 = MBTO
              12 = UBE.DMA                    4 = UBE.JOB
              11 = ABE.DMA                    3 = ABE.JOB
              10 = EN.BLK                     2 = EN.JOB
               9 = EN.DMA                     1 = EN.BLK
               8 = EN.JOB                     0 = EN.MBUS
              Latched by DBE-                 Latched by JBE-

E00016        15 = Boot.DMA-                  7 = TBUSY
              14 = BOOT.JOB-                  6 = DIAG.UART
              13 = SCSIDL- (Diag latch)       5 = HOLDMBUS
              12 = DIAG.PEH (force error)     4 = RESMB-
                                             (Multi bus INIT*)
              11 = DIAG.PEL (force error)     3 = CINTD.EN
              10 = DIAG.PESC (force error)    2 = CINTJ.EN
               9 = DIAG.MB (Multi bus)        1 = TINT.EN
                                            (Temperature)
               8 = DIS.MAP                    0 = UINT.EN (UPS)

E00018      Not used                          7  = EN.JOB
                                              6  = JKPD
                                            5-4 = spare
                                             3  = INT.JOB
                                             2  = INT.DMA
                                             1  = KILL.JOB-
                                                (Reset job -)
                                             0  = KILL.DMA
                                                (Reset DMA)

E0001A        15 = spare
              14 = spare
              13 = RI.B
              12 = RI.A
              11 = TCE.B-                     3 = DSR.D
              10 = TCE.A-                     2 = DSR.C
               9 = RCE.B-                     1 = DSR.B
               8 = RCE.A-                     0 = DSR.A


E0001C      Not used                        Not used

E0001E      Not used                        User number 7 - 0
```

5.2 Output Registers

All registers are written 16 bits at a time.

Note: N=0 and N=1 indicate the state in which that bit
MUST be to allow normal system operation.

Address	Reset selection
E00000	NOP
E00020	Reset Multi bus interface error flag
E00040	Reset SCSI parity error flag
E00060	Reset Job processor software interrupt
E00080	Set Job processor software interrupt
E000A0	Reset DMA processor software interrupt
E000C0	Set DMA processor software interrupt
E000E0	Reset Job processor clock interrupt
E00100	Reset DMA processor clock interrupt
E00120	Reset Job processor bus error flag
E00140	Reset DMA processor bus error flag
E00160	Reset Memory Parity error flag Master hardware reset sets this flag
E00180	Reset Switch Interrupt Latch
E001A0	Reset SCSI Bus Error Flag
E001C0	Unassigned
E001E0	Unassigned

Writing to these addresses causes the action. Data values are
ignored.

Address	High byte	Low byte
E00002	Not used	Not used
E00004	Not used	Not used
E00006	Not used 7-4 Not used 3-0 = SCSI byte count 19 - 16	
E00008	SCSI byte count 15 - 8	SCSI byte count 7 - 0
E0000A	Not used 7-4 Not used 3-0 = SCSI pointer 19 - 16	
E0000C	SCSI pointer 15 - 8	SCSI pointer 7 - 0
E0000E	15 = IOPTR 14 = MSGPTR 13 = CDPTR 12 = 1, buffer in static ram 11 = reset scsi interface 10 = scsi selection enable 9 = set SCSIBSY* 8 = Arbitration Flag	7 = set SCSIREQ* 6 = set SCSIMSG* 5 = set SCSIRST* 4 = set SCSII/O* 3 = set SCSIC/D* 2 = set SCSIATN* 1 = set SCSIACK* 0 = Auto Data Xfer enable

Arbitration Flag resets on winning arbitration.

```
       Auto Data Xfer enable resets on SCSIBSY* inactive.
       All 16 bits are reset low during System RESET

E00010      Not used                        7-4 Not used
                                        3-0 Software settable LEDs

E00012      Not used                        Not used

E00014      Not used                        Not used

E00016      15 = Boot.DMA-  (N=1)               7 = spare
            14 = BOOT.JOB-  (N=1)               6 = DIAG.UART (N=0)
            13 = SCSIDL- (Diag latch)  (N=1)    5 = HOLDMBUS
            12 = DIAG.PEH (force error) (N=0)   4 = RESMB-
                                                (Multi bus INIT*)
            11 = DIAG.PEL (force error) (N=0)   3 = CINTD.EN
            10 = DIAG.PESC (force error) (N=0)  2 = CINTJ.EN
             9 = DIAG.MB (Multi bus) (N=0)      1 = TINT.EN
                                                (Temperature)
             8 = DIS.MAP (N=0)                  0 = UINT.EN (UPS)
               All 16 bits are reset low during System RESET

E00018      Not used                            7 = spare
                                              6 = JKPD
                                            Job control pro-
                                            tection disable
                                              5 - 2 = spare
                                              1 = KILL.JOB-
                                            (Reset Job) (N=1)
                                              0 = KILL.DMA
                                              (Reset DMA) (N=0)
                                             All 8 bits are reset low
                                        during System RESET

E0001A        15 = spare                    Not used
              14 = spare
              13 = spare
              12 = spare
              11 = TCE.B
              10 = TCE.A
               9 = RCE.B
               8 = RCE.A

E0001C      Not used                        Not used

E0001E      Not used                        User number 7 - 0
```

6. INTERRUPTS

6.1 Interrupt Sources

Interrupts are generated by various sources as shown below:

Interrupt Type	Level	Source	Dest.	Vector
Real	7			40 - 5F
Bad News		Spurious int	Both	0100 0000
		Memory error	"	010x xxx1
		Power Fail	"	010x xx1x
		Diagnostic switch	"	010x x1xx
		UPS on battery	"	010x 1xxx
		Over temperature	"	0101 xxxx
Real Time Clock	6	Clock/ Cal Chip	Both	83
UARTs	5	UARTs	DMA	Software settable
Job Processor	4	JINT bit	Job	C1
SCSI Bus	3			60 - 6F
		(60 - 67 have highest priority)		
		Spurious int	DMA	0110 0000
		Selection int	|	0110 0xx1
		Reselection int	|	0110 0x1x
		Parity error int	|	0110 01xx
		Pointer int	|	0110 1mci
			m = /message flag	
			c = /command flag	
			i = /input flag	
		Pointer interrupts happen when SCSI block mover is enabled and unable to respond to a controller request. Events that can cause this are: Incorrect pointer type SCSI Bus parity error SCSI byte count or pointer equal to zero DMA Bus error during previous SCSI cycle		
DMA Processor	2	DINT bit	DMA	C2
Multibus	1		Job	70 - 77, 7F
		MB interface error	|	7F (highest priority)
		MB Interrupt 0	|	70 |
		MB Interrupt 1	|	71 |
		MB Interrupt 2	|	72 |
		MB Interrupt 3	|	73 |
		MB Interrupt 4	|	74 |
		MB Interrupt 5	|	75 |
		MB Interrupt 6	|	76 |
		MB Interrupt 7	|	77 (lowest priority)

6.2 Interrupts Between Processors

The two processors have the ability to send interrupts to each other by writing to an output register. The writing of any value to registers at addresses E00080 interrupts the Job processor (JINT bit).

The writing of any value to E000C0 interrupts the DMA processor(DINT bit). These cause interrupts at level 4 (Job processor) or level 2 (DMA processor).

6.3 Interrupt Summary

The interrupts are summarized below by processor:

Destination	Level	Source
Job	7	Really Bad News
	6	Clock
	4	JINT (from DMA processor)
	1	Multibus
DMA	7	Really bad news
	6	Clock
	5	UARTS
	3	SCSI interface
	2	DINT (from Job processor)

7. MEMORY MAPPER

All accesses to main memory go through the map circuit as mentioned previously. This function is described here.

The map circuit performs address translation plus access privilege checking for each page in memory.

The map registers are addressable only by the Job Processor in system space 16 bits at a time. The addresss are 900000 thru 903FFF (9 0 00up pppp pppp ppw0). The addressing for the map is given below:

Address decode:

```
u           = 1 if page is in system space
ppppppppppp = page number
w           = Word select
```

Data decode

```
Word 1 = rwxn nnnn nnnn nnnn

r              = 0, read enable
w              = 0, write enable
x              = 0, execute enable
bbb            = unused
nnnnnnnnnnnnn = physical page number

Word 0 = iiii iiii xxxx xxrd

iiiiiiii = user id
r        = 1, set when page is referenced
d        = 1, set when page is altered
```

8. BUS ERRORS

Bus errors are generated by multiple sources and have various

destinations. Below is a list of these showing the schematic net mnemonic and brief description of the function.

Source	Destination	Mnemonic	Function
DM timer	DMA	AS26	Deadman timer for all DMA transfers
Addr decode	DMA	S.OOPS	Any DMA access of Multibus or map
Map	initiator	UBE.DMA UBE.JOB	User id != id stored in the map for any page accessed
Map	initiator	ABE.DMA ABE.JOB	Priviledge violation on a per page level
Map	Job	AERR.JOB	User in system space
DMA environ.	Job	DERR.JOB	DMA bus error generated when Job processor is accessing the DMA bus
Multibus interface	Job	MBTO	Multibus access deadman timer

9. SCSI Messages

Code	Message	trg=target init=initiator
00	Command complete: Command is completed and status has been sent.	trg > init
01	Extended message follows: Multiple byte message follows.	trg > init or init > trg
02	Save data pointer: Command to save a copy of the present active data pointer for the currently attached LUN.	trg > init
03	Restore pointers: Restore the most recently saved pointers for the currently attached LUN.	trg > init
04	Disconnect: Message that connection is being broken.	trg > init
05	Initiator detected error: Initiator has detected a retryable error since data pointer was last saved.	init > trg
06	Abort: Clear any operation for the specified LUN from the selecting initiator.	init > trg
07	Message reject: Last message received was inappropriate or not implemented.	init < trg
08	No operation: Response to target’s request when no other message is to be sent.	init > trg
09	Message parity error: One or more bytes in the last message had a parity error.	init > trg
0A	Linked command complete: Execution of a linked command has completed and status has been sent.	trg > init
0B	Linked command complete with flag: Same as above but with FLAG set.	trg > init
0C	Bus device reset: Sent to cause target to reset.	init > trg

10. SCSI Commands

Commands are given for eight categories. These are:

Group 0 - 6 byte commands

Group 1 - 10 byte commands

Group 2 - RESERVED

Group 3 - RESERVED

Group 4 - RESERVED

Group 5 - 12 byte commands

Group 6 - VENDOR UNIQUE

Group 7 - VENDOR UNIQUE

The commands include such functions as read, write, seek, format, and rezero as well as many used for status transmitting and receiving. For complete descriptions see the ANSI specification.

10.1 Command Data Block

The Command Data Block is used for the issuing of all commands to the DMA processor. The blocks are chained so that the DMA processor has a queue of blocks from which to take commands. The general format of this block is as follows. Different commands will use more space depending on the functions.

Byte:	Meaning:
0	Command Operation Code
1	Logical Unit Number, Address
2	Block Starting Address
3	Block count
4	Control Byte

11. Signal Definitions

The following signals are provided:

One serial asynchronous channel - RxD, TxD

Read access to diagnostic registers:

Eight data bits

Three address bits

Strobe bit

Present data, strobe with setup and hold times of 20 nS each.

System reset control line

Voltages from all power sources +5, +/-12 for both supplies

Power supply control line

Level 7 interrupt input (SWINT)

Level 7 maskable interrupt input (UPSINT)

All signals are TTL levels.

12. Address Decodes

The following coded addresses are used:

A0-A2	Function
0	Read LED register
1	Read bus error, external bus states
2	Read system state
3	Read internal bus state
4	n/a
5	n/a
6	Reset error latches
7	n/a

12.1 Signal List

The following signals are presented for each address indicated. An asterisk or minus suffix on a signal name denotes active low.

```
REGISTER   BITS    FUNCTION
0     0-7   LED register (LEDS on bits 0 to 3)

1     This transparent latch is latched by PELATCH-
      0     BERR.DMA- (Bus error on DMA processor bus)
      1     BERR.JOB- (Bus error on job processor bus)
      2     SCSIBSY (SCSI BUSY)
      3     BUSY (Multibus)
      4     BREQ- (Multibus)
      5     BREQ1* (Multibus)
      6     BREQ2* (Multibus)
      7     BREQ3* (Multibus)

2     This transparent latch is latched by PELATCH-
      0     PFW (Power fail warning from power supply)
      1     TEMP (On board temperature sensor)
      2     UPS (Status input from remote UPS)
      3     HALT.JOB-
      4     RES.JOB-
      5     HALT.DMA-
      6     RES.DMA-
      7     DIS.MAP (Disable Map RAM)

3     This transparent latch is latched by PELATCH-
      0     EN.JOB (Job bus is driving the DMA bus)
      1     EN.DMA (DMA bus is driving the main memory)
      2     EN.MBUS (Multibus interface is driving the job bus)
      3     EN.BLK (SCSI interface is driving the DMA bus)
      4     PEL (Parity error on low byte)
      5     PEH (Parity error on high byte)
      6     MWT (DRAM write)
      7     REFON- (Refresh address enabled onto DMA bus)

6     A read of this location will reset PELATCH-
```

13. Connector

The connector is a 32 pin header mounted so as to allow a flat ribbon connector to be connected to it. Access to this connector is via the rear panel. The connector is not a "D" type so as to not confuse it with the serial port connectors in the same area.

The pinout of this connector is as follows:

```
1,2,3,4,5,6,10    GND
7           A1
8           GND or VCC (jumper on main board)
9           D6
11          RxD - Port 1
12          D2
13          TxD - Port 1
14          Aux. power supply +12v thru 1K resistor
15          Main power supply +5v thru 1K resistor
16          Main power supply +12v thru 1K resistor
17          Main power supply -12v thru 1K resistor
18          Aux. power supply +5v thru 1K resistor
19          Aux. power supply -12v thru 1K resistor
20          Data 0
21          Data 1
22          Data 3
23          Data 4
24          Data 5
25          Data 7
26          A2
27          A0
28          UPS status in (Connect to GND when UPS on battery)
29          Level 7 Switch interrupt (active low)
30          Key switch power on (active low)
31          Key switch reset (active low)
32          Address strobe (address bits must be stable from 20ns
                  BEFORE address strobe goes LOW to 20ns AFTER
                  address strobe goes HIGH) This bit enables
                  data onto the data bus.
```

The masters for the buses include the Job processor, Multibus, SCSI block mover, and the DMA processor. All addresses are in the system space.

Robin System and User Address Spaces

Bus Master				Space		Loc		Address Range	Function
Job	MB	DMA	BLK	Usr	Sys	Job	DMA		
x		x		x		x		000000 - 7FFFFF	Main User memory
x		x			x	x		000000 - 7FFFFF	Main Sys memory
	x				x	x		780000 - 7FFFFF	Main Sys Memory
			x		x	x		600000 - 6FFFFF	Main Sys Memory
x		x			x		x	800000 - 80FFFF	PROM (4 - 27128s)
x					x	x		900000 - 901FFF	User Page Map
x					x	x		902000 - 903FFF	Sys Page Map
x		x			x		x	A00001 - A0003F	UART ’A’ (odd)
x		x			x		x	A10001 - A1003F	UART ’B’ (odd)
x		x			x		x	A20001 - A2003F	UART ’C’ (odd)
x		x			x		x	A30001 - A3003F	UART ’D’ (odd)
x		x			x		x	A70000 - A70003	SCSI Data Buffers
x					x	x		B00000 - B7FFFF	MBus I/O Space
x					x	x		B80000 - BFFFFF	MBus Mem Space
x		x	x		x		x	C00000 - C03FFF	SRAM
x		x			x		x	D00001 - D0001B	Calendar (odd)
x		x			x		x	D0001D - D0007F	Calendar RAM (odd)
x		x			x		x	E00000 - E0001E	Control/Status Reg.
x		x			x		x	F00003	MBus Int Vector
x		x			x		x	F00005	Job Int Vector
x		x			x		x	F00007	DMA Int Vector
x		x			x		x	F00009	SCSI Int Vector
x		x			x		x	F0000B	UART Int Vector
x		x			x		x	F0000D	Clock Int Vector
x		x			x		x	F0000F	Panic Int Vector

The following is a pinout list for the DB-9 and DB-25 connectors.

DB-9 Pin#	Signal Name	DB-25 pin#	MODEM DB-25 pin#
1	TxD	3	
2	RTS	5	
3	DSR	20	
4	DTR	6	
5	Shield	1	
6	RxD	2	
	RI	22	
7	CTS	4	
	RxC	17	

```
8........Sgnl Gnd...........7

       TxC................15

9........DCD...............8
```

Signal names	Direction
TxD = Transmit Data	DTE -> DCE
RxD = Receive Data	DTE <- DCE
RTS = Request to Send	DTE -> DCE
DSR = Data Set Ready	DTE <- DCE
DTR = Data Terminal Ready	DTE -> DCE
Shield = Chassis ground	
CTS = Clear to Send	DTE <- DCE
Sgnl Gnd = Signal Ground	
DCD = Data Carrier Detect	DTE <- DCE
RI = Ring indicator	DTE <- DCE
TxC = Transmit clock (synch)	DTE <- DCE
RxC = Receive clock (synch)	DTE <- DCE

DCE = Data Communication Equipment
(MODEM)
DTE = Data Terminal Equipment
(tty)

The SCSI bus connector pinouts are indicated below:

PIN	SIGNAL
1,3,5,7,9,11,13,15,17 19,21,23,27,29,31,33 35,37,39,41,43,45,47,49	GND (note that pin 25 is not included)
2	D0
4	D1
6	D2
8	D3
10	D4
12	D5
14	D6
16	D7
18	Data Parity
25	xxxxxxxxx
26	TERM
32	ATN
36	BSY
38	ACK
40	RST
42	MSG
44	SEL
46	C/D
48	REQ
50	I/O

The Multibus connection to the main logic board is accomplished with a connector having the following pinout:

PIN	SIGNAL
1,2,9,10,12,13,14 19,20,23,24,27,33 34,43,44,53,54,63 64,65,66,75,76,85 86,89,90,91,92,93,97	GND
3,4	+5 Volts (Input from backplane, goes only to
5,6	+12 Volts test connector through 1K resistor)
7	BCLK*
8	INIT*
11	BUSY*
15	MRDC*
16	MWTC*
17	IORC*
18	IOWC*
21	XACK*
22	LOCK*
25	BHEN*
26	AD10*
28	AD11*
29	CCLK*
30	AD12*
31	INTA*
32	AD13*
35	MBINT6*
36	MBINT7*
37	MBINT4*
38	MBINT5*
39	MBINT2*
40	MBINT3*
41	MBINT0*
42	MBINT1*
45	ADRE*
46	ADRF*
47	ADRC*
48	ADRD*
49	ARDA*
50	ADRB*
51	ADR8*
52	ADR9*
55	ADR6*
56	ADR7*
57	ADR4*
58	ADR5*
59	ADR2*
60	ADR3*
61	ADR0*
62	ADR1*
67	DATE*
68	DATF*
69	DATC*
70	DATD*

```
71    DATA*
72    DATB*
73    DAT8*
74    DAT9*
77    DAT6*
78    DAT7*
79    DAT4*
80    DAT5*
81    DAT2*
82    DAT3*
83    DAT0*
84    DAT1*
87,88 -12 Volts (input from backplane, goes only to
              test connector through 1K resistor)
94    BREQ3*
95    BREQ2*
96    BREQ1*
98    BPRN3*
99    BPRN2*
100   BPRN1*
```

Calendar Clock and NV RAM

Address decode: D000AA odd bytes only. Note: Reg A (address D00015) is the only which can be read or written to without testing the UIP bit first. (The UIP bit is part of Reg A.) When UIP = 0 you have at least 244 u sec in which to read or write any address in the Calendar chip. Failure to observe this protocol causes Calendar errors.

AA Function

01 Seconds (from 0 to 59 decimal)

03 Seconds Alarm (from 0 to 59 decimal)

05 Minutes (from 0 to 59 decimal)

07 Minutes Alarm (from 0 to 59 decimal)

09 Hours (from 1 to 23 decimal in 24 hour mode,
or 1 to 12 with bit 7 set for PM in 12 hour mode)

0B Hours Alarm (from 1 to 23 decimal in 24 hour mode,
or 1 to 12 with bit 7 set for PM in 12 hour mode)

0D Days (from 1 to 7 decimal)

0F Day of the month (from 1 to 31 decimal)

11 Month (from 1 to 12 decimal)

13 Year (from 0 to 99 decimal)

15 Reg A Bit

7 UIP (Update in progress) READ ONLY

6,5,4 DV2,DV1,DV0

0	0	0	4.1943 MHz input
0	0	1	1.0486 MHz input
0	1	0	32.768 KHz input (Robin usage)

3,2,1,0 RS3,RS2,RS1,RS0 Periodic Interrupt

0	0	0	0	None
0	0	0	1	3.90625 ms
0	0	1	0	7.8125 ms
0	0	1	1	122.070 us
0	1	0	0	244.141 us
0	1	0	1	488.281 us
0	1	1	0	976.562 us
0	1	1	1	1.953125 ms
1	0	0	0	3.90625 ms
1	0	0	1	7.8125 ms
1	0	1	0	15.625 ms
1	0	1	1	31.25 ms
1	1	0	0	62.5 ms
1	1	0	1	125 ms
1	1	1	0	250 ms
1	1	1	1	500 ms

17 Reg B Bit

7 SET 0 = counting time; 1=holds UIP at 0 to allow
the setting of the date/time without
allowing any updates to occur.

6 PIE 1 = enable interrupt (not supported by robin)

```
          5     AIE    1 = enable alarm interrupt
          4     UIE    1 = enable undate ended interrupt
          3     SQWE   1 = enable square wave
          2     DM     0 = BCD format for date/time registers
                   1 = Binary format for date/time registers
          1     24/12  0 = 12 hour mode
                   1 = 24 hour mode
          0     DSE    1 = enable daylight savings changes

19      Reg C   Bit      Note: ALL bits are reset to 0 after this reg
                      is read.  This register is read only.
                7     IRQF   Interrupt request flag
                      = PF * PIE + AF * AIE + UF * UIE
                6     PF     Periodic interrupt flag
                5     AF     Alarm interrupt flag
                4     UF     Update ended interrupt flag
               3-0    0

1B      Reg D   Bit      Note:  This register is read only.
                7     VRT     Valid RAM and Time (always a 1)
               6-0    0

   1D to 7F  Non volatile RAM  (odd bytes only)
```

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