22 February 2023

Configuration File Manual

I/O Pin Mapping and Driver Configuration

I/O Module	IO397-50k
Minimum required I/O Blockset	9.5.1.1
Reference	speedgoat_IO397_50k_CI_DUT_DEMO_v1

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Document Version History

Rev.	Description	Date
1.0	Initial version of Configuration File Manual	22 February 2023

1 Introduction

This manual supplements the User Manual you received with your real-time target machine.

Your real-time target machine is equipped with at least one configurable I/O module for which a configuration file and Simulink Real-Time ™ driver blockset have been provided. Refer to your real-time target machine user manual for more information.

This document explains how to install, configure, and use the specific configuration file and Simulink Real-Time driver blockset you ordered upon purchase of your real-time target machine. Note that additional configuration files can also be purchased at a later date.

2 Implemented Functionality

This configuration file and Simulink Real-Time driver blockset implements the following functionality:

FPGA Code Module	Transceiver Type	No.of Modules/Channels	Version
Analog Input	Analog	4	1.0
Analog Output	Analog	4	1.0
DIO	TTL	14	1.3
I2CM	TTL	1	1.8
I2CS	TTL	1	1.9
PWM	TTL	1	5.11

Table 1: Implemented Functionality

3 Software Installation

Install the configuration file after installing the MathWorks tool chain and the Speedgoat I/O Blockset. The steps are as follows:

1. Download the configuration file archive, listed in the downloads/software section of the Speedgoat Customer Portal. If the archive is not available, please contact Speedgoat support.
2. The archive contains a test model, library, documentation and the configuration file (*.mat).
3. The content of this archive can be extracted to your current MATLAB workspace. The configuration file must be part of the MATLAB path. For your convenience, you can copy the file to the following directory, which is part of the MATLAB path. To obtain the predefined directory, in MATLAB type:
   `» fullfile(speedgoatroot,'sg_bitstream')`
4. After copying the MAT-file, type:
   `» rehash toolbox`

4 I/O Pin mapping

The I/O pin mapping for this configuration file implementation is shown below. This I/O pin mapping is specific to the configurable I/O module for which it has been designed and shows how to connect the pins to your hardware under test.

Note: Speedgoat delivers real-time target machines together with terminal boards (refer to your target machine user manual). The terminal board for the configurable I/O module must therefore be wired as described in section 7.2 of this document in order to execute the test model for this specific implementation.

4.1 Front I/O

Pin	Digital I/O	Code Module	Functionality	Direction	Transceiver	Port	Pull Resistors
	Channel number						
1b			0 V				
2b			5V				
3b	1	1	DIO	IN/OUT	TTL		
4b	2	2	DIO	IN/OUT	TTL		
5b	3	3	DIO	IN/OUT	TTL		
6b	4	4	DIO	IN/OUT	TTL		
7b	5	5	DIO	IN/OUT	TTL		
8b	6	6	DIO	IN/OUT	TTL		
9b	7	7	DIO	IN/OUT	TTL		
10b	8	8	DIO	IN/OUT	TTL		
11b	9	1	PWM - A	OUT	TTL		
12b	10	1	PWM - B	OUT	TTL		
13b	11	1	I2C Master - CLK	OUT	TTL		
14b	12	1	I2C Master - Data	IN/OUT	TTL		
15b	13	1	I2C Slave - CLK	IN	TTL		
16b	14	1	I2C Slave - Data	IN/OUT	TTL		
17b			GND				

pull-up 3.3 VDC

Terminal board A: analog I/O

Pin	Functionality	Analog
1a	Analog Input 01 (+)	
2a	Analog Input 01 (-)	
3a	Analog Input 02 (+)	
4a	Analog Input 02 (-)	
5a	Analog Input 03 (+)	
6a	Analog Input 03 (-)	
7a	Analog Input 04 (+)	
8a	Analog Input 04 (-)	
9a	Analog Output 01	
10a	Analog Output 02	
11a	Analog Output 03	
12a	Analog Output 04	
13a	GND	
14a	GND	
15a	0V	
16a	5 VDC	
17a	GND	

ADC

DAC

Figure 1: IO397-50k front pinout

5 Simulink Driver Library

To open the library blocks used for the configuration file, type:
» `speedgoat_lib_IO397_50k_CI_DUT_DEMO_v1`

at the MATLAB command line prompt. The blockset appears as follows:

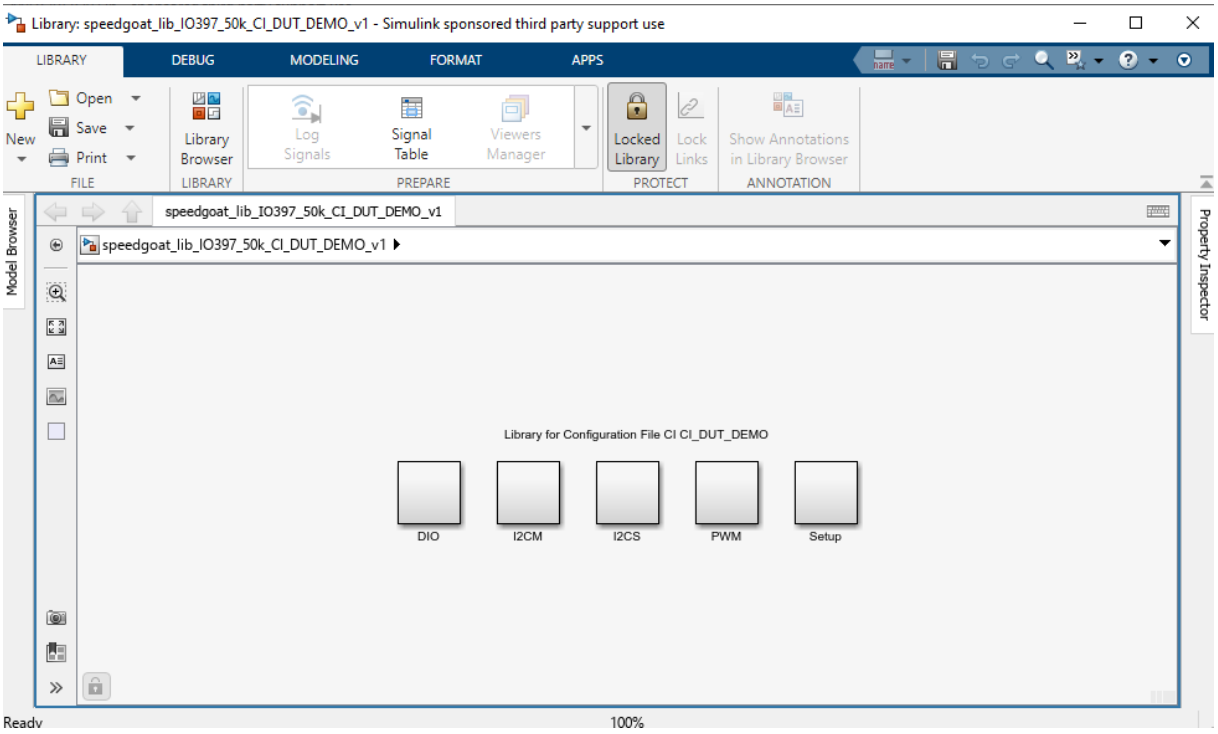

Figure 2: Library for Custom Implementation CI_DUT_DEMO

The configuration file library contains a subset of the Speedgoat I/O Blockset driver blocks implemented in this specific bitstream.

The Speedgoat I/O Blockset may contain different versions of the driver blocks which are not compatible with your configuration file. We therefore highly recommend that you use this custom library whenever you start to build a new Simulink model.

Alternatively, ensure you select the right version of the respective driver blocks. The version of your implemented Code Module functionality is listed in Section 2, where the major version number signifies the driver block version.

6 Configuration File

The configuration file is specified in the setup driver block.

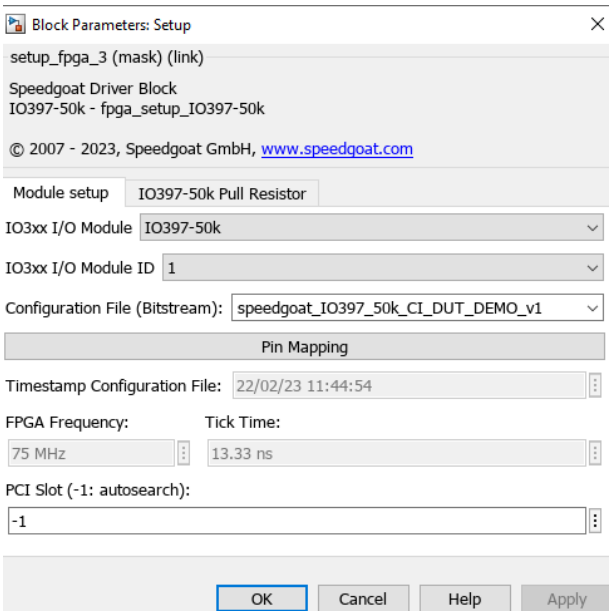

Figure 3: Setup block mask parameter

The FPGA frequency and the resulting tick time (see figure above) are used for time measurements and configuration in several Code Modules (like PWM, CAP) and for defining transmission frequencies for protocols (such as SPI, I2C).

7 Test Model

7.1 Test Model Description

A dedicated test model is included to test the custom set of Code Modules.

Note that this test model only tests I/O channels for which the loop-back test method is possible. The terminal board provided must be wired as indicated in chapter 7.2 of this manual.

To open the test model type:
» `speedgoat_IO397_50k_CI_DUT_DEMO_v1`

at the MATLAB command line prompt. The model appears as follows:

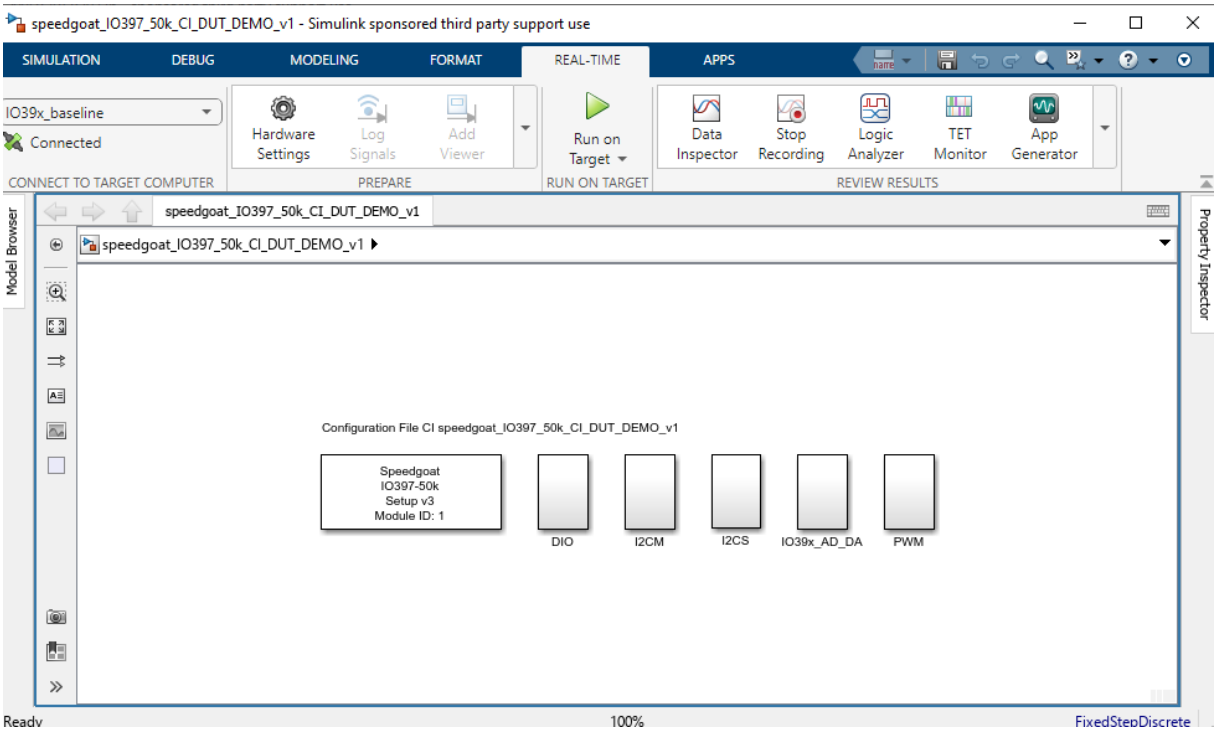

Figure 4: Test model speedgoat_IO397_50k_CI_DUT_DEMO_v1

7.2 Required Test Wiring of the Terminal Board

Front I/O (Analog):

From Pin	To Pin	Tested Functionality
1a	9a	VOUT01 - VIN01 (+) ADC01
3a	10a	VOUT02 - VIN02 (+) ADC01
5a	11a	VOUT03 - VIN03 (+) ADC02
7a	12a	VOUT04 - VIN04 (+) ADC03
13a	2a	Ground - VIN01 (-) ADC01
13a	4a	Ground - VIN02 (-) ADC02
13a	6a	Ground - VIN03 (-) ADC03
13a	8a	Ground - VIN04 (-) ADC04

Table 2: Terminal Board wiring IO397-50k Front I/O Analog

Front I/O:

From Pin	To Pin	Tested Functionality
13b	15b	I2CM - CLK channel 1 to I2CS - CLK channel 1
14b	16b	I2CM - Data channel 1 to I2CS - Data channel 1
11b	3b	PWM - A channel 1 to DIO channel 1
4b	5b	DO channel 2 to DI channel 3

Table 3: Terminal Board wiring IO397-50k Front I/O