Optical link latency measurement implemented in FPGA

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Latency in the optical link of the CMS systems

Overview:

- Back-End hardware is isolated from the main detector.
- The link between Front-End and Back-End systems is made of long Optical Fibers with different lengths, that produce different individual **latencies.**
- To correct for latency differences across multiple optical links, the **synchronization** of the FE modules can be tuned in 1-ns steps.
- It's desired to have an independent measurement of the link latency.

Latency in the optical link of the CMS systems

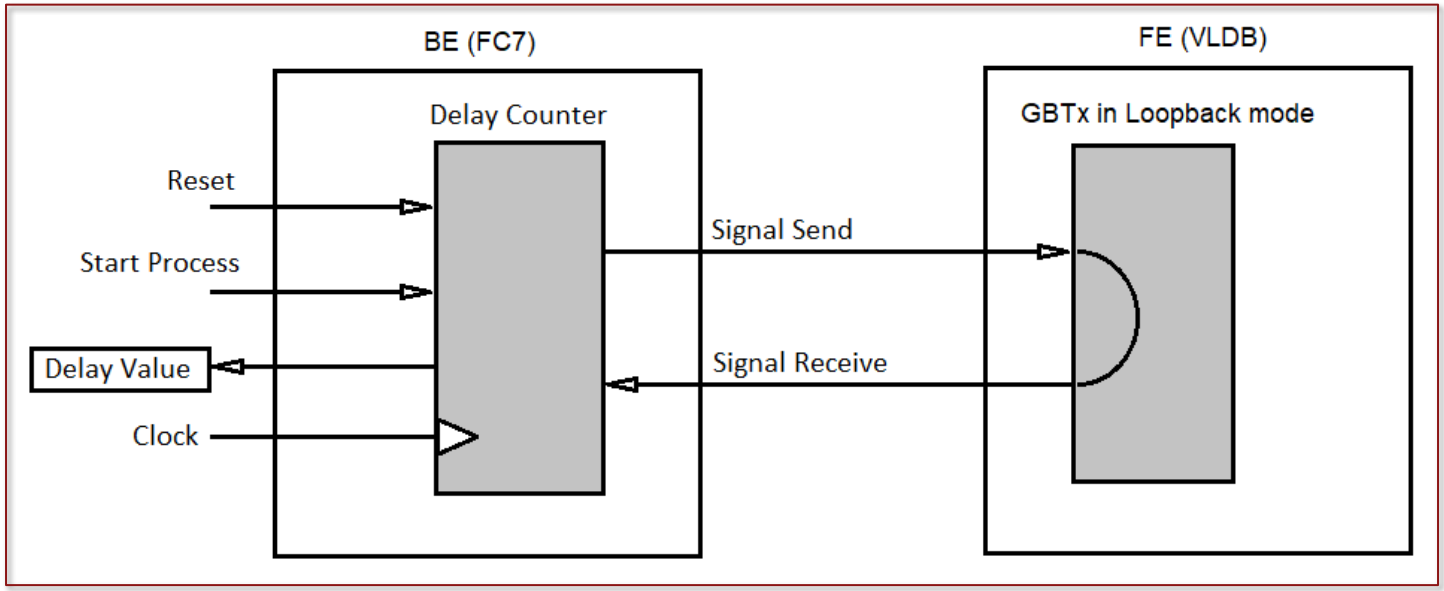
Aim of this work:

- The main objective of the project is to create a tool that estimates the Latency present on the communication between FE and BE, to help the synchronization process.
- The desired implementation runs in the Back-End, on **FPGA** hardware.
- The **Delay Counter firmware** returns measurements of the different lengths of Optical Fiber, as accurate as possible.

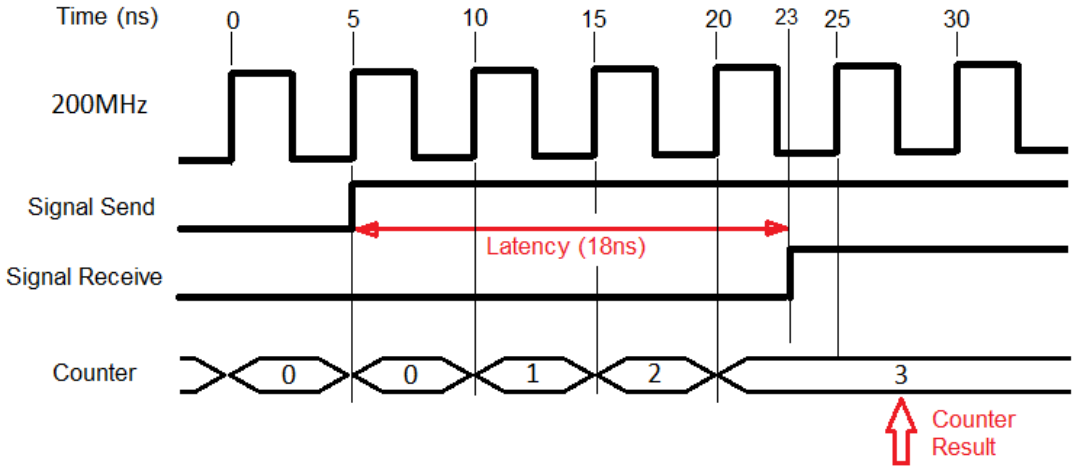
The Delay Counter firmware

How does it work?

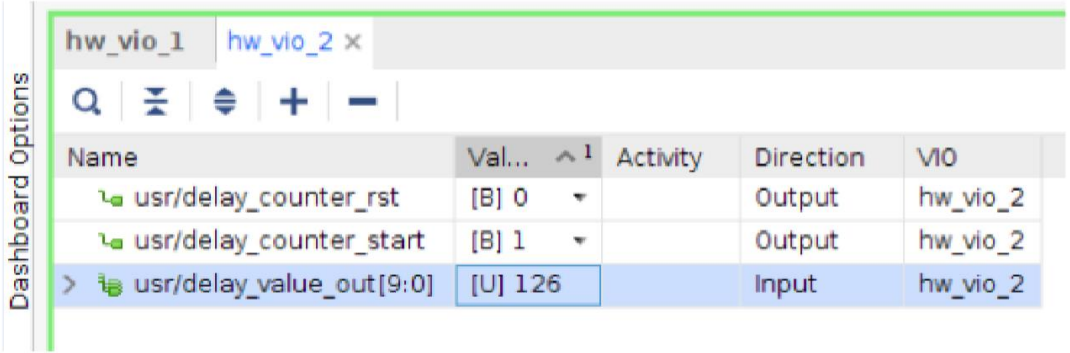
1. Send a probe signal through the link and start a synchronized counter.
2. FE receives the signal and sends it back (Loopback mode).
3. The signal returns to the BE and is detected by the system, ceasing the counting.
4. The delay between transmission and reception is used to estimate the Latency.



Counter main logic

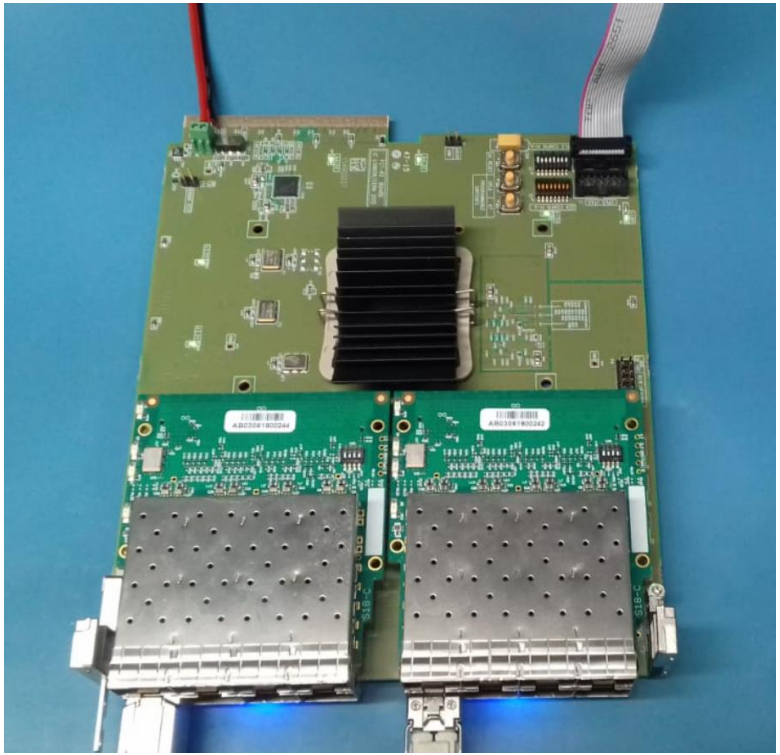


VIO interface in Vivado

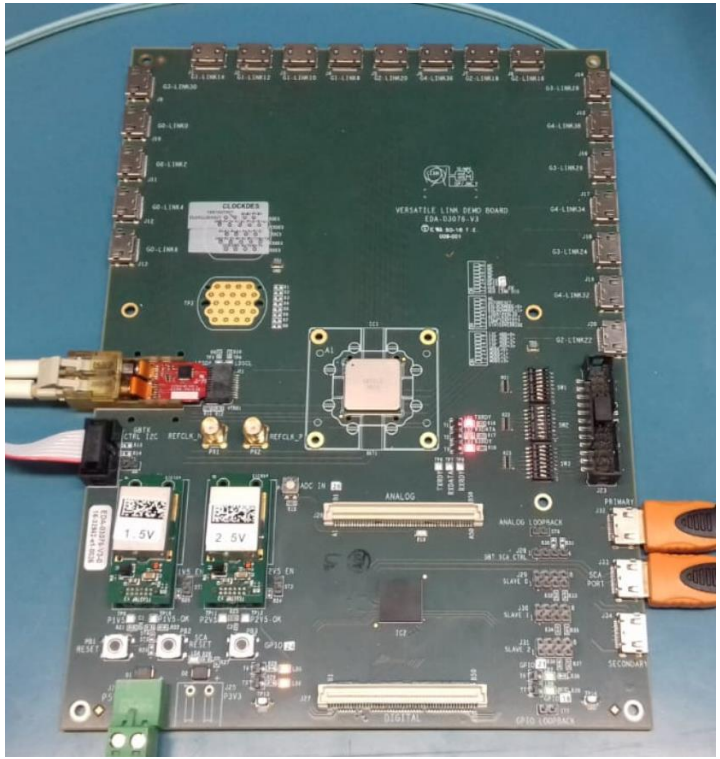


Hardware used

Back-End Board:
CERN FC7

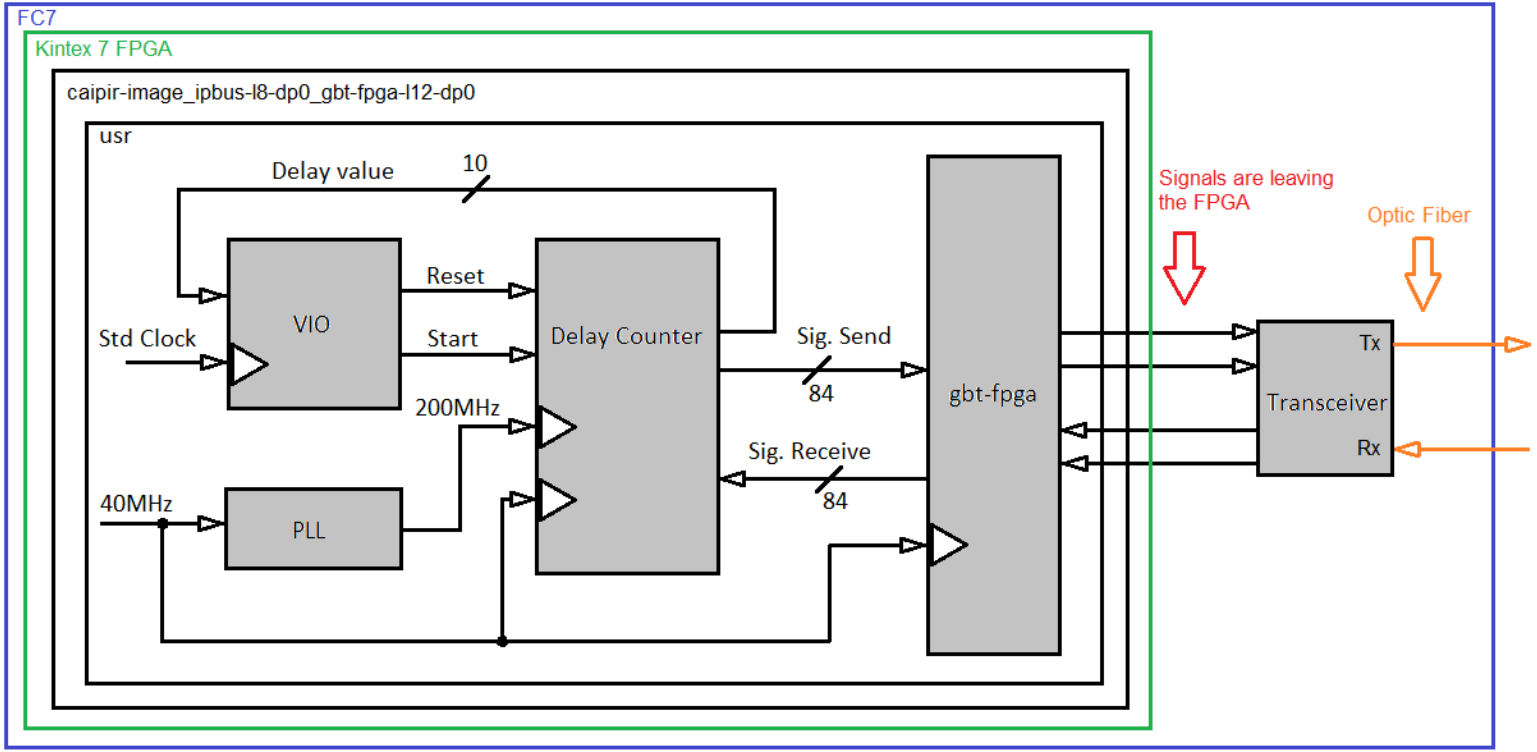


Front-End Board:
Versatile Link Demo Board (VLDB)



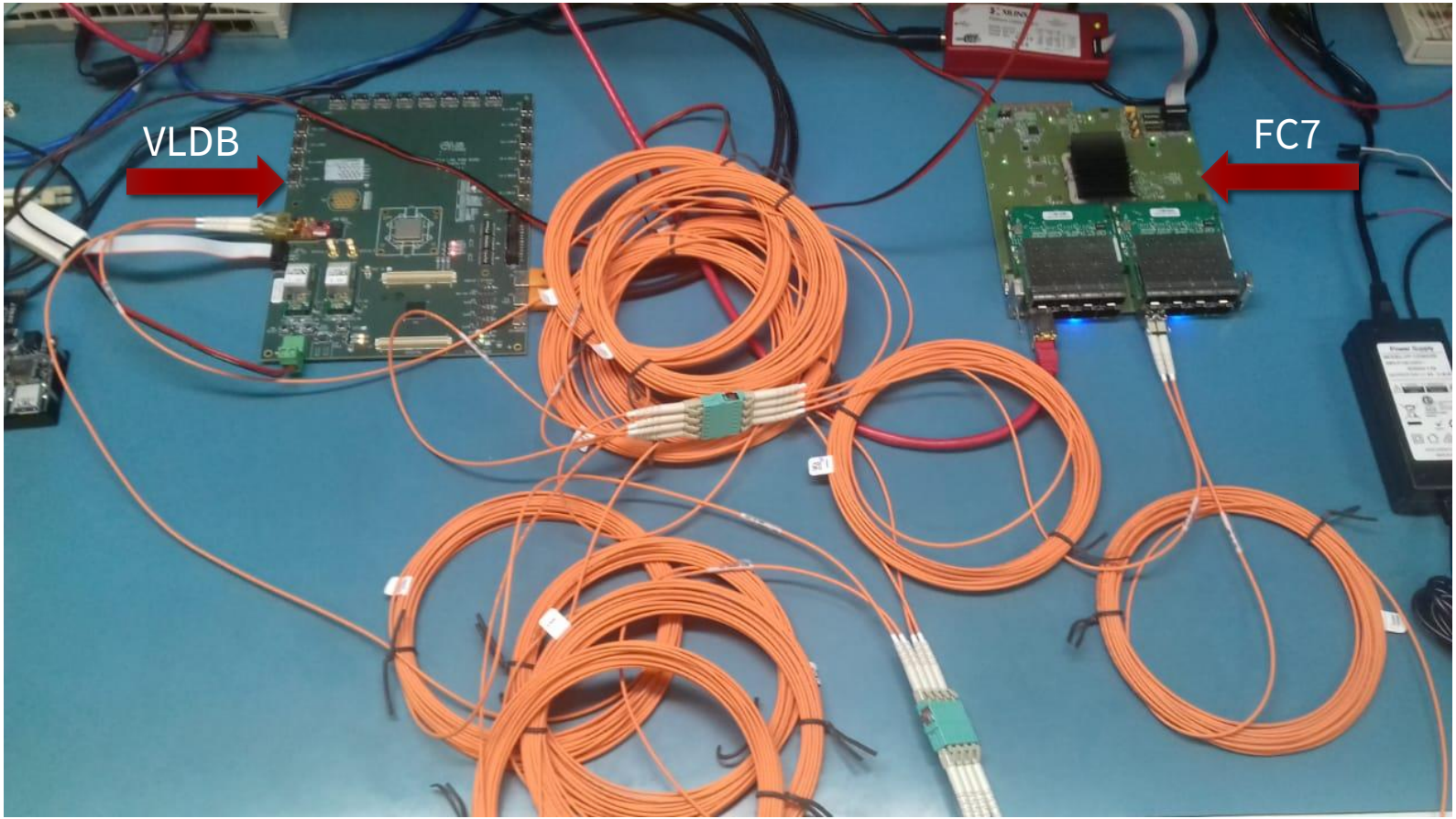
Implementation on the FC7 board

- Adapting the Delay Counter to work on the **caipir_image** firmware.
- Using the **gbt-fpga** data transmitting protocol to send the probe signal.

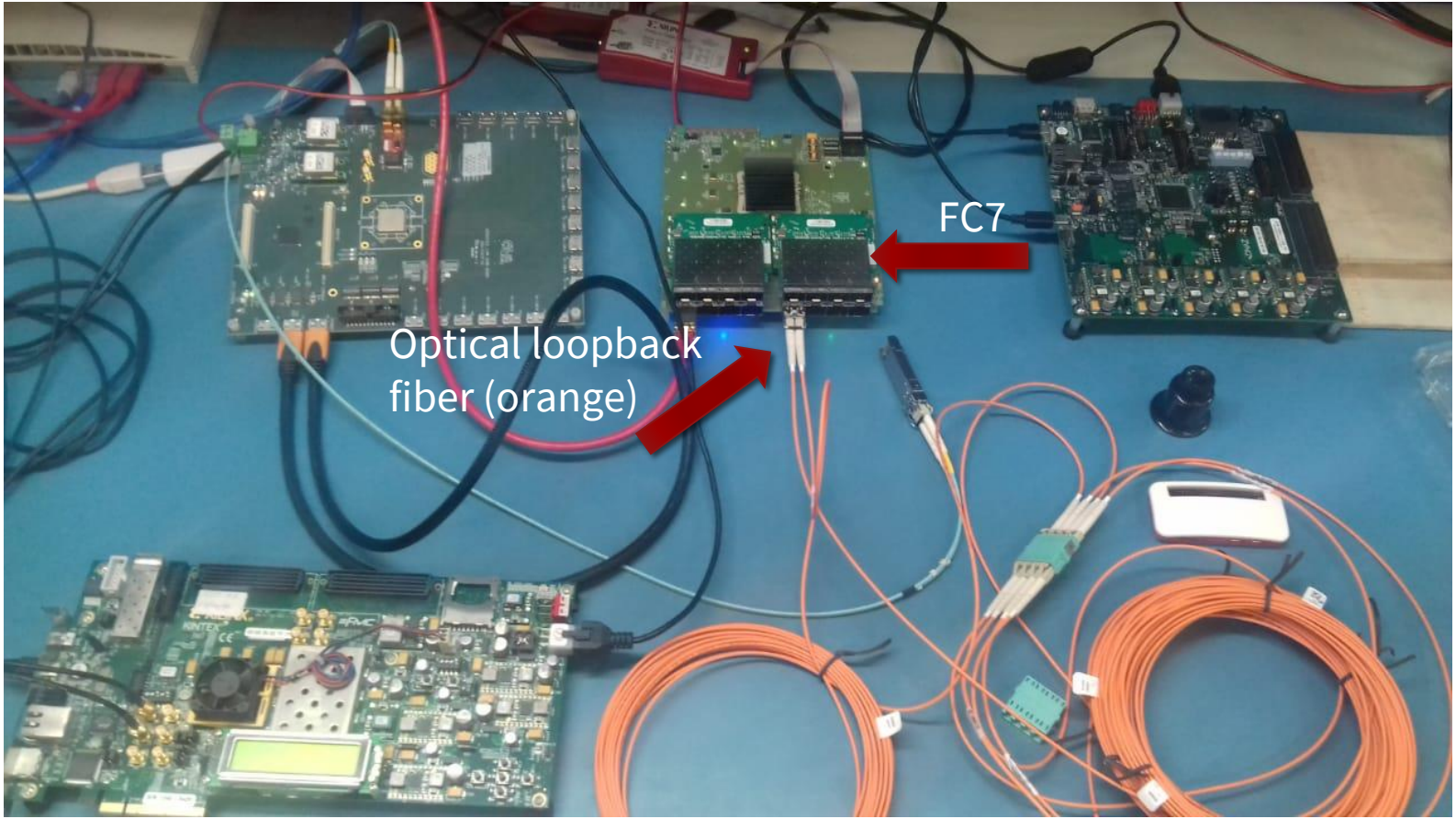


Tests and results

Link between Back-End and Front-End boards:



Link using only Back-End board:



Latency measurements results:

Latency Optimized (without FE board)		
EFFECTIVE MEASUREMENTS		
Length of the fiber (m)	Latency (clock cycles)	Latency (ns)
10	48	240
20	58	290
40	78	390
50	88	440
70	108	540
90	128	640

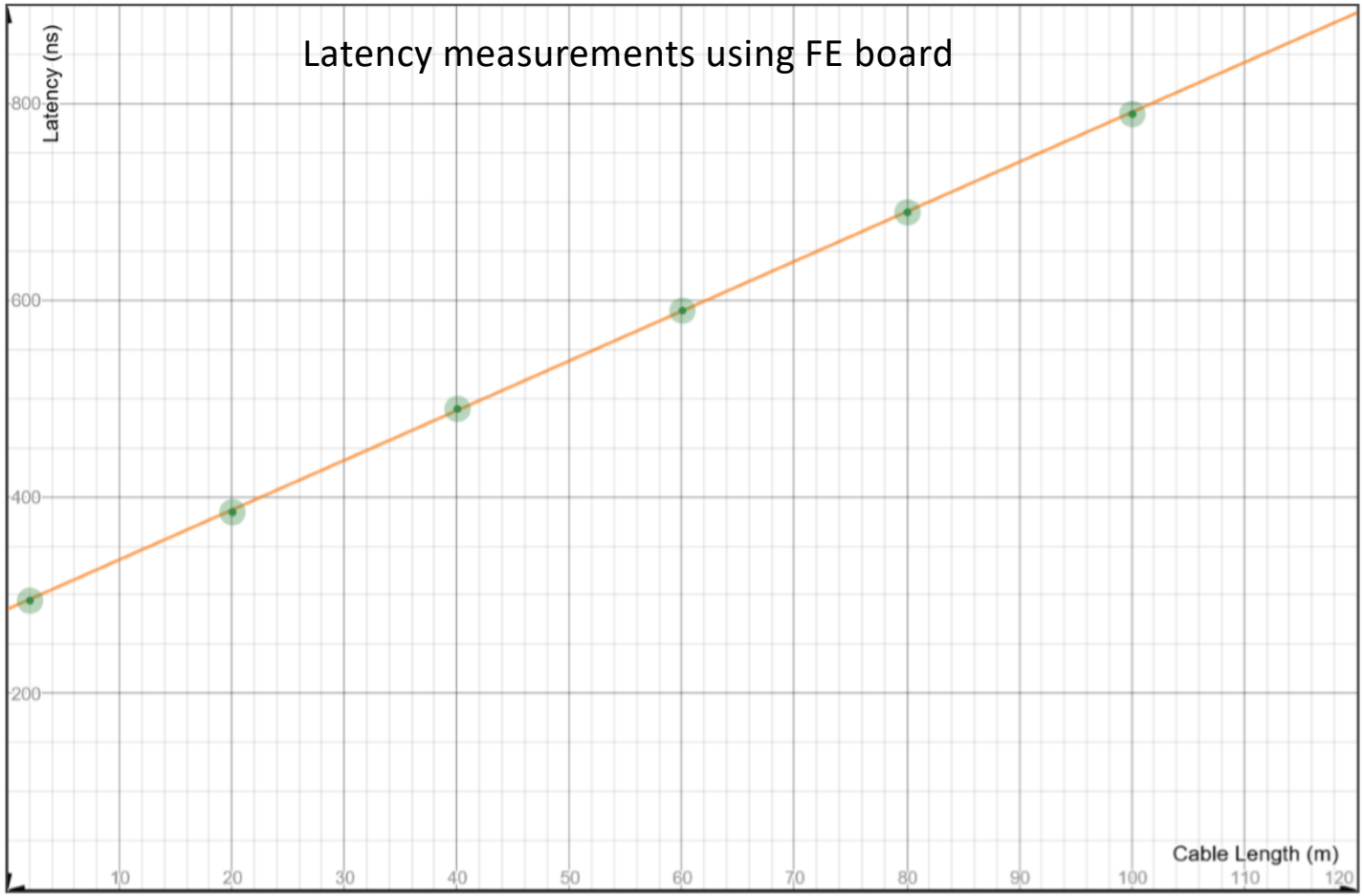
Latency Optimized (BE + FE boards)		
EFFECTIVE MEASUREMENTS		
Length of the fiber (m)	Latency (clock cycles)	Latency (ns)
2	59	295
20	77	385
40	98	490
60	118	590
80	138	690
100	158	790

- While the counter proceeds in steps of 5ns, the gbt-fpga and, most importantly, the GBTx use a data frame with an interval of 25ns.
- We believe that this is a limitation of using the GBTx in loopback mode.

Plots

Angular coefficient:
5.0578 ns/m

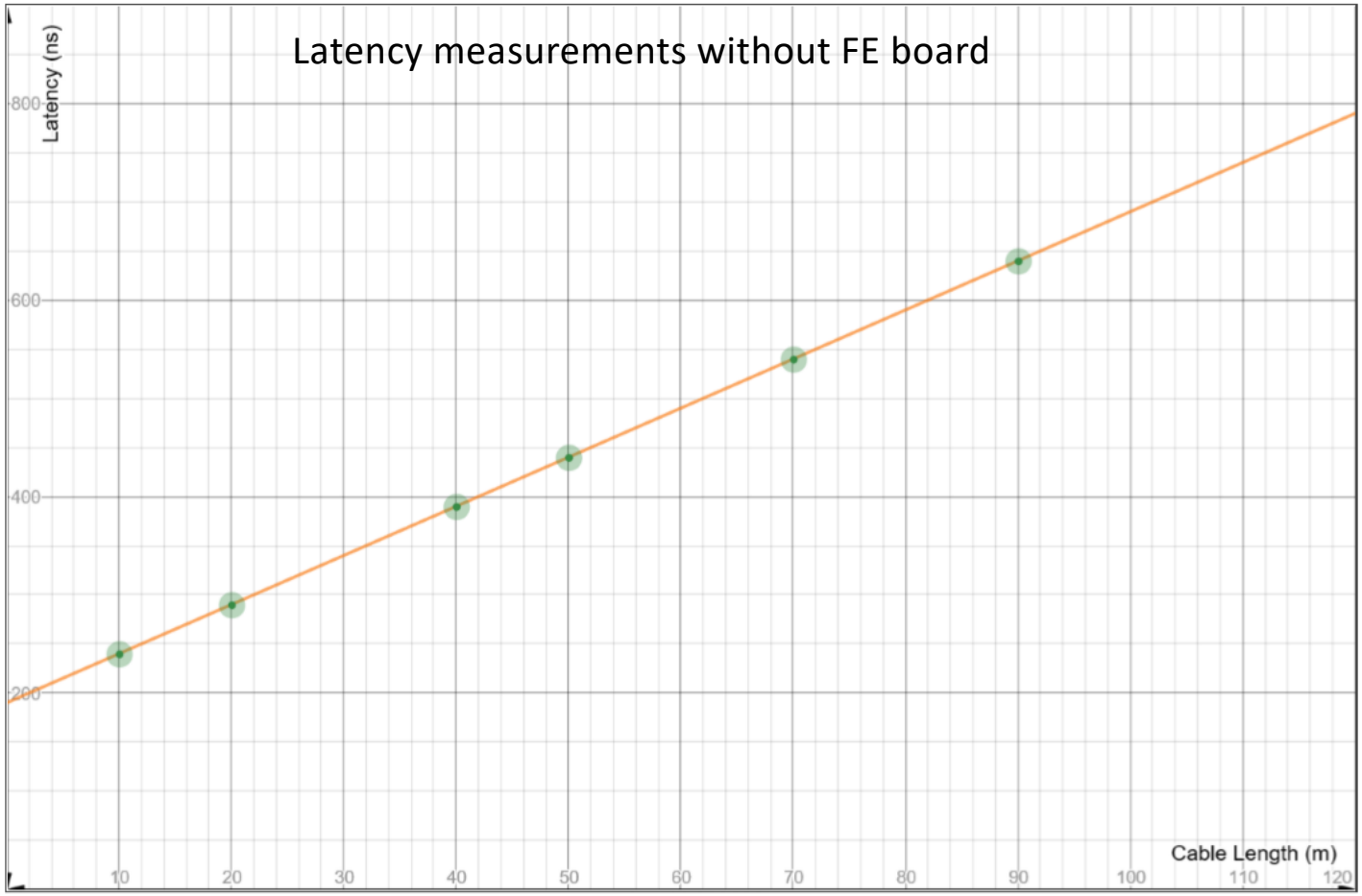
Additional term:
285.423 ns



Plots

Angular coefficient:
5.0000 ns/m

Additional term:
190.000 ns



Summary of results

Configuration	Latency Optimized	
Scenario	without FE	with FE
Latency per meter of optic fiber (ns/m)	5.0000	5.0578
GBT-FPGA Latency (ns)	190.000	190.000
GBTx Latency (ns)	Not used	95.423

Optical Fiber used: Multi Mode OM1
Laser wavelenght: 850nm

Using manufacturer's parameters:
Refractive Index: 1.496
Exp. latency for 100m cable: ~499ns

Using the Delay Counter subsystem:
Meas. latency for 100m cable: 505ns

Summary and outlook

- A firmware to measure the optical link latency has been produced.
  - The measurement precision is limited by the gbt frame interval (25ns).
- While the gbt-fpga may be modified we don't have control over the GBTx frame timing.
  - It may be very difficult, or impossible, to improve the measurement precision down to the current limit of the counter (5ns).
- We got news from the lpGBT developers that a latency measurement function would be available for the end users.

References

- GBT PROJECT. **GBTX MANUAL**. V0.16 Draft 22/10/2018. http://cern.ch/proj-gbt
- Fibre Fox. **Fibre Optic Cable – General Cable Specification**. http://fibrefox.co.uk
- Muschter, S. Bohm, C. Baron, S. Cachemiche, J. Soos, C. **Optimizing latency in Xilinx FPGA Implementations of the GBT.** 2010.
- Baron, S. **Versatile Link Demo Board**. BE/BI-PH-ESE GBT/VL meeting. 2015.
- CMS collaboration. **The Phase-2 Upgrade of the CMS Tracker**. Technical design report, july of 2017.
- Vahid, F. **Sistemas Digitais: Projeto, Otimização e HDLs**. 2008.
- VHDL codes of the Delay Counter firmware can be found in the SPRACE git hub repository.