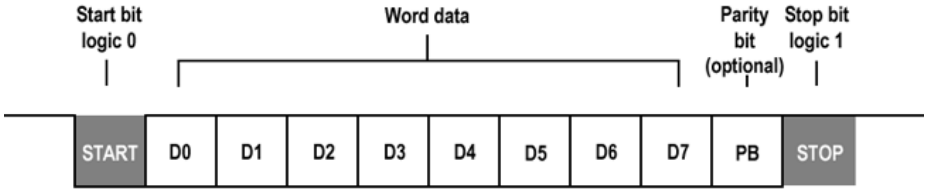
UART Receiver

The UART protocol is a serial protocol used for terminals of embedded systems. It can send words using different protocol configurations, in terms of:

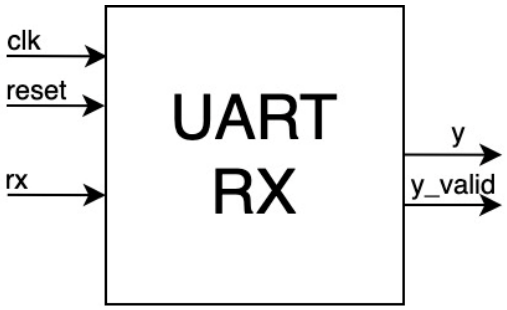
- Number of bits (W)
- Baud Rate (B)
- Parity (P)
- Number of stop bits (S)

In the following figure is reported an example with W = 8 and S = 1, P = Not Specified. When the serial line is idle, the value on the line must be 1.



The parity bit is set to 1 or 0 in order to match the parity defined by the protocol, e.g. in case of odd parity the number of 1s (parity bit included) must be odd.

Design a digital circuit that realises a receiver for the UART protocol with W = **7**, B = **115200**, P = **Even**, S = **2**. The interface of the circuit to be designed is as follows:



The receiver clock frequency is 8 times higher than the UART serial line one, in order to oversample the 'rx' signal and to synchronize the receiver with the START bit. The circuit emits new data on 'y' output indicating its validity with the 'y_valid' signal asserted for one clock cycle.

You are requested to deal with the various possible error situations, documenting the choices made.

The final project report must contain:

- Introduction (circuit description, possible applications, possible architectures, etc.)
- Description of the architecture designed (block diagram, inputs/outputs, etc.)
- VHDL code (with detailed comments) to be attached to the report.
- Test strategy (Test-plan) and related Testbench for verification; a detailed, though not exhaustive, verification is required, including error situations and borderline cases of functioning
- Interpretation of the results obtained in the automatic synthesis/implementation on a Xilinx FPGA platform in terms of maximum clock frequency (critical path), elements used (slice, LUT, etc.) and estimated power consumption. Comment on any warning messages.
- Conclusions