STN21xx

Multiprotocol OBD to UART Interpreter
Datasheet

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1.0 Overview

This datasheet summarizes the features of the STN21xx devices. It is not intended as a comprehensive reference source. To complement the information in this datasheet, refer to the **OBDLink® Family Reference and Programming Manual (FRPM).** We encourage you to download the latest FRPM from the OBD Solutions website (www.obdsol.com).

The STN2120 and STN2100 are OBD to UART interpreter ICs designed to provide bi-directional, half-duplex communication with the vehicle's On-Board Diagnostic system (OBD-II). They support all legislated OBD-II protocols, the STN2120 supports two additional proprietary networks: GM Single Wire CAN (GMLAN), and Ford Medium Speed CAN (MS CAN).

A wealth of information can be obtained by tapping into the OBD bus, including the status of the malfunction indicator light (MIL), diagnostic trouble codes (DTCs), inspection and maintenance (I/M) information, freeze frames, VIN, hundreds of real-time parameters, and more.

The STN21xx is fully compatible with the *de facto* industry standard ELM327 command set. Based on a 16-bit processor core, the STN21xx offers more features and better performance than any other ELM327 compatible IC.

2.0 Feature Highlights

- **Stable, field-tested firmware**
- Fully **compatible with the ELM327** AT command set
- Fully **backwards compatible with the STN1110 and STN1170**[2] command set
- **Extended ST command set**
- **UART interface** (baud rates from 62 bps to 8 Mbps[1])
- Secure **bootloader** for easy firmware updates
- Support for **all legislated OBD-II protocols:**
  - ISO 15765-4 (CAN)
  - ISO 14230-4 (Keyword Protocol 2000)
  - ISO 9141-2 (Asian, European, Chrysler vehicles)
  - SAE J1850 VPW (GM vehicles)
  - SAE J1850 PWM (Ford vehicles)
- Support for **non-legislated OBD protocols:**
  - ISO 15765
  - ISO 11898 (raw CAN)
  - GMLAN Single Wire CAN[2] (GMW3089)
  - Ford Medium Speed CAN[2] (MS CAN)
- Support for the heavy-duty **SAE J1939 OBD protocol**
- Superior **automatic protocol detection** algorithm
- **Large message buffer**
- Sophisticated **PowerSave Sleep/Wakeup Triggers**
- Available in **QFN** package
- **RoHS** compliant

Note 1: Maximum theoretical baud rate. Actual maximum baud rate is application dependent and may be limited by driver hardware.
Note 2: STN2120 IC only

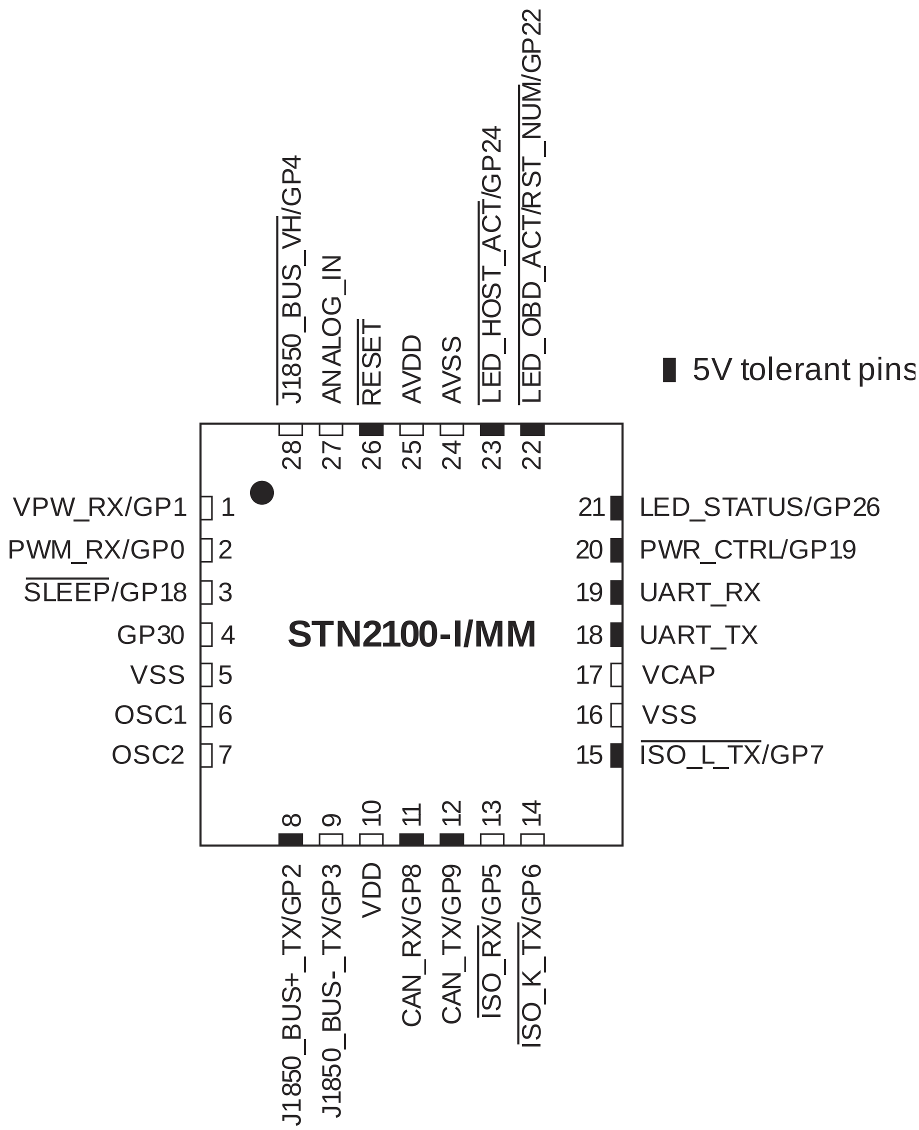
3.0 Typical Applications

- Vehicle telematics
- Fleet management and tracking applications
- Usage-based insurance (UBI)
- OBD data loggers
- Automotive diagnostic scan tools and code readers
- Digital dashboards

4.0 Pinouts

4.1 STN2100

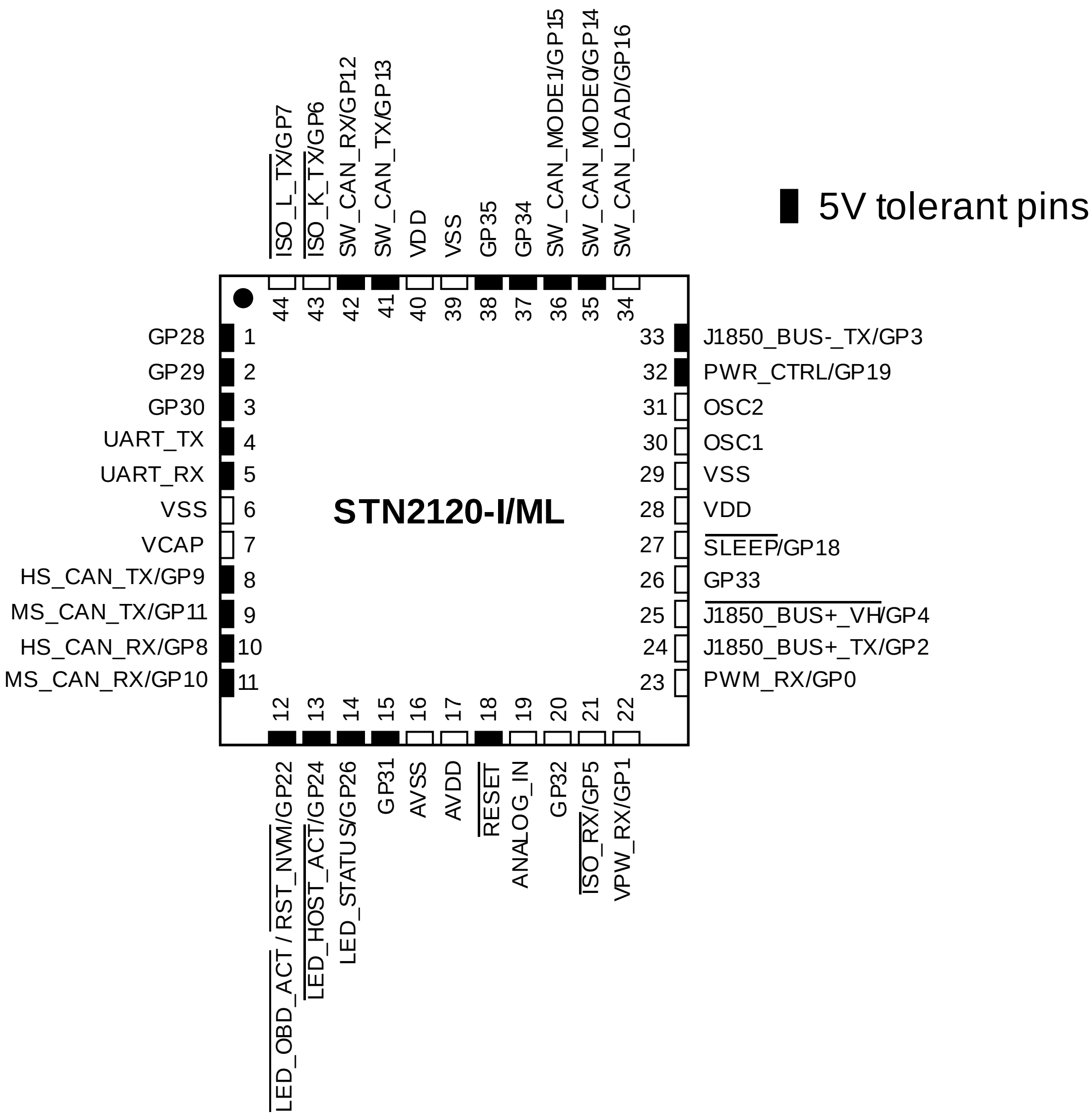
Figure 1 - STN2100 QFN(1)



Note 1. The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4.2 STN2120

Figure 2 - STN2120 QFN[1]



Note 1. The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4.3 Pinout Summary

Table 1: Pinout Summary

Pin Name	STN2100 Pin Type	STN2120 Pin Type	Pin Description
GP28	—	5V, 8x,	General purpose I/O pin
GP29	—	5V, 4x	General purpose I/O pin
GP30	4x	5V, 4x	General purpose I/O pin
UART_TX	OD, 5V, 8x	OD, 5V, 4x	UART transmit output
UART_RX	I, 5V, 8x	I, 5V, 4x	UART receive input
V_{SS}	P	P	Ground reference for logic and I/O pins
VCAP	P	P	CPU logic filter capacitor connection
HS_CAN_TX/GP9	OD, 5V, 4x	OD, 5V, 8x	High-speed CAN transmit output
MS_CAN_TX/GP11	—	OD, 5V, 8x	Medium-speed CAN transmit output
HS_CAN_RX/GP8	I, 5V, 4x	I, 5V, 8x	High-speed CAN receive input
MS_CAN_RX/GP10	—	I, 5V, 8x	Medium-speed CAN receive input
$\overline{\text{LED\_OBD\_ACT}}$/$\overline{\text{RST\_NVM}}$/GP22	OD/I, 5V, 8x	OD/I, 5V, 4x	Active low OBD activity LED output *and* active low input to reset non-volatile settings to factory defaults
$\overline{\text{LED\_HOST\_ACT}}$/GP24	OD, 5V, 8x	O, 4x	Active low host activity LED output
LED_STATUS/GP26	5V, 8x	O, 8x	Status LED output
GP31	—	5V, 8x	General purpose I/O pin
AV_{SS}	P	P	Analog ground reference
AV_{DD}	P	P	Analog positive supply
$\overline{\text{RESET}}$	I, 5V, 4x	I, 5V	Active low device reset input
ANALOG_IN	A	A	Analog voltage measurement input
GP32	—	4x	General purpose I/O pin
$\overline{\text{ISO\_RX}}$/GP5	I, 8x	I, 4x	Active low ISO 9141/ISO 14230 K-line input
VPW_RX/GP1	I, 4x	I, 4x	SAE J1850 VPW receive input
PWM_RX/GP0	I, 4x	I, 4x	SAE J1850 PWM receive input
J1850_BUS+_TX/GP2	5V, 4x	O, 4x	SAE J1850 Bus+ transmit output
$\overline{\text{J1850\_BUS+\_VH}}$/GP4	O, 4x	O, 4x	SAE J1850 PWM/VPW Bus+ high voltage select output
GP33	—	4x	General purpose I/O pin
$\overline{\text{SLEEP}}$/GP18	I, 4x	I, 4x	External sleep control input
V_{DD}	P	P	Positive supply for logic and I/O pins
V_{SS}	P	P	Ground reference for logic and I/O pins
OSC1	I	I	16.000 MHz oscillator crystal input
OSC2	0	O	16.000 MHz oscillator crystal output
PWR_CTRL/GP19	OD, 5V, 8x	OD, 4x	External power control output
J1850_BUS-_TX/GP3	O, 8x	O, 4x	SAE J1850 Bus- transmit output

Pin Name	STN2100 Pin Type	STN2120 Pin Type	Pin Description
SW_CAN_LOAD/GP16	—	O, 8x	Single-wire CAN high-speed tool load enable output
SW_CAN_MODE0/GP14	—	OD, 8x	Single-wire CAN transceiver operating mode selection output 0
SW_CAN_MODE1/GP15	—	OD, 8x	Single-wire CAN transceiver operating mode selection output 1
GP34	—	5V, 4x	General purpose I/O pin
GP35	—	5V, 4x	General purpose I/O pin
V_{SS}	P	P	Ground reference for logic and I/O pins
V_{DD}	P	P	Positive supply for logic and I/O pins
SW_CAN_TX/GP13	—	OD, 4x	Single-wire CAN transmit output
SW_CAN_RX/GP12	—	I, 5V, 4x	Single-wire CAN receive input
$\overline{\text{ISO\_K\_TX}}$/GP6	O, 8x	O, 8x	Active low ISO 9141/ISO 14230 K-line output
$\overline{\text{ISO\_L\_TX}}$/GP7	5V, 8x	O, 8x	Active low ISO 9141/ISO 14230 L-line output
PAD	P	P	Thermal pad

Legend:
I – Schmitt trigger input with CMOS levels
A – analog input
P – power pin
O – digital output
OD – open drain output
5V – 5 volt tolerant pin
2x – 2x source/sink driver
4x – 4x source/sink driver
8x – 8x source/sink driver

Note 1: Excessive continuous power cycling may cause failure of the IC. See Section 5.10 “Power and Sleep Considerations”
Note 2: General purpose pins (GPIO) can be configured for open drain outputs or pull ups. See Section 4.4 “GPxx”.

4.4 Detailed Pin Descriptions

ANALOG_IN

Analog voltage measurement input (AVDD max). By default, this input is calibrated for an external 62 kΩ/10 kΩ voltage divider connected to battery positive. Connect to AVSS if unused.

AVDD

Analog positive supply. Must be connected to VDD or an external voltage reference (between VDD - 0.3V or 3.0V, whichever is greater and VDD + 0.3V or 3.6V, whichever is less). AVDD may be decoupled from digital supply by connecting it to VDD via a 10 Ω resistor or a small (10 µH – 47 µH) inductor.

AVss

Analog ground reference. Must be connected to analog “clean” ground (between VSS - 0.3V and VSS + 0.3V) or VSS.

GPxx

General purpose input/output (GPIO) pins. There are two types of GPIOs: dedicated and multiplexed.

Dedicated GPIO pins support only GPIO functionality and are Hi-Z inputs by default. GPIO pins have internal pull-ups that can be enabled when the corresponding pin is configured as an input. GPIO pins can also be configured as open-drain outputs. When configured as open-drain outputs, GPIO pins must be connected to external pull-up resistors; do not leave them floating. Connect unused dedicated GPIO pins to VSS.

Multiplexed GPIOs share the physical pin with other functions (e.g., OBD transceivers, LEDs). The name of the pin defines the priority of each function associated with the pin. Attempting to control GPIO pins when the default multiplexed functionality is not disabled can lead to unpredictable behavior. For example, before HOST_ACT_LED/GP24 pin can be used as GPIO, LEDs must be disabled (see STUIL command description in OBDLink® FRPM). Consult individual pin descriptions for instructions on what to do when the pin is unused.

HS_CAN_RX

High-speed CAN receive input. Compatible with 3.3V and 5V logic. Pull up to VDD if unused.

HS_CAN_TX

High-speed CAN transmit output. Open drain – requires a pull-up to VDD or 5V. Pull-up value depends on CAN baud rates used and the trace length (higher resistor values can be used with lower baud rates and shorter traces); recommended value is 1 kΩ. Pull up to VDD via 100 kΩ resistor if unused.

$\overline{\text{ISO\_K\_TX}}$

Active low ISO 9141/ISO 14230 K-line output. When the pin is logic high, K-line should be low. Leave unconnected if unused.

$\overline{\text{ISO\_L\_TX}}$

Active low ISO 9141/ISO 14230 L-line output. When the pin is logic high, L-line should be low. Leave unconnected if unused.

$\overline{\text{ISO\_RX}}$

Active low ISO 9141/ISO 14230 K-line receive input. When K-line is high (recessive), this pin should be at a logic low level. Connect to VSS if unused.

J1850_BUS+_TX

SAE J1850 Bus+ transmit output. When the pin is high, Bus+ should be high (dominant). Leave unconnected if unused.

J1850_BUS-_TX

SAE J1850 Bus- transmit output. When the pin is high, Bus- should be low (dominant). Leave unconnected if unused.

J1850_BUS+_VH

The firmware uses this pin to control the voltage level of the SAE J1850 PWM/VPW Bus+ supply. When the PWM protocol is selected, it outputs a logic high to switch the supply voltage to a nominal 5V. When the VPW protocol is selected, it outputs a logic low to switch the supply voltage to a nominal 8V. Leave unconnected if unused.

LED_HOST_ACT

Active low host activity LED output. Leave unconnected if unused.

LED_OBD_ACT/RST_NVM

Active low OBD activity LED output and active low input to reset NVM to factory defaults. Must be pulled up to Vdd via a 100 kΩ resistor for proper device operation.

LED_STATUS

Status LED output. This pin will output constant high when the device is running and will output low with 5 ms high pulses every 3 seconds when in sleep mode. Leave unconnected if unused.

MS_CAN_RX

Medium-speed CAN receive input. Compatible with 3.3V and 5V logic. Pull up to Vdd if unused.

MS_CAN_TX

Medium-speed CAN transmit output. Open drain – requires a pull-up to Vdd or 5V. Pull-up resistor value depends on CAN baud rates used and the trace length (higher resistor values can be used with lower baud rates and shorter traces); recommended value is 1 kΩ (1.5 kΩ, if pulled up to 5V). Pull up to Vdd via 100 kΩ resistor if unused.

OSC1, OSC2

16.000 MHz oscillator crystal connection.

PAD

The metal plane on the bottom of the device (QFN package only). It is not connected to any pins internally. Connect to Vss externally.

PWM_RX

SAE J1850 PWM receive input. When the SAE J1850 bus is in the recessive state (Bus+ is low, Bus- is high), this pin should be at a logic low level. When the SAE J1850 bus is in the dominant (Bus+ is high) state, this pin should be at a logic high level. Connect to Vss if unused.

PWR_CTRL

External power control output. Used to switch external circuitry into low-power (sleep) state. Polarity can be configured in firmware; default configuration is active high (logic low = sleep mode). Open drain – requires a pull-up to Vdd or 5V; be mindful of the fact that the pull-up will draw current in low-power state. Pull down to Vss via 100 kΩ resistor if unused.

RESET

Device reset input. A logic low pulse (min 2 µs) on this pin will reset the device. Apply a continuous logic low to hold the device in reset. If your circuit does not use this functionality, pull up this pin to Vdd.

SLEEP

External sleep control input. When enabled in firmware, puts the device into low-power sleep mode. Polarity of this pin can be configured in firmware; default configuration is active low. Pull up to Vdd if unused.

SW_CAN_LOAD

Single-wire CAN high-speed tool load enable output. The pin outputs logic high when high-speed tool load is enabled via the STCSWM command. Leave unconnected if unused.

SW_CAN_MODE0, SW_CAN_MODE1

Single-wire CAN transceiver operating mode selection outputs. Connect to MODE0, MODE1 pins of a single-wire CAN transceiver IC. Open drain – require pull-ups to Vdd or 5V; recommended value is 10 kΩ. Both pins are driven low in sleep mode – it is recommended to pull up to a switched power to reduce power consumption during sleep. Leave unconnected if unused.

SW_CAN_RX

Single-wire CAN receive input. Compatible with 3.3V and 5V logic. Pull up to Vdd if unused.

SW_CAN_TX

Single-wire CAN transmit output. Open drain – requires a pull-up to Vdd or 5V. Pull-up resistor value depends on CAN baud rates used and the trace length (higher resistor values can be used with lower baud rates and shorter traces); recommended value is 1 kΩ (1.5 kΩ, if pulled up to 5V). Pull up to Vdd via 100 kΩ resistor if unused.

UART_RX

UART receive input. Compatible with 3.3V and 5V logic.

UART_TX

UART transmit output. Open drain – requires a pull-up to Vdd or 5V. Pull-up value depends on UART baud rate and the trace length (higher resistor values can be used with lower baud rates and shorter traces); typical value is 1 kΩ (1.5 kΩ, if pulled up to 5V).

VCAP

CPU logic filter capacitor connection. Connect to a low-ESR (< 1 Ω) tantalum or ceramic capacitor. Minimum value is 4.7 µF; typical value is 10 µF.

VDD

Positive 3.0 – 3.6V supply for logic and I/O pins.

VPW_RX

SAE J1850 VPW receive input. When the SAE J1850 Bus+ is in the recessive (low) state, this pin should be at a logic low level. When the SAE J1850 Bus+ is in the dominant (high) state, this pin should be at a logic high level. Connect to Vss if unused.

Vss

Ground reference for logic and I/O pins.

5.0 Guidelines for Getting Started with STN21xx

5.1 Basic Connection Requirements

Getting started with the STN21xx IC requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All **VDD and VSS** pins (see Section 5.2 "Decoupling Capacitors")
- **AVDD and AVSS** pins (see Section 5.2 "Decoupling Capacitors" and Section 5.4 "AVDD and AVSS Pins")
- **VCAP** (see Section 5.5 "Internal Voltage Regulator Filter Capacitor")
- **$\overline{\text{RESET}}$** pin (see Section 5.7 "Device Reset Pin")
- **OSC1 and OSC2** pins (see Section 5.6 "Oscillator Pins")
- **$\overline{\text{RST\_NVM}}$** pin (see Section 5.8 "NVM Reset Input")
- **Open Drain Output Pull-ups** (see Section 5.9 "Open Drain Outputs")

5.2 Decoupling Capacitors

You must use decoupling capacitors on every pair of power supply pins, such as VDD, VSS and AVDD, AVSS. Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 1 µF, 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within ¼" (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

5.3 Tank Capacitors

On boards with power traces running longer than six inches in length, use a tank capacitor for integrated circuits, including the STN21xx, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

5.4 AVDD and AVSS Pins

As a minimum, AVDD must be connected directly to VDD and AVSS must be connected directly to VSS.

It is recommended that AVDD be connected to to VDD via a 10 Ω resistor or a small (10 µH – 47 µH) inductor.

AVSS should be connected to the electrically cleanest ground net (plane). For best results, analog circuitry should have a separate ground plane with a point connection to VSS ground plane as close as possible to the AVSS pin.

5.5 Internal Voltage Regulator Filter Capacitor

A low-ESR (< 1 Ω) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must have a capacitor between 4.7 µF and 10 µF, 16V connected to ground. The type can be ceramic or tantalum. Refer to Section 7.2 "Electrical Characteristics" for additional information. The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceed ¼" (6 mm).

5.6 Oscillator Pins

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the STN21xx ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

5.7 Device Reset Pin

$\overline{\text{RESET}}$ pin must be logic high for STN21xx to run. If this pin is not controlled by the host controller, it must be connected to V_{DD}.

It is recommended to pull up $\overline{\text{RESET}}$ pin to V_{DD} via a 10 kΩ resistor.

5.8 NVM Reset Input

All programmable parameters will be turned off and reset to their default values by holding $\overline{\text{RST\_NVM}}$ input low for 5 seconds. After $\overline{\text{RST\_NVM}}$ input is released, device will set all factory defaults, and then perform an ATZ reset.

$\overline{\text{RST\_NVM}}$ pin must be pulled up to V_{DD} via a 100 kΩ resistor for proper device operation.

5.9 Open Drain Outputs

All open drain outputs (as specified in section 4.3) that are in use must be pulled up to V_{DD} or 5V. Specifically, UART_TX pin must be pulled up in order to be able to communicate with the device. See section 4.4 “Detailed Pin Descriptions” for more information.

5.10 Power and Sleep Considerations

While it is possible to disconnect the V_{DD}/AV_{DD} pins from the power source to reduce power consumption, we recommend using the PowerSave functionality instead (see the OBDLink® Family Reference and Programming Manual).

Be warned that continuous power cycling may cause failure of the IC.

5.11 Unused Inputs and Unused Open Drain Outputs

None of the unused inputs or unused open drain outputs (as specified in section 4.3) should be left unconnected. The STN21xx is a CMOS integrated circuit. Leaving any of its inputs or open drain outputs floating may result in IC damage.

Unused open drain outputs can only be terminated with a resistor connected to V_{DD} or 5V. Unused inputs can be terminated via a resistor or direct connection to V_{SS} or V_{DD}.

Unused inputs and open drain outputs should be connected as shown in Table 3 and Table 2. See section 4.4 “Detailed Pin Descriptions” and section 6.1 “Recommended Minimum Connection” for more information.

Table 2: STN2100 Recommended Unused Input and Open Drain Output Connections

Pin #	Pin Name	Level
1	$\overline{\text{VPW\_RX}}$/GP1	L[1]
2	PWM_RX/GP0	L[1]
3	$\overline{\text{SLEEP}}$/GP18	H
11	HS_CAN_RX/GP8	H
12	HS_CAN_TX/GP9	H[2]
13	$\overline{\text{ISO\_RX}}$/GP5	L[1]
18	UART_TX	H[2]
19	UART_RX	H
20	PWR_CTRL/GP19	L[3]
22	$\overline{\text{LED\_OBD\_ACT/RST\_NVM}}$ /GP22	H[2]
23	$\overline{\text{LED\_HOST\_ACT}}$/GP24	H[2]
26	$\overline{\text{RESET}}$	H
27	ANALOG_IN	L[1]

Note
1. These inputs may be connected to either VDD or VSS. However, the preferred level is shown.
2. These open drain outputs cannot be connected to VDD directly. They can only be connected to VDD or 5V via a resistor.
3. This open drain output should not be connected to VSS directly. For reduced current consumption during sleep, when unused, this output should be connected to VSS via a resistor.
4. General purpose I/O pins are configured as inputs by default. When unused, these inputs may be connected to either VDD or VSS.

Table 3: STN2120 Recommended Unused Input and Open Drain Output Connections

Pin #	Pin Name	Level
1	GP28	L[5]
2	GP29	L[5]
3	GP30	L[5]
4	UART_TX	H[2]
5	UART_RX	H
8	HS_CAN_TX/GP9	H[2]
9	MS_CAN_TXGP11	H[2]
10	HS_CAN_RX/GP8	H
11	MS_CAN_RX/GP10	H
12	$\overline{\text{LED\_OBD\_ACT/RST\_NVM}}$ /GP22	H[2]
15	GP31	L[5]
18	$\overline{\text{RESET}}$	H
19	ANALOG_IN	L[1]
20	GP32	L[5]
21	$\overline{\text{ISO\_RX}}$/GP5	L[1]
22	VPW_RX/GP1	L[1]
23	PWM_RX/GP0	L[1]
26	GP33	L[5]
27	$\overline{\text{SLEEP}}$/GP18	H
32	PWR_CTRL/GP19	L[3]
35	SW_CAN_MODE0/GP14	—[4]
36	SW_CAN_MODE1/GP15	—[4]
37	GP34	L[5]
38	GP35	L[5]
41	SW_CAN_TX/GP13	H[2]
42	SW_CAN_RX/GP12	H

Note
1. These inputs may be connected to either VDD or VSS. However, the preferred level is shown.
2. These open drain outputs cannot be connected to VDD directly. They can only be connected to VDD or 5V via a resistor.
3. This open drain output should not be connected to VSS directly. For reduced current consumption during sleep, when unused, this output should be connected to VSS via a resistor.
4. These open drain outputs are driven low when the single-wire CAN channel is not selected. Therefore, they can be left unconnected if single wire CAN is not used.
5. General purpose I/O pins are configured as inputs by default. When unused, these inputs must be connected to either VDD or VSS.

6.0 Reference Schematics

6.1 Recommended Minimum Connections

Figure 3 shows the recommended minimum of components necessary to get the STN2100 to operate reliably, while minimizing power consumption.

This is not a practical circuit; it is intended as a reference to show what to do with any unused pins. Refer to the detailed pin descriptions (Section 4.4) for more information.

Figure 3 - STN2100 Minimum Connections

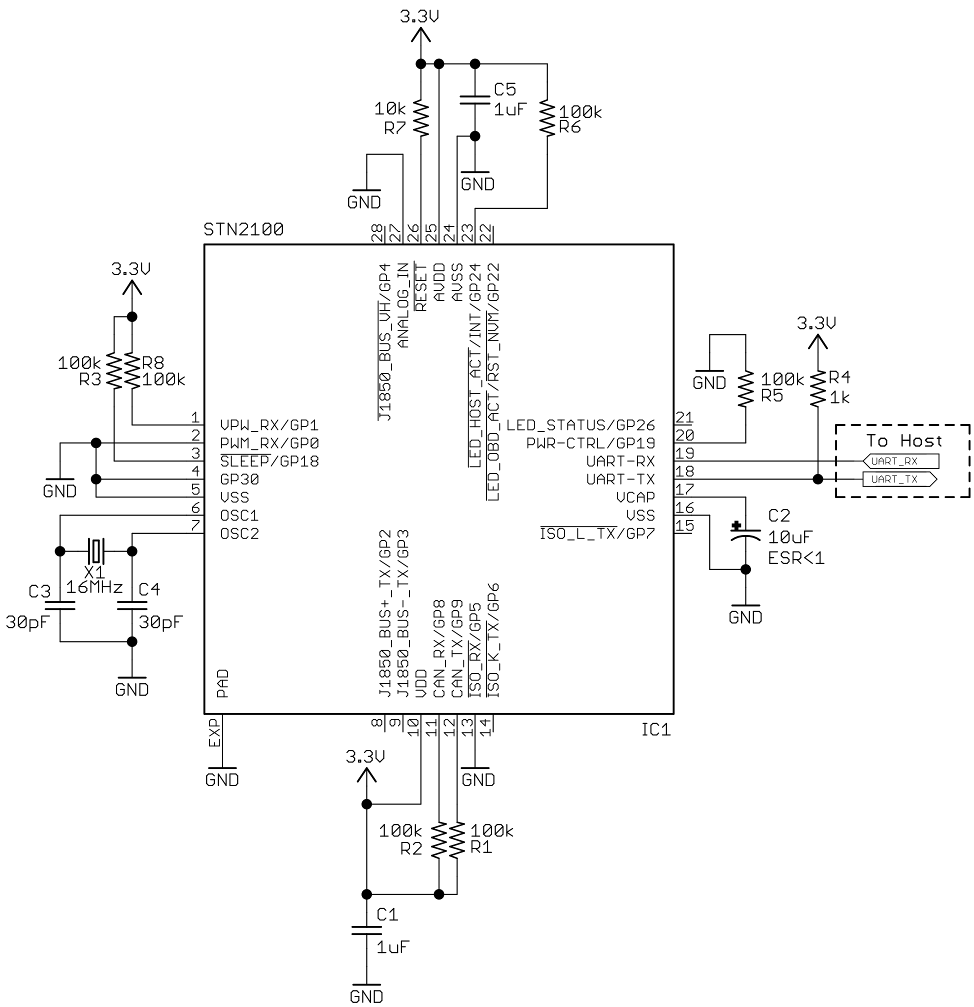
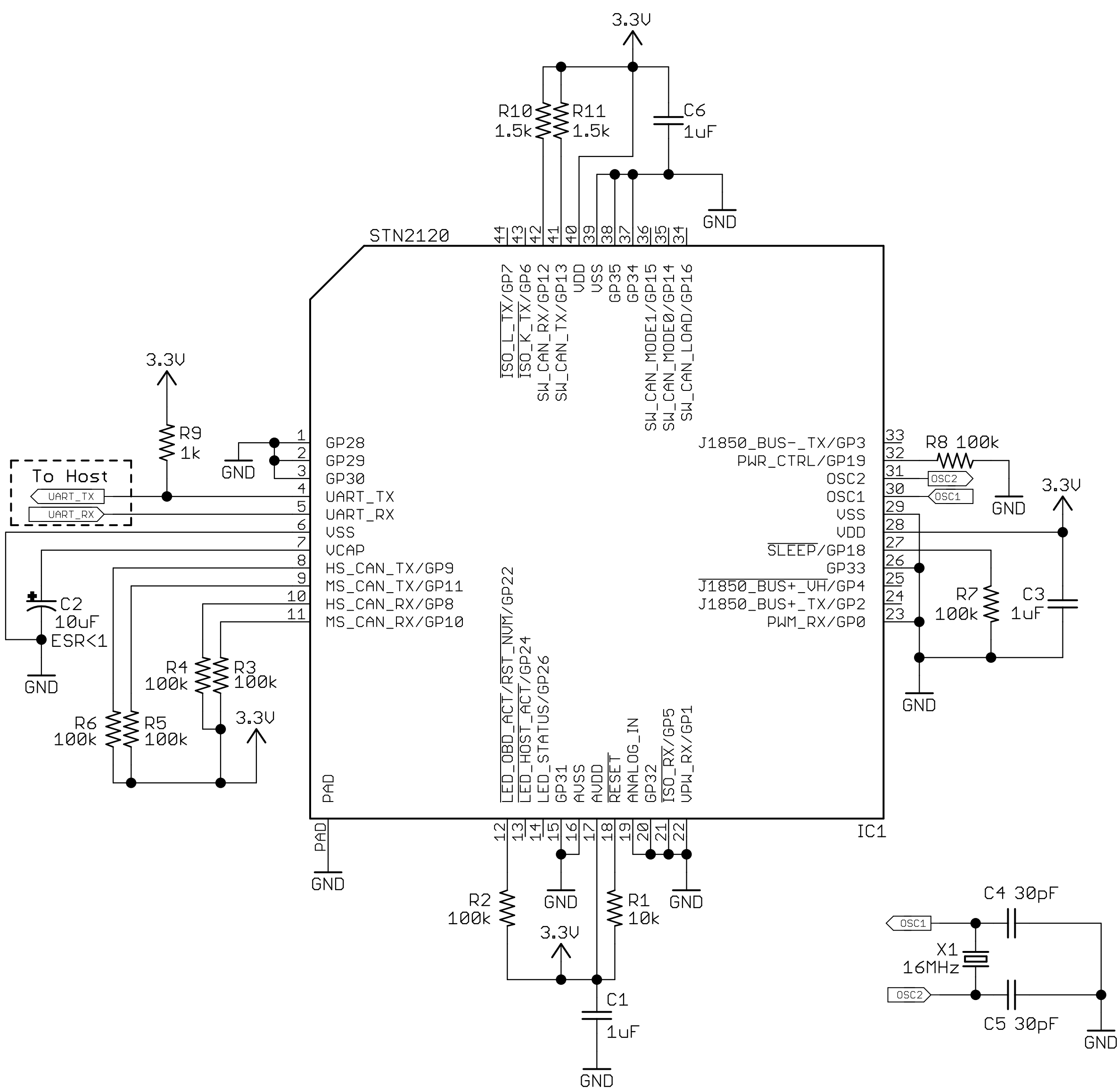


Figure 4 shows the recommended minimum of components necessary to get the STN2120 to operate reliably, while minimizing power consumption.

This is not a practical circuit; it is intended as a reference to show what to do with any unused pins. Refer to the detailed pin descriptions (Section 4.4) for more information.

Figure 4 - STN2120 Minimum Connections



6.2 Typical Configuration

This section contains schematics showing the typical configuration for the various circuit blocks. In this revision, the circuit blocks have been designed to meet the requirements of a “permanently attached device” scenario: low power consumption in sleep, and protection against interference with the OBD bus.

Pay special attention when choosing substitutes for components with specific part numbers, to make sure they have the same or better characteristics. Components without specific part numbers are generic. Use good engineering practices and common sense to make sure the specific parts you choose are appropriate for your application.

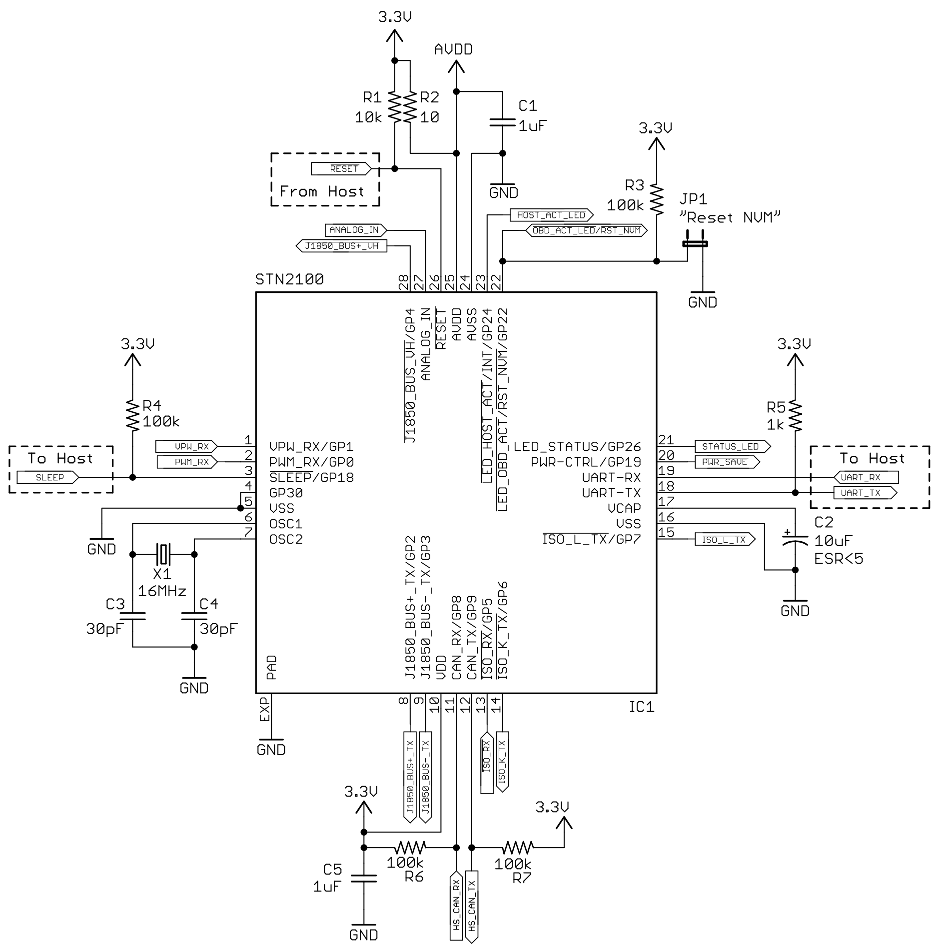
Also see **Note 1** on page 18 that applies to both STN2120 and STN2100 configurations.

6.2.1 STN2100 IC

Figure 5 shows the circuit block for the STN2100 IC, including:

- **Pull-up resistors** (Section 4.4)
- **Decoupling capacitors** (Section 5.2)
- **VCAP** (Section 5.5)
- **Crystal oscillator** (Section 5.6)
- **RESET pin** (Section 5.7)
- **RST_NVM pin** (Section 5.8)

Figure 5 - STN2100 IC

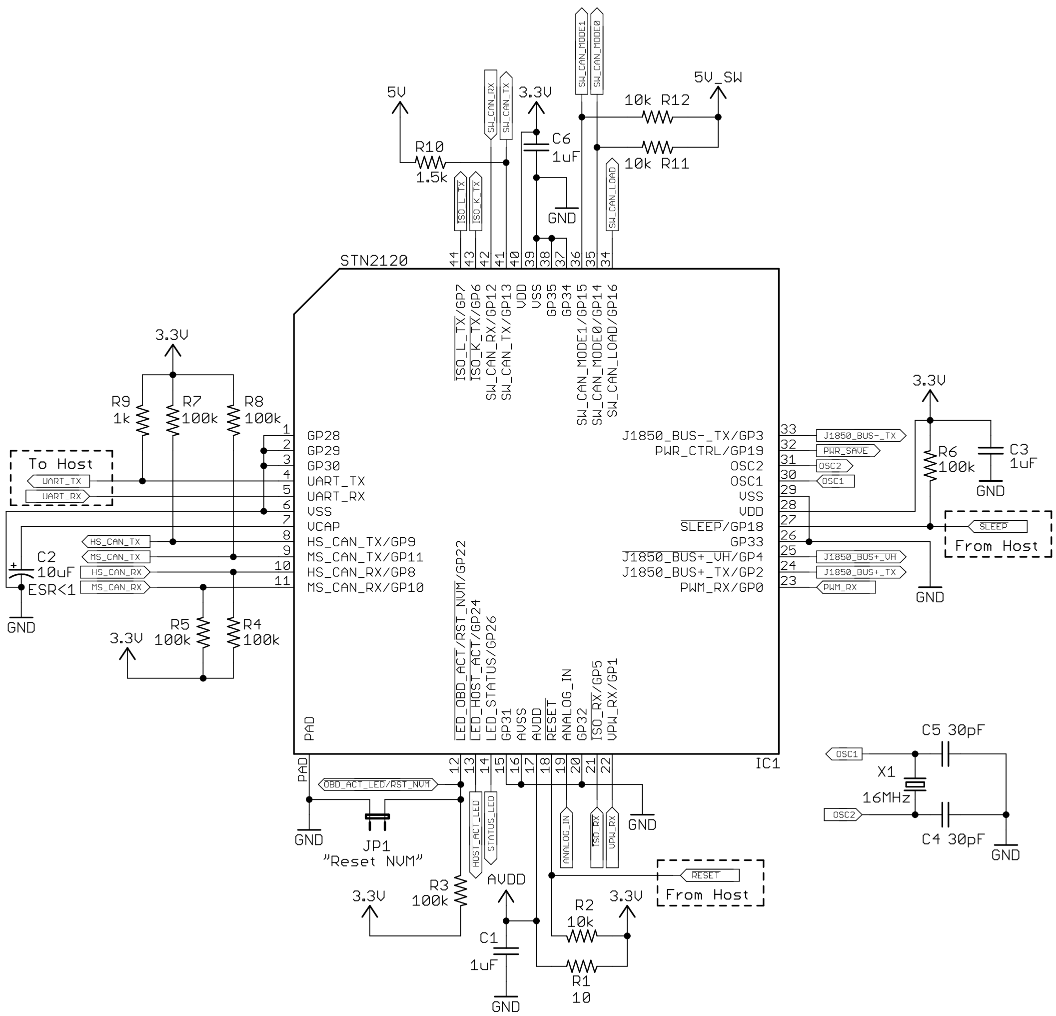


6.2.2 STN2120 IC

Figure 6 shows the circuit block for the STN2120 IC, including:

- **Pull-up resistors** (Section 4.4)
- **Decoupling capacitors** (Section 5.2)
- **VCAP** (Section 5.5)
- **Crystal oscillator** (Section 5.6)
- **$\overline{\text{RESET}}$ pin** (Section 5.7)
- **$\overline{\text{RST\_NVM}}$ pin** (Section 5.8)

Figure 6 - STN2120 IC



Note 1 - Be sure to pull up $\overline{\text{RST\_NVM}}$ pin to Vdd or 5V via a 100 kΩ resistor, whether an LED is connected or not. Failure to do so may result in mysterious and unpredictable device resets.

Another common mistake is to use the load capacitance (C_L) value specified by the crystal manufacturer as the capacitance for C4 and C5. This results in marginal oscillator performance and creates a potentially insidious problem that may not get discovered until after the design enters production: the circuit may work fine in the lab but would fail to start up in the field under certain conditions.

To avoid this, use the following formula to calculate the value of the loading capacitors:

$$C4 = C5 = \left(C_L - C_{stray}\right) \times 2$$

C_{stray} consists of: pin capacitance; capacitor, resistor, and crystal or resonator lead capacitance; and board or trace related capacitance. For the typical surface-mount design, use $C_{stray} = 3pF$.

Avoid using crystals with $C_L < 15pF$.

For more information, see Microchip Technology app notes AN826 and AN849.

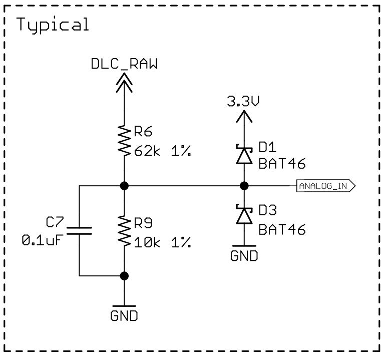
6.2.3 Voltage Sense

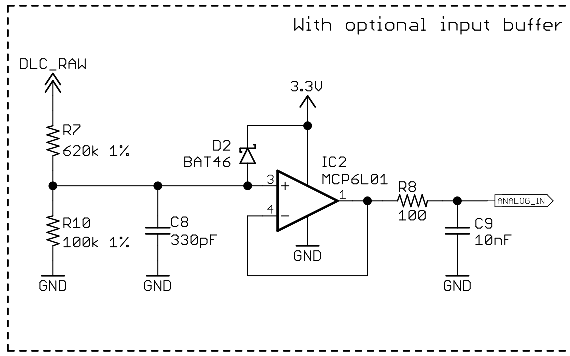
For best results, connect the voltage sense circuit directly to pin 16 of the OBD port (marked as DLC_RAW in the circuit examples), bypassing the overvoltage/reverse polarity and power conditioning circuitry.

D1, D3, R6, and the internal diode provide adequate protection of the ANALOG_IN pin against overvoltage and reverse polarity conditions.

If you choose to connect ANALOG_IN after the protection/filter circuit, expect a loss of accuracy and reduced sensitivity of the “wake-up on voltage change” (STSLVG) trigger in sleep. Use the offset parameter of the STVCAL command to compensate for the voltage drop across any series components (e.g., reverse polarity protection diode).

Figure 7 - Voltage Sense





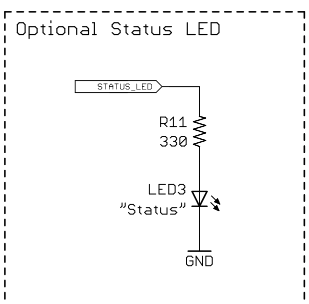
6.2.4 LEDs

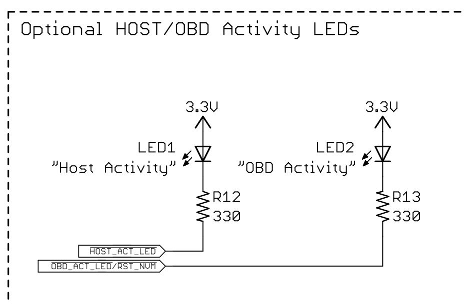
Even if your design does not use LEDs as part of the user interface, consider including them in your prototype as a troubleshooting aid.

Limiting resistor values are for reference only, actual values depend on the LEDs used.

Tip: use potentiometers to adjust the brightness and make it consistent across the LEDs, then measure the resistance to select fixed resistors of appropriate size.

Figure 8 - LEDs





6.2.5 OBD Port Connector and ESD Protection

Take care to provide sufficient spacing between power (pins 16, 4, & 5) and signal pins. Note that in the example schematic, pins 4 & 5 (Chassis & Signal grounds) are connected together. This is done because on a small number of vehicle models, either pin can be missing.

Place ESD protection as close as possible to the OBD port pins.

Figure 9 - STN2100 OBD Port Connector and ESD Protection

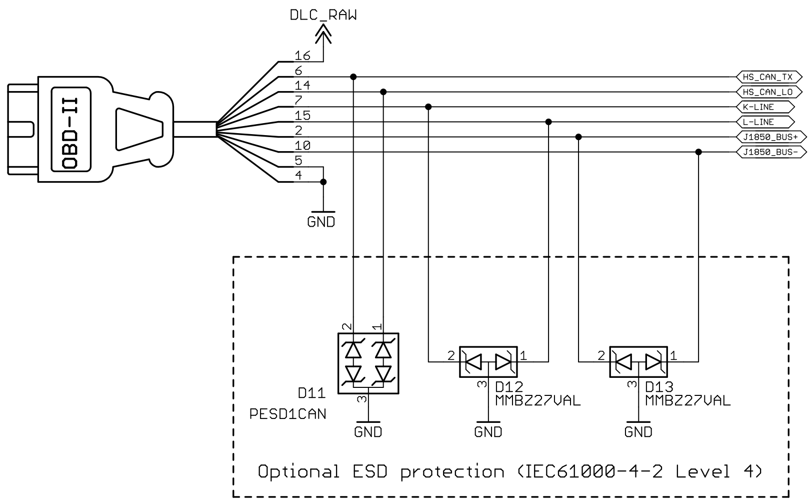
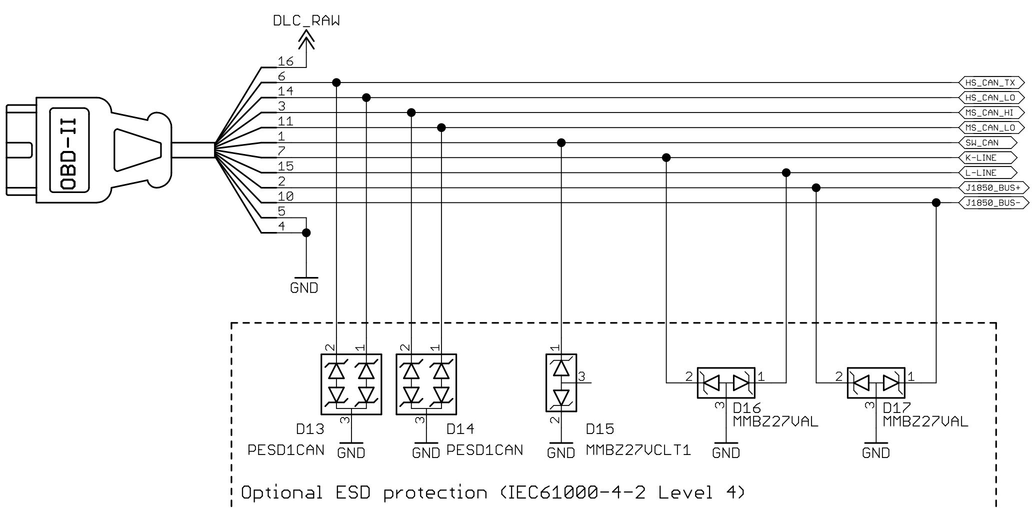


Figure 10 - STN2120 OBD Port Connector and ESD Protection

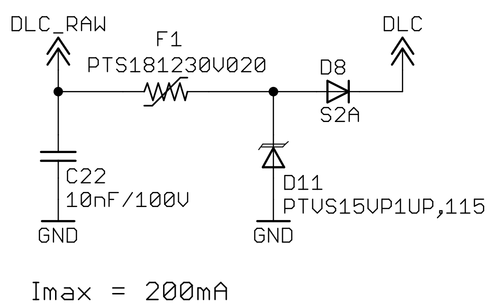


6.2.6 Overvoltage Protection Circuit

It is critically important to protect devices attached to the OBD port from voltage spikes. ISO 7637-2 describes several types of high-voltage transients, the most dangerous of which is the Pulse 5A/B ("load dump"), a high-energy pulse with voltage as high as 60V.

In this section, we present two options for overvoltage protection (OVP): PTC/TVS and transistor-based.

Figure 11 – Option 1: PTC/TVS Overvoltage Protection



PTC/TVS-based OVP (Figure 11) is the simpler of the two designs, with a lower part count. In addition, this circuit may allow the load to remain powered during an overvoltage event, which may be an advantage in some situations. However, it tends to be bulkier and more expensive, especially for voltages above 60V (e.g., load dump on 24V systems) and higher operating currents.

This circuit relies on the "shunt" action of the TVS ("transient voltage suppressor", similar to a Zener diode) which trips the PTC ("resettable fuse").

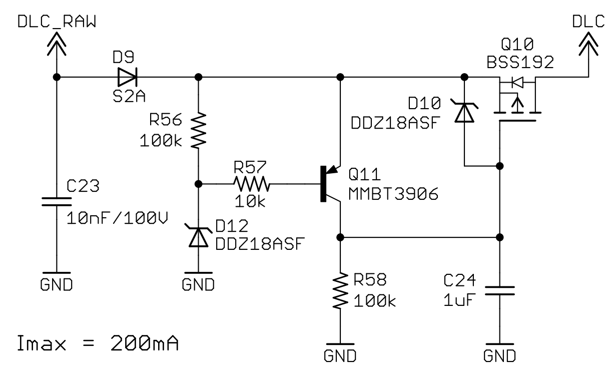
When the DLC_RAW voltage exceeds the breakdown voltage of the TVS (D11), its resistance drops rapidly, providing a low impedance path for the transient current. This causes the current through the PTC (F1) to increase, causing the PTC to change from low to high resistance and interrupt the current flow.

It is important to correctly match the PTC and TVS. Select a PTC with a trip current that is above the maximum normal operating current, then select a TVS with a trip current rating that is sufficient to reliably trip the PTC.

One inherent flaw of the PTC/TVS-based OVP is the existence of a "gray band" just above the breakdown voltage (V_{BR}) of the TVS where the circuit does not work as intended. The voltage inside this band is insufficient for the TVS to fully enter avalanche mode; as a result, the current through the TVS is lower than is necessary to trip the PTC, and can result in TVS damage from overheating. You should take care to select the TVS such that the circuit is not subjected to the voltages inside the "gray band" for longer than a few milliseconds.

The purpose of the small capacitor (C22) on the input of this OVP circuit is to help suppress fast transients. Note that the reverse polarity protection diode D8 is connected *after* the PTC/TVS, to avoid subjecting it to the high clamping currents during the overvoltage condition.

Figure 12 – Option 2: Transistor Based Overvoltage Protection



Transistor-based OVP (Figure 12) has a higher part count but can be physically smaller and less expensive than the PTC/TVS design.

This circuit relies on a small Zener diode to detect an overvoltage condition, and a series PFET (Q10) to disconnect the load.

When the DLC_RAW voltage exceeds the breakdown voltage of D12, the Zener diode begins to avalanche, turning on Q11 and turning off Q10.

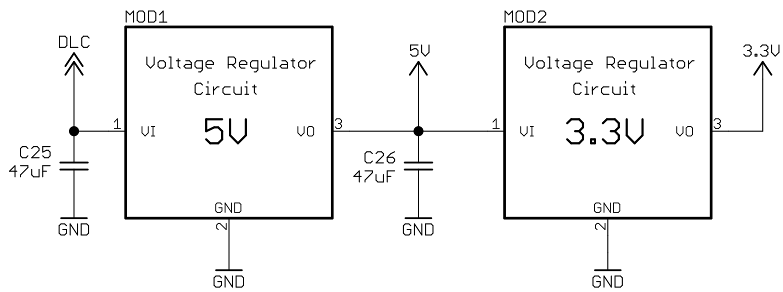
The circuit can remain in the overvoltage condition indefinitely.

R57 provides current limiting for Q11, R58 is a pull-down for Q10 (keeping it on during normal operation), and D10 is protecting the gate of Q10.

6.2.7 Power Supplies

In addition to V_{BAT}, your device will require 3.3V and likely 5V (for J1850 PWM and CAN transceivers). Figure 13 shows the block diagram of a typical “tandem” configuration, where the 5V supply is a low-quiescent current switching regulator, and 3.3V is a low-quiescent current linear regulator. This arrangement offers the best balance of functionality, cost, footprint, and power dissipation for most applications. C25 and C26 are tank capacitors of electrolytic or ceramic type. Details of the design depend on the specific requirements of your project. One practical example of the “switcher-linear regulator” configuration is the OBD power module that ships as part of the OBD Development Kit. Schematics for the OBD Power Module are available from the OBD Solutions website.

Figure 13 – Power Supplies

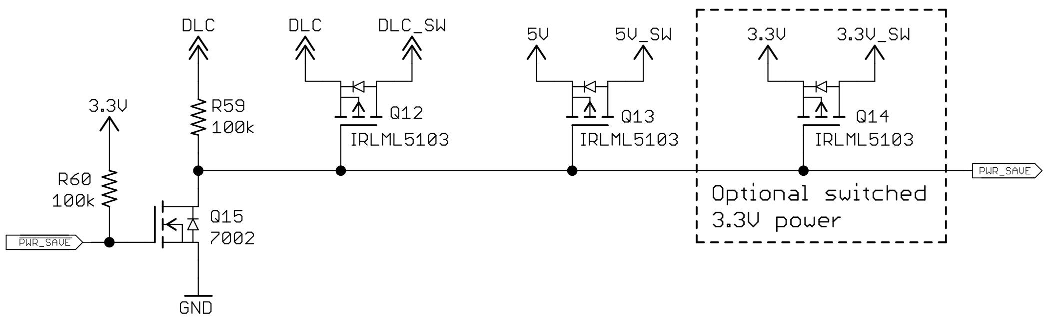


6.2.8 Switched Power Control

To avoid draining the vehicle battery, devices attached to the OBD port should enter sleep mode after a prolonged period of inactivity. The commonly accepted maximum long-term sleep current is 2 mA. In practice, this means that in sleep mode, most peripherals should be powered down.

Figure 14 shows transistor-based power switches that can be controlled by the $\overline{\text{PWR\_SAVE}}$ signal from the STN21xx.

Figure 14 – Switched Power Control



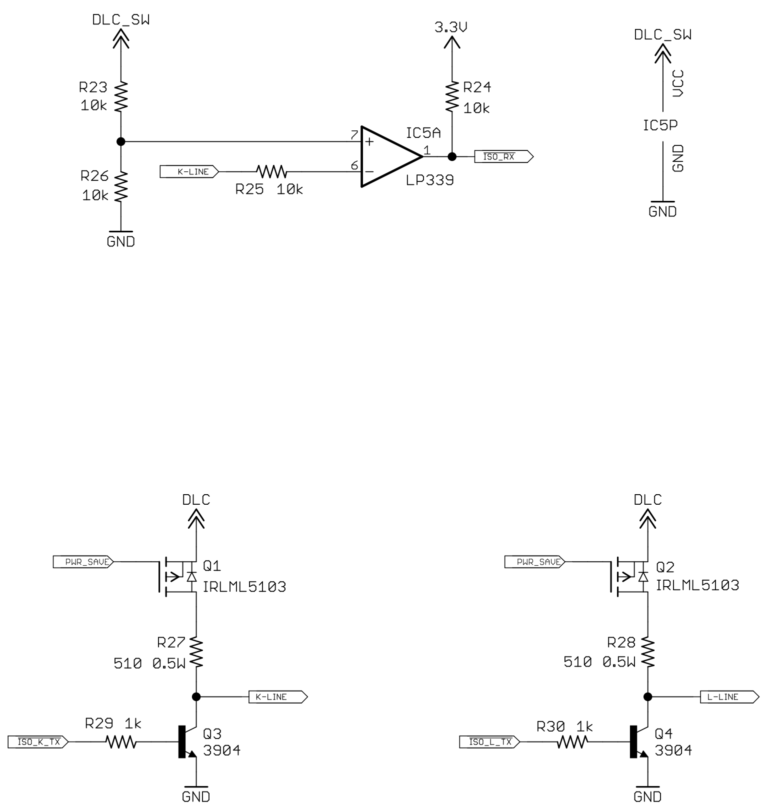
6.2.9 ISO 9141/ISO 14230 Transceiver

The ISO 9141/ISO 14230 transceiver consists of the K/L line transmitter (Q3, Q4) and a K-line receiver based on the LM339 comparator (IC5A).

Note that for proper operation, the LM339 *must* be powered from DLC_SW (not a lower voltage power source).

Also note that there are two transistors (Q1 and Q2) used to turn off the pull ups in power save mode. A common mistake is to not use a switch for DLC, and instead connect the transmitter pull-ups R27 and R28 directly to DLC or DLC_SW. Doing so can have negative consequences, ranging from excessive current draw in sleep to interference with the in-vehicle network communication resulting in an engine stall.

Figure 15 - ISO 9141/ISO 14230 Transceiver



6.2.10 High-Speed and Medium-Speed CAN Transceiver

The High-Speed CAN transceiver shown in Figure 16 is part of the “generic” OBD-II standard. We chose the MCP2562 for this reference circuit, for two reasons: it has very low standby current and is available in a small 3x3 DFN package.

The low standby current means that the transceiver does not need to be switched off in low power mode. Instead, the STN21xx can put the transceiver in low power mode by applying a logic “high” to the STBY pin. In this mode, the transmitter and the high-speed part of the receiver are switched off, but the low-power receiver and the wake-up filter block are enabled to allow the device to wake-up on CAN bus activity.

The only additional components are the decoupling capacitor C10, and the EMI filters R14/C11 and R15/C12.

A common mistake is to add bus termination to the CAN drivers; it is unnecessary, and even harmful, because it lowers the impedance of an already terminated vehicle CAN bus.

The Medium-Speed CAN transceiver circuit (Figure 17) typically used to communicate with the proprietary Ford MSC vehicle bus, is identical to the High-Speed CAN transceiver circuit.

Figure 16 – High Speed CAN Transceiver

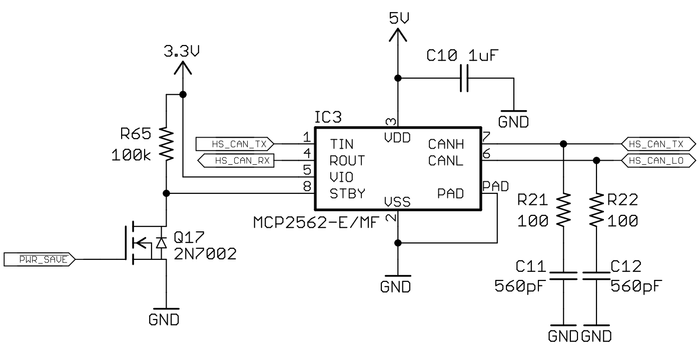
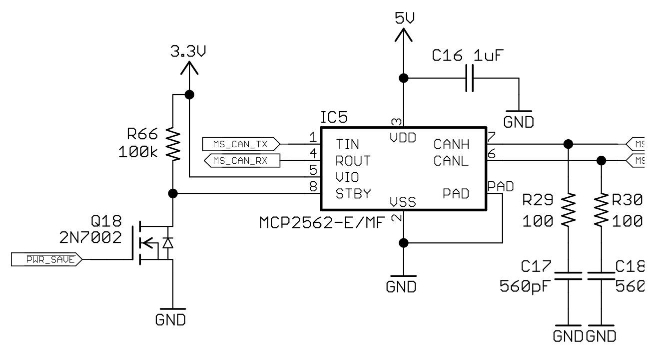


Figure 17 – Medium Speed CAN Transceiver



6.2.11 Alternative (MCP2551) HS-CAN/MS-CAN Transceiver

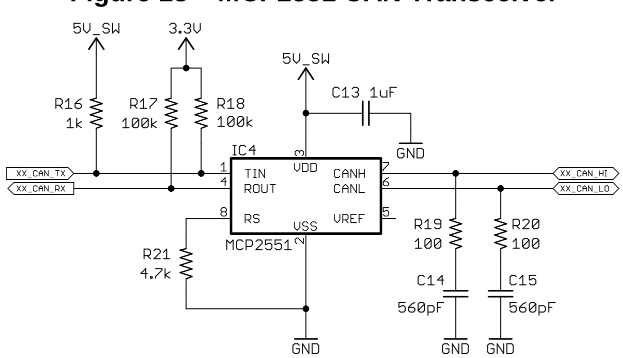
The MCP2551 is an older generation CAN transceiver which is sometimes used in new designs for cost reasons. Due to its high sleep current (up to 465 µA) it should be switched off in sleep. For this reason, the MCP2551 is powered from 5V_SW.

The R17 and R18 pull-ups to 3.3V on TIN and ROUT are necessary to keep the signal lines from floating in sleep mode.

The 1k pull-up to 5V_SW on the TIN pin (R16) is required for normal operation. It is switched off in sleep mode to reduce the current consumption.

R21 is used for slope control; the value of 4.7kΩ was selected to reduce EMI without compromising the reliability of communication. Do not increase it further.

Figure 18 – MCP2551 CAN Transceiver



6.2.12 Single Wire CAN Transceiver

The Single Wire CAN Transceiver is designed to interface with the SAE J2411 (GMLAN) vehicle bus. The TH8056KDCA8's low standby current allows it to remain powered in sleep mode. MODE0 and MODE1 are used to put the transceiver in Sleep mode, as well as switch between Normal, High Speed, and High Voltage Wake-Up modes.

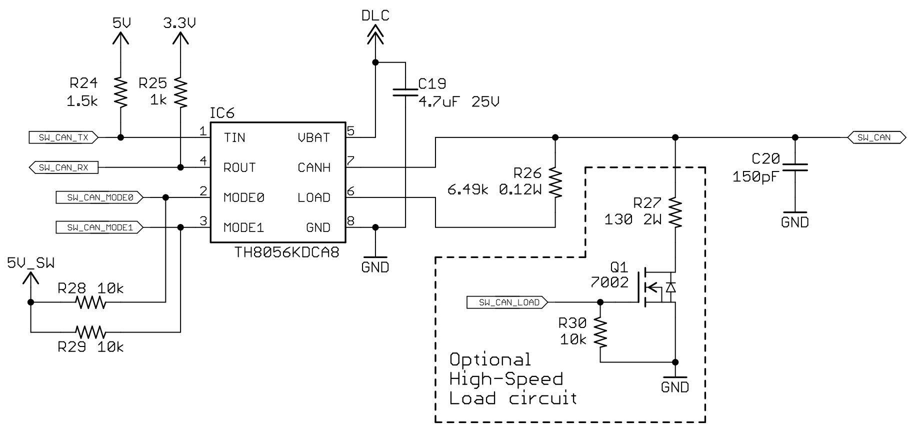
R24 is the pull-up for the open-drain STN2120 output SW_CAN_TX.

R25 is the pull-up for the ROUT pin of the transceiver. The ROUT input can be used to detect bus activity in sleep mode.

R28 and R29 are the pull-ups for the open drain STN2120 outputs SW_CAN_MODE0 and SW_CAN_MODE. They should be connected to 5V_SW to avoid unnecessary current draw in sleep mode when STN2120 applies logic-LOW to these pins.

The optional high-speed load circuit (controlled directly by the STN2120) can be omitted for "flight recorder" type (monitoring only) applications.

Figure 19 – Single Wire CAN Transceiver



6.2.13 SAE J1850 Transceiver

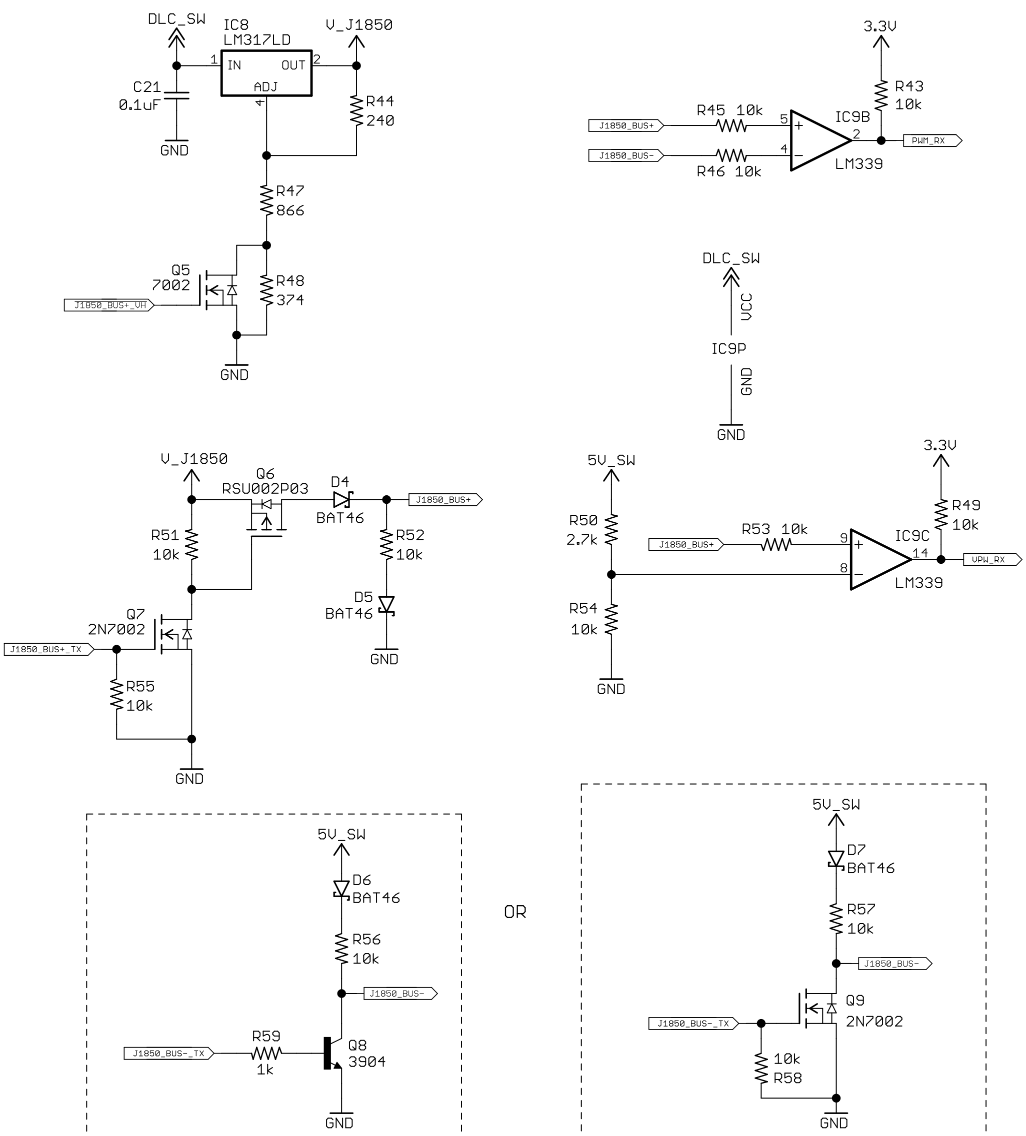
The SAE 1850 transceiver is made up of five blocks: V_J1850 power supply, J1850 BUS+ transmitter, J1850 BUS- transmitter, PWM receiver, and VPW receiver.

The V_J1850 power supply is used to power the J1850 BUS+ transmitter, which is used by both PWM and VPW protocols. PWM and VPW require different voltages, approximately 5V and 7V, respectively. STN21xx sets the voltage by controlling the LM317 adjustable regulator via the PWM/$\overline{\text{VPW}}$ signal. A logic-LOW on the PWM/$\overline{\text{VPW}}$ input causes the LM317 to output a voltage slightly higher than 7V (to account for the voltage drop in the J1850 BUS+ transmitter) while a logic-HIGH turns on Q5 which shunts R48, reducing the voltage to slightly higher than 5V. The power supply is powered from DLC_SW and is powered off in sleep.

The J1850 BUS+ transmitter consists of the R55 bus pull-down, and a two-stage transistor switch Q7/Q6. Schottky diodes D4 and D5 prevent current backflow from/into the J1850_BUS+ line.

The J1850 BUS- transmitter can be implemented using either an NPN bipolar transistor, or an n-channel MOSFET. The NPN version is less sensitive to ESD.

Figure 20 - SAE J1850 VPW/PWM Transceiver



Both the PWM and VPW receivers are based on the LM339 comparator, and are powered from DLC_SW, which means they are powered off in sleep mode.

The PWM receiver is connected to the differential J1850_BUS+/J1850_BUS- lines via 10kΩ resistors. The VPW receiver uses a voltage divider (R50/R54) to set up the input high/low threshold.

7.0 Electrical Characteristics

This section provides an overview of the STN21xx electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

The STN2120 is based on the dsPIC33EP256GP504 device from Microchip Technology. For more detailed device specifications or clarification, refer to Microchip documentation, available at http://www.microchip.com.

The STN2100 is based on the dsPIC33EP256GP502 device from Microchip Technology. For more detailed device specifications or clarification, refer to Microchip documentation, available at http://www.microchip.com.

7.1 Absolute Maximum Ratings (1)

Ambient temperature under bias .... -40°C to +125°C
Storage temperature .... -65°C to +150°C
Voltage on Vdd with respect to Vss .... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to Vss(2) .... -0.3V to (Vdd + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when Vdd ≥ 3.0V(2) .... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when Vdd < 3.0V(2) .... -0.3V to 3.6V
Maximum current out of Vss pin .... 300 mA
Maximum current into Vdd pin .... 300 mA
Maximum current sourced/sunk by any 4x output(3) .... 15 mA
Maximum current sourced/sunk by any 8x output(3) .... 25 mA
Maximum current sunk by all outputs .... 200 mA

Note
1. Stresses beyond those listed here can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.
2. See section 4.0 “Pinout” for the list of 5V tolerant pins.
3. See section 4.3 “Pinout Summary” to determine current rating of individual pins.

7.2 Electrical Characteristics

Table 4: Thermal Operating Conditions

Sym	Characteristic	Min	Typ	Max	Units	Conditions
T_J	**Operating Junction Temperature**	-40	—	+125	°C	
T_A	**Operating Ambient Temperature**	-40	—	+85	°C	

Table 5: Power Specifications

Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
V_{DD}	**Supply Voltage**	3.0	—	3.6	V	
V_{POR}	**V_{DD} Start Voltage** to ensure internal power-on reset (POR) signal	—	—	V_{SS}	V	
S_{VDD}	**V_{DD} Rise Rate(2)** to ensure internal power-on reset (POR) signal	0.03	—	—	V/ms	0V–1.0V in 0.1s

Sym	Characteristic	Min	Typ[1]	Max	Units	Conditions
AV_{DD}	**Analog Supply Voltage**	Greater of V_{DD} – 0.3 or 3.0	—	Lesser of V_{DD} + 0.3 or 3.6	V	
AV_{SS}	**Analog Ground Reference**	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
V_{BOR}	**Brown-out Reset Voltage[3]** on V_{DD} transition high-to-low	2.65[3]	—	2.95	V	
I_{DD}	**Operating Current[4]**	—	42	63[5]	mA	
I_{PD}	**Average Sleep Current[4,6]**	— —	130 450[5]	265[5] 800[5]	μA μA	T_A = +25°C T_A = +85°C
C_{EFC}	**External Filter Capacitor[7]** connected to V_{CAP} pin	4.7	10	—	μF	ESR < 1 Ω

Note
1. Data in Typ column is at 3.3V, 25°C, unless otherwise stated.
2. This spec must be met in order to ensure that a correct internal power-on reset (POR) occurs. It is easily achieved using most common types of supplies but may be violated if a supply with slowly varying voltage is used, as may be obtained through direct connection to solar cells or some charge pump circuits.
3. This parameter is for design guidance only and is not tested in manufacturing.
4. STN21xx device current only. Does not include any load currents.
5. Values are characterized, but not tested.
6. All wakeup triggers are on and wakeup trigger inputs are in their inactive states.
7. Typical V_{CAP} voltage = 1.8V when $V_{DD} \geq V_{DDMIN}$.

Table 6: Input Pin DC Specifications

Sym	Characteristic	Min	Typ	Max	Units	Conditions
V_{IL}	**Input Low Voltage[3]**					
	PWR_CTRL[8], $\overline{\text{J1850\_BUS-\_TX}}$[8], GP34[8], GP35[8] $\overline{\text{ISO\_L\_TX}}$/GP7[9] $\overline{\text{ISO\_K\_TX}}$/GP6[9]	V_{SS}	—	0.3 V_{DD}	V	
	All other inputs	V_{SS}	—	0.2 V_{DD}	V	
V_{IH}	**Input High Voltage**					
	non-5V tolerant pins[1]	0.8 V_{DD}	—	V_{DD}	V	
	5V tolerant pins[1]	0.8 V_{DD}	—	5.5	V	
I_{IPU}	**Internal Pull-up Current**	150	250	550	μA	V_{DD} = 3.3V, V_{PIN} = V_{SS}
I_{IPD}	**Internal Pull-down Current**	20	50	100	μA	V_{DD} = 3.3V, V_{PIN} = V_{DD}
V_{IN}	**ANALOG_IN Input Voltage**	AV_{SS}	—	AV_{DD}	V	
R_{IN}	**Recommended ANALOG_IN Voltage Source Impedance**	—	—	200	Ω	
I_{ICL}	**Input Low Injection Current**	0	—	-5[3,6]	mA	All pins, except V_{DD}, V_{SS}, AV_{DD}, AV_{SS}, $\overline{\text{RESET}}$, V_{CAP}, $\overline{\text{ISO\_K\_TX}}$/GP6[8], and $\overline{\text{ISO\_RX}}$/GP5[9]

Sym	Characteristic	Min	Typ	Max	Units	Conditions
I_{ICH}	**Input High Injection Current**	0	—	+5[(4,5,6)]	mA	All pins, except V_{DD}, V_{SS}, AV_{DD}, AV_{SS}, $\overline{RESET}$, V_{CAP}, $\overline{ISO\_K\_TX}$/GP6[(8)], $\overline{ISO\_RX}$/GP5[(9)] and all 5V tolerant pins
ΣI_{ICT}	**Total Input Injection Current** sum of all I/O and control pins	-20[(7)]	—	+20[(7)]	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins ($\lvert I_{ICL}\rvert + \lvert I_{ICH}\rvert) \le \Sigma I_{ICT}$

Note
1. See section 4.0 “Pinout” for the list of 5V tolerant pins.
2. Negative current is defined as current sourced by the pin.
3. V_{IL} source < (V_{SS} – 0.3). Characterized, but not tested.
4. Non-5V tolerant pins: V_{IH} source > (V_{DD} + 0.3), 5V tolerant pins: V_{IH} source > 5.5V. Characterized, but not tested.
5. Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.
6. Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
7. Any number and/or combination of inputs listed under I_{ICL} or I_{ICH} conditions are permitted, provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins does not exceed the specified limit. Characterized, but not tested
8. STN2120 IC only
9. STN2100 IC only

Table 7: Output Pin DC Specifications

Sym	Characteristic	Min	Typ	Max	Units	Conditions V_{DD} = 3.3V, -40°C ≤ T_A ≤ +85°C
V_{OL}	**Output Low Voltage**[(1)]					
	4x Sink Driver Pins[(2)]	—	—	0.4	V	I_{OL} ≤ 6 mA
	8x Sink Driver Pin[(2)]	—	—	0.4	V	I_{OL} ≤ 12 mA
V_{OH}	**Output High Voltage**[(1)]					
	4x Source Driver Pins[(2)]	2.4	—	—	V	I_{OH} ≥ -10 mA
	8x Source Driver Pin[(2)]	2.4	—	—	V	I_{OH} ≥ -15 mA
V_{OH1}	**Output High Voltage**[(1)]					
	4x Source Driver Pins[(2)]	1.5	—	—	V	I_{OH} ≥ -14 mA
		2.0	—	—	V	I_{OH} ≥ -12 mA
		3.0	—	—	V	I_{OH} ≥ -7 mA
	8x Source Driver Pin[(2)]	1.5	—	—	V	I_{OH} ≥ -22 mA
		2.0	—	—	V	I_{OH} ≥ -18 mA
		3.0	—	—	V	I_{OH} ≥ -10 mA

Note
1. Parameters are characterized, but not tested.
2. See section 4.3 “Pinout Summary” for the output driver current rating designations.

Table 8: I/O Pin Timing Requirements

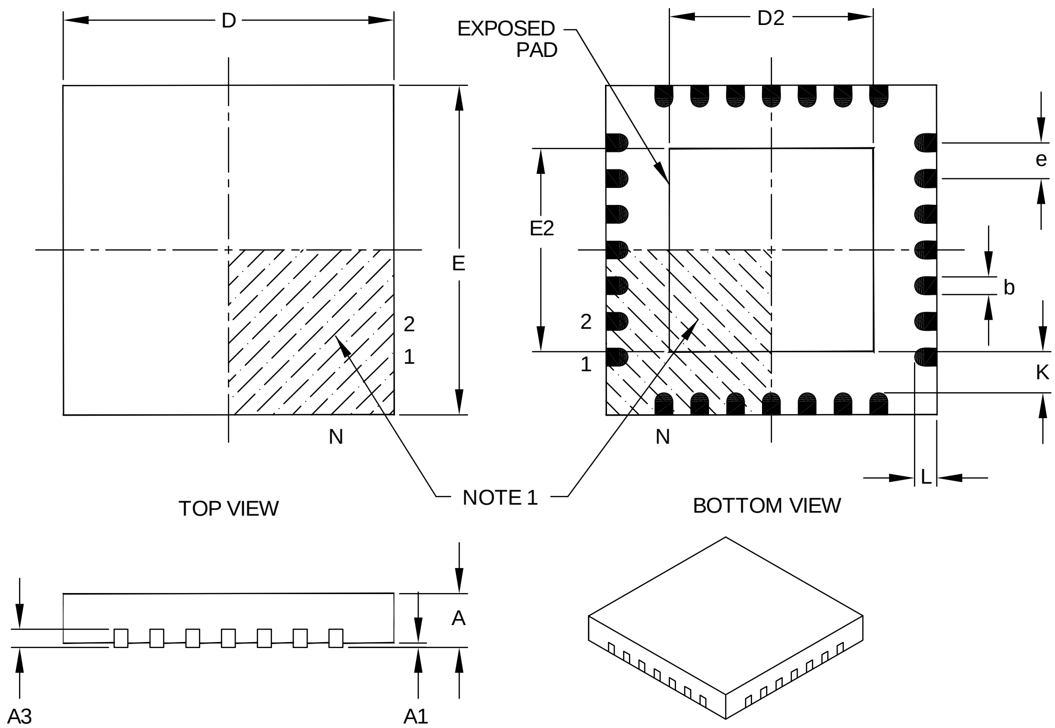
Sym	Characteristic	Min	Typ	Max	Units	Conditions
T_{RST}	$\overline{\textbf{RESET}}$ **Pulse Width** (low)	2	—	—	µs	
T_{UWM}	**Minimum UART Rx Pulse Width** required for wakeup (user settable)	—	20	—	ns	user setting < 15
		15	—	65,534	µs	user setting ≥ 15
T_{STM}	**Minimum** $\overline{\textbf{SLEEP}}$ **Input Time** to stay high before wakeup (user settable)	—	15	—	µs	user setting = 0
		1	—	65,534	ms	user setting > 0

8.0 Packaging Diagrams and Parameters

8.1 STN2100 QFN-S (MM) Package

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.70
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.70
Contact Width	b	0.23	0.38	0.43
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	—	—

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

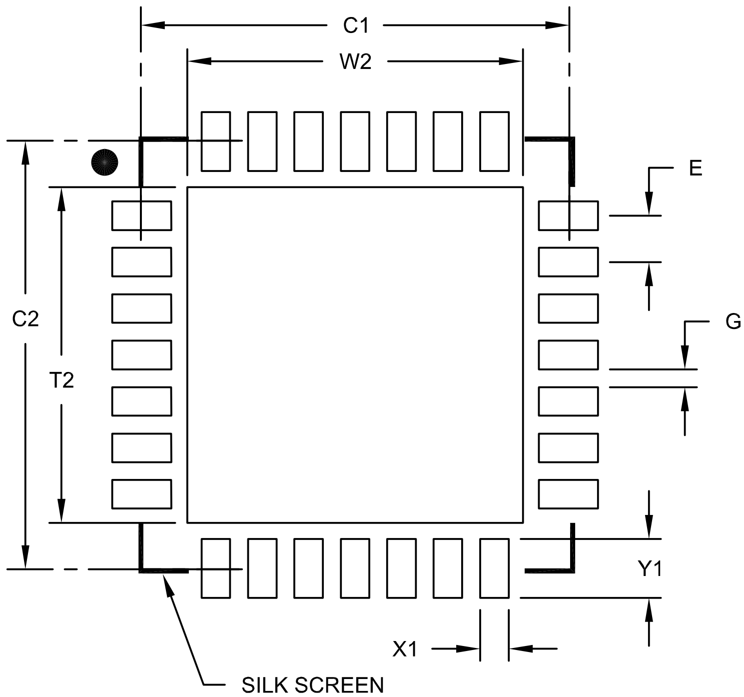
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124B

8.2 STN2100 QFN-S (MM) Land Pattern

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (x28)	X1			0.40
Contact Pad Length (x28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

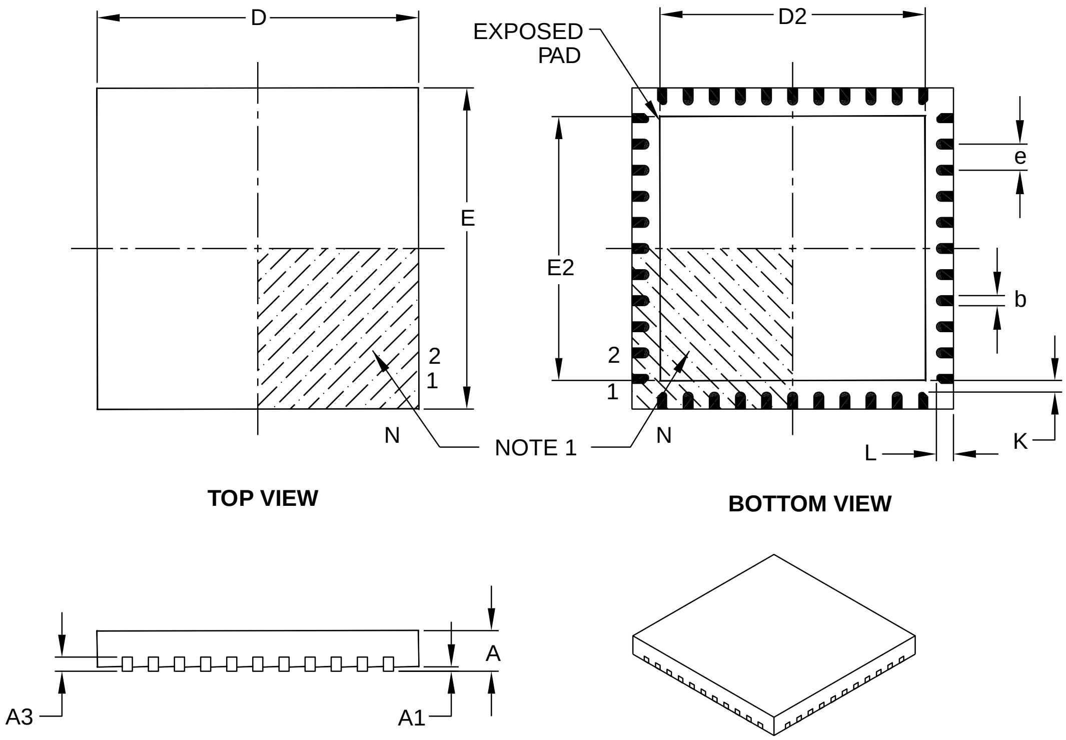
1. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2124

8.3 STN2120 QFN (ML) Package

44-Lead Plastic Quad Flat, No Lead Package – 8x8 mm Body

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



		Units	MILLIMETERS	
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.25	6.45	6.60
Contact Width	b	0.20	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	—	—

Notes:

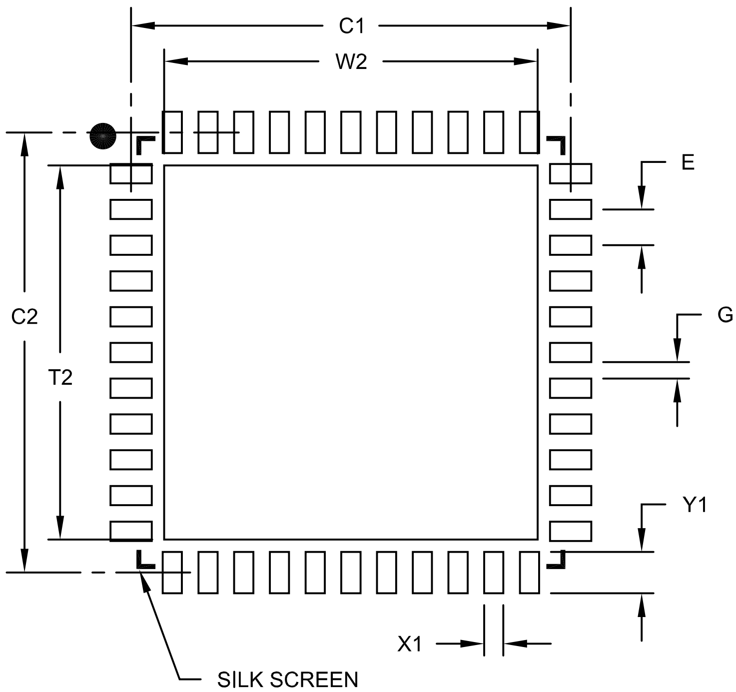
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103C

8.4 STN2120 QFN (ML) Land Pattern

44-Lead Plastic Quad Flat, No Lead Package – 8x8 mm Body

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS	
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2	—	—	6.60
Optional Center Pad Length	T2	—	—	6.60
Contact Pad Spacing	C1	—	8.00	—
Contact Pad Spacing	C2	—	8.00	—
Contact Pad Width (x44)	X1	—	—	0.35
Contact Pad Length (x44)	Y1	—	—	0.85
Distance Between Pads	G	0.25	—	—

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2103B

9.0 Ordering Information

T_A	Package		Part Number	SKU
-40°C to +85°C	QFN (MM)	Tube	STN2100-I/MM	366401
-40°C to +85°C	QFN (ML)	Tube	STN2120-I/ML	366201

Appendix A: Revision History

Revision A (February 28, 2018)

Initial release of this document.

Appendix B: Contact Information

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