Notes on v1.0.6

General notes: * Bypass capacitors should be ceramic, low ESR, low ESR (generally). We'll set default value as 100nF. * We need separate analog and digital ground planes connected at a single point * One noise document recommended including a digital buffer on the output of the ADC, might add one.

Voltage Ref

- 1uF and 10uF caps on VOUT should have an ESR between 1 and 1.5 ohm
- Change the bypass cap on V_in to 10uF
- Connect this device to AGND Follow this layout for the PCB:

10.2 Layout Example

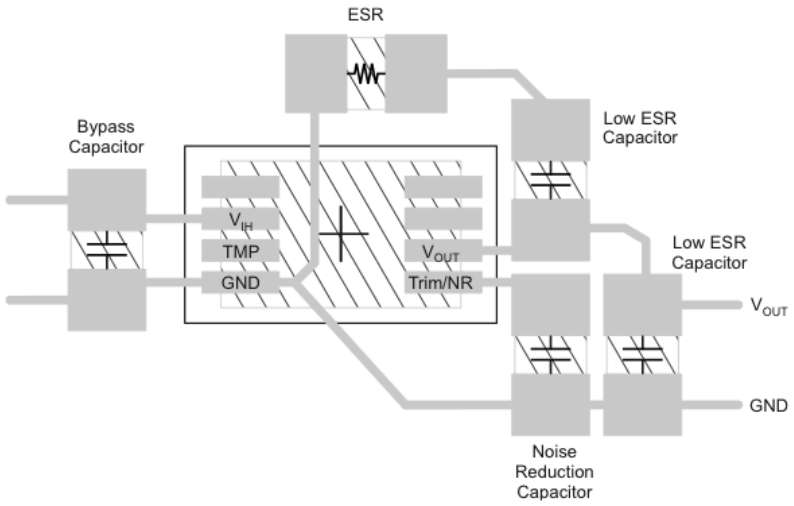

Figure 37. Recommended Layout for REF5025-HT

ADC

- Connect this device to AGND (even the pins I told you to connect to DGND before)
- 100nF decoupling caps needed at both +VA, +VBD.
- Just connect REFM to AGND like normal, no need for trace to base of C5

Follow this layout for the PCB (Minus var gain amp):

12 Layout

12.1 Layout Guidelines

- A copper fill area underneath the device ties the AGND, BDGND, AINM, and REFM pins together. This copper fill area must also be connected to the analog ground plane of the PCB using at least four vias.
- The power sources must be clean and properly decoupled by placing a capacitor close to each of the three supply pins, as shown in Figure 66. To minimize ground inductance, ensure that each capacitor ground pin is connected to a grounding via by a very short and thick trace.
- The REFP pin requires a 10-µF ceramic capacitor to meet performance specifications. Place the capacitor directly next to the device. This capacitor ground pin must be routed to the REFM pin by a very short trace, as shown in Figure 66.
- Do not place any vias between a capacitor pin and a device pin.

NOTE

The full-power bandwidth of the converter makes the ADC sensitive to high frequencies in digital lines. Organize components in the PCB by keeping digital lines apart from the analog signal paths. This design configuration is critical to minimize crosstalk. For example, in Figure 66, input drivers are expected to be on the left of the converter and the microcontroller on the right.

12.2 Layout Example

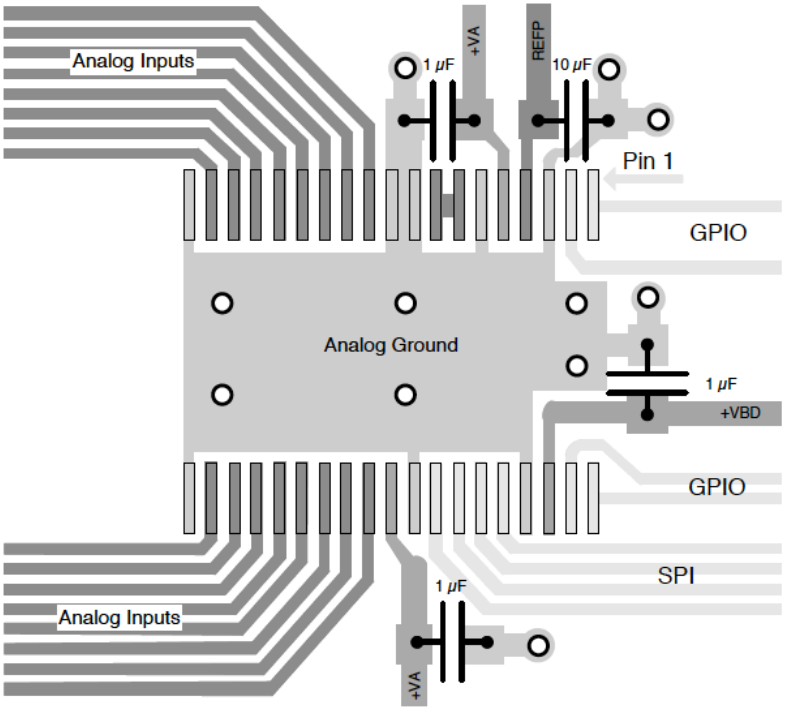

Figure 66. Recommended Layout

TSL237T

- Connect to DGND, should be on the 'digital side' of the board.

- Connect OUT to a female header on the board.
- VDD bypass cap should be 100nF.
- Connect a 10K pull-up resistor to the OE pin and tie it to a pin on the port expander.

OPT101

- Connect to AGND.
- Remove the second OPT101 and replace with another custom Photodiode + op amp using the TEMD5510
- In the schematic, add a 0ohm resistor and 0F capacitor between pins 4 and 5. Add the pads for the respective 0603 components so that we can add them later if desired, although generally we'll just solder bridge the pads.
    - We should not add a 1Mohm resistor by default.
- This device is a DIP package (fun) so be careful while laying out the PCB

Port Expander

- Connect to DGND
- Looks good, remember to add a 100nF bypass cap at VCC
- Connect GPB1 to OE of the TSL237 w/ pull-up resistor
- Add 5 LEDs to the board and connect to the port expander. Will get you these specs ASAP.

Photodiode + OP Amp design

- Connect to AGND
- Okay, generally try to work on readability of these circuits. Use 5-pin LTC6240
- Photodiode is mounted backwards.
- Connect photodiode across -IN and +IN pins visually.
- For now, avoid specifying the feedback resistor and capacitor values. We

might want to try 1Gohm feedback, but Sam brought up a good point that we need to be very careful in handling them.

Board headers:

- Single communication header should contain:
  i. MISO
  ii. MOSI
  iii. SCLK
  iv. PEX_CS
  v. PEX_RST
  vi. 3V3 (at choke point)
  vii. GND (at choke point)
  viii. OUT for TSL237
- Various smaller debugging headers should contain:
  i. Connections to more of the PEX GPIO pins.
  ii. Connections to OUT on the LTC6240s
  iii. Connections to all SPI lines.
  iv. Connection to V_OUT on the VREF
  v. Connection to OUT on the TSL237
  vi. Connection to OUT on the OPT101
  vii. Connection to AGND (at choke point)
  viii. Connection to DGND (at choke point)
  ix. Connection to 3V3 (at choke point)