IMX471 Application Note

IMX471
Module Design Reference Manual

Ver.1.0.0
2018/09/05
Mobile Imaging System Business Division
Sony Semiconductor Solutions Corporation

Other Available Documents

The following supplemental documents are available for supporting noise conscious module design:

- "Reference Pattern Layout - Appendix of Module Design Reference Manual" for each product type
- "Module Layout Design Guideline for Mobile CIS" as a common document explaining about noise conscious design principles

Revision History

Version	Date	Description
0.1.0	2017/12/08	First release
1.0.0	2018/09/05	Added chapter of PSRR Added Power Consumption Added CRA-Shading characteristics Added Spectral Sensitivity Characteristics

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1. Chip Physical Information

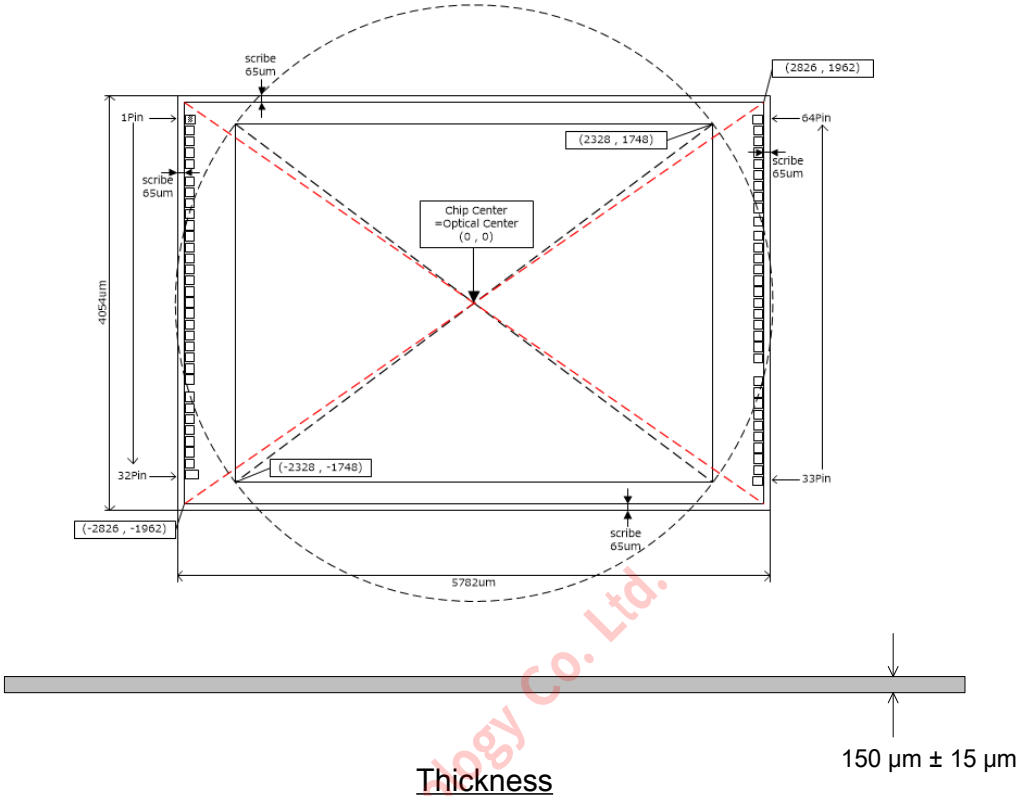


Figure 1-1 Chip Physical Information

Common Note

Note1: Actual size of a chip will be smaller than indicated when dicing (scribe) is taken into account.

Note2: Some PADs are located in image circle.

Table 1-1 Physical coordinates of pins

Pad No.	Pad name	Coordinate (origin=chip center)	
		X offset	Y offset
1	VDDHPL	-2763.25	1791
2	VSSHPL	-2769.25	1683
3	VDDMIO1	-2769.25	1575
4	INCK	-2769.25	1467
5	VDDLSC1	-2769.25	1359
6	VSSLSC1	-2769.25	1188.24
7	DMO3P	-2769.25	1080.72
8	DMO3N	-2769.25	973.2
9	DMO1P	-2769.25	865.68
10	DMO1N	-2769.25	758.16
11	VDDLSC2	-2769.25	650.64
12	VDDLIF1	-2769.25	543.12
13	VSSLSC2	-2769.25	435.6
14	DCKP	-2769.25	328.08
15	DCKN	-2769.25	220.56
16	VSSLSC3	-2769.25	113.04
17	VDDLIF2	-2769.25	5.52
18	VDDLSC3	-2769.25	-102
19	DMO2P	-2769.25	-209.52
20	DMO2N	-2769.25	-317.04
21	DMO4P	-2769.25	-424.56
22	DMO4N	-2769.25	-532.08
23	VSSLSC4	-2769.25	-639.6
24	VDDMIF	-2769.25	-747.12
25	VDDLCN1	-2769.25	-918
26	VSSLCN1	-2769.25	-1026
27	VDDSUB	-2769.25	-1134
28	VDDLSC4	-2769.25	-1242
29	VSSLSC5	-2769.25	-1350
30	VDDHCM1	-2769.25	-1458
31	VSSHSN1	-2769.25	-1566
32	VDDHSN1	-2751	-1674
33	VDDHSN2	2763.25	-1737
34	VSSHSN2	2769.25	-1629
35	VDDHCM2	2769.25	-1521
36	VSSLSC6	2769.25	-1413
37	VDDMIO2	2769.25	-1305
38	TENABLE	2769.25	-1197
39	XVS	2769.25	-1089
40	SWTCK	2769.25	-981
41	SLASEL	2769.25	-873
42	VSSLCN2	2769.25	-765
43	VDDLCN2	2769.25	-538.2
44	VDDLSC5	2769.25	-430.2
45	VSSLSC7	2769.25	-322.2
46	VDDHSN3	2769.25	-214.2
47	VSSHSN3	2769.25	-106.2
48	VDDHAN	2769.25	1.8
49	VSSHAN	2769.25	109.8
50	TVMON	2769.25	217.8
51	VDDMIO3	2769.25	325.8
52	FSTROBE	2769.25	433.8
53	GPO	2769.25	541.8

Pad No.	Pad name	Coordinate (origin=chip center)	
		X offset	Y offset
54	SCL	2769.25	654.3
55	SDA	2769.25	792.9
56	POREN	2769.25	927
57	VSSLSC8	2769.25	1035
58	VDDLSC6	2769.25	1143
59	XCLR	2769.25	1251
60	VPI	2769.25	1359
61	VRL	2769.25	1467
62	VRLRD	2769.25	1575
63	VSSHSN4	2769.25	1683
64	VDDHSN4	2763.25	1791

2. Assembly Guideline

Prohibited Area for the Contact of Collet

- Pixel area: Abnormal images
- Bonding pad: Circuit electrostatic breakdown
  (Note that this rule is not applicable for electrostatic breakdown prevention areas)
- Scribe area Dust emission due to chipping
- Chip edge: Dust emission due to breakage

Common Note

Note1: Ensure sufficient positional accuracy during the pickup work.

Separate the collet contact surfaces and contact-prohibited areas as much as possible.

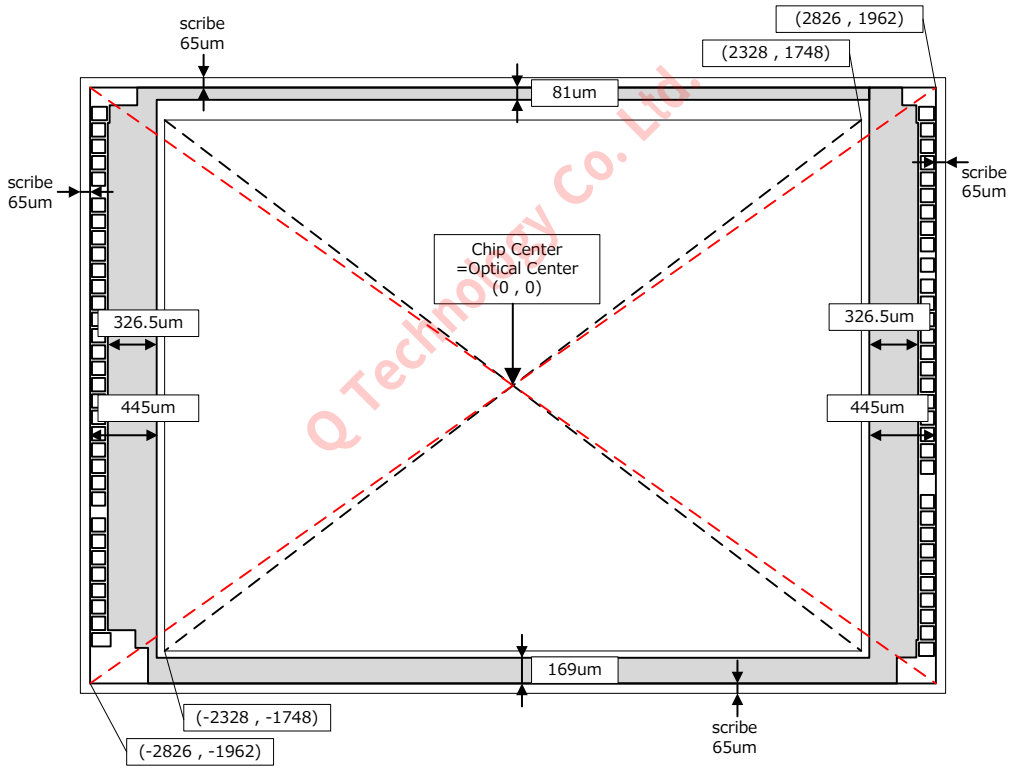


Figure 2-1 Chip Collet Information

Ultrasonic chip cleaning is prohibited.

This may result in dust emission from cut surfaces.

3. Pin Information

Table 3-1 Pin information list

No.	Symbol	I/O	A/D	Description	Remarks
1	VDDHPL	Power	A	analog input	
2	VSSHPL	GND	A	VANA GND	
3	VDDMIO1	Power	D	VIF power supply	
4	INCK	I	D	digital input	Clock Input
5	VDDLSC1	Power	D	VDIG power supply	
6	VSSLSC1	GND	D	VDIG GND	
7	DMO3P	O	D	digital output	MIPI output (DATA+)
8	DMO3N	O	D	digital output	MIPI output (DATA–)
9	DMO1P	O	D	digital output	MIPI output (DATA+)
10	DMO1N	O	D	digital output	MIPI output (DATA–)
11	VDDLSC2	Power	D	VDIG power supply	
12	VDDLIF1	Power	D	VDIG power supply	
13	VSSLSC2	GND	D	VDIG GND	
14	DCKP	O	D	digital output	MIPI output (CLK+)
15	DCKN	O	D	digital output	MIPI output (CLK-)
16	VSSLSC3	GND	D	VDIG GND	
17	VDDLIF2	Power	D	VDIG power supply	
18	VDDLSC3	Power	D	VDIG power supply	
19	DMO2P	O	D	digital output	MIPI output (DATA+)
20	DMO2N	O	D	digital output	MIPI output (DATA–)
21	DMO4P	O	D	digital output	MIPI output (DATA+)
22	DMO4N	O	D	digital output	MIPI output (DATA–)
23	VSSLSC4	GND	D	VDIG GND	
24	VDDMIF	Power	D	VIF power supply	
25	VDDLCN1	Power	D	VDIG power supply	
26	VSSLCN1	GND	D	VDIG GND	
27	VDDSUB	Power	A	VANA power supply	
28	VDDLSC4	Power	D	VDIG power supply	
29	VSSLSC5	GND	D	VDIG GND	
30	VDDHCM1	Power	A	VANA power supply	
31	VSSHSN1	GND	A	VANA GND	
32	VDDHSN1	Power	A	VANA power supply	
33	VDDHSN2	Power	A	VANA power supply	
34	VSSHSN2	GND	A	VANA GND	
35	VDDHCM2	Power	A	VANA power supply	
36	VSSLSC6	GND	D	VDIG GND	
37	VDDMIO2	Power	D	VIF power supply	
38	TENABLE	I	D	digital input	NC(pull-down internal)
39	XVS	I/O	D	digital I/O	for dual sync(pull-up internal)
40	SWTCK	I	D	digital input	NC(pull-down internal)
41	SLASEL	I	D	digital input	I2C slave address select Pull down(pull-down internal)
42	VSSLCN2	GND	D	VDIG GND	
43	VDDLCN2	Power	D	VDIG power supply	
44	VDDLSC5	Power	D	VDIG power supply	

No.	Symbol	I/O	A/D	Description	Remarks
45	VSSLSC7	GND	D	VDIG GND	
46	VDDHSN3	Power	A	VANA power supply	
47	VSSHSN3	GND	A	VANA GND	
48	VDDHAN	Power	A	VANA power supply	
49	VSSHAN	GND	A	VANA GND	
50	TVMON	O	A	Analog output	NC
51	VDDMIO3	Power	D	VIF power supply	
52	FSTROBE	O	D	digital output	
53	GPO	O	D	digital output	
54	SCL	I/O	D	digital I/O	I2C pin
55	SDA	I/O	D	digital I/O	I2C pin
56	POREN	I	D	digital input	NC(pull-up internal)
57	VSSLSC8	GND	D	VDIG GND	
58	VDDLSC6	Power	D	VDIG power supply	
59	XCLR	I	D	digital input	Chip clear(pull-down internal)
60	VPI	Power	A	analog input	
61	VRL	Minus	A	analog input	
62	VRLRD	Minus	A	analog input	
63	VSSHSN4	GND	A	VANA GND	
64	VDDHSN4	Power	A	VANA power supply	

4. Pin Status List

In this chapter, two kinds of sensor's I/O related information are shown for supporting hardware design. One is Pin Status List which summarizes sensor's internal state (for output terminals) and requirements for external circuit (for input terminals and power rails). “Description of the purpose” column shows use case of the terminals. And “Power off”, “HW STB” and “SW STB” columns show possible states of each use case. The other is I/O equivalent circuits for better understanding of the equivalent diagram including protection means.

Table 4-1 Pin status list

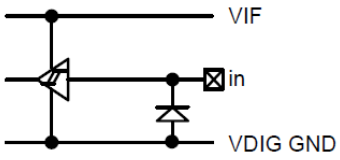
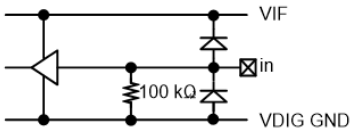
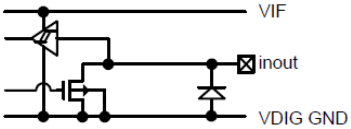
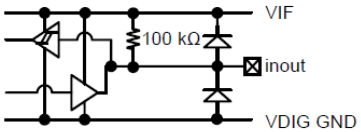
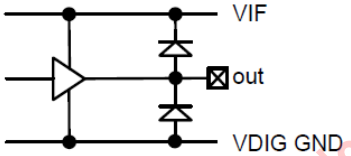
Name	Description of the purpose	Purpose of use	Power off	HW STB	SW STB	Internal state or requirement for external circuit
DCKP	MIPI output (CLK+)	O	HiZ	Low	Low	Internal state
DCKN	MIPI output (CLK-)	O	HiZ	Low	Low	
DMO1P	MIPI output (Data+)	O	HiZ	Low	Low	
DMO1N	MIPI output (Data-)	O	HiZ	Low	Low	
DMO2P	MIPI output (Data+)	O	HiZ	Low	Low	
DMO2N	MIPI output (Data-)	O	HiZ	Low	Low	
DMO3P	MIPI output (Data+)	O	HiZ	Low	Low	
DMO3N	MIPI output (Data-)	O	HiZ	Low	Low	
DMO4P	MIPI output (Data+)	O	HiZ	Low	Low	
DMO4N	MIPI output (Data-)	O	HiZ	Low	Low	
FSTROBE	Flash Strobe	O	Low(VIF)	Low	Data output	
GPO	General purpose output	O	Low(VIF)	Low	HiZ	
XVS	XVS output (Single use or master mode in dual sensor application)	O	Low(VIF)	HiZ(Pull-up)	Pull-up	Internal state
	XVS input (Slave mode in dual sensor application)	I	Low or HiZ	Low or High or HiZ	Low or High or HiZ	Expected external state

Name	Description of the purpose	Purpose of use	Power off	HW STB	SW STB	Internal state or requirement for external circuit
SDA	I2C Data	O	HiZ	HiZ	HiZ	Internal state
		I	Don't Care*1	Don't Care*1	Data input	Expected external state
SCL	I2C Clock	I	Don't Care*2	Don't Care*2	Clock input	
INCK	Image sensor clock	I	Low	Low	Clock input	
XCLR	Image sensor reset	I	Low(VIF)	Low	High	
SLASEL	I2C slave address select	I	HiZ/Low or Low(VIF)	HiZ/Low or High(VIF)	HiZ/Low or High(VIF)	
VDDLx	Digital Power(1.05V)	Power	Low(DGND) or HiZ	High(1.05V)	High(1.05V)	
VDDM	I/O Power(1.8V)	Power	Low(DGND) or HiZ	High(1.8V)	High(1.8V)	
VDDHx	Analog Power(2.8V)	Power	Low(DGND) or HiZ	High(2.8V)	High(2.8V)	
VSSHx	Analog GND	GND	AGND	AGND	AGND	
VSSLx	Digital GND	GND	DGND	DGND	DGND	

Note1: Presence of data signal due to common connection with other devices is accepted despite of the expected external state requirement in these cells.

Note2: Presence of clock signal due to common connection with other devices is accepted despite of the expected external state requirement in these cells.

Table 4-2 Input / Output Equivalent Circuit

Symbol	Equivalent Circuit	Symbol	Equivalent Circuit
INCK		XCLR SLASEL	
SCL SDA		XVS	
GPO FSTROBE			

5. Peripheral Circuit (Recommended schematic)

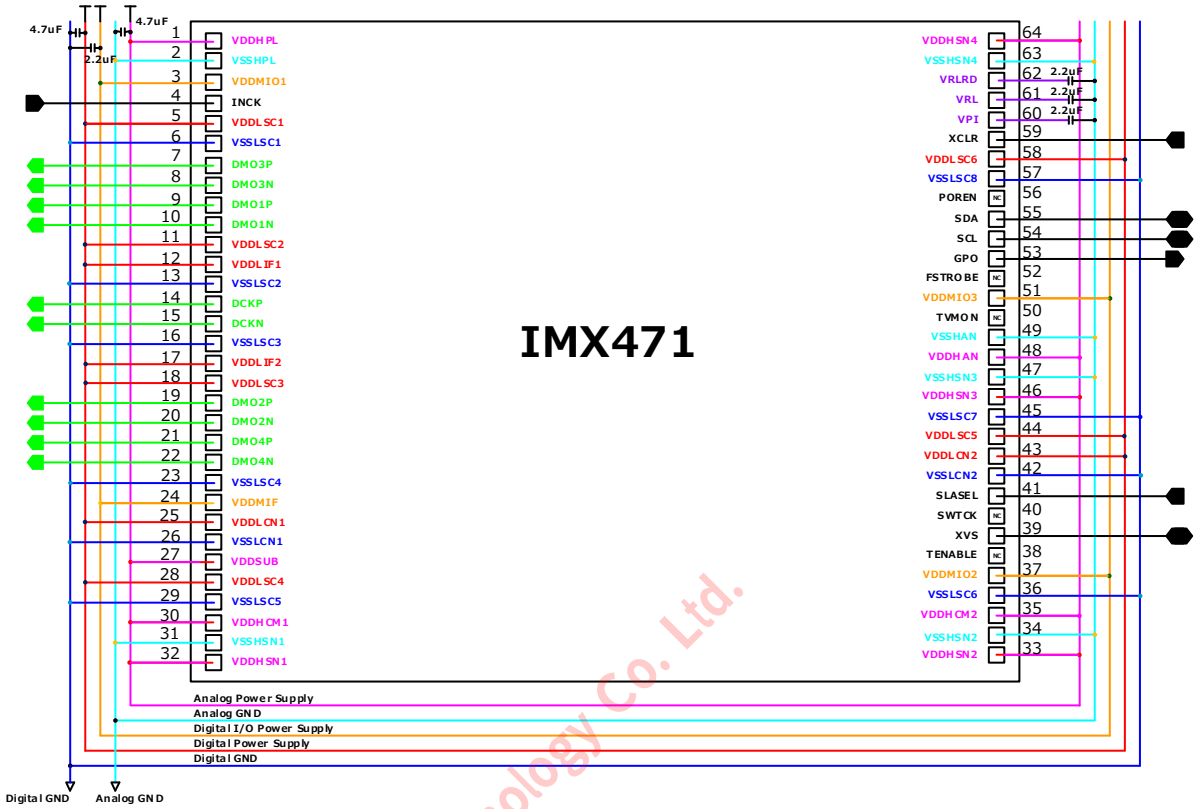


Figure 5-1 Peripheral Circuit (Recommended schematics)

Note1: I2C Slave Address can be changed by SLASEL pin.

Table 5-1 I2C Slave Address

SLASEL	I2C Slave Address
L or NC	0x34(write), 0x35(read)
H(VIF)	0x20(write), 0x21(read)

Common Note

Note2: Relationships between functions and status of the terminals are shown in Table 5-2.

Table 5-2 Relationships between functions and status of the terminals

Function	Relative pin	Status of the terminal in the schematic above
OTP	VDDHSN	use (VANA)
I2C Slave Address change	SLASEL	use(optional)
HWSTB Trigger	XCLR	use
Dual Sensor Synchronization	XVS	Use
Flash Strobe	FSTROBE	Not use(optional)
GPO	GPO	use

Note3: Back side or substrate of the sensor chip has a contact with Digital GND (VSSLSC) internally by following the above schematics. No other additional or intentional electrical contact is necessary.

Note4: The capacitor values and parts count used for decoupling of power supply lines in this diagram are determined only with Sony's testing environment. The capacitor values and/or parts count for power line decoupling may have to be reviewed and optimized by each manufacture depending on their design.

6. PSRR characteristics

PSRR [dB] is defined as shown in Figure 6-1and means how ripple noises induced onto power rails could be rejected and finally observed as horizontal seam noise at outputs of the sensor. PSRR performance discussed here is defined as the sensor's standalone performance against such noises that is modeled almost directly at sensor terminals. PSRR could be a guideline for understanding sensor's sensitivity and controlling power supply circuit design over power line ripple noises.

PSRR is measured for ripple noises on VANA and VDIG separately.

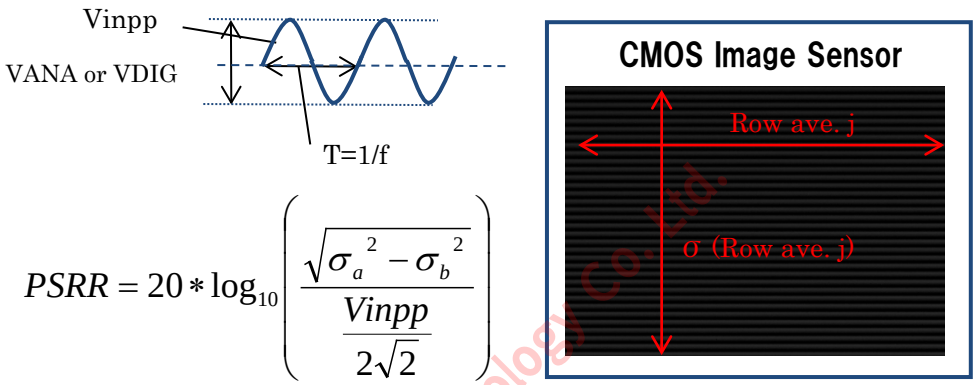


Figure 6-1 PSRR definition

Where:

Vinpp: Peak to peak voltage of input ripple on analog or digital power supply

σa: Standard deviation of row averages at Gr pixels [Vrms] by capturing a frame which has ripple noises.

σb: Standard deviation of row average at Gr pixels [Vrms] by capturing a frame which has no ripple noises.

The following figures show typical PSRR performance plots of this sensor which are measured on a random sample and the acceptable ripple noise plots which are derived by reverse calculation starting from the measured PSRR as known value and σa as a given parameter. For doing this, first determine acceptable noise level σa according to your product's design criteria of noise ratio index (NRI) within a range of 1/10 ~ 1/14(*1) of random noise (RN) of the sensor.

$$NRI = \sigma a / RN$$

$$\sigma a = NRI \times RN$$

Where, NRI stands for Noise Ratio Index and is an index value with which smaller the horizontal noise is less visible. RN stands for Random Noise and is defined as random noise measured over entire screen after removing any fixed pattern noise components.

Figure 6-2 shows measured PSRR values for the imposed ripple noises on VANA or VDIG. Figure 6-3 below shows example of allowable ripple noises derived from PSRR performance shown in Figure 6-2 for NRI value of 1/10, 1/12 and 1/14. One over ten (1/10) of RN is, for example, most compromised value as far as visibility of horizontal noise and technical difficulty. As the NRI goes smaller, the horizontal noise gets less visible but technically more difficult.

Note1: As the horizontal noise ratio over random noise goes smaller, the horizontal noise becomes less visible, but technically, it becomes more difficult. The NRI range shown here is only example and can be below or beyond of it depending on individual product situation.

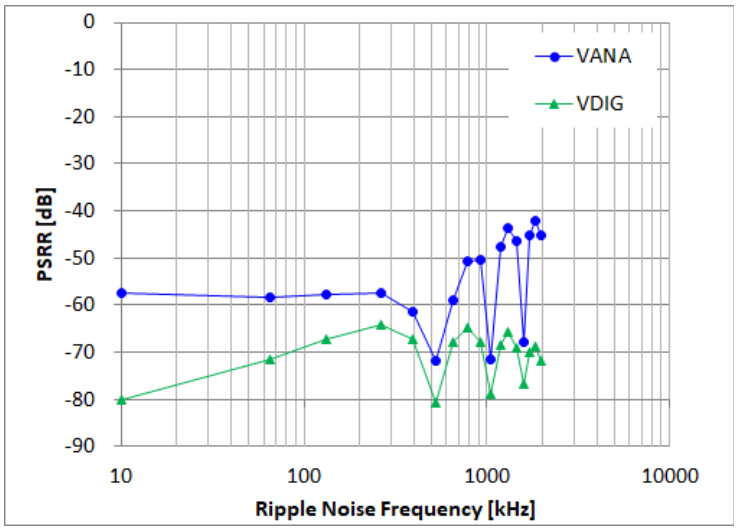
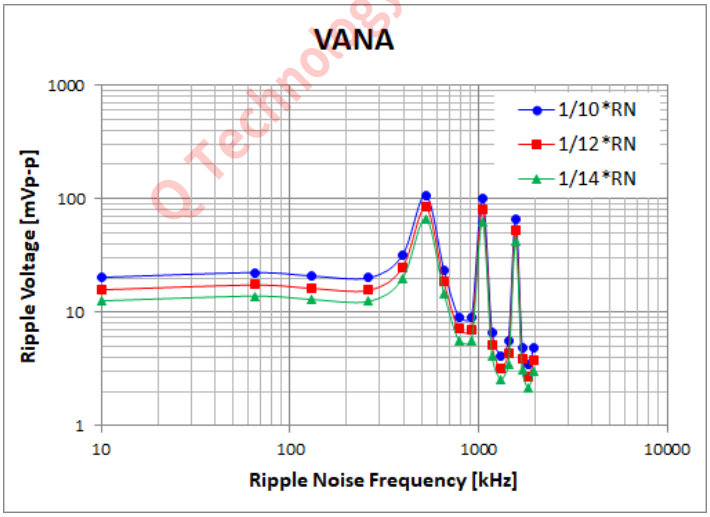
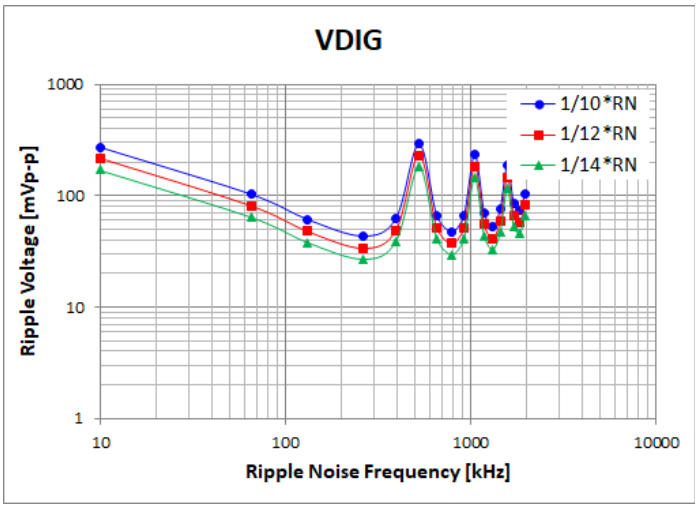


Figure 6-2 PSRR characteristics of VANA/VDIG



Pattern noise level: 1/10, 1/12, 1/14 of random noise

Figure 6-3 PSRR characteristics of VANA



Pattern noise level: 1/10, 1/12, 1/14 of random noise

Figure 6-4 PSRR characteristics of VDIG

7. PAD Structure

7.1. Normal Pad

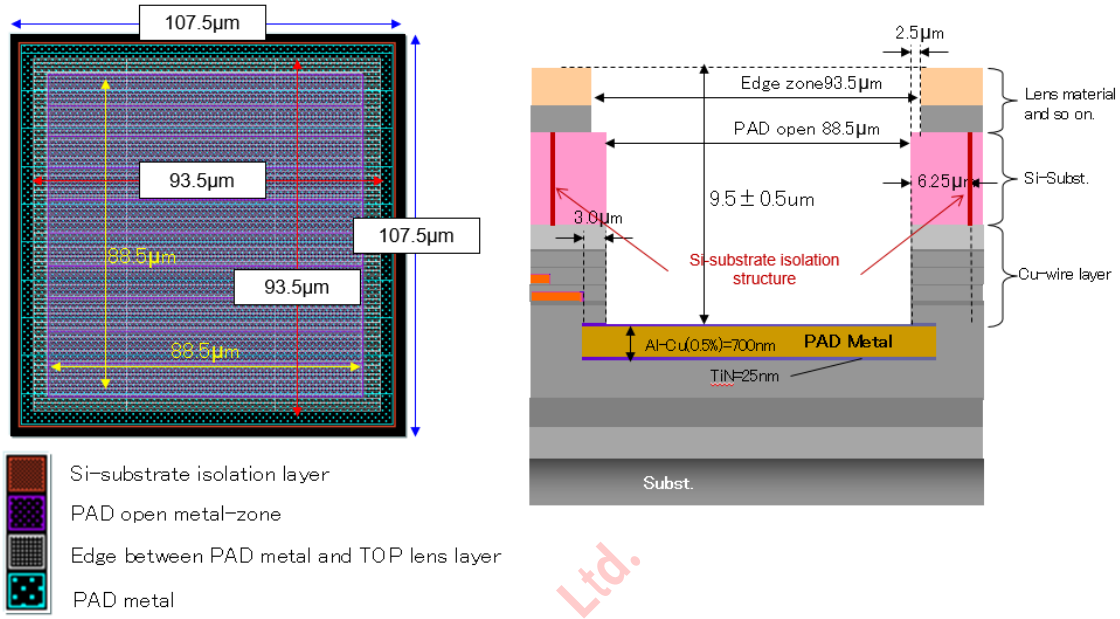


Figure 7-1 Normal pad structure (detail)

・PAD Pitch:108µm

・The distance between PAD-open area and metal wire: 3.0µm

・WB-Ball is not in contact with cavity-wall because of concern with crack.

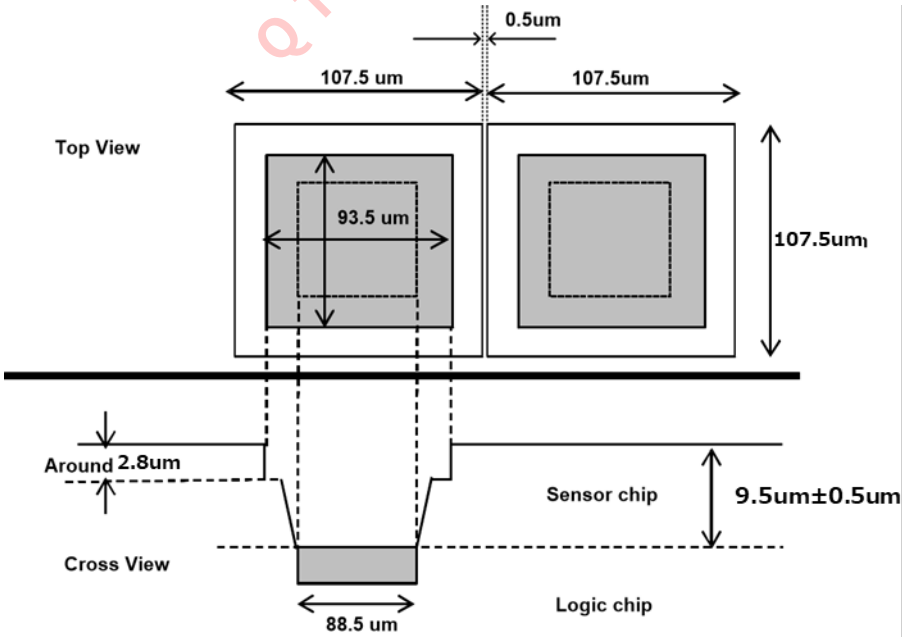


Figure 7-2 Dimensions of Normal Pad

7.2. Large Pad

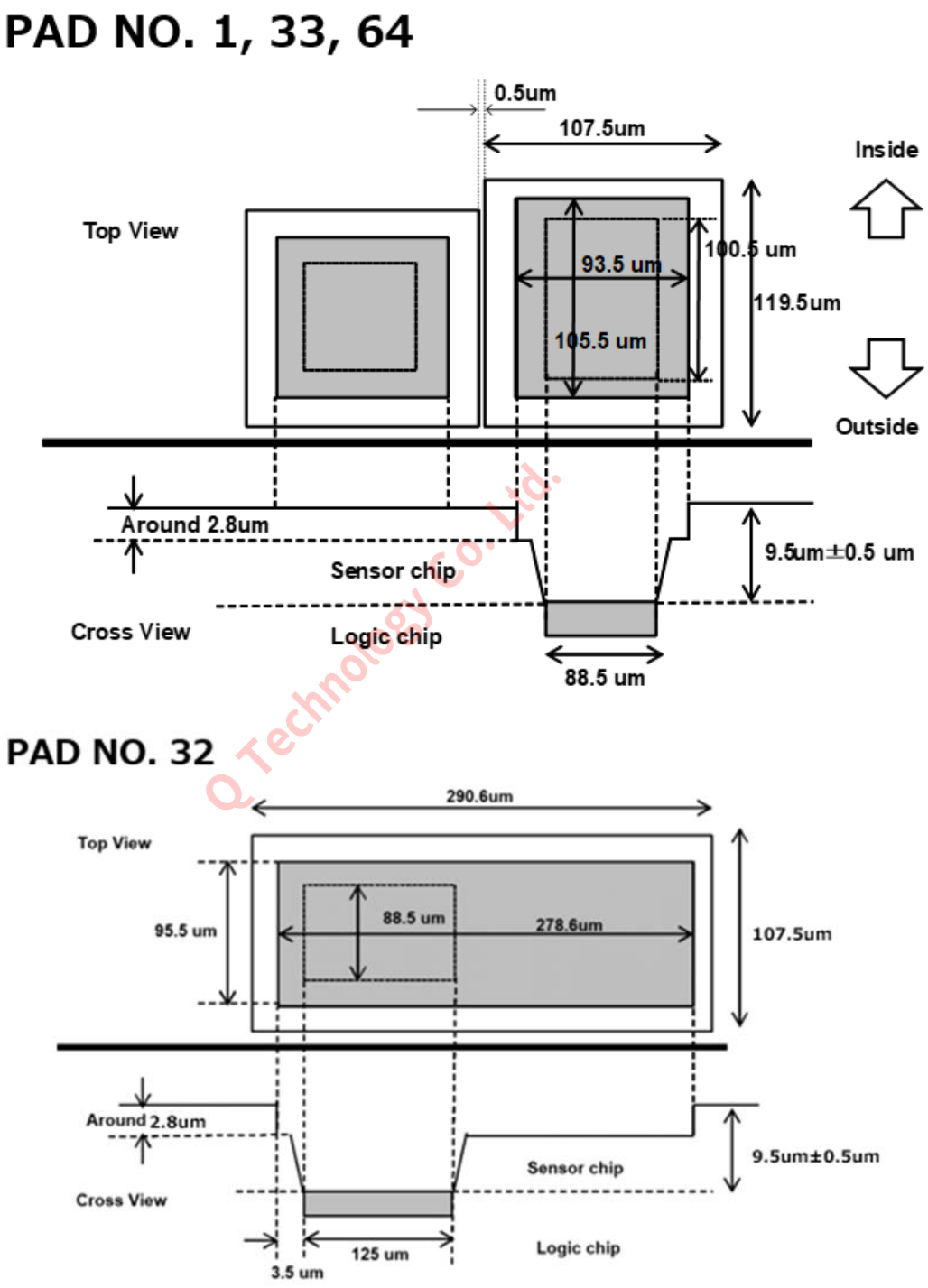


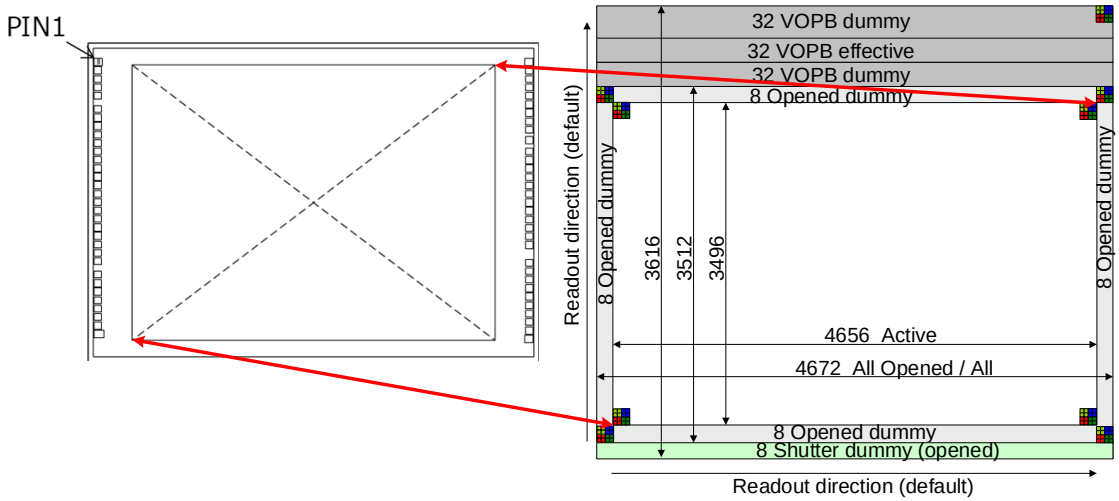
Figure 7-3 Dimensions of Large Pad

If a large pad is required by module integrator for wire-bonding testing, use “Large Pad”.

Both “Large Pad” is required pads for sensor operation;

Treat “Large Pad” the same as normal pad.

8. Pixel Array Information



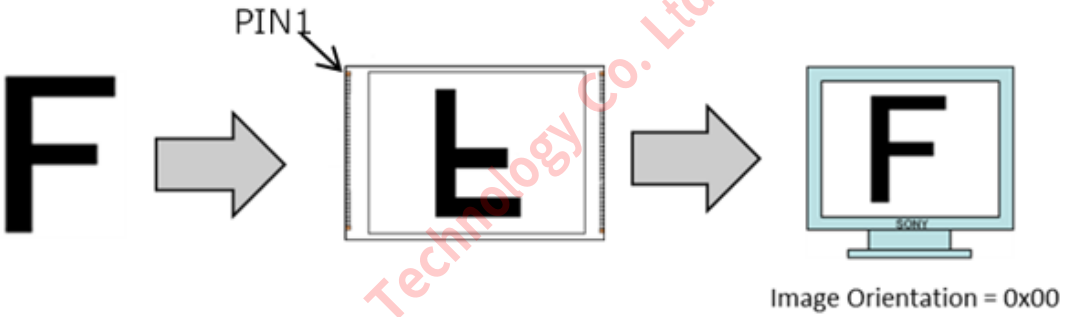


Figure 8-1 Pixel array information

9. Electrical Characteristics

Table 9-1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage (analog)	VANA	-0.3 to +3.3	V
Supply voltage (digital)	VDIG	-0.3 to +1.8	V
Supply voltage (interface)	VIF	-0.3 to +3.3	V
Input voltage (digital)	VI	-0.3 to +3.3	V
Output voltage (digital)	VO	-0.3 to +3.3	V
Guaranteed Operating temperature	TOPR	-20 to +70	˚C
Guaranteed storage temperature	TSTG	-30 to +80	˚C
Guaranteed performance temperature	TSPEC	-20 to +60	˚C

Table 9-2 Power Supply Voltage

Item	Symbol	Ratings	Unit	Remarks
Supply voltage (analog)	VANA	2.8 - 0.1/+0.2	V	
Supply voltage (digital)	VDIG	1.05 ± 0.1	V	
Supply voltage (interface)	VIF	1.8 ± 0.1	V	

10. Power Consumption

In this chapter, power consumptions of this sensor in each condition for typical case and worst case are shown.

Table 10-1 Current consumption

Item		Symbol	Normal mode(*3)		Unit
			Typ.(*1)	Worst(*2)	
Full Pixel 30fps (H: 4656, V: 3496)	Analog Current(VANA)	IANA	40.9	46.0	mA
	Digital Current(VDIG)	IDIG	162.0	256.7	mA
	I/O Current(VIF)	IIF	2.3	2.8	mA
	Total Power		288.8	438.5	mW
2×2 Binning(4:3) 120fps (H:2328, V:1748)	Analog Current(VANA)	IANA	46.4	52.1	mA
	Digital Current(VDIG)	IDIG	149.1	248.5	mA
	I/O Current(VIF)	IIF	2.4	2.8	mA
	Total Power		290.8	447.2	mW
2×2 Binning(16:9) 150fps (H:2328, V:1748)	Analog Current(VANA)	IANA	44.8	50.4	mA
	Digital Current(VDIG)	IDIG	143.7	239.3	mA
	I/O Current(VIF)	IIF	2.4	2.9	mA
	Total Power		280.7	432.0	mW
SW STB	Analog Current(VANA)	IANA	2.5	2.7	mA
	Digital Current(VDIG)	IDIG	2.1	14.8	mA
	I/O Current(VIF)	IIF	16.5	20.4	µA
	Total Power		9.2	25.2	mW
HW STB(*4)	Analog Current(VANA)	IANA	0.87	17.3	µA
	Digital Current(VDIG)	IDIG	0.66	27.2	µA
	I/O Current(VIF)	IIF	0.07	1.8	µA
	Total Power		3.3	86.6	µW

Note1: VANA=2.8V, VDIG=1.05V, VIF=1.8V, Ta=25°C Process corner of transistors: TT*

Note2: VANA=3.0V, VDIG=1.15V, VIF=1.9V, Ta=60°C Process corner of transistors: FF*

(Remarks, * TT: T stands for Typical, FF: F stands for Fast)

Note3: [Function] DPC2D: ON

Note4: XCLR:Low fixed, INCK:stop, SLASEL:NC or Low fixed, XVS:NC or High fixed

Common Note

Note5: Typ. and Worst values are result of ES evaluation; they are not the specification value.

Note6: The above values are values during stable state, not instantaneous values.

11. CRA Characteristics of Recommended Lens

11.1. Target CRA

The following figure and table show the target CRA (chief ray angle)

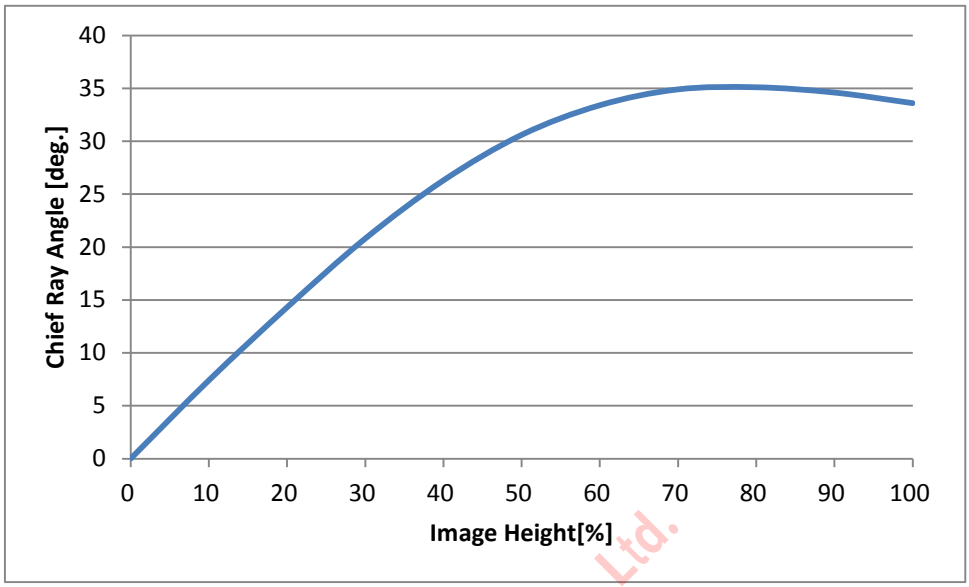


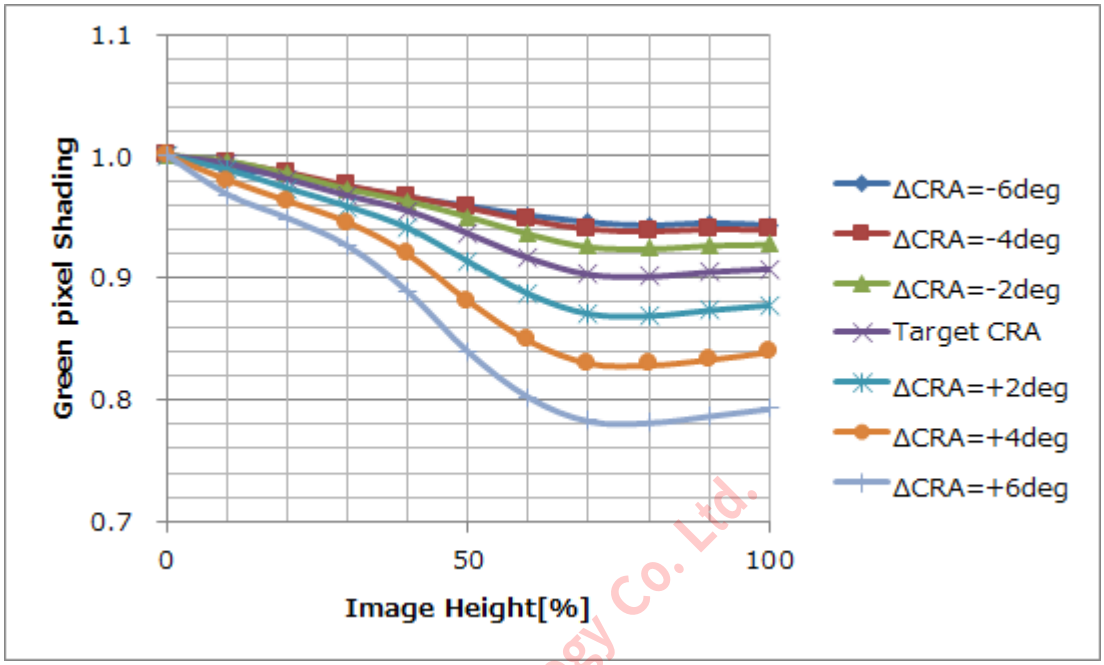
Figure 11-1 Target CRA

Table 11-1 Target CRA values

Image Height		Target CRA
[%]	[mm]	[deg.]
0.0	0.00	0.0
10.0	0.291	7.4
20.0	0.582	14.3
30.0	0.873	20.8
40.0	1.164	26.3
50.0	1.455	30.6
60.0	1.746	33.4
70.0	2.037	34.9
80.0	2.328	35.1
90.0	2.619	34.6
100.0	2.911	33.6

11.2. ΔCRA-Shading characteristics

The following figure shows shading characteristics of Green (average of Gr and Gb) pixel over difference between given lens's CRA and the target CRA by image height.

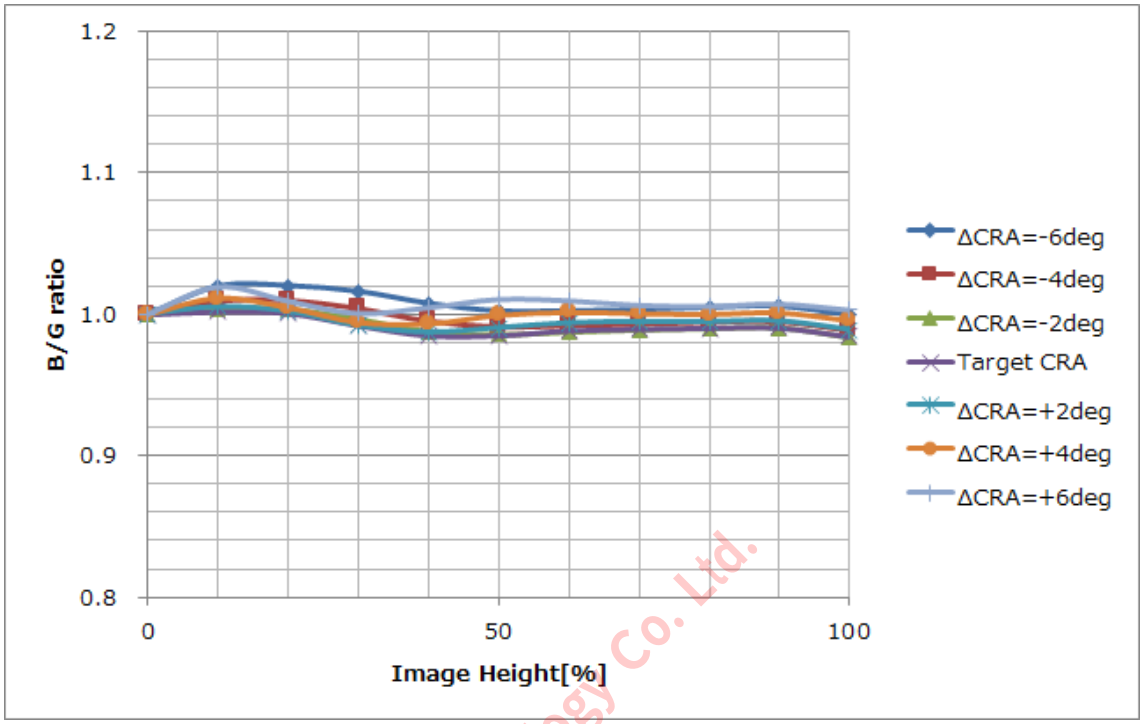


Common Note

Note1: Figure 11-2 plot range of ΔCRA does not directly linked with acceptable performance shift. Actual judgment may be done by customer's own criteria.

Figure 11-2 ΔCRA- Green Shading characteristics

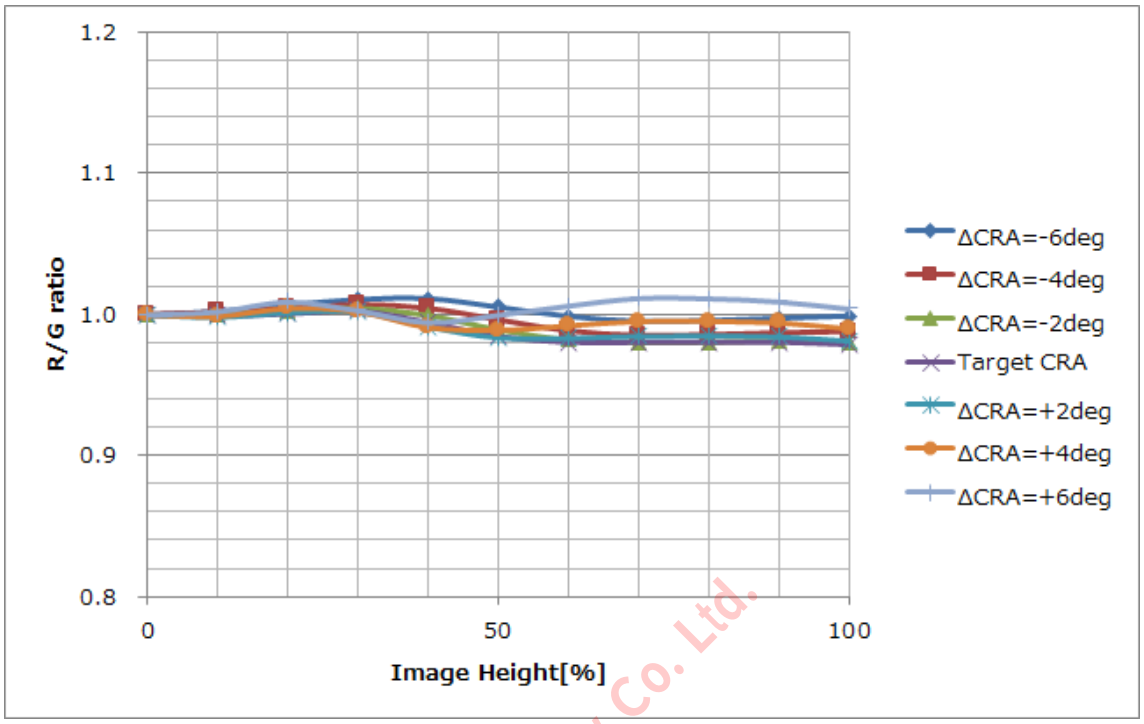
The following two table shows sensitivity ratio characteristics of B/G and R/G over difference between given lens's CRA and the target CRA by image height.



Common Note

Note1: Figure 11-3 plot range of ΔCRA does not directly linked with acceptable performance shift. Actual judgment may be done by customer's own criteria.

Figure 11-3 ΔCRA-Sensitivity Ratio(B/G) characteristics



Common Note

Note1: Figure 11-4 plot range of ΔCRA does not directly linked with acceptable performance shift. Actual judgment may be done by customer's own criteria.

Figure 11-4 ΔCRA-Sensitivity Ratio (R/G) characteristics

12. Spectral Sensitivity Characteristics

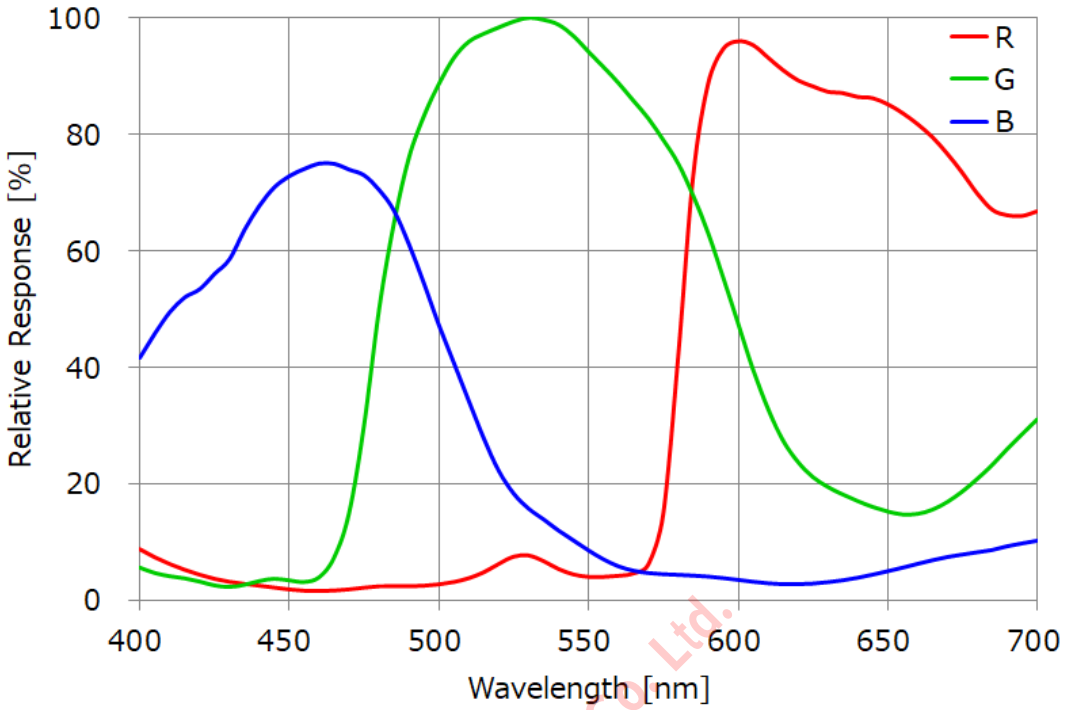


Figure 12-1 Spectral sensitivity characteristics

Table 12-1 Spectral sensitivity values

Wave Length [nm]	Relative response			
	R	GR	GB	B
400	8.77	5.67	5.67	41.69
405	7.38	4.74	4.75	45.83
410	6.21	4.20	4.19	49.51
415	5.23	3.83	3.83	52.07
420	4.38	3.27	3.27	53.47
425	3.66	2.62	2.61	56.10
430	3.15	2.34	2.36	58.64
435	2.80	2.73	2.71	63.65
440	2.49	3.37	3.37	67.83
445	2.17	3.75	3.76	70.98
450	1.84	3.49	3.47	72.91
455	1.63	3.21	3.19	74.13
460	1.57	4.03	4.03	75.06

Wave Length [nm]	Relative response			
	R	GR	GB	B
465	1.66	7.40	7.42	75.01
470	1.86	15.11	15.08	74.02
475	2.16	30.13	30.12	73.05
480	2.38	50.01	49.94	70.54
485	2.41	64.91	64.84	66.95
490	2.38	76.02	76.03	61.17
495	2.50	83.16	83.17	54.46
500	2.72	88.66	88.62	47.31
505	3.13	93.15	93.09	40.81
510	3.78	95.89	95.87	34.28
515	4.81	97.26	97.27	27.84
520	6.24	98.31	98.35	22.30
525	7.48	99.32	99.39	18.37
530	7.68	99.93	100.00	15.79
535	6.70	99.62	99.66	13.94
540	5.36	98.80	98.81	12.02
545	4.42	96.86	96.86	10.33
550	4.02	94.19	94.17	8.61
555	4.01	91.56	91.54	7.09
560	4.19	88.81	88.80	5.89
565	4.60	85.75	85.80	5.14
570	6.16	82.69	82.75	4.74
575	14.80	79.03	79.04	4.54
580	41.98	75.03	74.90	4.42
585	72.86	69.62	69.38	4.28
590	88.73	63.22	62.87	4.12
595	94.65	55.69	55.28	3.86
600	95.98	47.82	47.34	3.56
605	95.34	39.95	39.39	3.23
610	93.21	33.23	32.64	2.97
615	91.05	27.84	27.20	2.82
620	89.30	24.14	23.48	2.81
625	88.26	21.57	20.86	2.92
630	87.34	19.89	19.12	3.16

Wave Length [nm]	Relative response			
	R	GR	GB	B
635	87.09	18.62	17.80	3.48
640	86.44	17.52	16.65	3.92
645	86.23	16.50	15.66	4.46
650	85.19	15.72	14.87	5.05
655	83.66	15.21	14.38	5.66
660	81.77	15.30	14.47	6.30
665	79.51	16.00	15.23	6.94
670	76.65	17.30	16.58	7.48
675	73.40	19.07	18.42	7.91
680	69.83	21.21	20.60	8.31
685	67.05	23.58	23.03	8.70
690	66.12	26.30	25.73	9.33
695	66.00	28.85	28.29	9.83
700	66.79	31.36	30.85	10.28

13. Notes on IR-Cut Selection

Common Note

Note1: Image captured at 2300K (Low color temp.)

Figure 13-1 IR-Cut filter dependency for the image quality

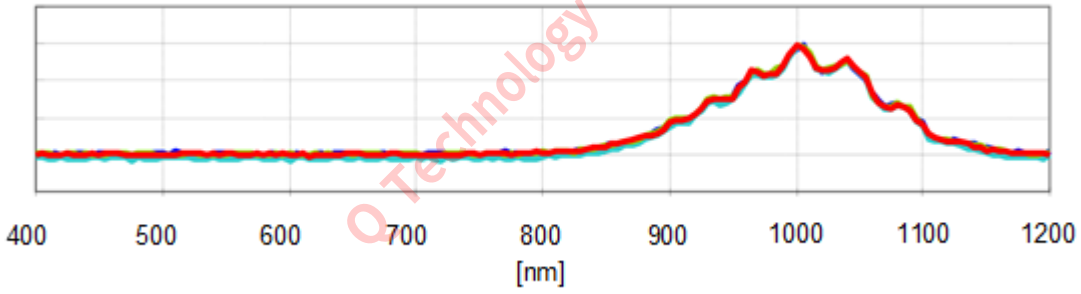


Figure 13-2 Output response of the optical black (OB)

Proper selection of IR-Cut filter is critical for an overall image quality of camera system. Optical Black output response at different wavelength is one of important factors when selecting IR Cut filter.

For this sensor, SONY recommends IR cut filter with cut off from 780 to 1200nm.

14. Power Supply Slew Rate

Maximum slew rate (mV/μs) is specified for each power supply to avoid excess inrush current or oscillation during power on sequence.

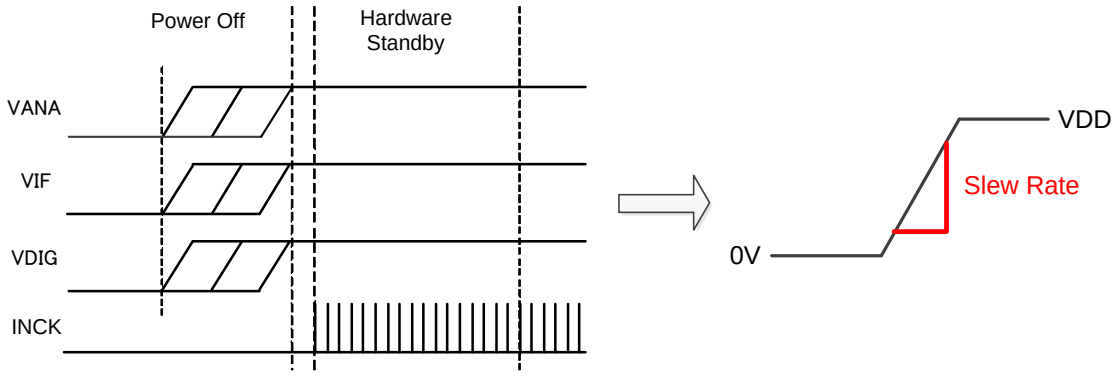


Figure 14-1 Power on slew rate

Table 14-1 Limitation on power-on slew rate

Power Supplies	Slew Rate			Comment
	Min	Max	Unit	
VANA, VIF, VDIG	-	50	mV/μs	

15. Consideration for camera module design

In this chapter, some of key information and tips for camera module design for achieving preferable overall signal integrity performance and hence the good picture quality is discussed.

15.1. Recommended sensor placement (orientation)

For eliciting potential performance of the sensor, the following precaution must be cared.

- Keep the pattern layout of digital power supply rails away from the analog power supply, analog GND and other sensitive analog signal lines such as VRL/VPI as far as possible.
- Keep wiring space underneath the sensor chip as wide as possible.

See Module Layout Design Guide for mobile CIS for more practical explanation.

In practically realizing the above key issues, consideration on placement or orientation of the sensor chip within the module PWB is going to be shown in below diagram, Figure 15-1 (a) – (d).

(a) Best layout for IMX471. This layout would realize both widest wiring space and no overwrap over analog power/analog GND.
(b) This layout is not recommended because of overwrap with power supply/analog GND pad.
(c) Alternative layout for IMX471. This layout still keeps relatively wider space and avoiding overwrap with analog power supply/analog GND pad.
(d) Same as (c).

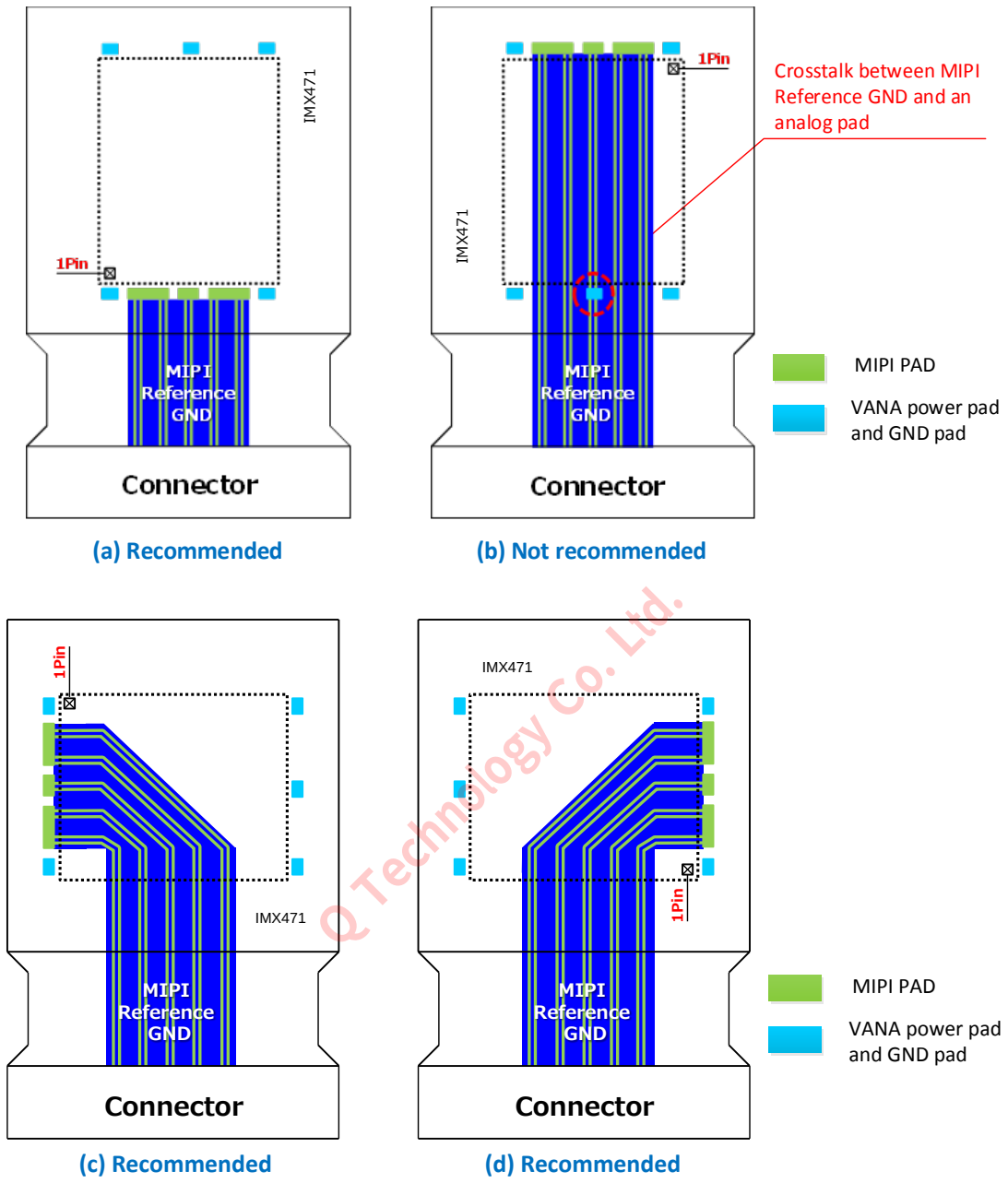


Figure 15-1 Camera module design layout

15.2. Setting upright image

As you may already aware, following the recommended layout of either Figure 15-1 (a), (c) or (d), you may have to have flexibility of mirroring and/or flipping of the image. In this section, method of the image orientation arrangement is explained.

Image's flip and mirror settings

The recommended module layouts are proposals of favorable module structure from a view point of overall image quality. Contrary, they substantially reduce a potential flexibility of physical arrangements in module design for mounting into individual phone design.

To manage such physical difficulties, the sensor has a capability of flipping and mirroring the image outputs. The flipping and/or mirroring operation can be achievable with the register called "IMG_ORIENTATION_V/H" (0x0101). See Figure 15-2 for the flipping and mirroring example.

The following diagram shows an example of flexibility in mounting orientation using the common module design. In this way, the module structure can be determined only from noise interference point of view.

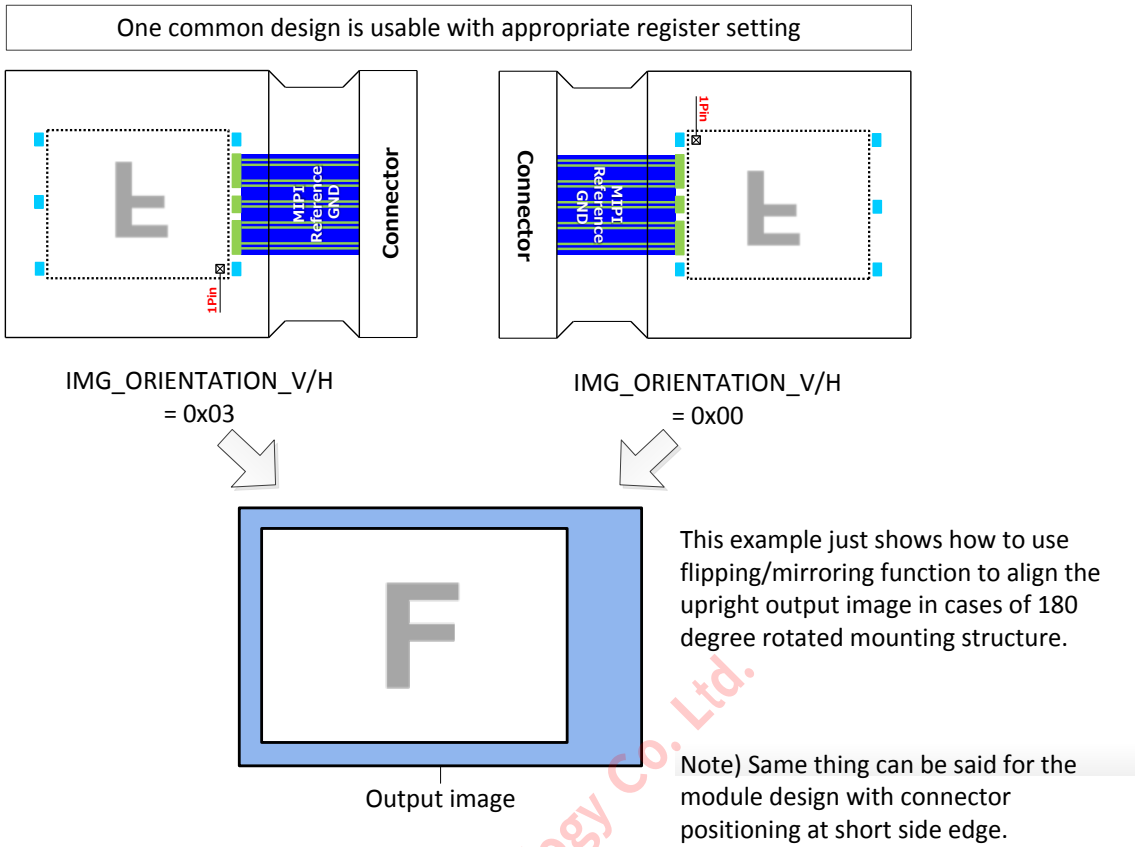


Figure 15-2 Layout with priority on MIPI out and image flip/mirror relation

Refer to “4.4 Readout start position” in Software Reference Manual for the complete information to meet your specific requirement.

16. Design concept for critical pattern layout

In this chapter, some module example patterns are shown to indicate how to follow Sony "Module Layout Design Guide for mobile CIS" (hereinafter referred to as "Design Concept").

See "Module Layout Design Guide for mobile CIS" for more practical explanation.

From the recommended orientation which is explained in the section「15.1. Recommended sensor placement (orientation)」, two kinds of the Design Concept are prepared.

One is in the case of pulling out MIPI signals from a short side edge of the chip (hereinafter referred to as "Portrait orientation"), which is shown in below Figure 16-1.
Another is in the case of pulling out MIPI signals from a long side edge of the chip (hereinafter referred to as "Landscape orientation"), which is shown in below Figure 16-2.

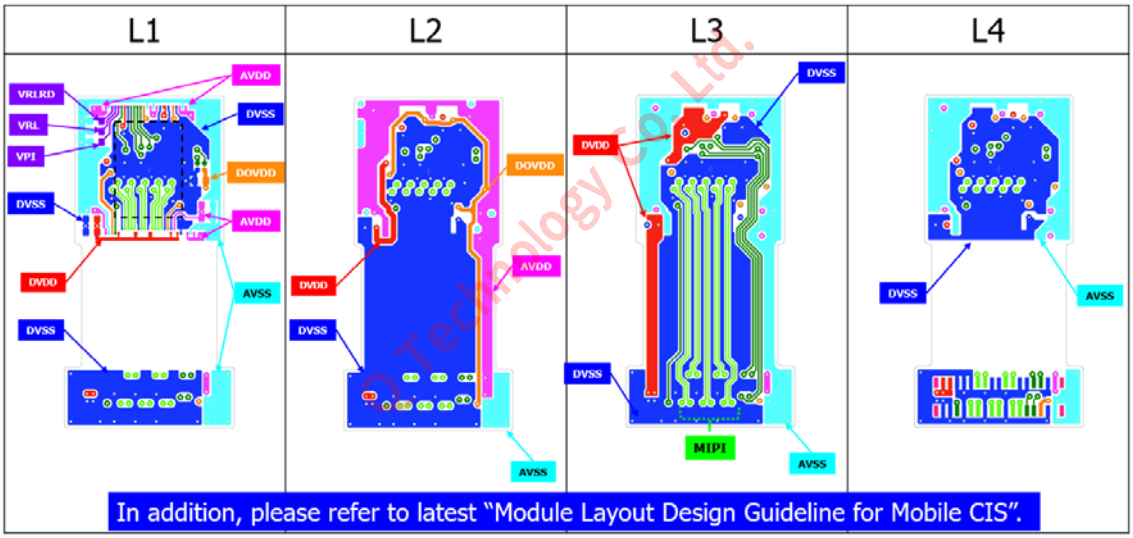


Figure16-1 Design Concept pattern(Portrait location)

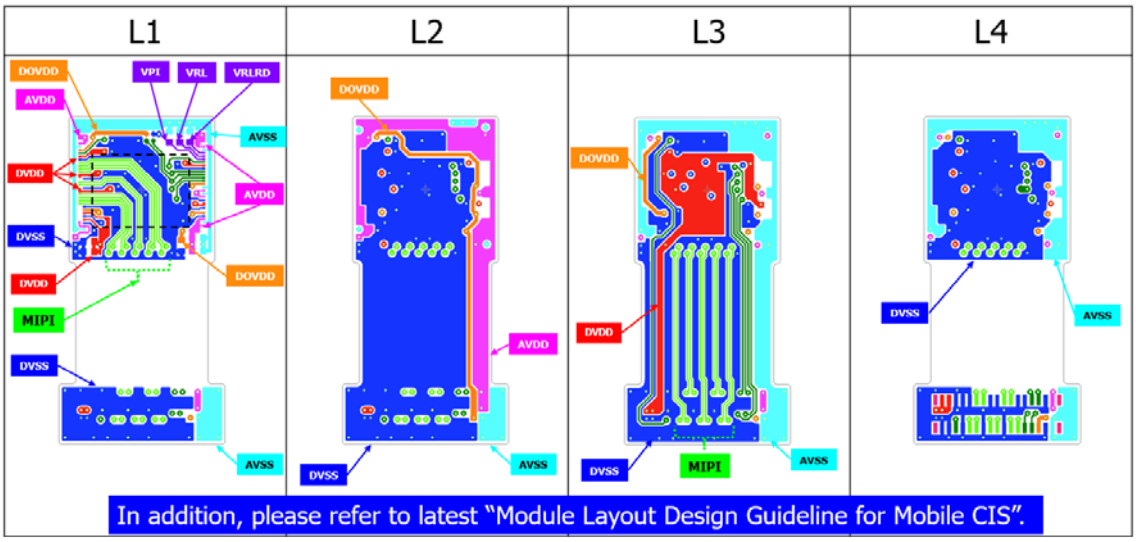
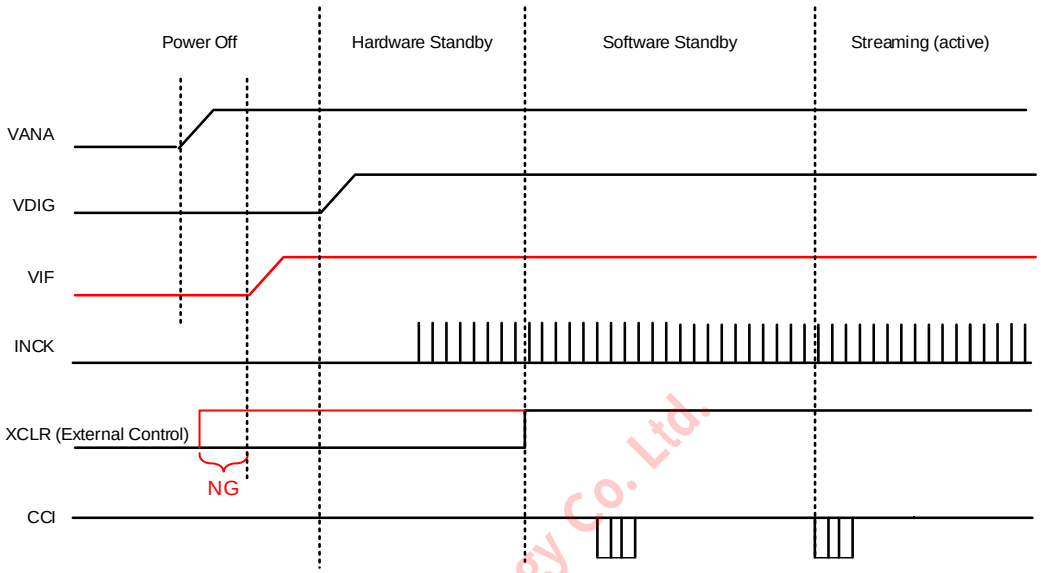


Figure16-2 Design Concept pattern(Landscape location)

Appendix

A-1. Constraints of XCLR in Startup sequence

XCLR must remain low when VIF is off.



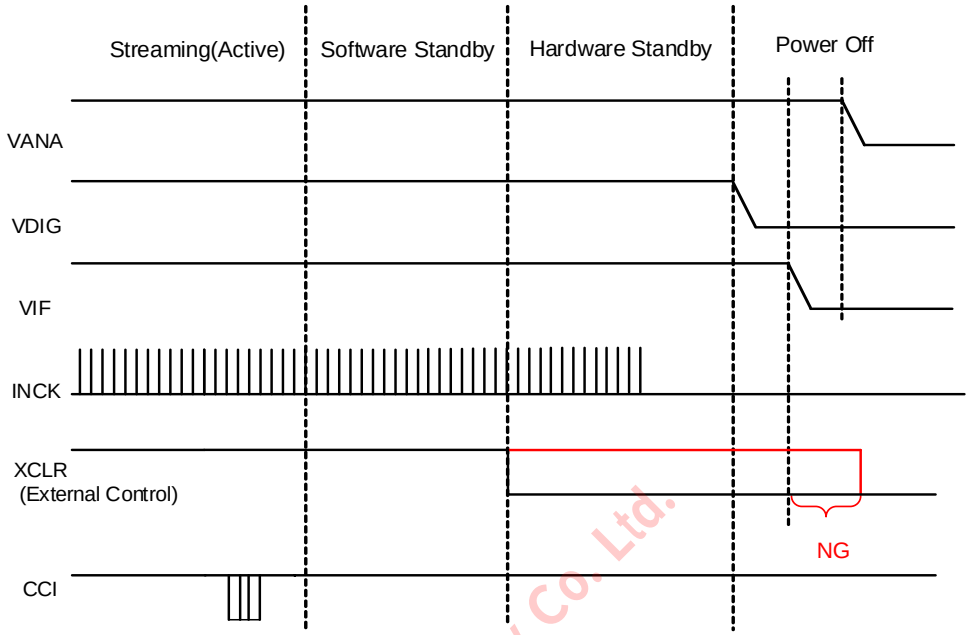
Common Note

Note1: Ignore this constraint if XCLR is not controlled externally (XCLR is open).

Figure A-1 Constraint of XCLR in Startup sequence

A-2. Constraints of XCLR in Power down sequence

XCLR must remain low when VIF is low.



Common Note

Note1: Ignore this constraint if XCLR is not controlled externally (XCLR is open).

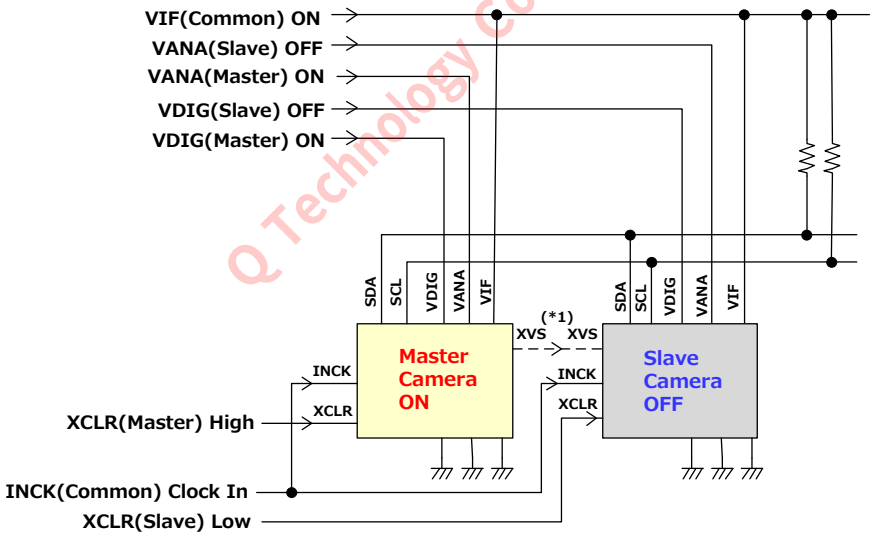
Figure A-2 Constraint of XCLR in Power down sequence

A-3. Sharing power and signal lines with other sensors

In use case with sharing power rails between this sensor and other devices, refer to the following conditions to follow; relations XCLR and ON/OFF combinations of power supplies and INCK.

Table A-1 Signal / power supply sharing constraints(external reset)

XCLR	INCK	VDIG	VANA	VIF	Sensor status	Availability tolerance
Low	Low or Clock	OFF	OFF	OFF	Power off	OK
	Low or Clock	At least one of them is ON			Hardware standby	OK
High	Low	ON	ON	ON		OK
	Low or Clock	At least one of them is OFF		ON		Forbidden (Not recommended)
	Low or Clock	Any combinations of ON/OFF		OFF		Forbidden (Risk of excess current)
	Clock	ON	ON	ON	Software standby or Streaming	OK



Note1: This Note doesn't apply to the sensor without XVS terminal. In Slave mode and connecting XVS terminal with master sensor, it is required to share power supplies of VIF. Because there is a risk of excess current when slave VIF is OFF and master inputs high signal to XVS terminal.

Figure A-3 Sharing of I2C, INCK and VIF

A-4. Detailed circuit diagram of each Power source and GND

The following figure shows the detailed circuit diagram of each Power source and GND.

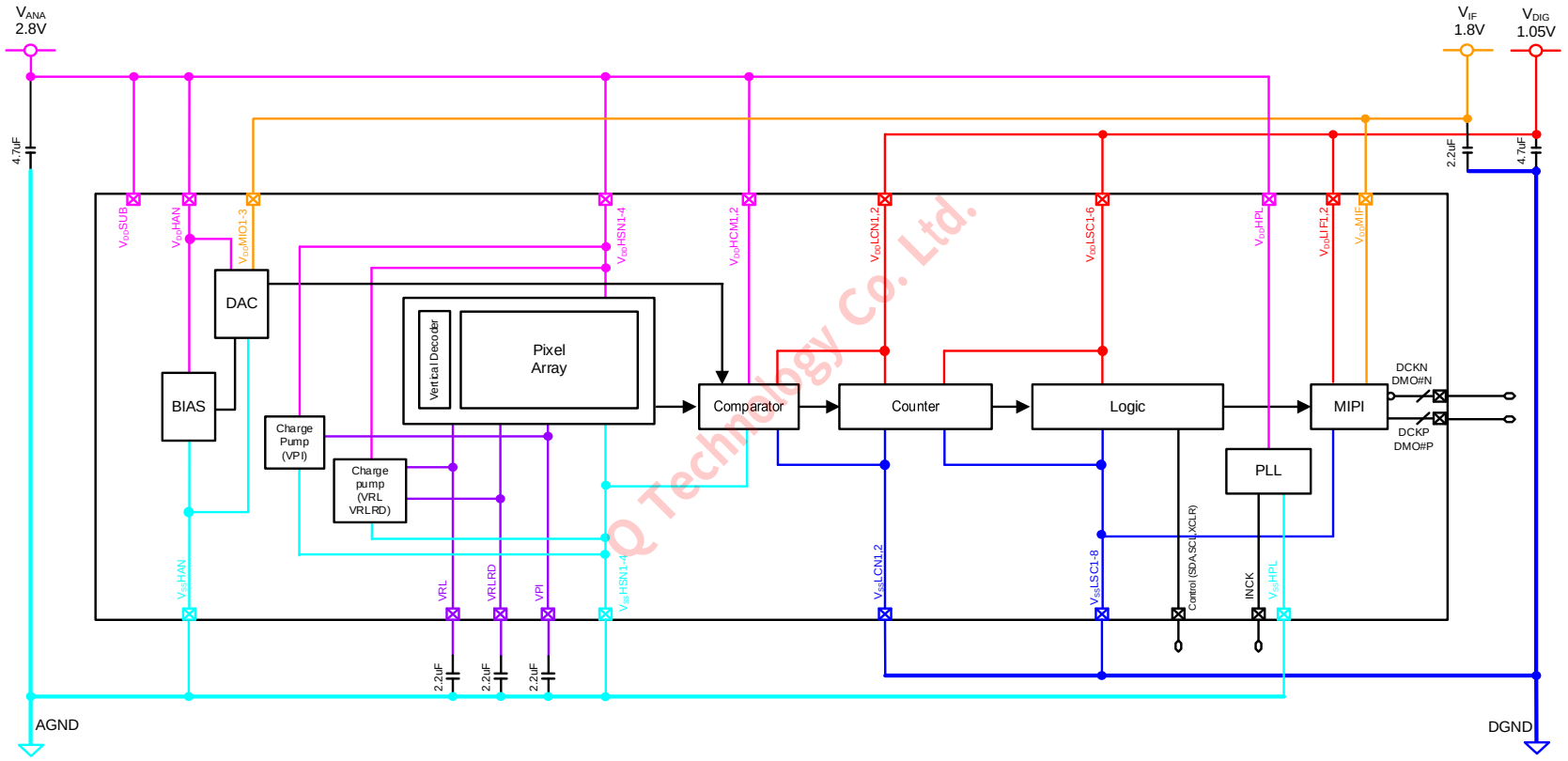


Figure A-4 Detailed circuit diagram of each Power source and GND