SONY

Diagonal 5.822 mm (Type 1/3.09) 16Mega-Pixel CMOS Image Sensor with Square Pixel for Color Cameras

IMX471-AAJH5-C

General description and application

IMX471-AAJH5-C is a diagonal 5.822 mm (Type 1/3.09) 16 Mega-pixel CMOS active pixel type stacked image sensor with a square pixel array. It adopts Sony's back-illuminated and stacked CMOS image sensor to achieve high speed image capturing by column parallel A/D converter circuits and high sensitivity and low noise image (comparing with conventional CMOS image sensor) through the backside illuminated imaging pixel structure. R, G, and B pigment primary color mosaic filter is employed. It equips an electronic shutter with variable integration time. It operates with three power supply voltages: analog 2.8 V, digital 1.05 V and 1.8 V for input/output interface and achieves low power consumption.
In addition, this product is designed for use in cellular phone and tablet pc. When using this for another application, Sony Semiconductor Solutions Corporation does not guarantee the quality and reliability of product. Therefore, don't use this for applications other than cellular phone and tablet pc. Consult your Sony Semiconductor Solutions Corporation sales representative if you have any questions.

Functions and Features

- ◆ Back-illuminated and stacked CMOS image sensor
- ◆ High Signal to Noise Ratio (SNR)
- ◆ High Frame Rate 30fps@Full resolution / 120fps@2x2 Adjacent Pixel Binning(4:3) / 150fps@2x2 Adjacent Pixel Binning(16:9)
- ◆ Quasi-synchronous system for dual camera system
- ◆ Built-in 2D Dynamic Defect Pixel Correction
- ◆ 4-ch Lens Shading Correction (LSC)
- ◆ Output video format of RAW10/8, COMP8
- ◆ CSI-2 serial data output (MIPI 2lane/4lane, Max. 1.84Gbps/lane, D-PHY spec. ver. 1.2 compliant)
- ◆ 2-wire serial communication
- ◆ Two PLLs for independent clock generation for pixel control and data output interface
- ◆ 4K bit of OTP ROM for users
- ◆ Built-in temperature sensor
- ◆ Quad Bayer Coding color filter arrangement

Device Structure

◆CMOS image sensor
◆Image size : Diagonal 5.822 mm (Type 1/3.09)
◆Total number of pixels : 4672 (H) × 3572 (V) approx. 16.69 M pixels
◆Number of effective pixels : 4672 (H) × 3512 (V) approx. 16.41 M pixels
◆Number of active pixels : 4656 (H) × 3496 (V) approx. 16.28 M pixels
◆Chip size : 5.782 mm (H) x 4.054 mm (V)
◆Unit cell size : 1.00 µm (H) × 1.00 µm (V)
◆Substrate material : Silicon

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	-0.3 to +3.3	V	refer to VSS level
Supply voltage (digital)	VDIG	-0.3 to +1.8	V	
Supply voltage (interface)	VIF	-0.3 to +3.3	V	
Input voltage (digital)	VI	-0.3 to +3.3	V	
Output voltage (digital)	VO	-0.3 to +3.3	V	
Guaranteed Operating temperature	TOPR	-20 to +70	˚C	
Guaranteed storage temperature	TSTG	-30 to +80	˚C	
Guaranteed performance temperature	TSPEC	-20 to +60	˚C	

Recommended Operating Voltage

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	VANA	2.8 -0.1 / +0.2	V	refer to VSS level
Supply voltage (digital)	VDIG	1.05 ± 0.1	V	
Supply voltage (interface)	VIF	1.8 ± 0.1	V	

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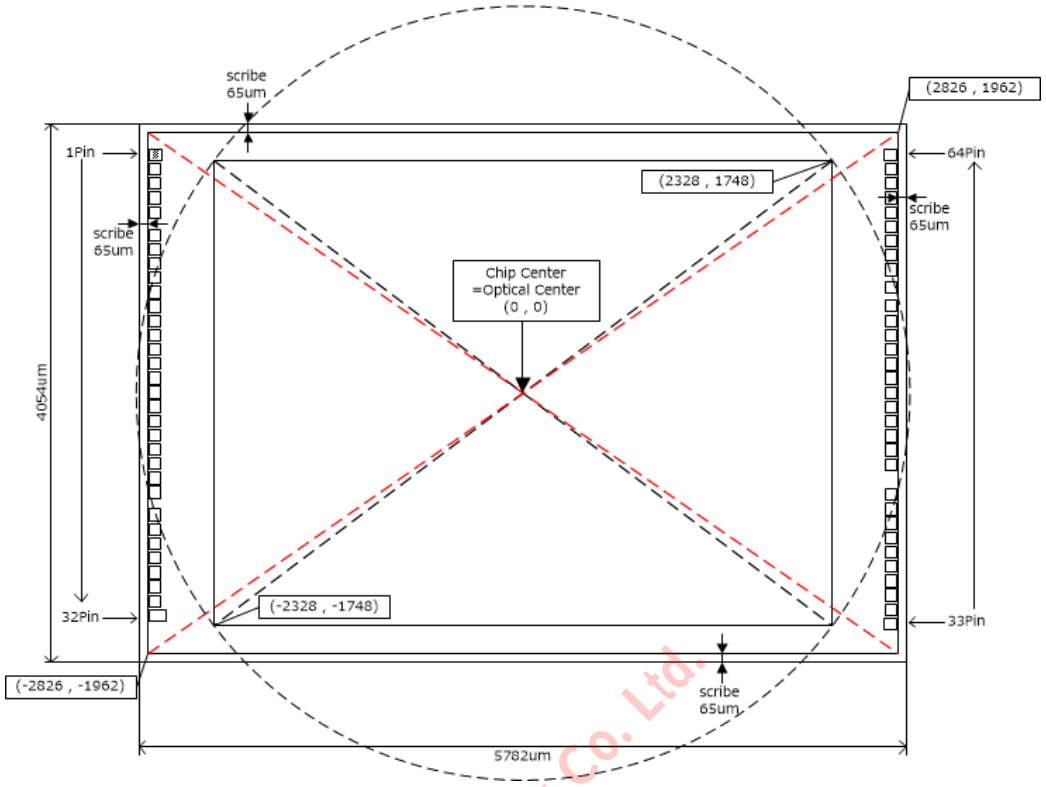
General-0.0.9

Contents

1. Chip Center and Optical Center



*1 Actual size of a chip will be smaller than indicated when dicing (scribe) is taken into account.

*2 Some PADs are located in image circle.

Figure 1 Chip Center and Optical Center (x and y coordinates in µm)

2. Pin Coordinates

Table 1 Pin Coordinates

No.	Symbol	X	Y
1	VDDHPL	-2763.25	1791
2	VSSHPL	-2769.25	1683
3	VDDMIO1	-2769.25	1575
4	INCK	-2769.25	1467
5	VDDLSC1	-2769.25	1359
6	VSSLSC1	-2769.25	1188.24
7	DMO3P	-2769.25	1080.72
8	DMO3N	-2769.25	973.2
9	DMO1P	-2769.25	865.68
10	DMO1N	-2769.25	758.16
11	VDDLSC2	-2769.25	650.64
12	VDDLIF1	-2769.25	543.12
13	VSSLSC2	-2769.25	435.6
14	DCKP	-2769.25	328.08
15	DCKN	-2769.25	220.56
16	VSSLSC3	-2769.25	113.04
17	VDDLIF2	-2769.25	5.52
18	VDDLSC3	-2769.25	-102
19	DMO2P	-2769.25	-209.52
20	DMO2N	-2769.25	-317.04
21	DMO4P	-2769.25	-424.56
22	DMO4N	-2769.25	-532.08
23	VSSLSC4	-2769.25	-639.6
24	VDDMIF	-2769.25	-747.12
25	VDDLCN1	-2769.25	-918
26	VSSLCN1	-2769.25	-1026
27	VDDSUB	-2769.25	-1134
28	VDDLSC4	-2769.25	-1242
29	VSSLSC5	-2769.25	-1350
30	VDDHCM1	-2769.25	-1458
31	VSSHSN1	-2769.25	-1566
32	VDDHSN1	-2751	-1674
33	VDDHSN2	2763.25	-1737
34	VSSHSN2	2769.25	-1629
35	VDDHCM2	2769.25	-1521

No.	Symbol	X	Y
36	VSSLSC6	2769.25	-1413
37	VDDMIO2	2769.25	-1305
38	TENABLE	2769.25	-1197
39	XVS	2769.25	-1089
40	SWTCK	2769.25	-981
41	SLASEL	2769.25	-873
42	VSSLCN2	2769.25	-765
43	VDDLCN2	2769.25	-538.2
44	VDDLSC5	2769.25	-430.2
45	VSSLSC7	2769.25	-322.2
46	VDDHSN3	2769.25	-214.2
47	VSSHSN3	2769.25	-106.2
48	VDDHAN	2769.25	1.8
49	VSSHAN	2769.25	109.8
50	TVMON	2769.25	217.8
51	VDDMIO3	2769.25	325.8
52	FSTROBE	2769.25	433.8
53	GPO	2769.25	541.8
54	SCL	2769.25	654.3
55	SDA	2769.25	792.9
56	POREN	2769.25	927
57	VSSLSC8	2769.25	1035
58	VDDLSC6	2769.25	1143
59	XCLR	2769.25	1251
60	VPI	2769.25	1359
61	VRL	2769.25	1467
62	VRLRD	2769.25	1575
63	VSSHSN4	2769.25	1683
64	VDDHSN4	2763.25	1791

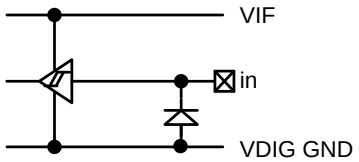
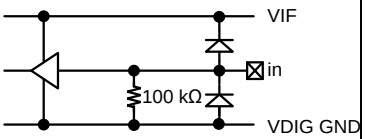
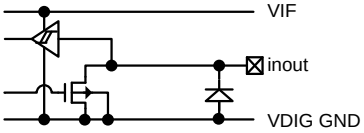
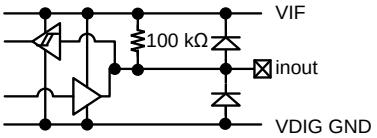
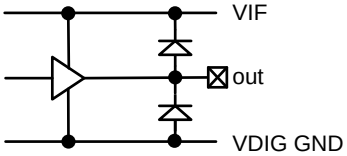
3. Pin Description

Table 2 Pin Description

No.	Symbol	I/O	A/D	Description	Remarks
1	VDDHPL	Power	A	analog input	
2	VSSHPL	GND	A	VANA GND	
3	VDDMIO1	Power	D	VIF power supply	
4	INCK	I	D	digital input	Clock Input
5	VDDLSC1	Power	D	VDIG power supply	
6	VSSLSC1	GND	D	VDIG GND	
7	DMO3P	O	D	digital output	MIPI output (DATA+)
8	DMO3N	O	D	digital output	MIPI output (DATA-)
9	DMO1P	O	D	digital output	MIPI output (DATA+)
10	DMO1N	O	D	digital output	MIPI output (DATA-)
11	VDDLSC2	Power	D	VDIG power supply	
12	VDDLIF1	Power	D	VDIG power supply	
13	VSSLSC2	GND	D	VDIG GND	
14	DCKP	O	D	digital output	MIPI output (CLK+)
15	DCKN	O	D	digital output	MIPI output (CLK-)
16	VSSLSC3	GND	D	VDIG GND	
17	VDDLIF2	Power	D	VDIG power supply	
18	VDDLSC3	Power	D	VDIG power supply	
19	DMO2P	O	D	digital output	MIPI output (DATA+)
20	DMO2N	O	D	digital output	MIPI output (DATA–)
21	DMO4P	O	D	digital output	MIPI output (DATA+)
22	DMO4N	O	D	digital output	MIPI output (DATA-)
23	VSSLSC4	GND	D	VDIG GND	
24	VDDMIF	Power	D	VIF power supply	
25	VDDLCN1	Power	D	VDIG power supply	
26	VSSLCN1	GND	D	VDIG GND	
27	VDDSUB	Power	A	VANA power supply	
28	VDDLSC4	Power	D	VDIG power supply	
29	VSSLSC5	GND	D	VDIG GND	
30	VDDHCM1	Power	A	VANA power supply	
31	VSSHSN1	GND	A	VANA GND	
32	VDDHSN1	Power	A	VANA power supply	
33	VDDHSN2	Power	A	VANA power supply	
34	VSSHSN2	GND	A	VANA GND	
35	VDDHCM2	Power	A	VANA power supply	
36	VSSLSC6	GND	D	VDIG GND	
37	VDDMIO2	Power	D	VIF power supply	
38	TENABLE	I	D	digital input	NC(pull-down internal)
39	XVS	I/O	D	digital I/O	for dual sync(pull-up internal)
40	SWTCK	I	D	digital input	NC(pull-down internal)
41	SLASEL	I	D	digital input	I2C slave address select Pull down (pull-down internal)
42	VSSLCN2	GND	D	VDIG GND	
43	VDDLCN2	Power	D	VDIG power supply	
44	VDDLSC5	Power	D	VDIG power supply	
45	VSSLSC7	GND	D	VDIG GND	
46	VDDHSN3	Power	A	VANA power supply	
47	VSSHSN3	GND	A	VANAGND	
48	VDDHAN	Power	A	VANA power supply	

No.	Symbol	I/O	A/D	Description	Remarks
49	VSSHAN	GND	A	VANA GND	
50	TVMON	O	A	analog output	NC
51	VDDMIO3	Power	D	VIF power supply	
52	FSTROBE	O	D	digital output	Flash strobe
53	GPO	O	D	digital output	
54	SCL	I/O	D	digital I/O	I2C pin
55	SDA	I/O	D	digital I/O	I2C pin
56	POREN	I	D	digital input	NC(pull-up internal)
57	VSSLSC8	GND	D	VDIG GND	
58	VDDLSC6	Power	D	VDIG power supply	
59	XCLR	I	D	digital input	
60	VPI	Power	A	analog input	
61	VRL	Minus	A	analog input	
62	VRLRD	Minus	A	analog input	
63	VSSHSN4	GND	A	VANA GND	
64	VDDHSN4	Power	A	VANA power supply	

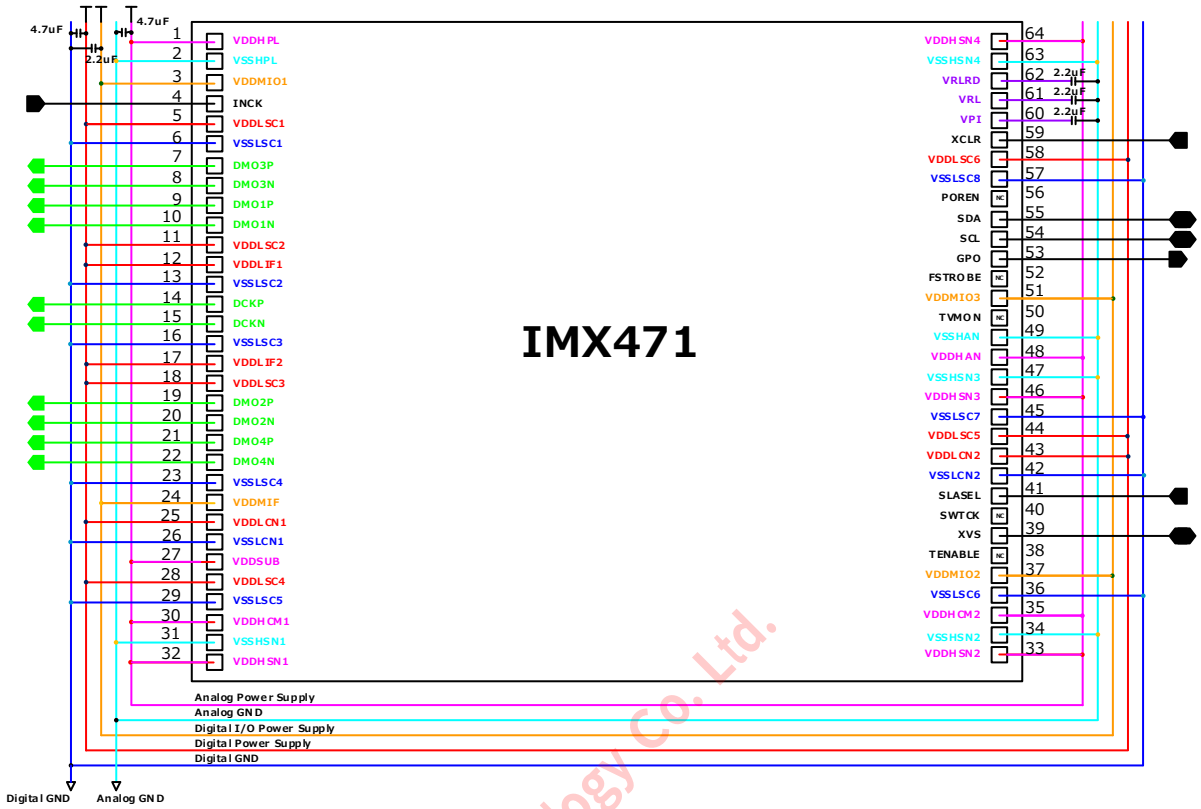
4. Input / Output Equivalent Circuit

Symbol	Equivalent Circuit	Symbol	Equivalent Circuit
INCK		XCLR SLASEL	
SCL SDA		XVS	
GPO FSTROBE		—	—

VIF : 1.8 V power supply

Figure 2 Input / Output Equivalent Circuit

5. Peripheral Circuit Diagram



Note: When fixing the potential of the chip back side, connect it to digital GND.

Note: The capacitor values and parts count used for decoupling of power supply lines in this diagram are determined only with Sony Semiconductor Solutions Corporation's testing environment. The capacitor values and/or parts count for power line decoupling may have to be reviewed and optimized by each manufacture depending on their design.

Figure 3 Peripheral Circuit (Recommended schematics)

6. Functional Description

6-1 System Outline

IMX471 is a CMOS active pixel type image sensor which adopts Sony's back-illuminated and stacked CMOS image sensor to achieve high sensitivity, low noise, and high speed image capturing. It is embedded with backside illuminated imaging pixel, low noise analog amplifier, column parallel A/D converters which enables high speed capturing, digital amplifier, image binning circuit, timing control circuit for imaging size and frame rate, CSI2 image data high speed serial interface, PLL oscillator, and serial communication interface to control these functions. Several additional image processing functions and peripheral circuits are also included for easy system optimization by the users.
A onetime programmable memory is embedded in the chip for storing the user data. It has 4 K-bit for user, 14 K-bit as a whole.

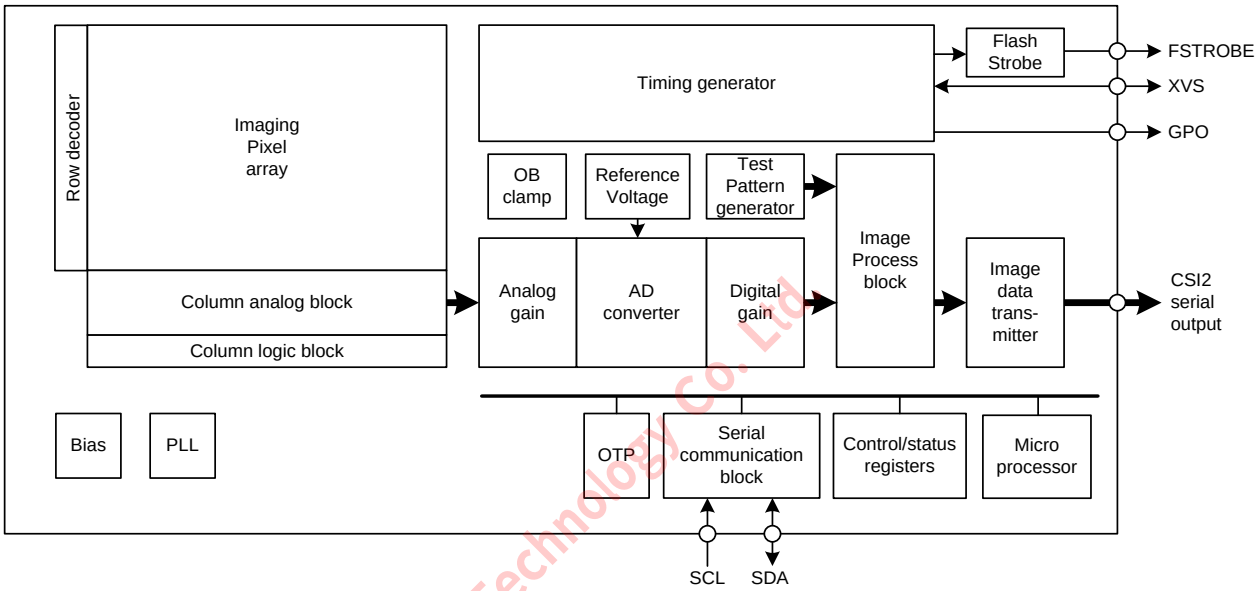


Figure 4 Overview of functional block diagram

6-2 Control register setting by the serial communication

The IMX471 can use the 2-wire serial communication method for sensor control. These specifications are described for sensor control using the 2-wire serial communication as follows. See Application Notes for more details of each function beyond the following description.

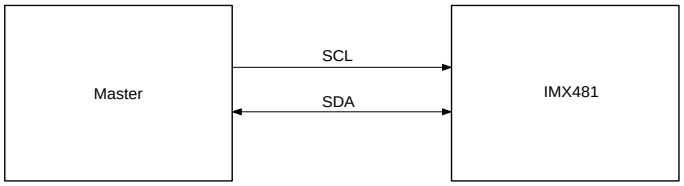


Figure 5 2-wire serial communication

6-2-1 2-wire Serial Communication Operation Specifications

The 2-wire serial communication method conforms to the Camera Control Instance (CCI). CCI is an I2C fast-mode compatible interface, and the data transfer protocol is I2C standard.
This 2-wire serial communication circuit can be used to access the control-registers and status-registers of IMX471.

Table 3 Description of 2-wire Serial Communication Pins

pin name	description
SDA	Serial data input/output pin
SCL	Serial clock input pin

The control registers and status registers of IMX471 are mapped on the 16-bit address space and the register categories shown as below. Detail register information is shown in Register Map.

Table 4 Specification of register address map for 2-wire serial communication

	address range	description
I^2C register	0x0000 - 0x0fff	Configuration register Read Only and Read/Write Dynamic register
	0x1000 - 0x1fff	Reserved
	0x2000 - 0x2fff	Reserved
	0x3000 - 0xffff	Manufacture specific register

6-2-2 Communication Protocol

2-wire serial communication supports a 16-bit register address and 8-bit data message type.

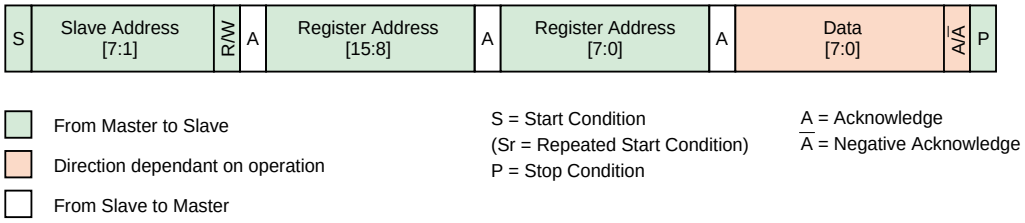
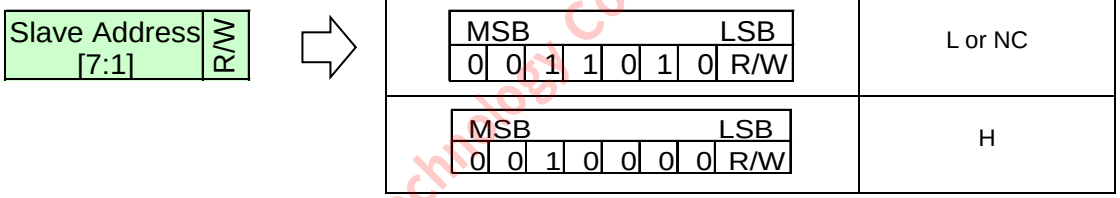


Figure 6 2-wire serial communication protocol

IMX471 has a default slave address shown as below.
The slave address is selectable by pin connection of SLASEL.
When called by the selected slave address, serial communication interface is activated.
Duplication of the address on the same bus must be prevented.
*For other slave address options, refer to Application Note.



R/W shows the direction of communication.

Figure 7 Slave address

Table 5 R/W bit

R/W bit	direction of communication
0	Write (Master → Sensor)
1	Read (Sensor → Master)

6-3 Clock generation and PLL

IMX471 equips embedded PLL to generate the necessary internal clocks and CSI2 transmission clocks. Set the related registers according to the operation condition. See Application Notes for more details of each function.

6-3-1 Clock System Diagram

IMX471 is equipped with two PLL, One outputs IVTCK for image processing, the other is IOPCK for MIPI output. Based on the clock that is input in the range of 6-27MHz, output of 338-1740MHz can be of the PLL for IVTCK, PLL of IOPCK for is capable of outputting 338-1840MHz.

Typically, IMX471 can be driven from the dual PLL mode to operate the both of PLLs, but it also supports single PLL mode to move only one side of the PLL.

In PLL single mode, IOP_PREPLLCK_DIV and IOP_PLL_MPY are ignored..

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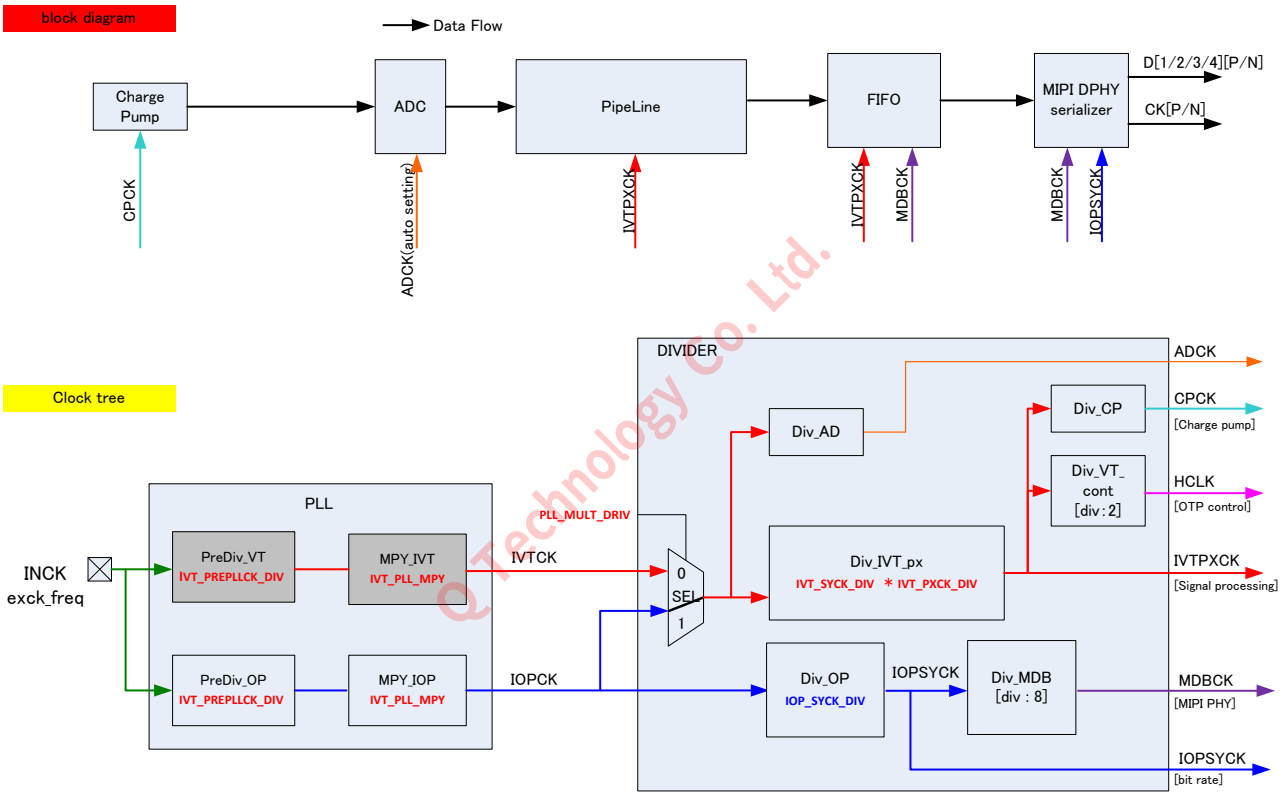

Figure 8 Clock System Diagram (PLL single mode)

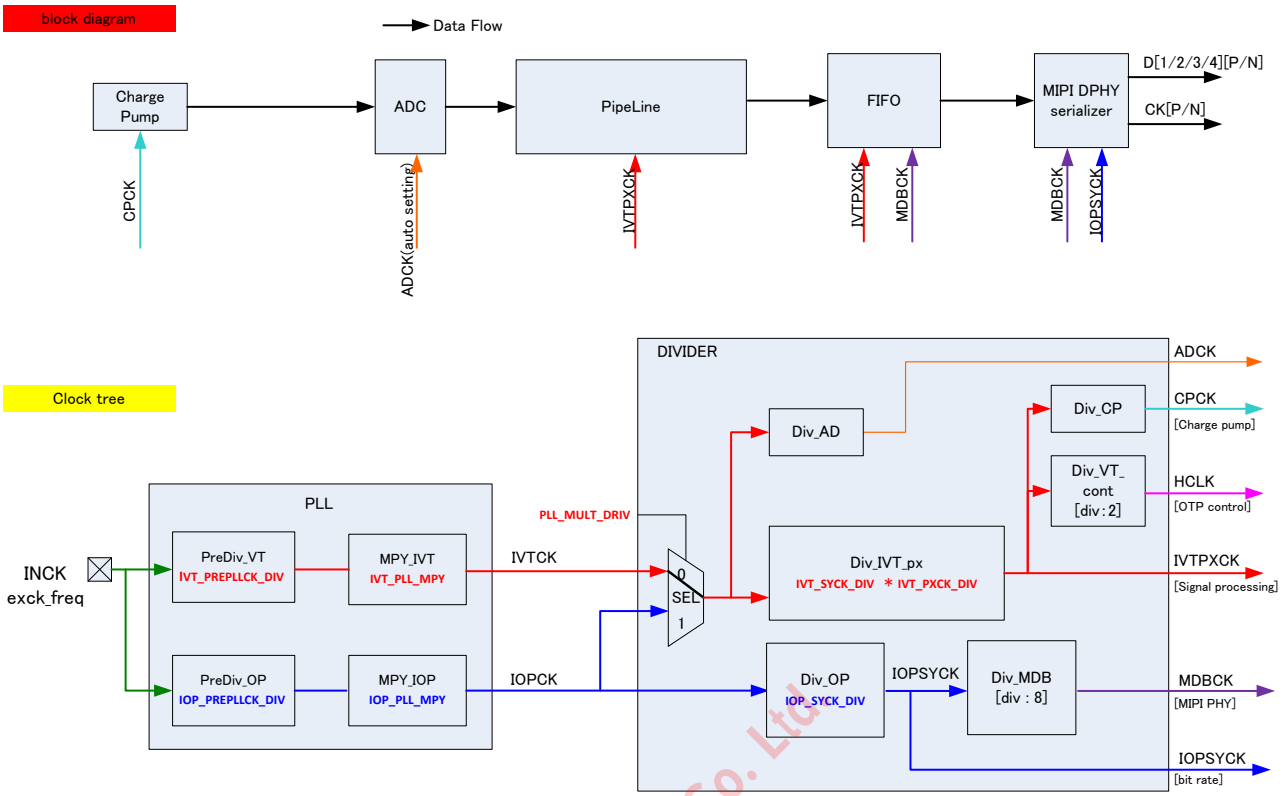

Figure 9 Clock System Diagram (PLL dual mode)

6-4 Description of operation clocks

The followings are general descriptions for each clock. See Application Note for more detail.

6-4-1 INCK

INCK is an external input clock (6 to 27MHz). See “AC characteristics” for electrical requirements to INCK.

6-4-2 IVTCK, IOPCK(PLL output)

These clocks are the root of all the operation clocks in IMX471 and it designates the data rate.
DCKP/DCKN; CSI2 interface clock is generated from IOPCK by dividing into 1/2 frequency since the interface is operated in double data rate format.

6-4-3 IVTPXCK Clock

The clock for internal image processing is used as the base of integration time, frame rate, and etc.

6-4-4 IOPSYCK Clock

The clock for internal image processing is designating the pixel rate and etc.

6-5 Image Readout Operation

By setting the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, binning, shutter mode, integration time, gain, and output format via 2-wire serial communication, IMX471 outputs the image data.

See Application Notes for more details of each function.

6-5-1 Physical alignment of imaging pixel array

The figure below shows the physical alignment of the imaging pixel array with pin #1 located at the upper left corner.

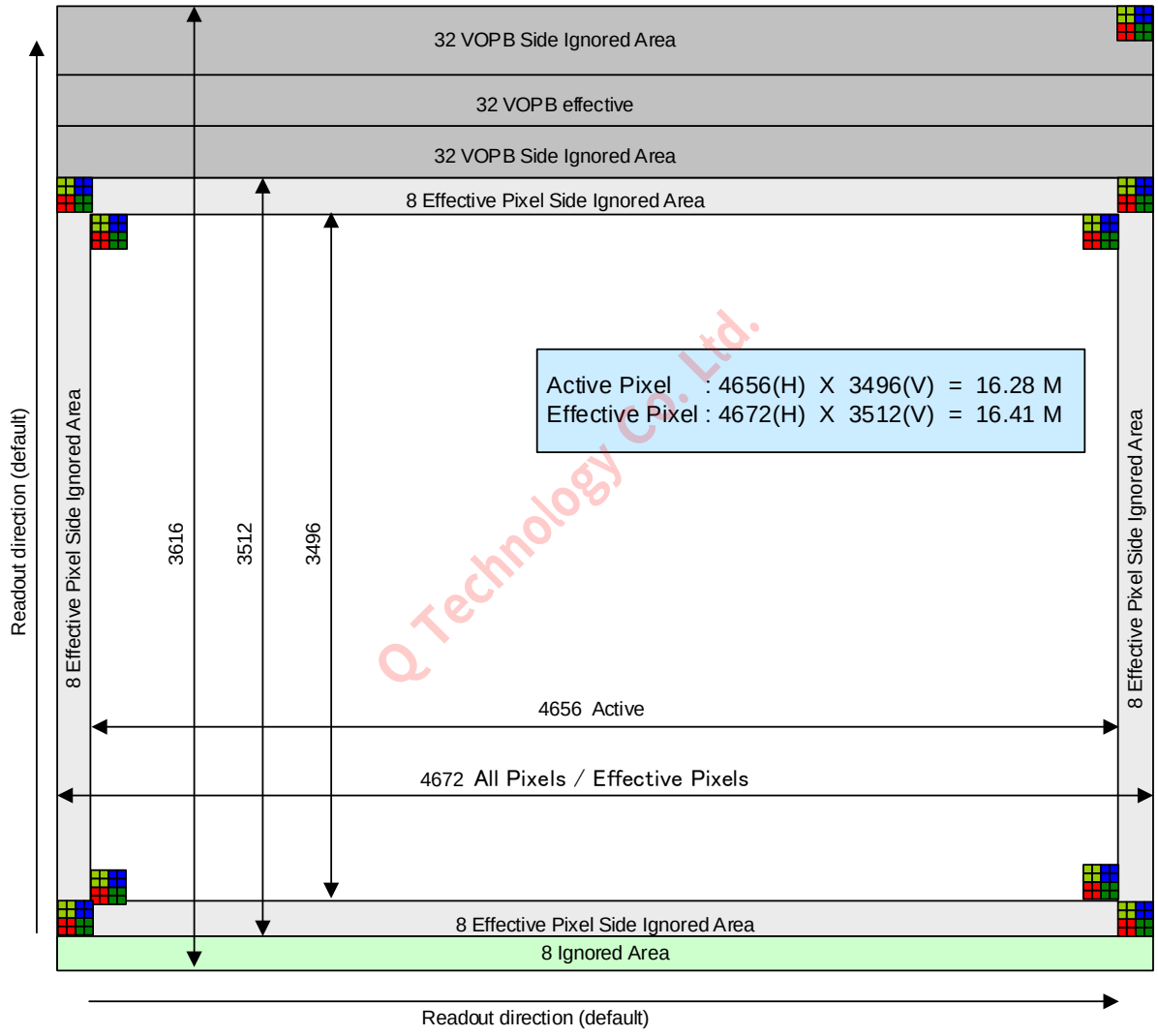

Figure 10 physical alignment of the imaging pixel array

6-5-2 Color coding and order of reading image date

The original color filter arrangement of the sensor is shown in the figure below. Gr and Gb are the G signals shown at the same line as R signals and B signals respectively. The line with R & Gr signals and the line with Gb & B signals are output alternating one after the other.

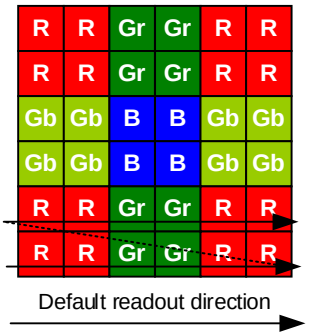

Figure 11 Color coding alignment

6-6 Output Image Format

This is the output image diagram of full pixel output mode, Image data is output from the upper left corner of the diagram.

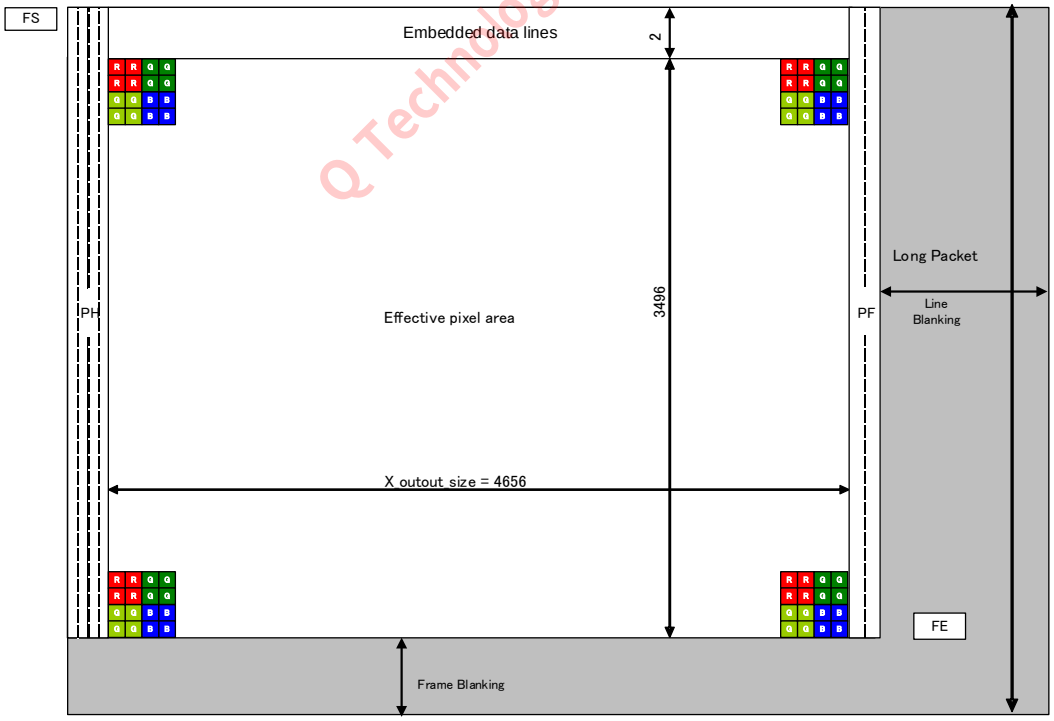

Figure 12 Full pixel output mode image data structure

6-6-1 Embedded Data Line control

It is possible to output certain 2-wire serial register contents on the 2 lines just after the FS sync code of the frame. The corresponding registers are indicated by “EDL” column of the Register Map.
An unfixed value is output when not outputting embedded data.

See Application Notes for contents and output sequence of Embedded Data Lines.

6-6-2 Image size of mode

IMX471 can capture and output full size, cropped/scaled image in combination with the normal mode. Examples are shown in the table below. Definitions of each parameter are shown in the below figure.

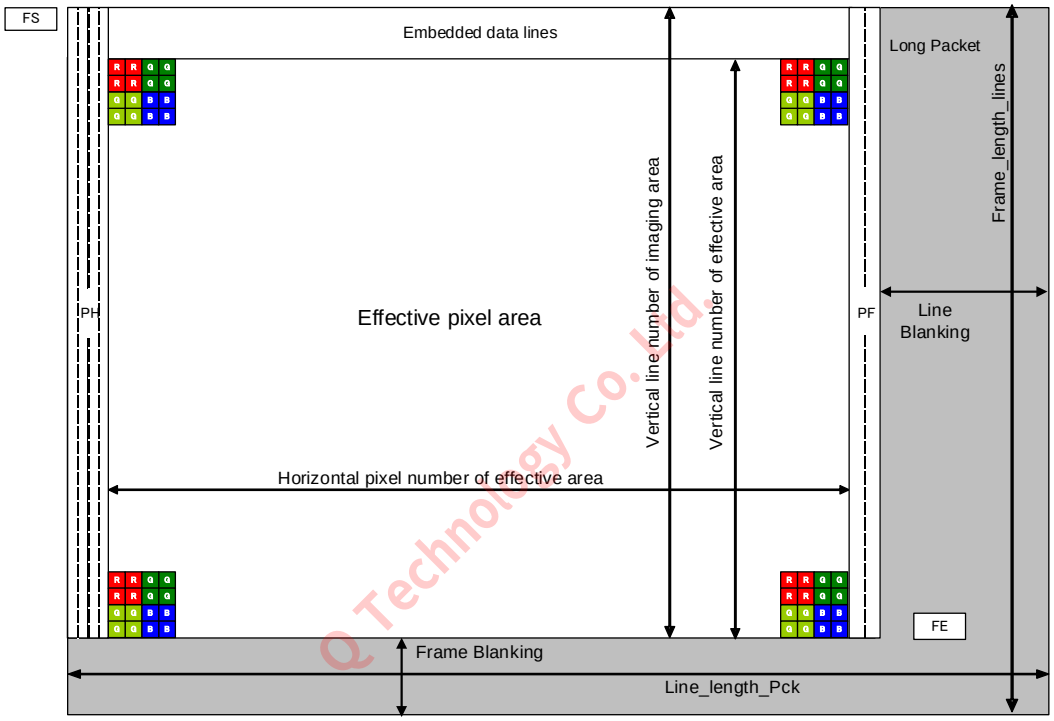

Figure 13 Image size parameter definition

Table 6 modes and image sizes

	Modes		
	Full size @30fps	2x2 Adjacent Pixel Binning @120fps	2x2 Adjacent Pixel Binning @150fps
VT/OP	1.0 :1.0	1.0 :1.0	1.0 :1.0
Cropping	Non(4:3)	Non(4:3)	Vcrop(16:9)
Sub-sampling	Non	Non	Non
Binning	Non	H/V	H/V
Scaling	Non	Non	Non
H Pixels	4656	2328	2328
V Pixels	3496	1748	1304
Frame Rate	30fps	120fps	150fps
FOV			
Output			

6-6-3 Available operation mode

IMX471 has two modes that All-pixel and binning (H&V:1/2).

6-6-4 Image area control capabilities

As control function for image's viewing area and /or image size, IMX471 has capability of analog crop, digital crop, scaling and output crop. The relation of image output size and the resister is shown below.

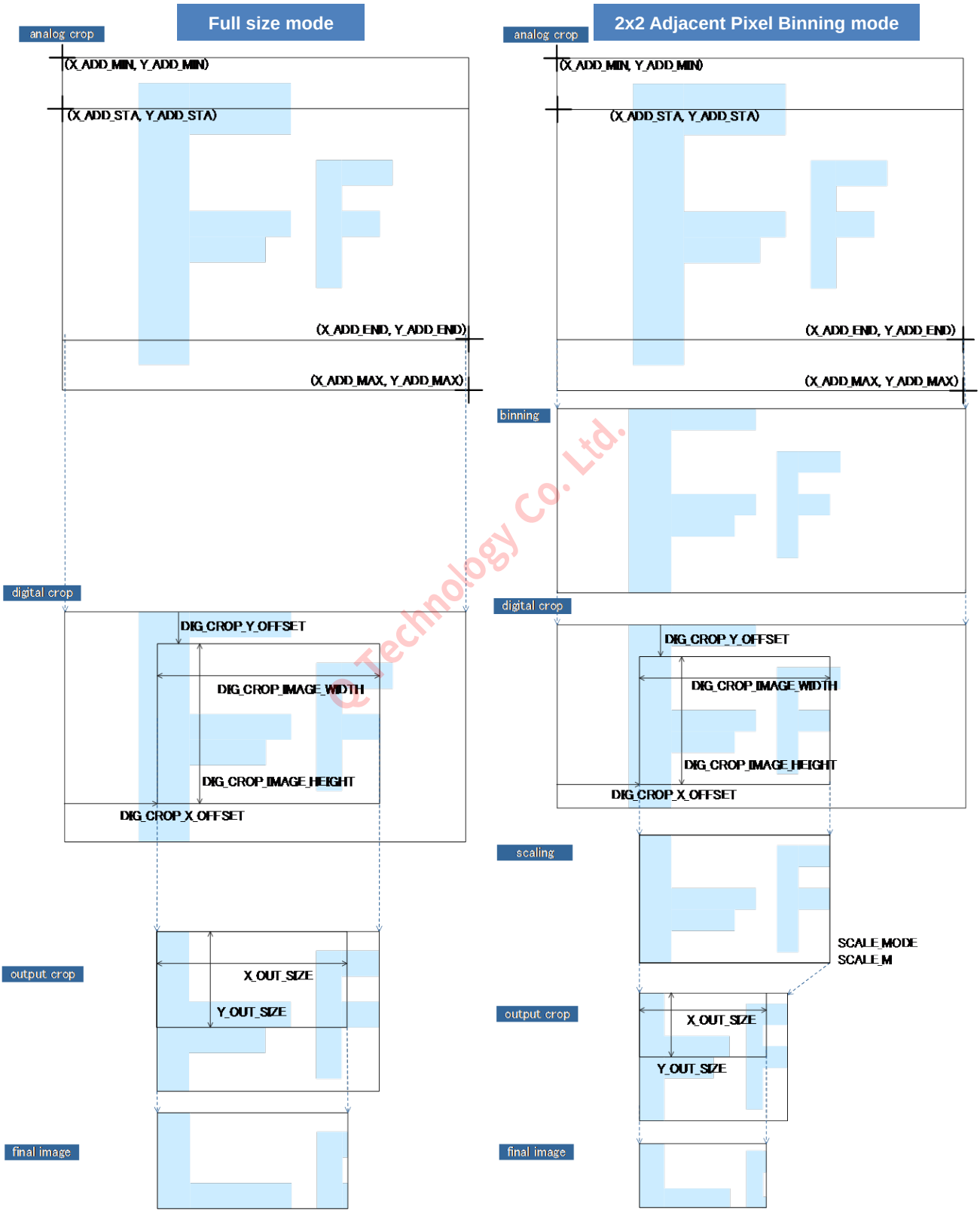

Figure 14 image area control capabilities

Readout Start Position

Default readout position of IMX471 starts from the lower left when PIN1 is placed at the upper left corner. Because the lens will invert the image both vertically and horizontally, the proper image can be archived when PIN1 is placed at the upper left corner.

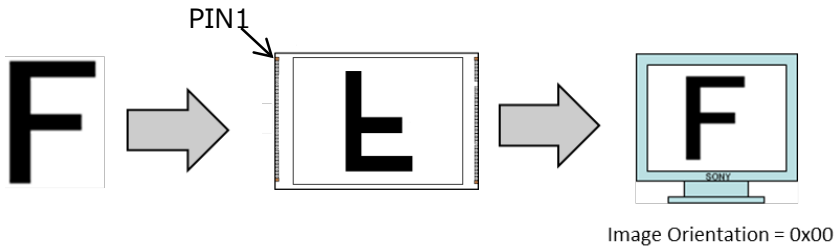

Figure 15 Readout start position

Vertical flip and horizontal mirror readout modes can be specified by the register below. And when readout start and end positions are matching the readout size, the same area is displayed when flipping/mirroring the image.

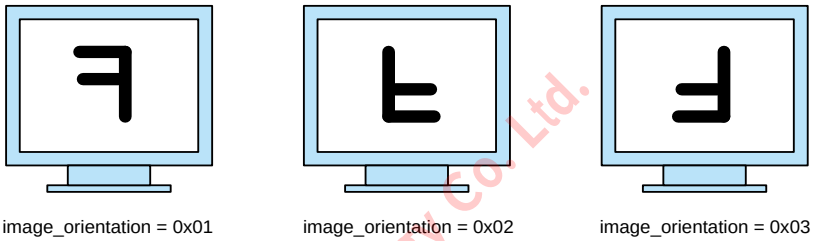

Figure 16 Read out image for each combination of flip and mirror

6-7 Gain setting

IMX471 can apply analog gain on photo-electron signal and digital gain on digital signal after ADC. Range of settable range is as follows.

Table 7 Range of Gains

Function	Max.	Note
Analog Gain	24 dB	-
Digital Gain	24 dB	Functionally Settable

6-8 Image compensation function

In IMX471 defect pixel correction is available. Use-case may be chosen in terms of trade-off for power consumption and image quality for example.

See Application Notes for more details of each function.

6-8-1 Defect Pixel Correction

The defect correction function includes static defect correction and dynamic defect correction. Note that this function is available only on 2x2 Adjacent Pixel Binning mode.

The static defect correction is to correct the defective pixels according to address data stored in OTP. There is only area for Sony Semiconductor Solutions Corporation's factory area.
The dynamic defect correction eliminates any critical defects detected on RGB array by estimating from surrounding adjacent pixels value.

6-8-2 Lens Shading Correction (LSC)

Lens Shading Correction (LSC) is a function to correct the shading by lens distortion. Note that this function is available only on 2x2 Adjacent Pixel Binning mode.

6-9 Miscellaneous functions

IMX471 has the following additional functions to be used for various final products' features.
See Application Notes for more details of each function.

6-9-1 Thermal Meter

This function is to measure the thermal data from internal sensor then average it. Measurement results could be read via I2C or EBD data.

6-9-2 Test pattern output

IMX471 can output the following test pattern by build-in pattern generator.
Test patterns of Solid Color, 100% Color Bar, Fade to Gray Color Bar, PN9 are available.
For Solid Color mode, each value of R, Gr, Gb and B is adjustable.

6-9-3 Long Exposure Setting

IMX471 can achieve a very long exposure time (up to 128 times of 1 vertical period) by simply expanding the vertical blanking time setting.

6-9-4 OTP (One Time Programmable Read Only Memory)

Total of 4 K bit of OTP is available for users.
It is divided into 8 pages and 192 byte of them are usable at user's discretion while other 320 byte are assigned as the area for the particular purpose like lens shading correction, model ID, etc., and partially write protected.
See OTP manual for details.

6-9-5 Dual sensor synchronization operation

IMX471 supports synchronized shooting operation of two image sensors by implementing both slave and master mode for each sensor. To enable this feature, master/slave must be set for each sensor by software control method. XVS is dedicated output for the synchronization.

6-9-6 Flash light control sequence

IMX471 can internally generate the control pulse assuming to trigger the flash light emission and output from the external pins.
See Software Reference Manual for details.

6-9-7 Monitor terminal settings

IMX471 can output 3 internal signals (H Sync/V Sync/OIS pulse) via monitor terminals.
The monitor terminals mean the following two (2) terminals, such as XVS(39 pin) and GPO(53 pin).
See Software Reference Manual for details.

6-10 Image signal interface

6-10-1 MIPI transmitter

IMX471 outputs image signal by CSI2 high speed serial interface consisted of one pair of clock line and four pairs of data line. See MIPI Alliance Standard for Camera Serial Interface2 (CSI-2) version 1.2 and MIPI Alliance Specification for D-PHY version 1.2 for details.

Because signal is transmitted by differential pair, impedance (generally 100 Ω) between differential pair near the receiver side during HS mode is required. Otherwise, select receiver with build-in impedance between differential pair. Different delay time of differential pairs may reduce the input timing margin of ISP device, which leads to malfunction. Therefore, delay time within and among differential pairs must be as similar as possible in layout.

7. How to operate IMX471

7-1 Power on Reset

IMX471 does not have the built in “Power On Reset” function.
The XCLR pin is set to “LOW” and the power supplies are brought up. Then the XCLR pin should be set to “High” after INCK supplied.

7-2 Power on sequence

7-2-1 Power on slew rate

Maximum slew rate (mV/us) is specified for each power supply to avoid oscillation during power on.

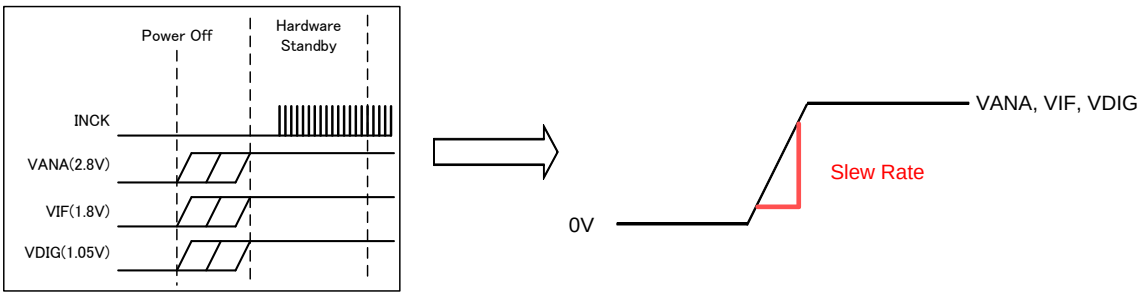

Figure 17 Power on slew rate

Table 8 Limitation on power-on slew rate

Power Supplies	Slew Rate			Comment
	Min	Max	Unit	
VANA, VIF, VDIG	-	50	mV/µs	

7-2-2 Startup sequence with 2-wire serial communication

Follow the power supply start up sequence as below.

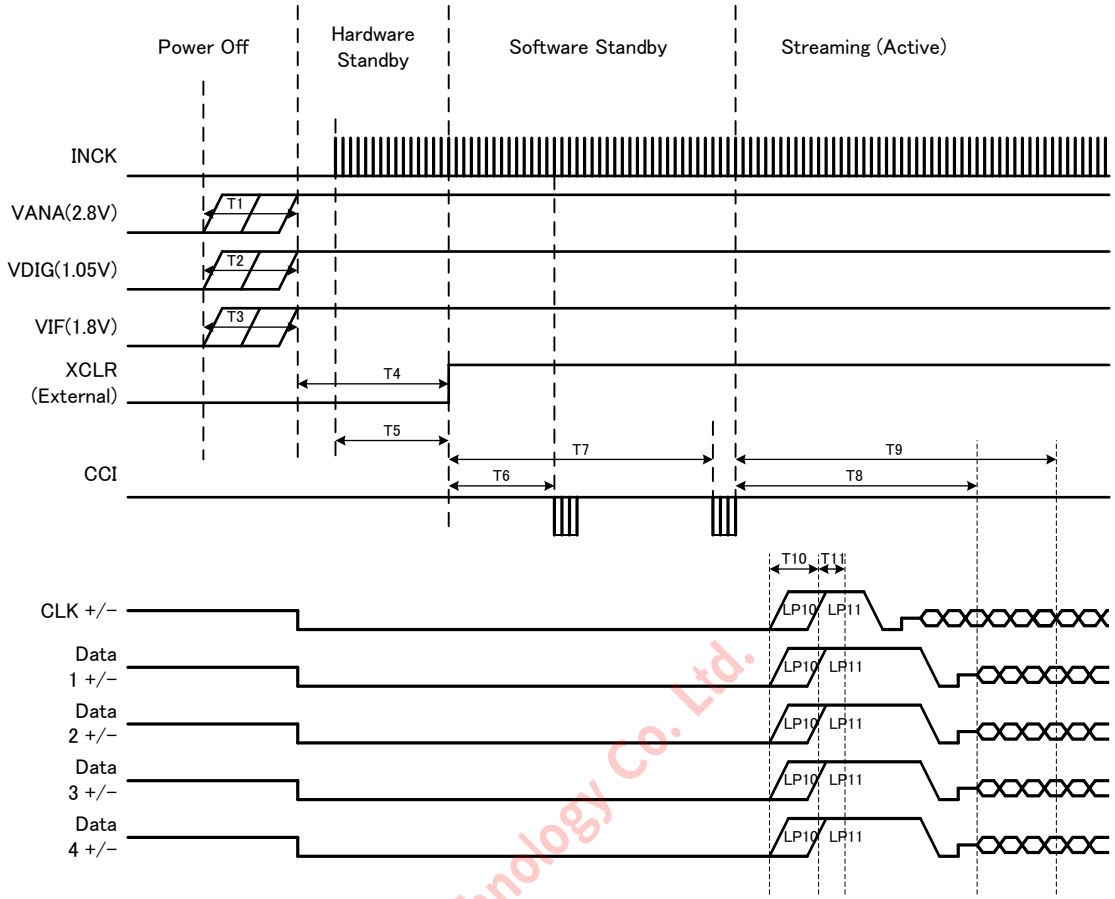

Figure 18 Startup sequence with 2-wire serial communication

* Presence of INCK during Power Off is acceptable despite of above chart.

Table 9 Startup sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA on	T1	VANA, VDIG and VIF may rise in any order.		µs	Slew rate of VANA, VDIG and VIF(0%-100%) :Refer to Table.8
VDIG rising – VDIG on	T2			µs	
VIF rising – VIF on	T3			µs	
VANA, VDIG and VIF rising – XCLR rising	T4	0		µs	Later of T1, T2 and T3
INCK start - XCLR rising	T5	0		ms	
XCLR rising till CCI Read Version ID register wait time	T6	0.6		ms	
XCLR rising till Send Streaming Command wait time (To complete reading all parameters from OTP)	T7	8		ms	
Start of first frame after power-on sequence.	T8		4.0 ms + The delay of the coarse integration time value + 13H		
Start of first streaming with valid frame after power-on sequence.	T9		T8 + 1Frame	ms	
DPHY power up	T10	1		ms	
DPHY init	T11	100		µs	

Note) XCLR needs to be Low until all power supplies complete power-on

7-3 Power down sequence

7-3-1 Power down sequence with 2-wire serial communication

Follow the power down sequence below.

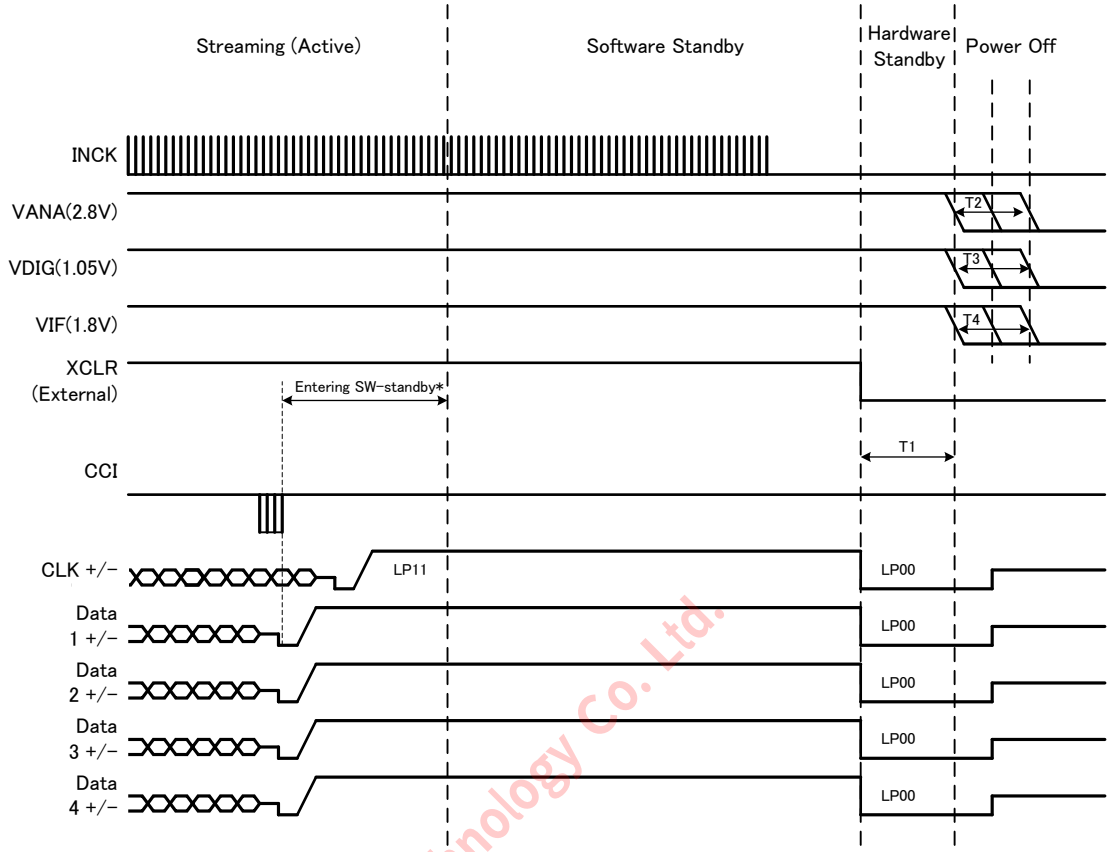

Figure 19 Power down sequence with 2-wire serial communication

Table 10 Power down sequence timing constraints (2-wire serial communication mode with external reset)

Item	Label	Min.	Max.	Unit	Comment
XCLR Neg-edge – VANA (VDIG or VIF) fall	T1	0		µs	Presence of INCK during Power Off is acceptable.
Sequence free of VANA falling and VDIG falling and VIF falling	T2,T3,T4	VANA, VDIG and VIF may fall in any order.		µs	

7-4 Register Map

See Register Map.

8. Electrical Characteristics

The Electrical Characteristics of the IMX471 is shown below

8-1 DC characteristics

Table 11 DC Characteristics

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VDDSUB VDDHSN1,2,3,4 VDDHAN VDDHCM1,2 VDDHPL	VANA		2.7	2.8	3.0	V
	VDDLCN1,2 VDDLSC1,2,3,4,5,6 VDDLIF1,2	VDIG		0.95	1.05	1.15	V
	VDDMIO1,2,3 VDDMIF	VIF		1.7	1.8	1.9	V
Digital input voltage	SDA, SCL	VIH		0.7VIF		2.9	V
		VIL		-0.3		0.3VIF	V
Digital input voltage	XCLR, INCK, SLASEL, XVS	VIH		0.65VIF		VIF+0.3	V
		VIL		-0.3		0.35VIF	V
Digital output voltage	SDA	VOH		VIF-0.2		-	V
		VOL		-		0.2VIF	V
	GPO, FSTROBE,XVS	VOH		VIF-0.2		-	V
		VOL		-		0.2	V

8-2 AC Characteristics

8-2-1 Master Clock Waveform Diagram

8-2-1-1 INCK Square Waveform Input Specifications

Input specifications are shown below when square-wave signal is input directly into the external pin INCK.

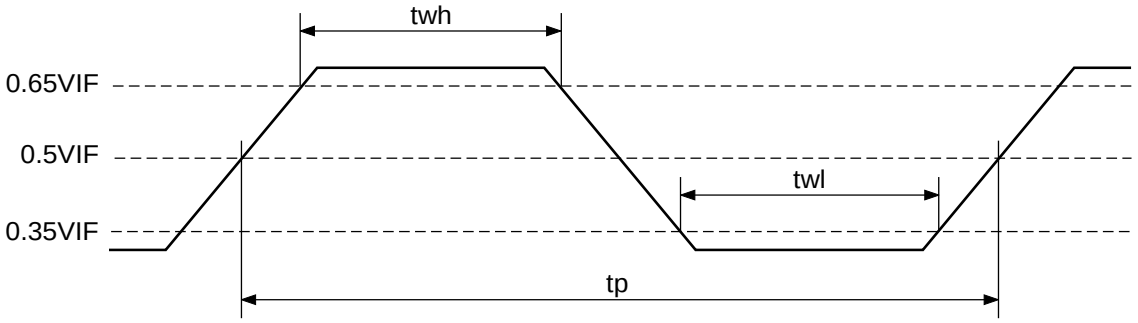

Figure 20 Master Clock Square Waveform Input Diagram

Table 12 Master Clock Square Waveform Input Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
INCK clock frequency	f_{SCK}	6		27	MHz
INCK clock period	t_p	37.0		166.7	ns
INCK low level width	t_{wl}	0.4tp		0.6tp	ns
INCK high level width	t_{wh}	0.4tp		0.6tp	ns
INCK jitter	Tjitter			600	ps

8-2-1-2 INCK Sine Waveform Input Specifications

IMX471 does not support the “AC coupled connection”.
Therefore, there is no description of AC characteristics

8-2-2 PLL block characteristics

Electrical characteristics of PLL block is shown below.

Table 13 PLL block characteristics (VT system)

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6.0		27.0	MHz	
Input frequency range of phase comparator	6.0		12.0	MHz	
VCO frequency range	338		1740	MHz	
Output frequency range	338		1740	MHz	
Settling time			1000	μs	

Table 14 PLL block characteristics (OP system)

Item	Min.	Typ.	Max.	Unit	Note
Input frequency range	6.0		27.0	MHz	
Input frequency range of phase comparator	1.0		12.0	MHz	
VCO frequency range	338		1840	MHz	
Output frequency range	338		1840	MHz	
Settling time			1000	μs	

8-2-3 Definition of settling time of PLL block

After start operation, the oscillation frequency of PLL output transits from 0 Hz to target frequency then gradually become stable. The duration for oscillation frequency becomes within 5 % of the target frequency is defined as “settling time”.

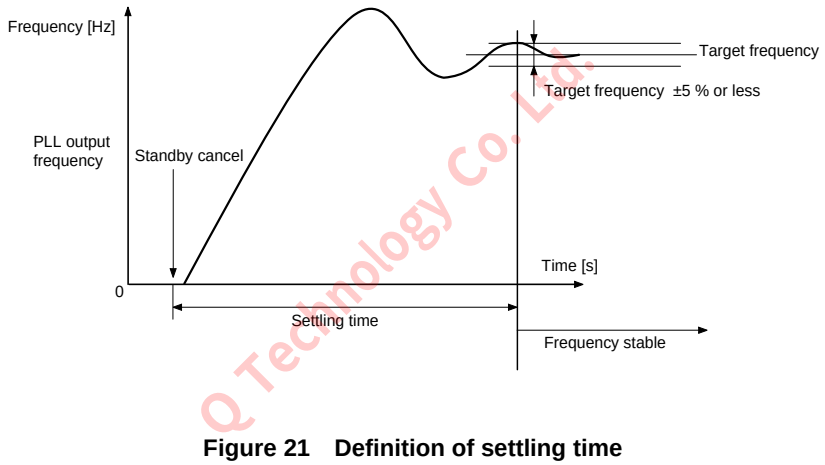

Figure 21 Definition of settling time

8-2-4 2-wire serial communication block characteristics

2-wire serial communication characteristics are shown below.

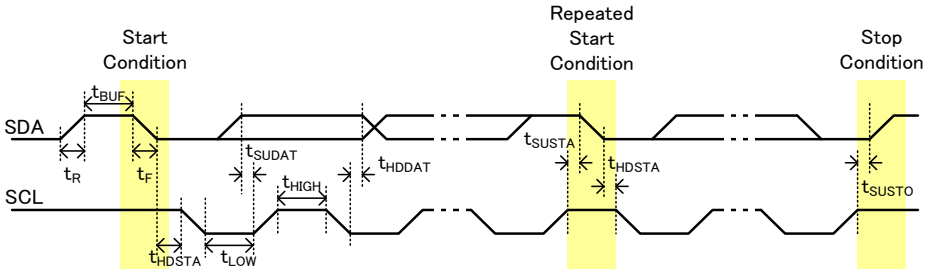

Figure 22 2-wire serial communication block specification

Table 15 2-wire serial communication block specification

Parameter	Symbol	Conditions	Min.	Max. (Fast-mode Plus)	Unit
Low level input voltage	V_{IL}		-0.5	$0.3V_{IF}$	V
High level input voltage	V_{IH}		$0.7V_{IF}$	2.9	V
Low level output voltage	V_{OL1}	VIF > 2 V, Sink 3 mA	0	0.4	V
	V_{OL2}	VIF < 2 V, Sink 3 mA	0	$0.2V_{IF}$	V
Output fall time	t_{of}	Load 10 pF – 400 pF, 0.7 VIF→0.3 VIF		250 (120)	ns
Input current	I_I	0.1 VIF→0.9 VIF	-10	10	µA
SDA I/O capacitance	$C_{I/O}$			10	pF
SCL Input capacitance	C_I			10	pF

Table 16 2-wire serial communication block AC specification

Fast-mode

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Rise time (SDA and SCL)	t_R	-	300	ns
Fall time (SDA and SCL)	t_F	-	300	ns
Hold time (start condition)	t_{HDSTA}	0.6	-	µs
Setup time (rep.-start condition)	t_{SUSTA}	0.6	-	µs
Setup time (stop condition)	t_{SUSTO}	0.6	-	µs
Data setup time	t_{SUDAT}	100	-	ns
Data hold time	t_{HDDAT}	0	0.9	µs
Bus free time between Stop and Start condition	t_{BUF}	1.3		µs
Low period of the SCL clock	t_{LOW}	1.3		µs
High period of the SCL clock	t_{HIGH}	0.6		µs

Fast-mode Plus (Note: Only available with INCK ≥ 13 MHz; See module design reference manual for detail.)

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	1000	kHz
Rise time (SDA and SCL)	t_R	-	120	ns
Fall time (SDA and SCL)	t_F	-	120	ns
Hold time (start condition)	t_{HDSTA}	0.26	-	µs
Setup time (rep.-start condition)	t_{SUSTA}	0.26	-	µs
Setup time (stop condition)	t_{SUSTO}	0.26	-	µs
Data setup time	t_{SUDAT}	50	-	ns
Data hold time	t_{HDDAT}	0	-	µs
Bus free time between Stop and Start condition	t_{BUF}	0.5		µs
Low period of the SCL clock	t_{LOW}	0.5		µs
High period of the SCL clock	t_{HIGH}	0.26		µs

Note) Fast-mode Plus supports only available with INCK ≥ 13MHz
See module design reference manual for detail.

8-2-5 Current consumption and standby current

Table 17 Current consumption and standby current

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Current consumption (analog)	I_{ANA}		40.9	46.0	mA	
Current consumption (digital)	I_{DIG}		162.0	256.7	mA	
Current consumption (IF)	I_{IF}		2.3	2.8	mA	
Standby current (analog)	I_{STBANA}			17.3	µA	XCLR : Low fixed INCK :stop SLASEL:NC or Low fixed XVS:NC or High fixed
Standby current (digital)	I_{STBDIG}			27.2	µA	XCLR : Low fixed INCK :stop SLASEL:NC or Low fixed XVS: NC or High fixed
Standby current (IF)	I_{STBIF}			1.8	µA	XCLR : Low fixed INCK :stop SLASEL:NC or Low fixed XVS: NC or High fixed

Note1: Full size @ 30 frame/s, V_{ANA} = 2.8V, V_{DIG} = 1.05 V, V_{IF} = 1.8 V, Ta = 25 ˚C, Process corner of transistors: TT*
Note2: Full size @ 30 frame/s, V_{ANA} = 3.0V, V_{DIG} = 1.15 V, V_{IF} = 1.9 V, Ta = 60 ˚C, Process corner of transistors: FF*
(Remarks, * TT: T stands for Typical, FF: F stands for Fast)

9. Spectral Sensitivity Characteristics

(Includes neither lens characteristics nor light source characteristics.)

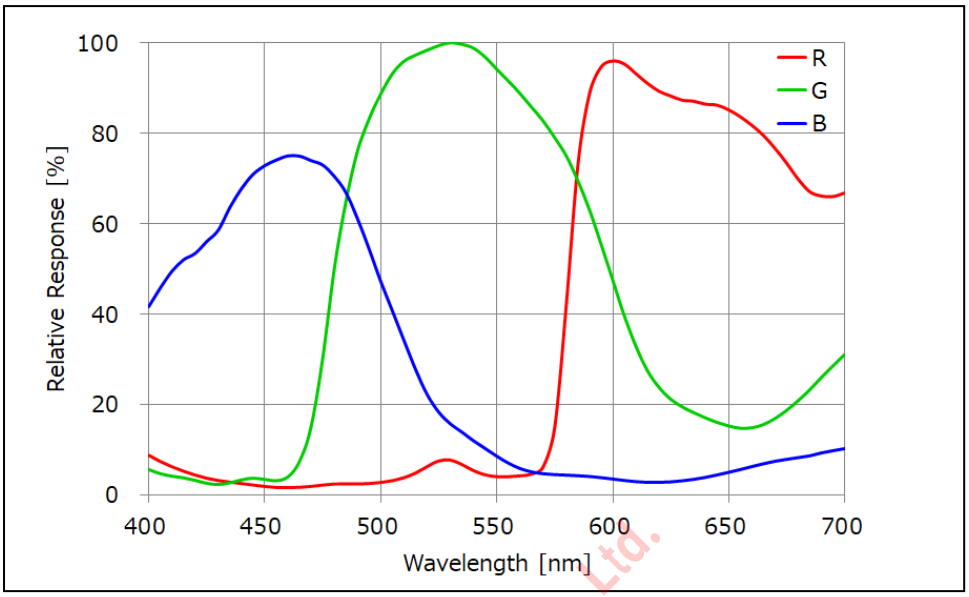

Figure 23 Spectral sensitivity characteristics

10. Image Sensor Characteristics

10-1 Image Sensor Characteristics

Table 18 Image Sensor Characteristics

(Full size @ 30 frame/s, V_{ANA} = 2.8V, V_{DIG} = 1.05 V, V_{IF} = 1.8 V, Tj = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Range	Measurement method	Remarks
Sensitivity	S	157			LSB	Center	1(*1)	
Sensitivity ratio	RG	0.43	0.49	0.55		Center	2(*1)	
	BG	0.33	0.39	0.45				
Saturation signal	Vsat	1023			LSB	Zone1	3(*1)	Include OB level (*2)
Video signal shading	SH			88	%	Zone2D	4(*1)	Design assurance
Dark signal	Vdt			0.5	LSB	Zone2D	5(*1)	When operation at 15 frame/s

The data described at this image sensor characteristics are the measurement standard without base gain setting, and indicates the results evaluated with OB as a reference.

Note 1) These refer to the descriptions of the Measurement Methods on Chapter 11.

Note 2) LSB is the abbreviation of Least Significant Bit. 10 bits = 1023 digital is the maximum output code for the output unit. The gain setting (base gain setting) in which the saturation signal output matches with 1023 LSB requires 0[dB] when the OB level is 64 LSB (standard recommended value).

10-2 Zone Definition used for specifying image sensor characteristics

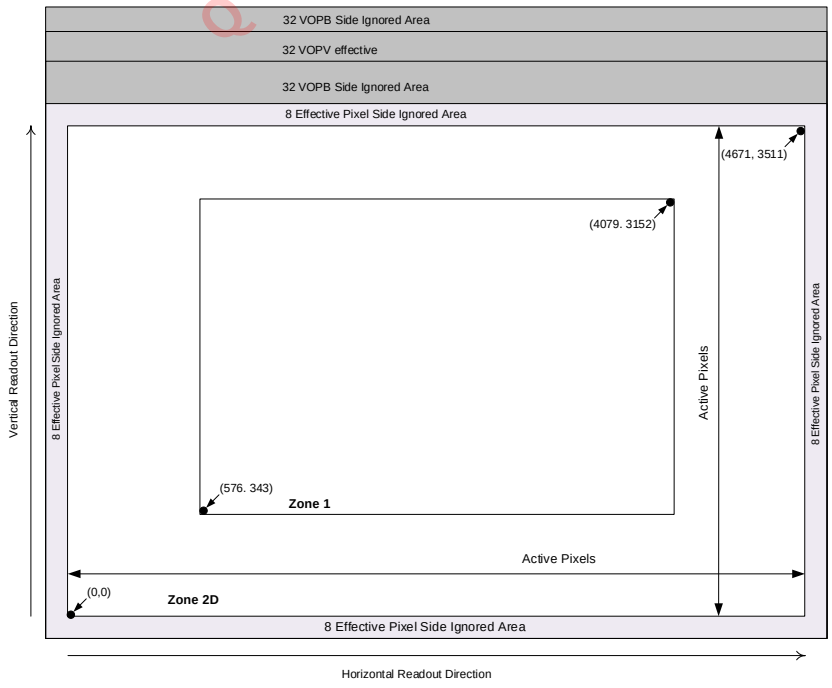

Figure 24 Zone Definition Diagram

11. Measurement Method for Image Sensor Characteristics

11-1 Measurement conditions

The device operation conditions are at the typical values of the bias and clock voltage.

Table 19 Measurement Conditions

Supply voltage	VANA 2.8 V, VDIG 1.05 V, VIF 1.8 V
Clock	INCK 18 MHz

In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr, Gb, R and B digital signal outputs of the measurement system.

11-2 Pixel position of This Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively. The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.

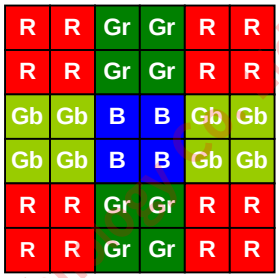

Figure 25 Coding alignment

11-3 Definition of Standard Imaging Conditions

11-3-1 Standard imaging condition I

Use a pattern box (luminance: 706 cd/m2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F2.8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

11-3-2 Standard imaging condition II

A testing lens with CM500S (t = 1.0 mm) is used as an IR cut filter for light source with 3200 K color temperature. The luminous intensity to the sensor receiving surface is adjusted to the luminous intensity level shown in each measurement item by the light source output, lens aperture or storage time control by the electronic shutter.

11-4 Measurement method

11-4-1 Sensitivity

Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/300 s, measure the Gr and Gb signal outputs (VGr,VGb) at the center of imaging area, and substitute the values into the following formula.

S = {((VGr + VGb)/2) × (300/120)} [LSB]

11-4-2 Sensitivity ratio

Set the measurement condition to the standard imaging condition II. After adjusting so that the average value of the Gr and Gb signal output is 341 [LSB], measure the R signal output (VR [LSB]), the Gr and Gb signal outputs (VGr, VGb [LSB]) and the B signal output (VB [LSB]) at the imaging area Center in frame readout mode, and substitute the values into the following formulas.

VG = (VGr + VGb) /2

RG = VR/VG

RB = VB/VG

11-4-3 Saturation signal

Set the measurement condition to the standard imaging condition II. After adjusting the luminous Intensity to 20 times the intensity with the average value of the Gr,Gb signal outputs, 341 [LSB], measure the average value of the Gr,Gb,R and B signal outputs.

11-4-4 Video signal shading

Set the measurement condition to the standard imaging condition II. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 341 [LSB]. Then measure the maximum value (Gmax [LSB]) and minimum value (Gmin [LSB]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

SH = ((Gmax – Gmin) /Gmax) × 100 [%]

11-4-5 Dark signal

Measure the output difference between 1/15 [s] signal output (Va) and 1/15000 or less [s] signal output (Vb) at the device ambient temperature of 60 ˚C and the device in the light-obstructed state, and calculate the signal output at 1/15 [s] storage by them using the following approximate formula. Then, this is Vdt [LSB].

Vdt = (Va – Vb) × (1/15) / (1/15) – (1/15000) ≈ (Va –Vb) [LSB]

12. Spot Pixel Specification

Table 20 Spot Pixel Specifications

(Full Size@30 frame/s, V_{ANA} = 2.8V, V_{DIG} = 1.05 V, V_{IF} = 1.8 V, Tj = 60 ˚C)

Type of distortion	Level Note 1)	Maximum distorted pixels in each zone		Measurement method	Remarks
		Zone2D	Other		
Black or white pixels at high light	30 % ≤ D	80	No evaluation criteria applied	12-3-1	
White pixels in the dark	28 (LSB) ≤ D	1200	No evaluation criteria applied	12-3-2	1/30 storage Note 2)

Note) 1. D...Spot pixel level.
2. Continuous same color pixels in the horizontal or vertical direction are NG.
3. Defect pixels are measured with all optional image processing features (DPC, HDR, LSC) disabled.
4. The maximum quantity pixel counts of 80 for Bright Pixels and 1200 for Dark Pixels are total of R + Gr + Gb + B individual pixels from any color channels.
5. The analog gain for both the Illuminated and Dark defect conditions is 0dB.
6. The above chart (hereinafter referred to as the “Spot Pixel Specifications”) is the standard only for sorting image sensor products in this specification book (hereinafter referred to as the “PRODUCTS”) before shipment from a manufacturing factory. Sony Semiconductor Solutions Corporation and its distributors (collectively hereinafter referred to as the “Seller”) disclaim and will not assume any liability even if actual number of distorted pixels of the PRODUCTS delivered to you exceeds the maximum number set forth in the Spot Pixel Specifications. You are solely liable for any claim, damage or liability arising from or in connection with such distorted pixels. If the Seller separately has its own product warranty program for the PRODUCTS (the “Program”), the conditions in this specification book shall prevail over the Program and the Seller shall not assume any liability under the Program to the extent there is contradiction.

12-1 Notice on White Pixels Specifications

After shipment inspection of CMOS image sensors, pixels of CMOS image sensors may be distorted and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels.")
Particle radiation such as cosmic rays etc. is one of the causes of White Pixels.
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such distorted pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against White Pixels, such as adoption of automatic compensation systems for White Pixels and establishment of quality assurance standards.
White Pixels may be also caused by alpha radiation, which will be emitted in a process of decay of radioactive isotopes which inevitably exist in the air in minute amounts and may exist in materials or parts of CMOS image sensor devices (e.g. packaging materials, seal glass, wiring materials and IC chips). It is recommended that you should use materials or parts which do not include radioactive isotopes, which are sources of alpha radiation, and consider taking measures, such as adoption of vacuum packaging technologies in order to ensure that the PRODUCTS are not exposed to the air. As the density of radioactive isotopes in the air of the underground space may become thicker than that on the ground, it is highly recommended to ensure the PRODUCTS are not exposed to the air in using or storing the PRODUCTS at the underground space.

[For Your Reference]

The Annual number of White Pixels Occurrence Caused by Particle Radiation such as cosmic rays etc.

The data in the below chart shows the estimated annual number of White Pixels occurrence caused by particle radiation such as cosmic rays etc. in a single-story building in Tokyo at an altitude of 0 meters. The data shows estimated number of White Pixels based on records of past field tests calculated taking structures and electrical properties of each device into account. However, the data in the chart is for your reference purpose only, and shall not be construed as part of any CMOS image sensor product specifications which the Seller warrants.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
17.6 LSB or higher	2.4 pcs
31.4LSB or higher	1.6 pcs
75.3 LSB or higher	0.9 pcs
156.8 LSB or higher	0.5 pcs
225.8 LSB or higher	0.4 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the annual number of White Pixels occurrence.

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12-2 Measurement Method for Spot Pixels

Measure under the standard imaging condition II.

12-3 Spot Pixel Pattern Specifications

12-3-1 Black or white pixels at high light

After adjusting the average value of the Gr/Gb signal output to 341 LSB, measure the local dip point (black pixel at high light, VXB) and peak point (white pixel at high light, VXK) in the Gr/Gb/R/B signal output Vx(x = Gr/Gb/R/B), and substitute the values into the following formula.
The 341 LSB does not include the dark level offset of 64. The average value is calculated using the signal level output of Zone 2D.

$$D_K(\text{White Pixel level}) = (V_{XK} / \overline{V_X}) \times 100\ [\%]$$

$$D_B(\text{Black Pixel level}) = (V_{XB} / \overline{V_X}) \times 100\ [\%]$$

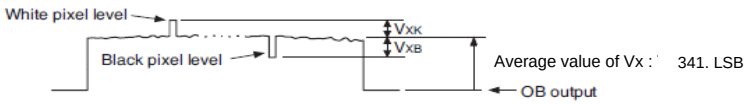

Figure 26 Measurement Method for Spot Pixels

12-3-2 White pixels in the dark

Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

13. CRA Characteristics of Recommended Lens

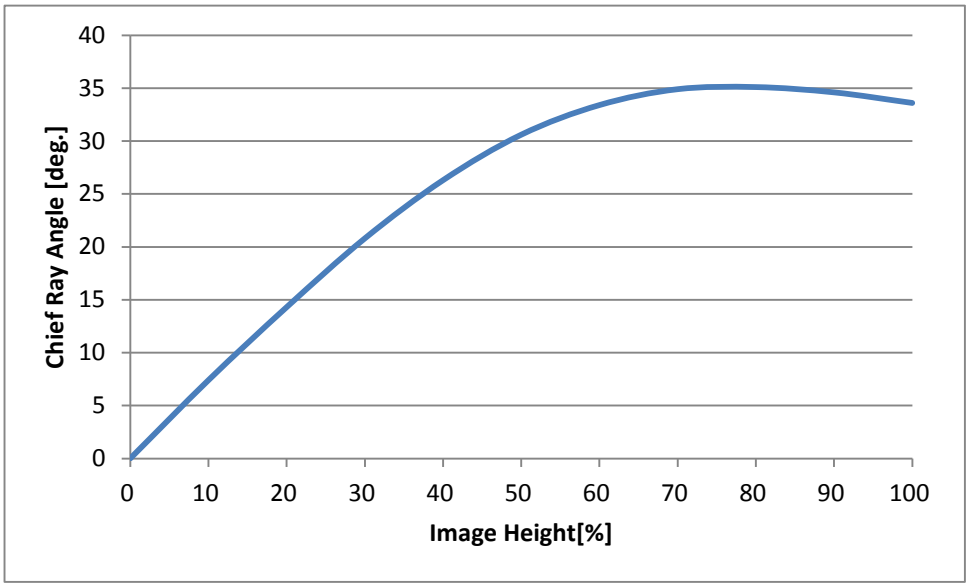

Figure 27 CRA characteristics

14. Notes on Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

(1) Perform all work in a clean environment.
(2) Do not touch the chip surface with hand and make any object contact with it.
(3) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

3. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Reliability assurance of this product should be ignored because it is a bare chip.
(5) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(6) Note that X-ray inspection may damage characteristics of the sensor.
(7) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.
(8) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

15. Notes on Handling (Additional items concerning bare chip mounting of stacked-type CMOS image sensors)

Collet contact is allowed in areas other than the pixel area, bonding pads, scribe area, and chip edge. Contact with areas other than the contact-allowed area may result in problems such as dust emission or electrostatic breakdown.

Collet contact-prohibited areas

- Pixel area: Abnormal images
- Bonding pad: Circuit electrostatic breakdown
  (Please note that this rule is not applicable for electrostatic breakdown prevention areas.)
- Scribe area: Dust emission due to chipping
- Chip edge: Dust emission due to chip breakage

Note: Ensure sufficient positional accuracy during the pickup work.
Separate the collet contact surfaces and contact-prohibited areas as much as possible.

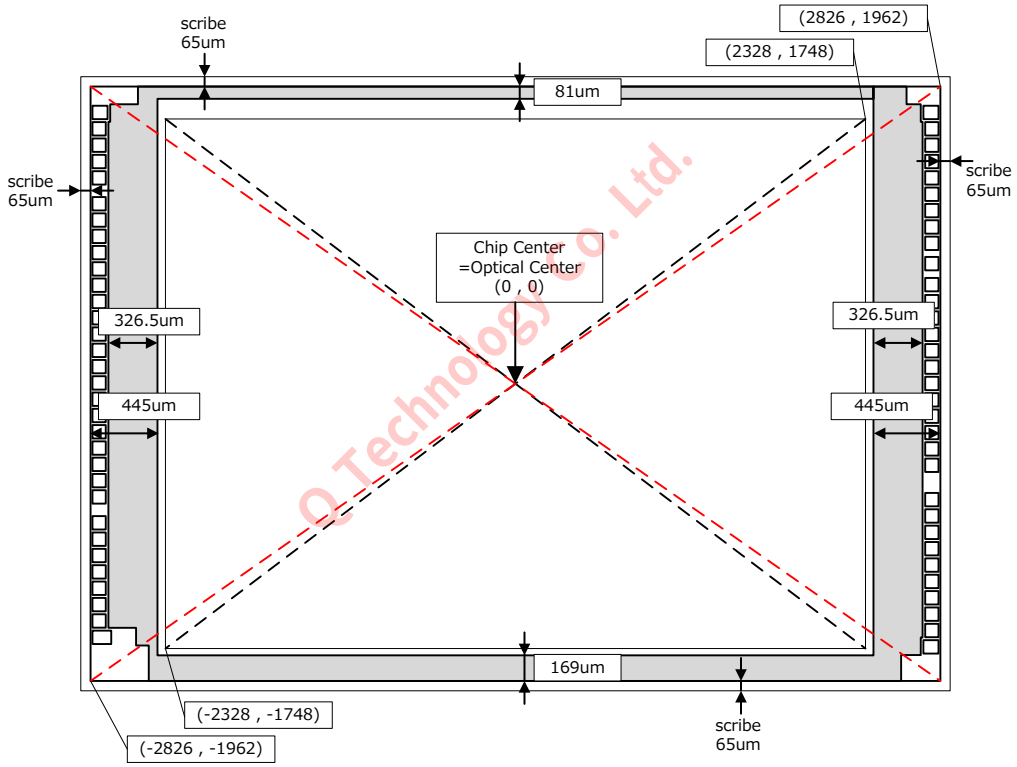

Figure 28 Prohibited Area

Ultrasonic chip cleaning is prohibited.
This may result in dust emission from cut surfaces.

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