

## IMX471 Application Note

**IMX471**

# Software Reference Manual

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Mobile Imaging System Business Division  
Sony Semiconductor Solutions Corporation

## Revision History

Version	Date	Description
0.0.1	2018/1/19	First release.
1.0.0	2018/7/31	Revise: "Table 8-16 CDS clock cycle" Revise: "Table 8-36 Slave control registers to thin out XVS signal input" Revise: "Table 8-37 Slave control registers to thin out or multiply XVS signal input"

Q Technology Co., Ltd.

## Note

In this specification, it covers the major F/W or H/W registers with functionality explanation, however the default value which set by Sony is not written. Because H/W or F/W defaults value is sometimes updated faster than document update timing. See "Register setting" (Excel sheet) for the latest default value shown as "Global Setting".

There are two types of "default value".

- H/W default value: is a default value that is embedded with metal wiring into the silicon. It is decided in very early stage of device design and cannot be changed afterward. These values can be found in the Register Map.
- S/W default value: is a default value that is recommended value and/or bug fix values to be externally over writing H/W default values after evaluation of engineering samples. These values are shown in "Register Setting". Sony recommended register setting table or customer unique register setting table will be supplied upon request.

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Q Technology Co., Ltd.

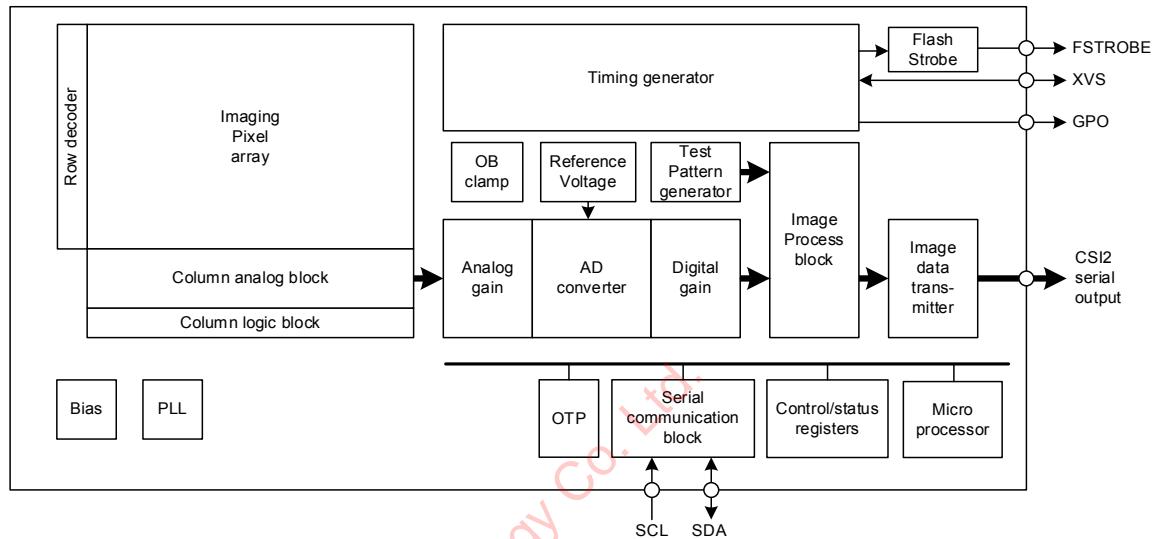
## Glossary

- **Contrast Value**: the value of strength of high-frequency component
- **CRA**: Chief Ray Angle
- **DAC value**: the value of digital analog converter of lens actuator(= the distance from image sensor to lens )
- **DPC**: Defect Pixel Correction
- **Image Height**: the distance from optical light axis on image sensor
- **I2C**: Inter-Integrated Circuit (= serial bus description)
- **LSC**: Lens Shading Correction
- **MIPi**: Mobile Industry Processor Interface
- **OCL**: On Chip Lens
- **OTP**: One Time Programmable ROM
- **OIS**: Optical Image Stabilization(= the lens shifting function for avoiding blurring the image by hand shake)
- **Register**: a small amount of storage in digital processor

SRM-499-00623-01-471-01064-01

## 1. System Outline

This sensor is a diagonal 5.822 mm (Type1/3.09) 16.28 Mega-pixel CMOS active pixel type stacked image sensor with a square pixel array. It adopts Sony's back-illuminated and stacked CMOS image sensor to achieve high speed image capturing by column parallel ADC circuits and high sensitivity and low noise image.



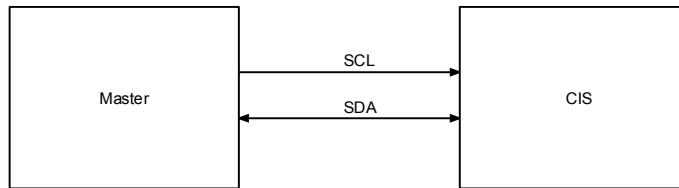
**Figure 1-1 System block diagram**

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## 2. Control Register Settings by Serial Communication

This sensor can use the 2-wire serial communication method for sensor control.

In this chapter, specification, method of 2-wire serial communication between the master device and this sensor is described.



**Figure 2-1 2-wire serial communication**

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### 2.1. 2-wire serial communication operation specifications

The 2-wire serial communication method conforms to the camera control interface (CCI). CCI is an I2C Fast-mode Plus compatible interface, and the data transfer protocol is I2C standard.

This 2-wire serial communication circuit can be used to access the control-registers and status-registers of this sensor.

**Table 2-1 Description of 2-wire serial communication pins**

Pin name	Description
SDA	Serial data input/output pin
SCL	Serial clock input pin

The control registers and status registers of this sensor are mapped on the 16-bit address space.

The register categories are shown below. Detail register information is shown in each chapter/section in this document and in Register Map.

**Table 2-2 Abstract of register address map for 2-wire serial communication**

I <sup>2</sup> C register	Address range	Description	Note
	0x0000 - 0x0fff	Configuration register Read only and read/write dynamic register	
	0x1000 - 0x1fff	Parameter limit register	

		Read only static register	
	0x2000 - 0x2fff	Reserved	
	0x3000 - 0x3fff	Manufacturer specified register	SONY customer register
	0x4000 - 0xffff	Manufacturer specified register	SONY internal register

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## 2.2. Communication protocol

2-wire serial communication supports a 16-bit register address and 8-bit data message type.

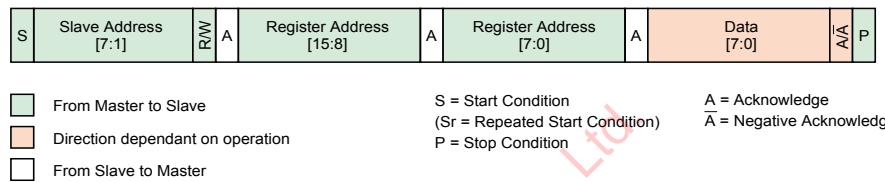


Figure 2-2 2-wire serial communication protocol

SRM-230-00025-03

## 2.3. Default CCI slave address configuration

### 2.3.1. First slave address

This sensor has a default Camera Control Interface (CCI) or 1st I2C slave address shown below. When called by this slave address, the serial communication interface is activated. Duplication of the address on the same bus must be prevented. This slave address is controlled by hardware connection of SLASEL pin.

Slave Address [7:1]	R/W	→	<table border="1"> <tr> <td colspan="8">Slave Address (Read or Write) * See Table 2-3 for R/W bit</td><td>SLASEL (pin#41)</td></tr> <tr> <td colspan="8"> <table border="1"> <tr> <td>MSB</td><td>LSB</td></tr> <tr> <td>0 0 1 1 0 1 0 R/W</td><td>*1</td></tr> </table> </td><td>L or NC</td></tr> <tr> <td colspan="8"> <table border="1"> <tr> <td>MSB</td><td>LSB</td></tr> <tr> <td>0 0 1 0 0 0 0 R/W</td><td>*1</td></tr> </table> </td><td>H</td></tr> </table>	Slave Address (Read or Write) * See Table 2-3 for R/W bit								SLASEL (pin#41)	<table border="1"> <tr> <td>MSB</td><td>LSB</td></tr> <tr> <td>0 0 1 1 0 1 0 R/W</td><td>*1</td></tr> </table>								MSB	LSB	0 0 1 1 0 1 0 R/W	*1	L or NC	<table border="1"> <tr> <td>MSB</td><td>LSB</td></tr> <tr> <td>0 0 1 0 0 0 0 R/W</td><td>*1</td></tr> </table>								MSB	LSB	0 0 1 0 0 0 0 R/W	*1	H
Slave Address (Read or Write) * See Table 2-3 for R/W bit								SLASEL (pin#41)																														
<table border="1"> <tr> <td>MSB</td><td>LSB</td></tr> <tr> <td>0 0 1 1 0 1 0 R/W</td><td>*1</td></tr> </table>								MSB	LSB	0 0 1 1 0 1 0 R/W	*1	L or NC																										
MSB	LSB																																					
0 0 1 1 0 1 0 R/W	*1																																					
<table border="1"> <tr> <td>MSB</td><td>LSB</td></tr> <tr> <td>0 0 1 0 0 0 0 R/W</td><td>*1</td></tr> </table>								MSB	LSB	0 0 1 0 0 0 0 R/W	*1	H																										
MSB	LSB																																					
0 0 1 0 0 0 0 R/W	*1																																					

Note \*1: R/W shows the direction of communication.

Figure 2-3 CCI (I2C) Slave address

**Table 2-3 R/W bit**

R/W bit	Direction of communication	Address
0	Write (master → sensor)	0: 0x34 or 0x20
1	Read (sensor → master)	1: 0x35 or 0x21

### 2.3.2. Secondary slave address

In this sensor, 2<sup>nd</sup> I2C Slave address is available also. This value is fixed as 0x6c (0x6d in case of read timing). It can be switched On/Off by "SLAVE\_ADD\_EN\_2ND" and "SLAVE\_ADD\_ACKEN\_2ND" for ACK to 2<sup>nd</sup> CCI. Refer to the table below.

**Table 2-4 2<sup>nd</sup> CCI ACK control register**

I <sup>2</sup> C register	Address	Bit	Name	Description
	0x3010	[0]	SLAVE_ADD_EN_2ND	2nd Slave Address Enable 0: disable 1: enable
	0x3011	[0]	SLAVE_ADD_ACKEN_2ND	2nd Slave Address Ack Enable 0: disable 1: enable

### 2.3.3. Second CCI slave address for synchronous dual sensor operation

Two sensors are capable to be differently controlled by one host. In this case two sensors could be operated in parallel with even different integration time and gain while keeping synchronization each other. This kind of dual camera application requires having different first slave address and the same second address at the same time between the two sensors.

See "8.8 Dual camera" for more detail.

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## 2.4. Specification of communication bus state

### 2.4.1. Idle state

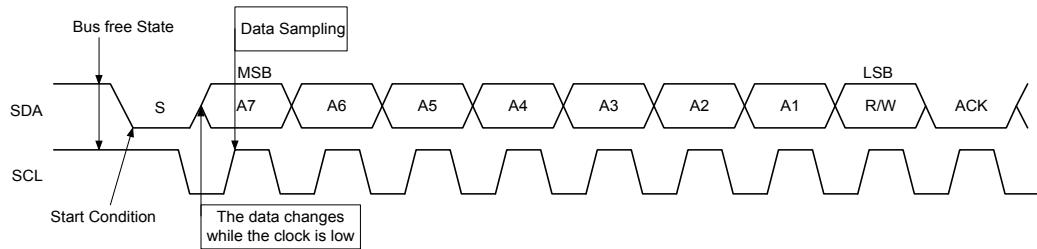
Idle state is specified as follows; neither master nor slave device drives the SDA or SCL, and these bus lines are pulled up to V<sub>dd</sub> via resister.

### 2.4.2. Issue "Start condition"

While the 2-wire communication bus is in idle state, master device (ex. subsequent image processing

LSI, etc.) issues the communication-start: Start condition S by driving SDA from “High” to “Low” level. Serial data are transmitted in 8-bit-unit MSB first format. For every 8-bit data transmission, the slave device issues acknowledge or negative acknowledge (explained later). A (acknowledge)/ $\bar{A}$  (negative acknowledge).

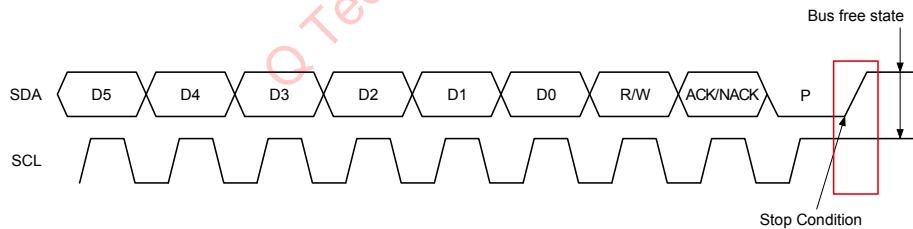
Data (SDA) is transmitted in sync with the SCL cycle. SDA toggles while SCL is “Low” and holds the value while SCL is “High”.



**Figure 2-4 Start condition**

#### 2.4.3. Issue “Stop condition”

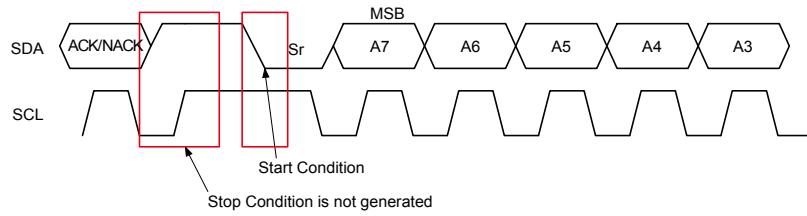
After A (acknowledge)/ $\bar{A}$  (negative acknowledge) and while SCL is High, master device issues communication-stop condition: “Stop condition” P by driving SDA from a low to high level. After issuing a “Stop condition”, master release 2-wire serial bus enters into an idle state.



**Figure 2-5 Stop condition**

#### 2.4.4. Issue “Repeated start condition”

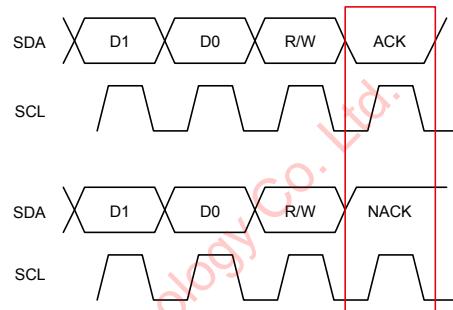
Master device can issue a start condition after previous transaction without issuing a stop condition. In this case this start condition is recognized as the “Repeated started condition” Sr.



**Figure 2-6 Repeated start condition**

#### 2.4.5. Issue acknowledge/negative acknowledge

After transmitting each byte, a master or slave device issues an acknowledgement or negative acknowledgement and can release the bus to the idle state. When negative acknowledgement is issued, the master must issue the stop and terminate the communication immediately.



**Figure 2-7 Acknowledge and negative acknowledge**

SRM-230-00029-05

#### 2.5. Read/write operation of 2-wire serial communication

This sensor has an index function that indicates which address is to be accessed. When reading/writing the value from/to a requested address, the master must set the address value to the index. Index value is designated by 2 bytes of dummy write operation after the slave address transmission. The index value is automatically incremented by “one” with the “Acknowledge/Negative Acknowledge” for the following data transfer.

This sensor supports four read modes and two write modes being compliant to Camera Control Interface (CCI).

**Table 2-5 Read/Write operations supported by 2-wire serial communication**

Access mode	1	CCI single read from random location (Single read from an arbitrary address)
	2	CCI single read from current location (Single read from the held address)
	3	CCI sequential read starting from random location (Sequential read starting from an arbitrary address)
	4	CCI sequential read starting from current location (Sequential read starting from the held address)
	5	CCI single write to random location (Single write to an arbitrary address)
	6	CCI sequential write starting from random location (Sequential write starting from an arbitrary address)

### 2.5.1. CCI single read from random location

The upper part of the below figure below shows the sensor internal index value, and the lower part shows the SDA data flow. The master sets the sensor index value of M by designating the sensor slave address with a write request. Then the Master generates the Start condition. The Start condition is generated without generating the Stop condition, so it becomes the Repeated Start condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the data at the index address on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop condition to end the communication.

When reading single datum from the requested address register, the master device starts write-operation with the slave address of this sensor and by making 2 bytes of dummy write master sets the address value (M) to the index. After that master issues the “start condition” again instead of issuing a “stop condition”. This “start condition” is recognized as “repeated start condition”. Then transmitting the read request with the slave address, this sensor issues the “Acknowledge” and starts transmitting the register value from indexed address (M). Master issues the “Negative Acknowledge” and “stop condition” after receiving the transmission.

The figure below indicates the transition of index value and data on SDA line.

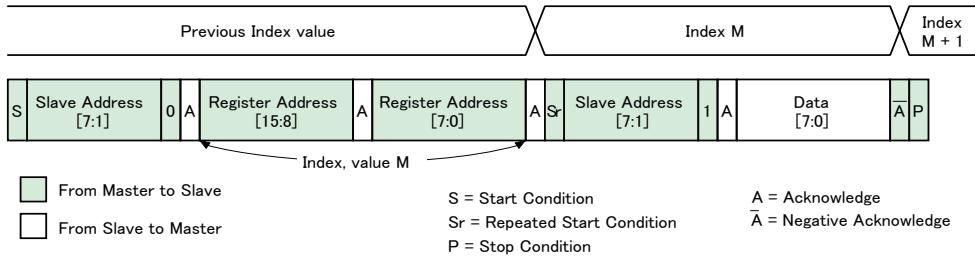


Figure 2-8 CCI single read from random location

### 2.5.2. CCI single read from current location

When master transmits slave address, but does not designate an index, the previous value is held. And the index value is incremented at the “Acknowledge/Negative Acknowledge” after reading/writing the register value. When master knows the current index value is set to the requested address, master transmits the slave address and read request, then the value in the register appears on SDA line right after the “Acknowledge” issued by this sensor. Master issues the “Negative Acknowledge” and “Stop” and terminates the communication. Since the index value is incremented by “one” with this “Negative Acknowledge”, master can read the register value of the next address with the same procedure.

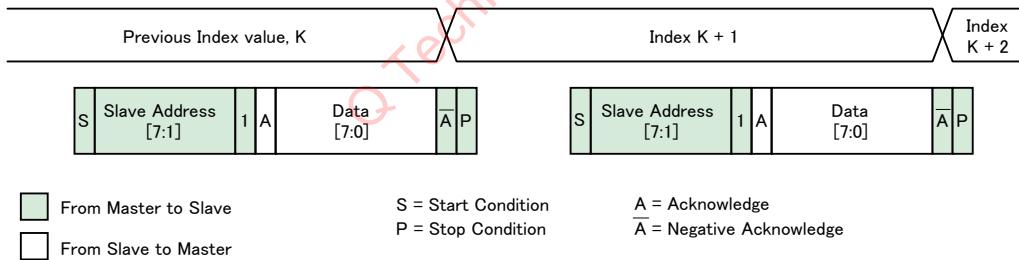
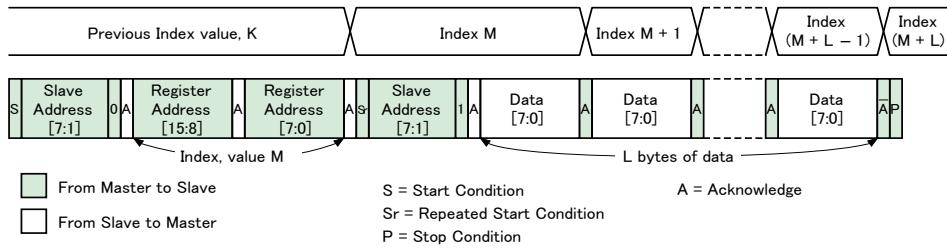


Figure 2-9 CCI single read from current location

### 2.5.3. CCI sequential read starting from random location

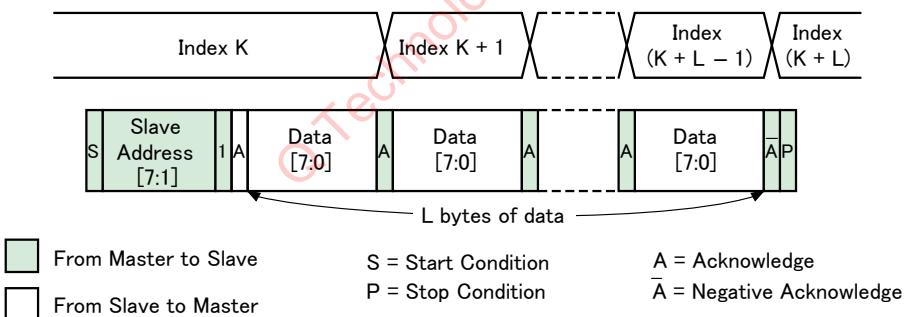
When reading the data from an arbitrary address sequentially, master reads the first data by the similar procedure to “CCI single read from random location” but issues the “Acknowledge” instead of “Negative Acknowledge”, the index is incremented by “one” with this “Acknowledge” then master can repeat the read operation. This operation is terminated when master issues the “Negative Acknowledge”, “Stop condition”, and the communication is terminated.



**Figure 2-10 CCI sequential read starting from random location**

#### 2.5.4. CCI sequential read starting from current location

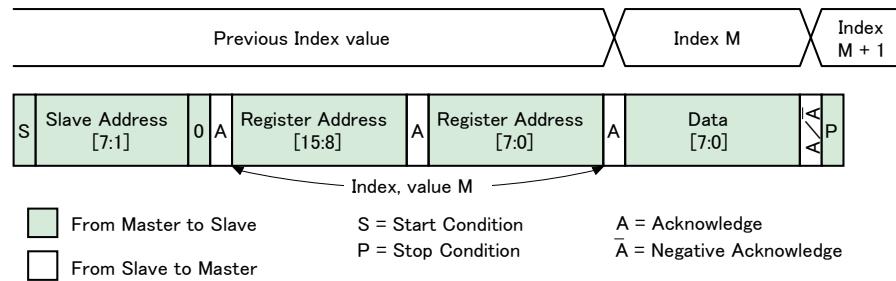
When master knows the current index value is set to the requested address, master transmits the slave address and read request, then the value from the register appears on SDA line right after the “Acknowledge” issued by this sensor. Master issues the “Acknowledge” after receiving 1-byte of the data and this sensor continuously transmits the data from the next address of register since the index value is incremented by “one” with this “Acknowledge”. By repeating issue of the “Acknowledge” for every 1-byte reading, master can read the data sequentially. After reading necessary bytes of data, master issues “Negative Acknowledge” and “stop condition” and then terminates the communication.



**Figure 2-11 CCI sequential read starting from current location**

#### 2.5.5. CCI single write to random location

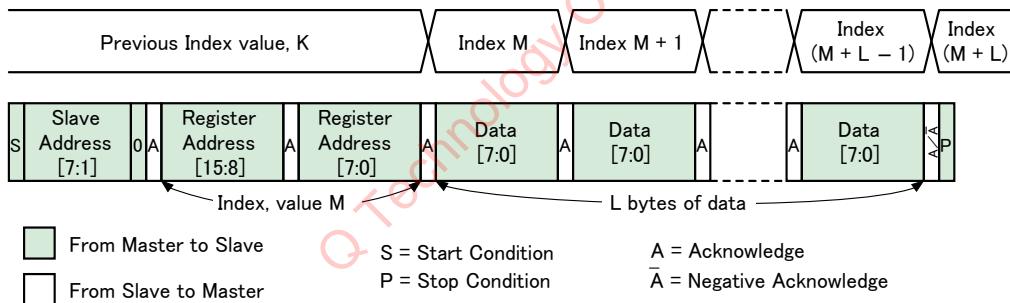
When writing single datum to a register of target address, the master device starts write-operation with the slave address of this sensor and by making 2-bytes of dummy write master sets the address value (M) to the index. And then master transmits the data to be written to the register addressed by index value. Master issues “stop condition” after it transmits the data and terminates the communication



**Figure 2-12 CCI single write to random location**

### 2.5.6. CCI sequential write starting from random location

When master writes the data sequentially from the requested address, master uses a similar procedure to do “CCI single write to random location” and without issuing a “stop condition” and continuously transmits the data after each “Acknowledge” issued. This sensor issues “Acknowledge” for each 1-byte write operation. After transmitting necessary data, master issues a “stop condition” and terminates the communication.

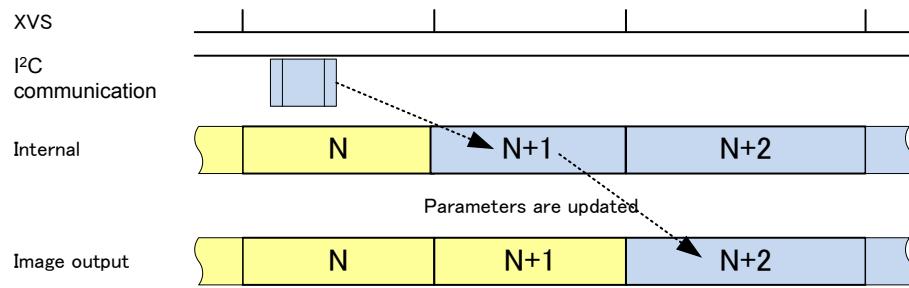


**Figure 2-13 CCI sequential write starting from random location**

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### 2.6. 2-wire serial communication register update timing

There are two types of registers in terms of the update timing of the transmitted data: the immediate type and the double buffered type. For immediate type registers, the transmitted data will be written to the registers immediately. As for the v-latched or double buffered type registers, the actual update timing of the register contents are controlled to the proper timing and become valid in the +1frame or +2frame depending on register function. Users can transmit the commands regardless of the internal update timing of this sensor. The registers of double buffered types are indicated with “v” mark at the “reflection” column of Register Map of this sensor.



**Figure 2-14 2-wire serial communication register update timing diagram (v-latched or double buffered type registers)**

Regarding the use case based CCI communications and reflection timings, refer to each sections as follows:

For reflection timing of capture mode transition, see 7.2 Streaming mode transition

For reflection timing of exposure time and gain change, see 7.3 Exposure and gain change sequence and AE bracketing

#### **Cautions on pre-latch timing of double buffered registers**

Retimed registers are pre-latched before V-sync for internal transaction.

Pre-latch timing exist several lines ahead of the embedded data (FS), and the timing changes depending on the operating condition settings. Registers written ahead of the pre-latch timing are updated internally during the next frame, however registers afterwards are updated internally but may be delayed a frame in addition to the normal update timings. The data transmission to be updated shall be completed within the communication period outlined in Figure2-15 in order to internally update the settings for the target frame; first frame for non-GPH registers and second frame for GPH registers after register settings.

The same timing rule applies for GPH release setting too.

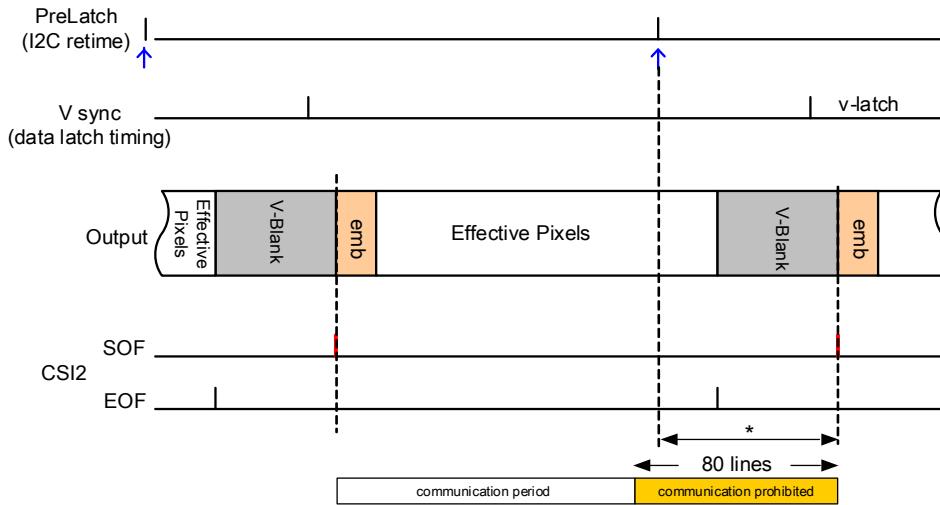


Figure 2-15 Pre-latch timing.

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## 2.7. Grouped parameter hold function

### 2.7.1. Purpose and functional description of grouped parameter hold function

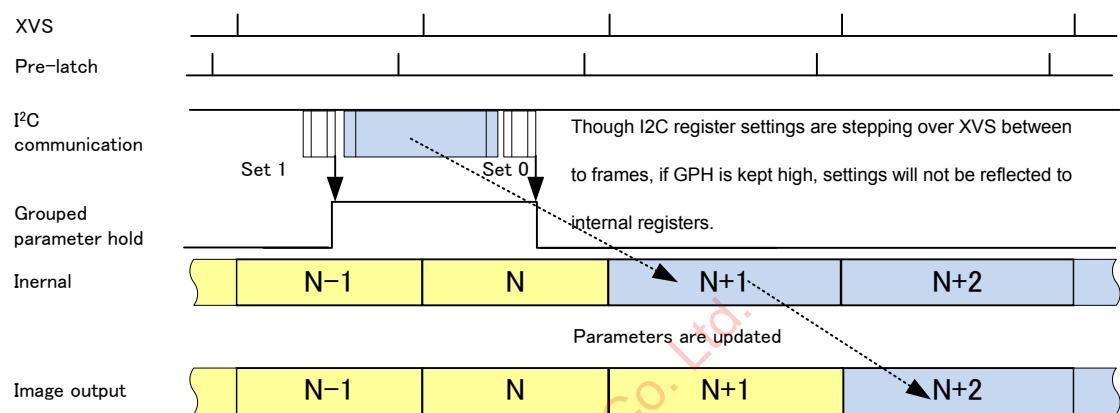
The image shooting parameters are assigned with many registers and they need to be changed within one frame period of the image. However the communication speed is limited and setting all of necessary registers might not be completed. So the double buffered type registers have the “grouped parameter hold” function to behave to be updated at once. While “grouped parameter hold” register is set to “1” the transmitted data are held in the buffer registers and after resets “grouped parameter hold” register to “0”, imaging parameter register values are updated as if they are transmitted at the same time and realize a smooth transition for changing the imaging condition.

In this section, basic concept of the functionality and general ideas of application are explained. It is required to refer to individual sections for complete understanding on application. In such cases pointers to reference sections are also shown.

The register update timing using the “Group parameter hold function” is shown in Figure2-16. If the timing to set “Group parameter hold” from 1 to 0 is before the pre-latch timing, the register is updated internally during the next frame, however if it is afterwards, the update is delayed by 1 frame. It is recommended to release GPH within the “communication period” outlined in Figure2-15 in order to update the register with the target timing.

**Table 2-6 Grouped parameter hold function**

<sup>I<sup>2</sup>C register</sup>	Address	Bit	Name	Description
	0x0104	[0]	GRP_PARAM_HOLD	This register is a hold control register for updating multiple parameters within the same frame. 0 : hold release 1 : hold

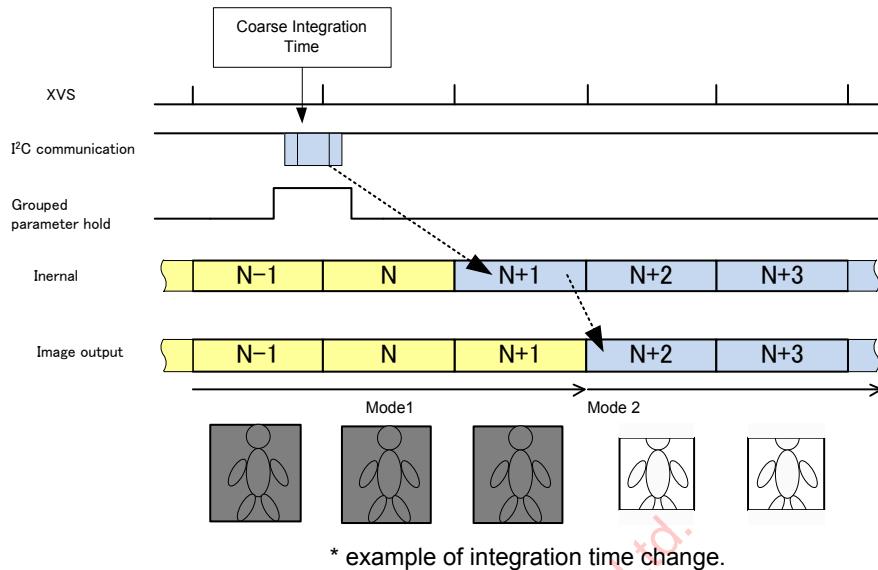


\* example of integration time change.

**Figure 2-16 GRP\_PARAM\_HOLD function timing diagram**

### 2.7.2. Example of mode transition using grouped parameter hold

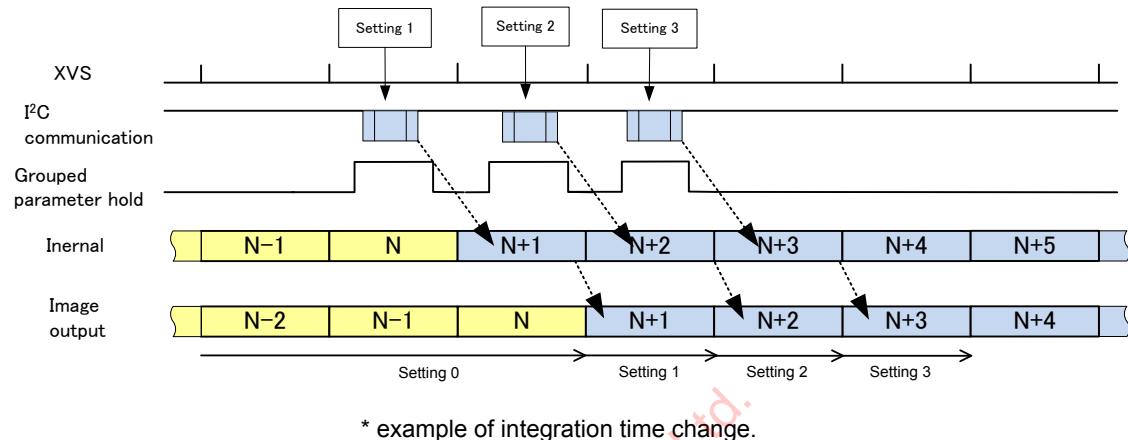
An example of "On the fly" mode transition using "grouped parameter hold" is shown in the following chart. For more detail of "On the fly" mode transition, see section 7.2 and Appendix A-1.2



**Figure 2-17 Mode transition using GRP\_PARAM\_HOLD**

### 2.7.3. Example of using grouped parameter hold continuously

With this sensor, GPH can be used to update registers in continuous frames, unlikely from older product design. This is outlined in the following timing chart. Note that settings for both setting and resetting GPH must be completed within 1 frame ("communication period" shown in Figure2-15).



**Figure 2-18 GRP\_PARM\_HOLD continuous frame register update**

In 7.2 Streaming mode transition and gain feedback, you can find more about the grouped parameter function.

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### 3. Image Signal Interface

SRM-230-00035-01

#### 3.1. MIPI transmitter

This sensor outputs image signals by CSI2 high speed serial interface consisting of one pair of clock lines and four pairs of data lines. Refer to MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) version 1.2 and MIPI Alliance Specification for D-PHY version 1.2 for details. Because signals are transmitted in differential pairs, impedance (generally 100Ω) between differential pairs near the receiver side during HS mode is required.

Otherwise, select a receiver with built-in impedance between differential pairs. Different delay times of differential pairs may reduce the input timing margin of ISP devices, which leads to malfunctions. Therefore, delay time within and among differential pairs must be as similar as possible in layout.

##### 3.1.1. CSI lane mode

**Table 3-1 CSI lane mode register**

I <sup>2</sup> C register	Address	Bit	Name	Description
	0x0114	[1:0]	CSI_LANE_MODE	Number of lanes for CSI 0 : 1-lane *not supported 1 : 2-lane 2 : 3-lane *not supported 3 : 4-lane

MIPI pins function as shown in the following table according to CSI\_LANE\_MODE.

**Table 3-2 MIPI transmitter**

MIPI transmitter	Pin name	2Lane	4Lane
	DCKP/DCKN	Clock lane	Clock lane
	DMO1P/DMO1N	Data lane 1	Data lane 1
	DMO2P/DMO2N	Data lane 2	Data lane 2
	DMO3P/DMO3N	Not used (LP only)	Data lane 3
	DMO4P/DMO4N	Not used (LP only)	Data lane 4

### 3.1.2. CSI data format

The following register table specifies data format of the image output.

It sets data format from the options of output format as shown in the table below.

**Table 3-3 CSI data format registers**

I2C register	Address	Bit	Name	Description
	0x0112	[7:0]	CSI_DT_FMT_H	The output data format for CSI CSI_DT_FMT_H : Uncompressed Data Bit Width CSI_DT_FMT_L : Compressed Data Bit Width 0x0808 : RAW8 (top 8bit of internal data) 0x0A08 : COMP8 (10bit to 8bit compression) 0x0A0A : RAW10 (top 10bit of internal data) Setup other than the above is forbidden.
	0x0113	[7:0]	CSI_DT_FMT_L	

### 3.1.3. CSI-2 bus

#### 3.1.3.1. RAW8/COMP8

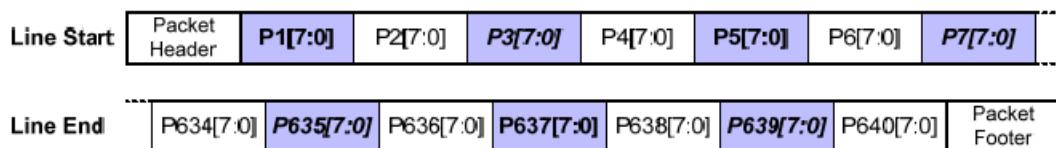
The 8-bit compression data transmission is performed by transmitting the pixel data over a CSI-2 bus.

The following table specifies the packet size constraints for RAW8/COMP8 packets. The length of each packet must be a multiple of the values in the table.

**Table 3-4 Packet size constraints for RAW8/COMP8 packet**

Pixels	Bytes	Bits
1	1	8

Bit order in transmission follows the general CSI-2 rule, LSB first.



**Figure 3-1 RAW8/COMP8 transmission**

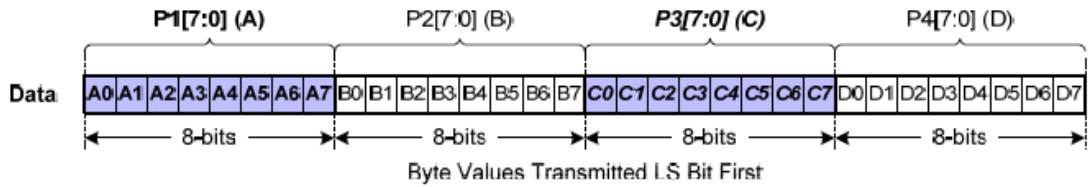


Figure 3-2 RAW8/COMP8 data transmission on CSI-2 bus bitwise illustration

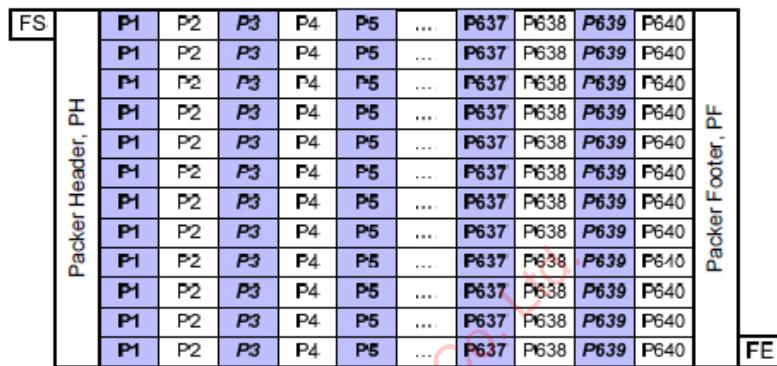


Figure 3-3 RAW8/COMP8 frame format

### 3.1.3.2. RAW10

The transmission of 10-bit Raw data is accomplished by packing the 10-bit pixel data to look like 8-bit data format. The following table specifies the packet size constraints for RAW10 packets. The length of each packet must be a multiple of the values in the table.

Table 3-5 Packet size constraint for RAW10 packets

Pixels	Bytes	Bits
4	5	40

Bit order in transmission follows the general CSI-2 rule, LSB first.

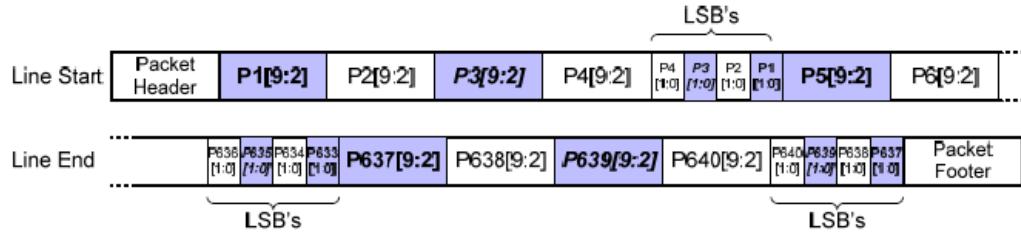


Figure 3-4 RAW10 transmission

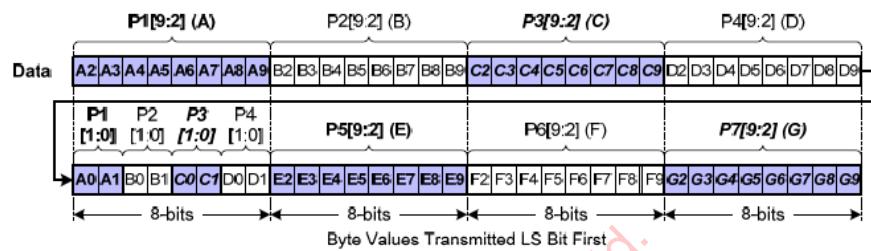


Figure 3-5 RAW10 data transmission on CSI-2 bus bitwise illustration

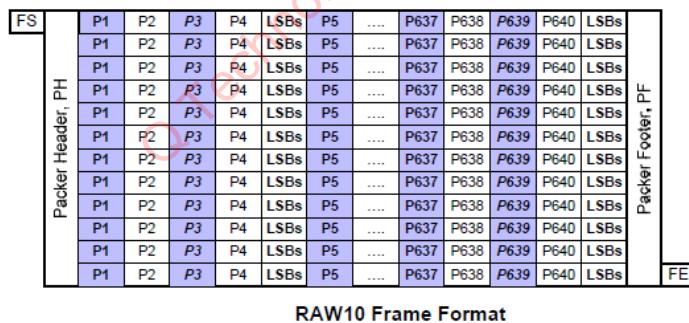


Figure 3-6 RAW10 frame format

### 3.1.4. MIPI Global Timing setting

MIPI Global Timing parameters are set with the registers below.

The setting method of MIPI Global Timing can be selected with the DPHY\_CTRL register.

DPHY\_CTRL=0, Use automatic control (Automatic Mode)

MIPI Global timing automatically set the appropriate value which is calculated by the below bitrate setting.

In case of PLL single mode (PLL\_MULT\_DRIV=0),

$$\text{Bitrate} = (\text{PLL output frequency}) / (\text{OP Sys Clock Divider})$$

$$(\text{PLL output frequency}) = \text{INCK} \times \text{IVT_PLL_MPY} / \text{IVT_PREPLLCK_DIV}$$

In case of PLL dual mode (PLL\_MULT\_DRIV=1)

$$\text{Bitrate} = (\text{PLL output frequency}) / (\text{OP Sys Clock Divider})$$

$$(\text{PLL output frequency}) = \text{INCK} \times \text{IOP_PLL_MPY} / \text{IOP_PREPLLCK_DIV}$$

When externally set as DPHY\_CTRL=1, MIPI Global Timing is automatically set using the values of REQ\_LINK\_BIT\_RATE\_MBPS and CSI\_LANE\_MODE.

Global Timing Setting is automatically set every time the setting of REQ\_LINK\_BIT\_RATE\_MBPS is changed.

The value of the REQ\_LINK\_BIT\_RATE\_MBPS can be obtained from the following relational equation.

$$\text{REQ\_LINK\_BIT\_RATE\_MBPS} = \text{Output bitrate} * (\text{CSI\_LANE\_MODE} + 1)$$

Where Output bitrate = IOPSYCK

\* REQ\_LINK\_BIT\_RATE[31:0] consist of integer part (REQ\_LINK\_BIT\_RATE\_MBPS[31:16]) and decimal part (REQ\_LINK\_BIT\_RATE\_MBS[15:0]).

\* For IOPSYCK, more detail refers to “5.1.4 IOPSYCK Clock”.

When set as DPHY\_CTRL=2, Global Timing must be set with registers from 0x080a to 0x0819 manually.

**Table 3-6 MIPI Global timing setting**

<b>I<sup>2</sup>C register</b>	Address	Bit	Name	Description
	0x0808	[1:0]	DPHY_CTRL	MIPI Global Timing control selection 0 : automatic control 1 : UI control 2 : register control 3 : reserved
	0x080a	[1:0]	TCLK_POST_EX [9:8]	MIPI Global Timing (Tclk)
	0x080b	[7:0]	TCLK_POST_EX [7:0]	
	0x080c	[1:0]	THS_PREPARE_EX [9:8]	MIPI Global Timing (Ths_prepare)
	0x080d	[7:0]	THS_PREPARE_EX [7:0]	
	0x080e	[1:0]	THS_ZERO_MIN_EX [9:8]	MIPI Global Timing (Ths_zero_min)
	0x080f	[7:0]	THS_ZERO_MIN_EX [7:0]	
	0x0810	[1:0]	THS_TRAIL_EX [9:8]	MIPI Global Timing (Ths_trail)
	0x0811	[7:0]	THS_TRAIL_EX [7:0]	
	0x0812	[1:0]	TCLK_TRAIL_MIN_EX [9:8]	MIPI Global Timing (Tclk_trail_min)
	0x0813	[7:0]	TCLK_TRAIL_MIN_EX [7:0]	
	0x0814	[1:0]	TCLK_PREPARE_EX [9:8]	MIPI Global Timing (Tclk_prepare)
	0x0815	[7:0]	TCLK_PREPARE_EX [7:0]	
	0x0816	[1:0]	TCLK_ZERO_EX [9:8]	MIPI Global Timing (Tclk_zero)
	0x0817	[7:0]	TCLK_ZERO_EX [7:0]	
	0x0818	[1:0]	TLPX_EX [9:8]	MIPI Global Timing (Tlpx)
	0x0819	[7:0]	TLPX_EX [7:0]	
	0x0820	[7:0]	REQ_LINK_BIT_RATE_MBPS[31:24]	Output Data Rate [Mbps] Bit[32:16] integer Bit[15:0] decimal
	0x0821	[7:0]	REQ_LINK_BIT_RATE_MBPS[23:16]	
	0x0822	[7:0]	REQ_LINK_BIT_RATE_MBPS[15:8]	
	0x0823	[7:0]	REQ_LINK_BIT_RATE_MBPS[7:0]	

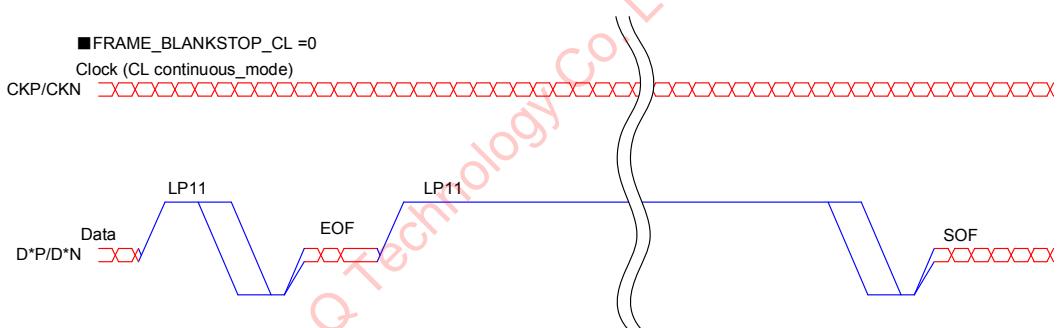
### 3.1.5. CLK mode during Frame blanking

This is a function to stop the MIPI clock during Frame Blanking.

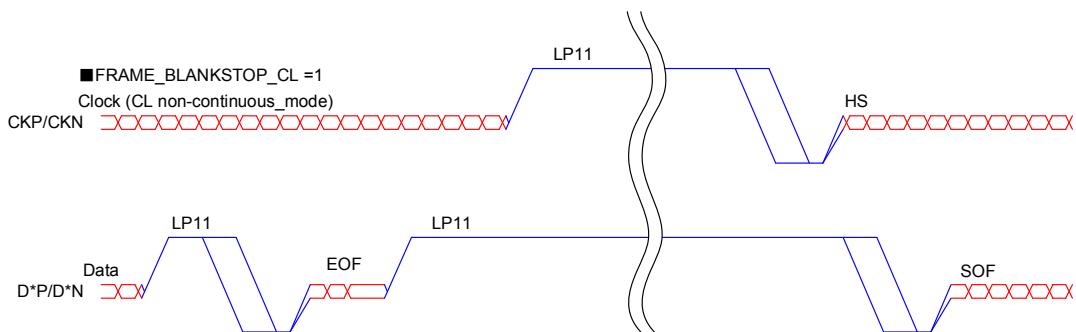
The details of the register and timing are shown below.

**Table 3-7 CLK mode setting register during Frame Blanking**

<sup>I<sup>2</sup>C register</sup>	Address	Bit	Name	Description
	0xe000	[0]	FRAME_BLANKSTOP_CL	<p>FRAME_BLANKSTOP_CL Control RUN/STOP of CSI2 during Frame Blanking</p> <p>0 : Stay in HS mode (Clock/Strobe output) during CLK Frame Blanking</p> <p>1 : Transition to LP11 (Clock/Strobe stop) during CLK Frame Blanking</p> <p>Details are as follows:</p> <ul style="list-style-type: none"> <li>- When a valid frame starts, transition to HS-Clock status.</li> <li>- When the frame ends (after EOF output), transition from HS-Clock to LP11.</li> </ul>



**Figure 3-7 CLK mode during Frame Blanking (FRAME\_BLANKSTOP\_CL = 0)**



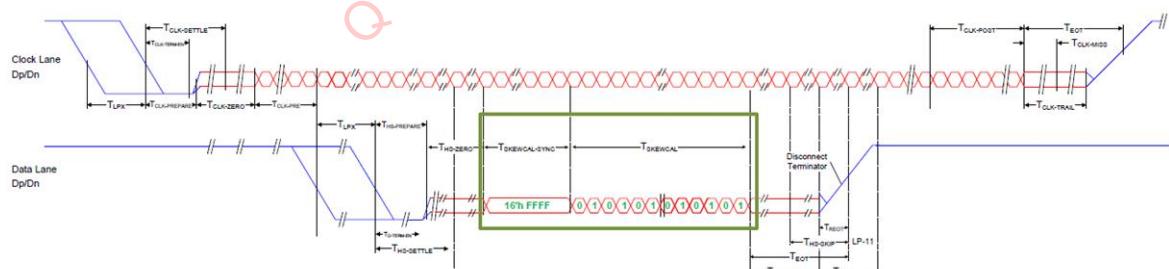
**Figure 3-8 CLK mode during Frame Blanking (FRAME\_BLANKSTOP\_CL = 1)**

### 3.1.6. MIPI Skew Calibration Data Output

This sensor supports Skew calibration data output compliant with MIPI Alliance Specification for D-PHY version 1.2. When outputting the data with the bit rate higher than 1.5 Gbps/lane, initial and periodic skew calibration can be transmitted before High-Speed Data Transmission. In this case, the initial skew calibration output can select by SCAL\_INIT\_EN and the periodic skew calibration output can select by SCAL\_PERIOD\_EN register. Initial and periodic skew calibrations are composed of a combination of a sync pattern consisting only of "1s" and a clock pattern (010101...) as shown in the following figure. The initial skew calibration transmits a clock pattern for 100 $\mu$ sec after transmitting the 16UI sync pattern. The periodic skew calibration transmits a clock pattern for 10 $\mu$ sec after transmitting the 16UI sync pattern.

**Table 3-8 Skew calibration control register**

I2C Address	Bit	Name	Description
0x0830	[0]	SCAL_PERIOD_EN	For period skew calibration control This register can be set only when SW Standby. 0: disable calibration during frame blanking(not auto clear) 1: enable calibration during frame blanking(not auto clear)
0x0832	[0]	SCAL_INIT_EN	For initial skew calibration control This register can be set only when SW Standby. 0: disable calibration in start streaming(not auto clear) 1: enable calibration in start streaming(not auto clear)



**Figure 3-9 Skew calibration data output**

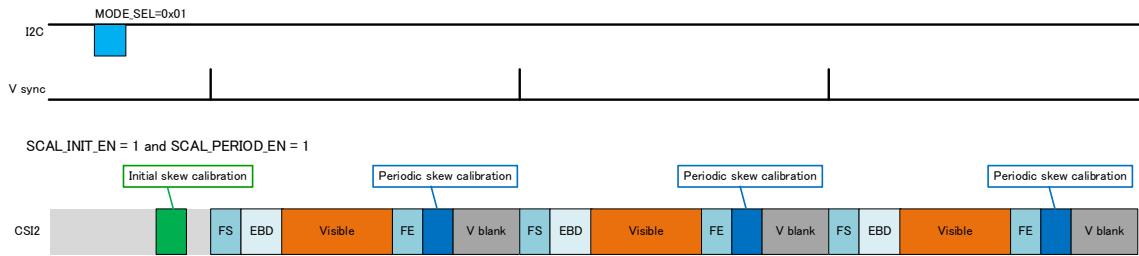


Figure 3-10 Initial and Periodic skew calibration data output

SRM-318-100-519-002

## 4. Image Readout Operation

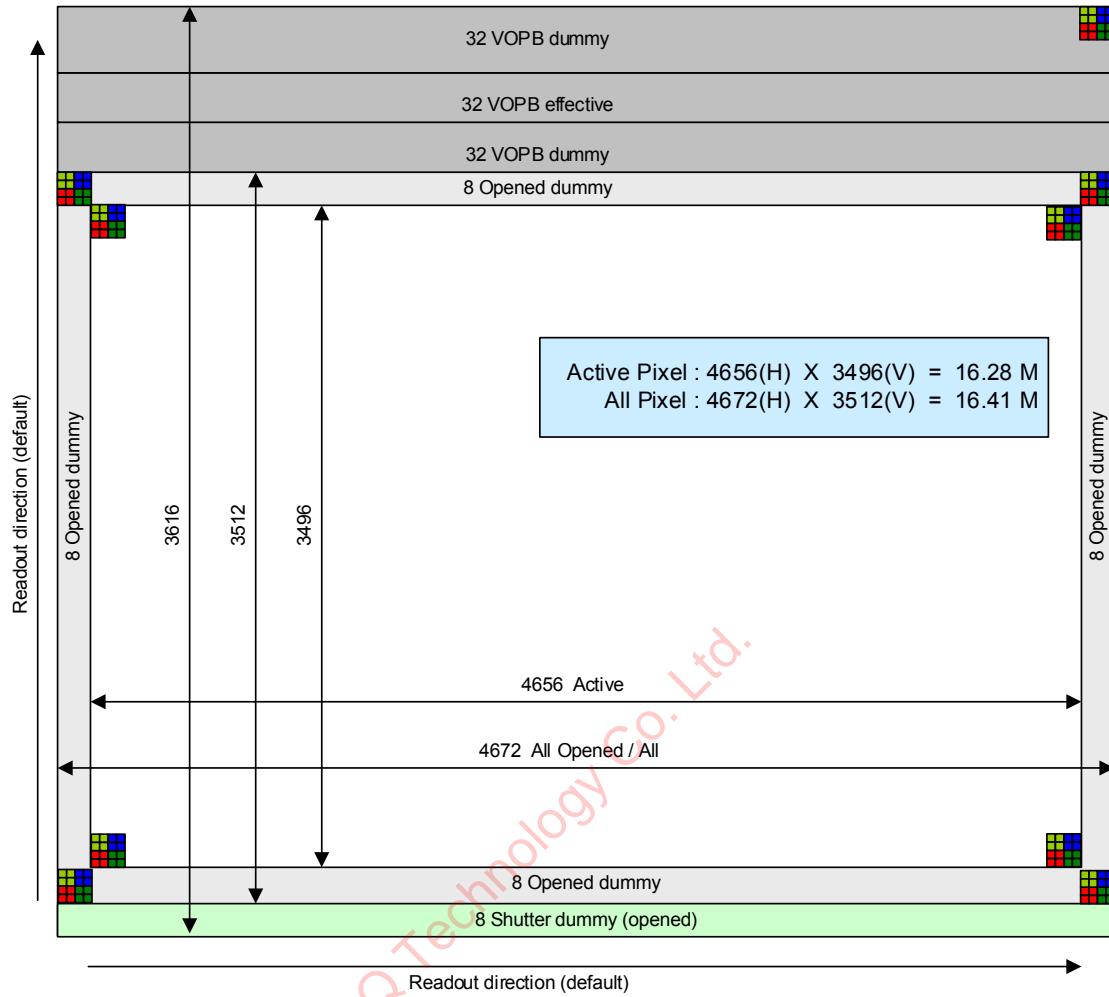
In this chapter, you can find relations among imaging area, pixel readout orientation/readout and transmission frame/signal structure.

By setting the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, binning, shutter mode, integration time, gain, and output format via 2-wire serial communication, this sensor outputs the image data.

SRM-230-00041-01-258-00042-02

### 4.1. Physical alignment of imaging pixel array

The figure below shows the physical alignment of the imaging pixel array with pin #1 located at the upper left corner.

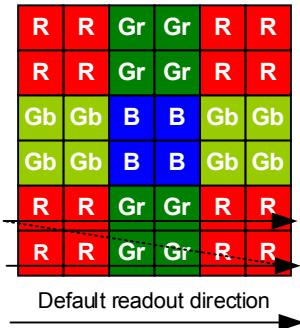


**Figure 4-1 Physical alignment of imaging pixel array**

SRM-371-00463-01-471-00978-01

#### 4.2. Color coding and order of reading image data

The original color filter arrangement of the sensor is shown in the figure below. Gr and Gb are the G signals shown at the same line as R signals and B signals respectively. The line with R & Gr signals and the line with Gb & B signals are output alternating one after the other.



**Figure 4-2 Color coding alignment**

SRM-350-00192-01-371-00464-01

#### 4.3. Imaging area determination

Imaging area is specified on the output signal with physical coordinate with lower left as (0, 0) and determined by registers shown as below.

**Table 4-1 Imaging area determining registers**

I <sup>2</sup> C register	Address	Bit	Name	Description
	0x0344	[4:0]	X_ADD_STA [12:8]	Horizontal direction analog cropping start position within the active pixels area Unit : pixels Format : 13-bit unsigned integer Should be set to 0. * Note that this is the cropping end position when mirroring (IMG_ORIENTATION_H=1)
	0x0345	[7:0]	X_ADD_STA [7:0]	
	0x0346	[3:0]	Y_ADD_STA [11:8]	Vertical direction analog cropping start position within the active pixels area Unit : pixels Format : 13-bit unsigned integer * Note that this is the cropping end position when flipping (IMG_ORIENTATION_V=1)
	0x0347	[7:0]	Y_ADD_STA [7:0]	
	0x0348	[4:0]	X_ADD_END [12:8]	Horizontal direction analog cropping end position within the active pixels area Unit : pixels Format : 13-bit unsigned integer Should be set to 4655. * Note that this is the cropping start position when mirroring (IMG_ORIENTATION_H=1)
	0x0349	[7:0]	X_ADD_END [7:0]	

	0x034a	[3:0]	Y_ADD_END [11:8]	Vertical direction analog cropping end position within the active pixels area Unit : pixels Format : 13-bit unsigned integer * Note that this is the cropping start position when flipping (IMG_ORIENTATION_V=1)
	0x034b	[7:0]	Y_ADD_END [7:0]	

\* Above settings shall be always set based on full pixel basis even in binning mode.

Q Technology Co., Ltd.

There are capture mode and/or binning mode dependent restrictions in setting Imaging area as shown in the following table.

**Table 4-2 Register setting Restrictions list for each mode**

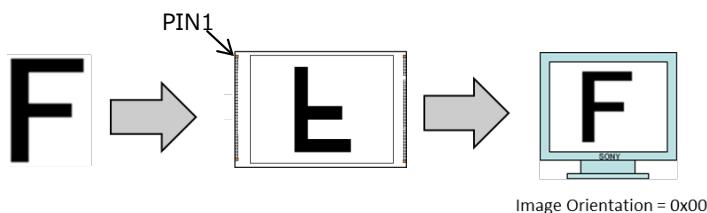
Mode		
	Full-pixel	H:2-bin V:2-bin
Y_ADD_STA	4N	4N
Y_ADD_END – Y_ADD_STA+ 1	4M	4M
X_ADD_STA	0	0
X_ADD_END – X_ADD_STA + 1	4656	4656

\*N,M : Integer

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#### 4.4. Readout start position

Default readout position of this sensor starts from the lower left whenever PIN1 is placed at the upper left corner. Because the lens will invert the image both vertically and horizontally, the proper image can be achieved when PIN1 is placed at the upper left corner.

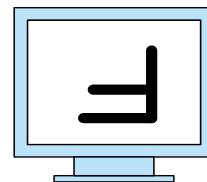
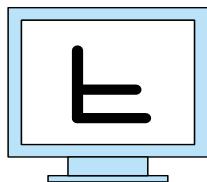


**Figure 4-3 Readout start position**

Vertical flip and horizontal mirror readout modes can be specified by the register below. When the readout direction is changed, the color of the first pixel (R/Gr/Gb/B) read out also changes with it.

**Table 4-3 Vertical flip and horizontal mirror**

<sup>I<sup>2</sup>C register</sup>	Address	bit	Name	Description
0x0101	[1]	IMG_ORIENTATION_V	Image orientation for Vertical direction 0 : normal 1 : reverse	Image orientation for Vertical direction 0 : normal 1 : reverse



IMAGE\_ORIENTATION = 0x01   IMAGE\_ORIENTATION = 0x02   IMAGE\_ORIENTATION = 0x03

**Figure 4-4 Read out image for each combination of flip and mirror**

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#### 4.5. Frame structure

Each line of each image frame will be output according to the General Frame Format of CSI2 specification. A period of time from the line end sync code (Packet Footer (PF)) to the line start sync code (Packet Header (PH)) of the next line is called “line blanking”.

Similarly, a period of time from the frame end sync code (Frame End (FE)) to the frame start sync code (Frame Start (FS)) of the next frame is called “frame blanking”.

Frame size is determined by “FRM\_LENGTH\_LINES” in the vertical direction and “LINE\_LENGTH\_PCK” in the horizontal direction.

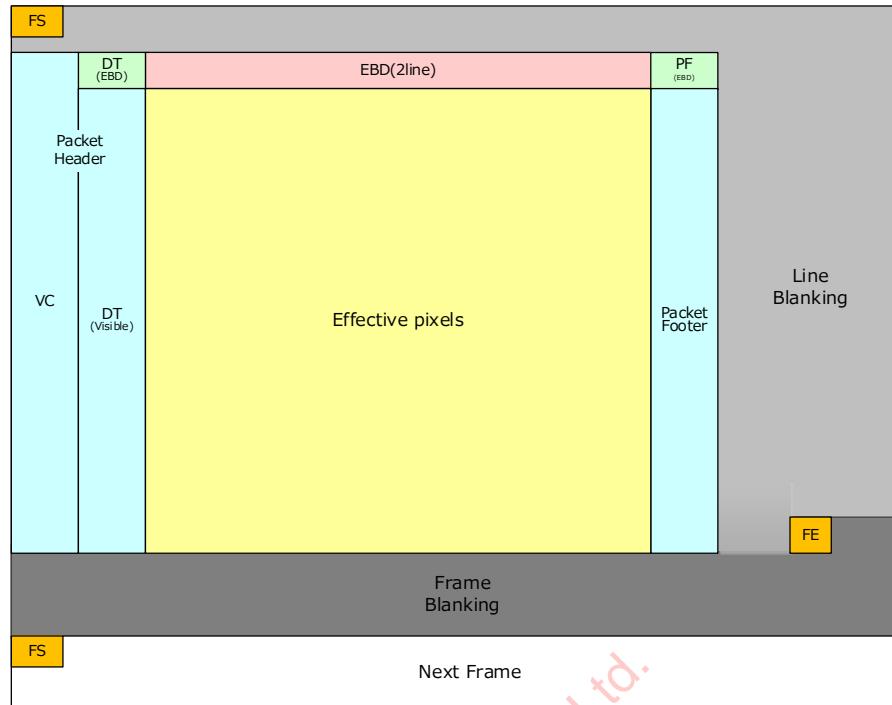


Figure 4-5 Frame structure (Normal)

#### 4.5.1. Registers that determine frame size

**Table 4-4 Registers that determine frame size**

I <sup>2</sup> C register	address	bit	name		description
	0x0340	[7:0]	FRM_LENGTH_LINES [15:8]		The length of frame Unit : lines Format : 16-bit unsigned integer *set value for given capture mode $\leq 65534d$
	0x0341	[7:0]	FRM_LENGTH_LINES [7:0]		
	0x0342	[7:0]	LINE_LENGTH_PCK [15:8]		The length of line Unit : pixels Format : 16-bit unsigned integer * LINE_LENGTH_PCK has been constrained. * Must be set fixed value as Table4-5.
	0x0343	[7:0]	LINE_LENGTH_PCK [7:0]		

##### 4.5.1.1. Constraints of LINE\_LENGTH\_PCK

Setting value that can be set as LINE\_LENGTH\_PCK is constrained. Must be set fixed value as follows for each mode setting.

Setting other than these values prohibited.

**Table 4-5 Constraints of LINE\_LENGTH\_PCK**

	0x0900 [0]	0x0901 [7:0]	0x0342 [7:0], 0x0343 [7:0]
Mode	BINNING_MODE [0]	BINNING_TYPE_H [7:4] BINNING_TYPE_V [3:0]	LINE_LENGTH_PCK [15:0] Default is bold
Full resolution	0x0	x	<b>5120, 10240</b>
2x2 Adjacent Pixel Binning	0x1	0x22	<b>2560, 5120</b>

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#### 4.6. Output image format

This is the output image diagram of full pixel output mode, Image data is output from the upper left corner of the diagram.

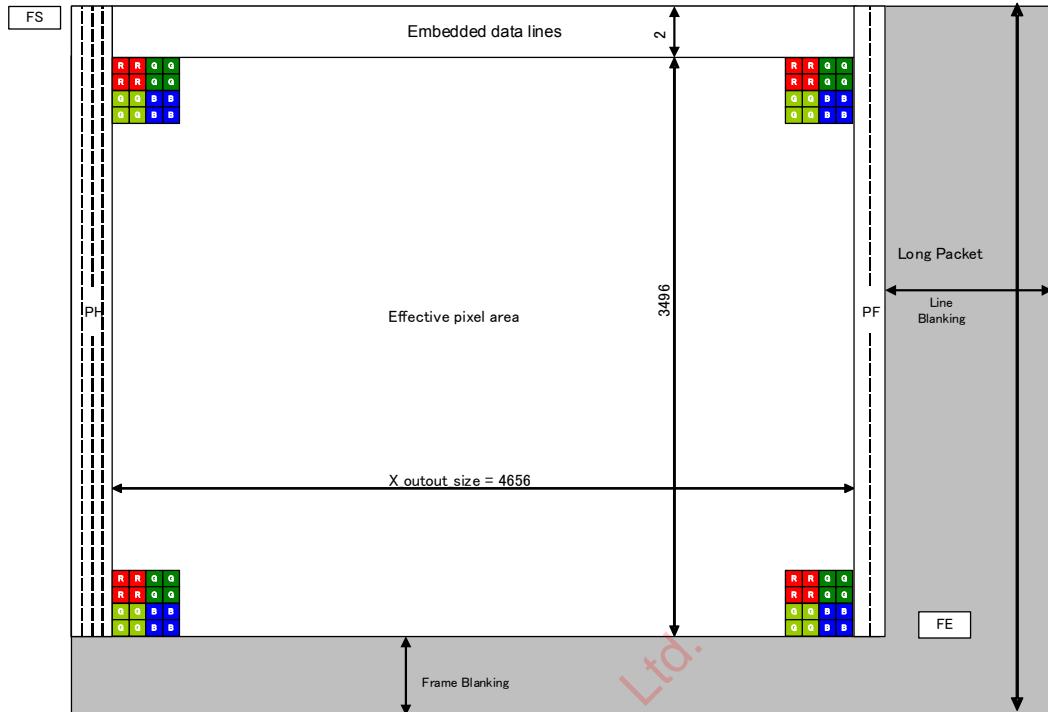


Figure 4-6 Full pixel output mode image data structure

#### 4.6.1. Contents of packet header

The contents of the first byte in the packet header (data identifier) and the corresponding register settings are described in the table below.

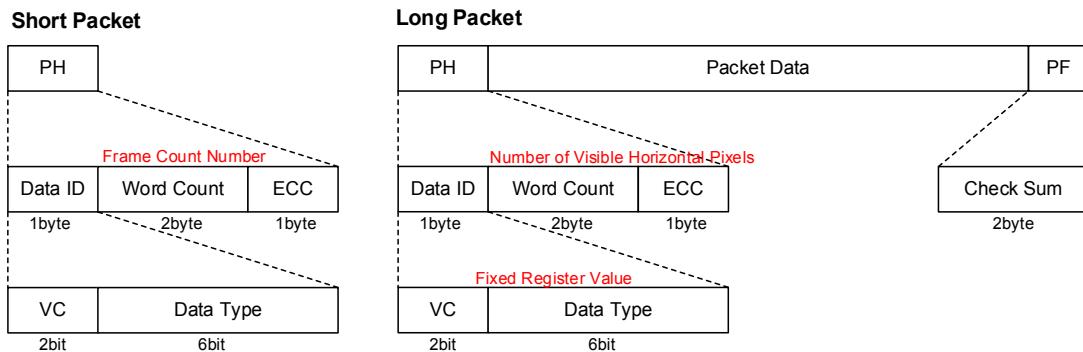
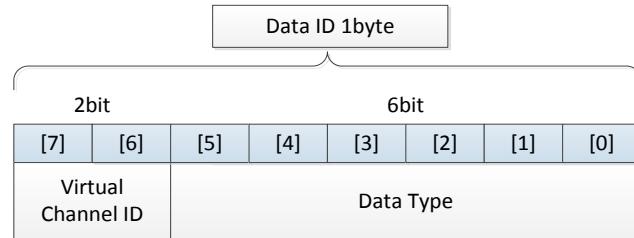


Figure 4-7 Short packet & long packet structures

**Figure 4-8 Configuration of Data ID****Table 4-6 Data Identifier**

Packet header	Bit assignment	Value	Name	Corresponding registers (I2C)	Description
	[7:6] Virtual Channel ID	2'h0 (Default)	-	0x 0110 CSI_CH_ID [2:0]	Refers LSB 2bits
[5:0] Data types	6'h00	Frame Start Code	NA		
	6'h01	Frame End Code	NA		
	6'h12	Embedded Data	NA		For embedded data line
	6'h2A	RAW8	NA	0x0112:CSI_DT_FMT_H=0x08 0x0113:CSI_DT_FMT_L=0x08	
	6'h2B	RAW10	NA	0x0112:CSI_DT_FMT_H=0x0a 0x0113:CSI_DT_FMT_L=0x0a	
	6'h30	COMP8 (10bit to 8bit)	NA	0x0112:CSI_DT_FMT_H=0x0a 0x0113:CSI_DT_FMT_L=0x08	

Note: CSI\_CH\_ID[2:0] should be updated during SW-standby.

#### 4.6.2. Data type

Types of data in each line are shown below.

**Table 4-7 Image pixel area and data type**

Image pixel area	Data type
Embedded data lines	Embedded data
Effective pixels	RAW10, COMP8(10bit to 8bit), RAW8

#### 4.6.3. Embedded data line control

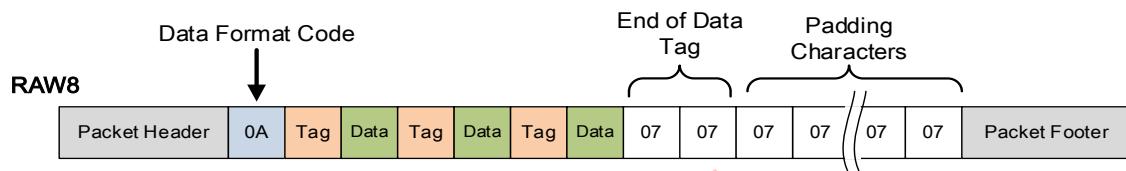
It is possible to output certain 2-wire serial register contents on the 2 lines just after the FS sync code

of the frame. Undefined value is output when not outputting embedded data. Regarding actual contents of the embedded data line are listed in Appendix.

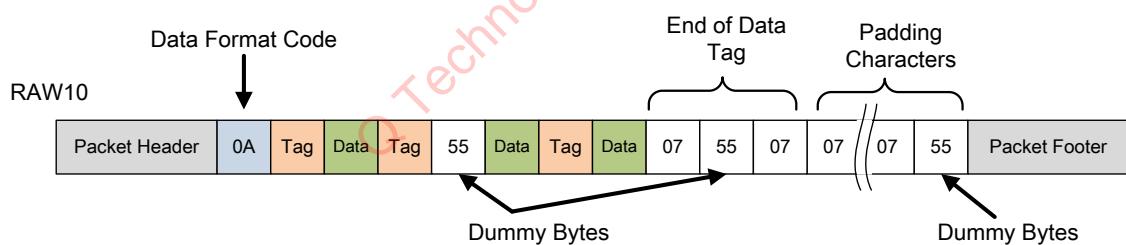
**Table 4-8 Embedded data line control**

I <sup>2</sup> C register	Address	Bit	Name	Description
	0xBCF1	[7:0]	EBD_SIZE_V	0 is no EBD 2 is EBD 2 line others are forbidden

The sequence of EBD in each output format is as shown in the figures below.



**Figure 4-9 Embedded data lines alignment in RAW8 mode**



**Figure 4-10 Embedded data lines alignment in RAW10 mode**

Addresses and the end of register values are distinguished by “Tags” embedded in the data sequence.

**Table 4-9 Embedded data line tag**

Tag	Data byte description
00h	Illegal Tag. If found treat as end of Data
07h	End of Data (Data Byte Value = 07H)
aah	CCI Register Index MSB [15:8]
a5h	CCI Register Index LSB [7:0]
5ah	Auto increment the CCI index after the data byte – valid data Data byte contains valid CCI register data
55h	Auto increment the CCI index after the data byte – null data A CCI register does NOT exist for the current CCI index. The data byte value is the 07H
ffh	Illegal Tag. If found treat as end of Data

The definite data sequence is described in the table in the Appendix.

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## 5. Operation Mode Setting

SRM-230-00061-01

### 5.1. Clock generation and PLL

This sensor is equipped with embedded oscillator and PLL to generate the necessary internal clocks and CSI2 transmission clocks. Set the related registers according to the operation conditions.

#### 5.1.1. Clock system diagram

This sensor is equipped with 2 PLLs, one to output IVTCK for image processing, and the other to output IOPSYCK for MIPI output. The IVTCK PLL can output at 338 to 1740 MHz, and the IOPCK PLL can output at 338 to 1840 MHz, based on a clock input with the 6 to 27 MHz range.

The IVTCK PLL could be configured with divider of up to 1/1 to 1/4 range, and multiply in the 29 to 290 range.

The IOPCK PLL could be configured with divider of up to 1/1 to 1/15 range, and multiply in the 29 to 1840 range.

This sensor normally recommend to make it operate in single PLL mode by driving just one PLL (IOPCK PLL), however can also operate in dual PLL mode by driving both PLLs from parameter setting flexibility point of view.

In PLL single mode, IVT\_PREPLLCK\_DIV and IVT\_PLL\_MPY are applied to IOPCK PLL, and IOP\_PREPLLCK\_DIV and IOP\_PLL\_MPY are ignored.

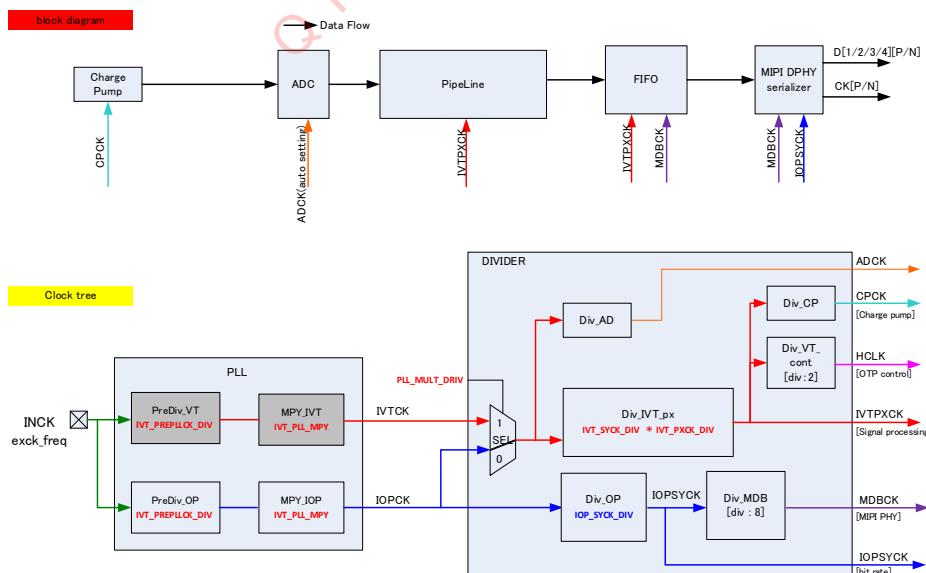
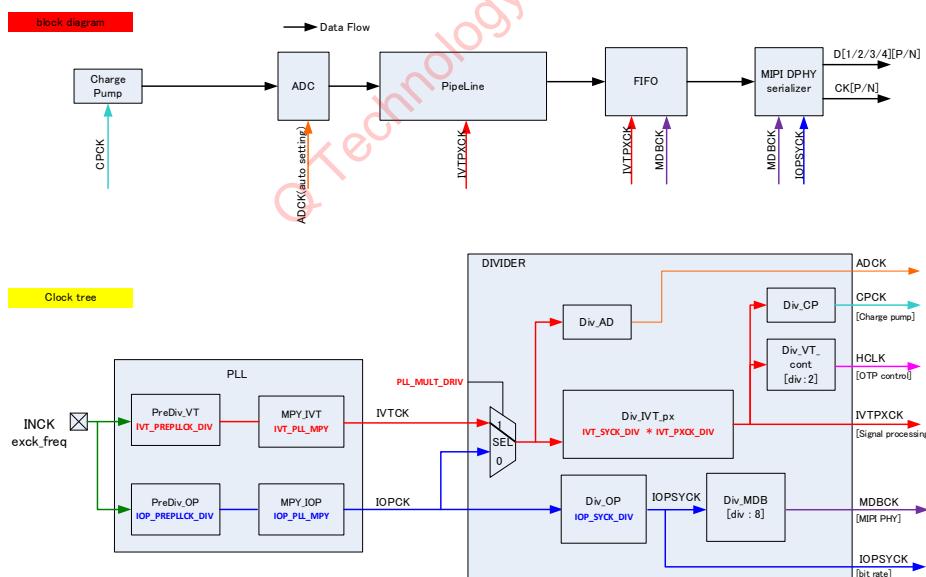


Figure 5-1 Clock system diagram (PLL single mode)

**Table 5-1 PLL pre divider & multiplier setting (PLL single mode)**

<sup>I<sup>2</sup>C register</sup>	Address	Bit	Name	Description	Setting constraint
	0x0305	[3:0]	IVT_PREPLLCK_DIV	The pre-PLL Clock Divider for Internal Video Timing System Clock Range : 1 to 4 Step : 1 Format : 4-bit unsigned integer *Setup other than the above is forbidden.	INCK / IVT_PREPLLCK_DIV = 6 to 12 MHz
	0x0306	[2:0]	IVT_PLL_MPY[10:8]	The PLL multiplier for Internal Video Timing System Clock Range : 29 to 290 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.	IVTCK & IOPCK = 338 to 1740 MHz
	0x0307	[7:0]	IVT_PLL_MPY[7:0]		

\*IOP\_PREPLLCK\_DIV and IOP\_PLL\_MPY are ignored

**Figure 5-2 Clock system diagram (PLL dual mode)**

**Table 5-2 PLL pre divider & multiplier setting (PLL dual mode)**

	Address	Bit	Name	Description	Setting constraint
I <sup>2</sup> C register	0x0305	[3:0]	IVT_PREPLLCK_DIV	The pre-PLL Clock Divider for Internal Video Timing System Clock Range : 1 to 4 Step : 1 Format : 4-bit unsigned integer *Setup other than the above is forbidden.	INCK / IVT_PREPLLCK_DIV = 6 to 12 MHz
	0x030d	[3:0]	IOP_PREPLLCK_DIV	The pre-PLL Clock Divider for Internal Output Pixel System during "Dual PLL mode" (PLL_MULT_DRIV=1). Range : 1 to 15 Step : 1 Format : 4-bit unsigned integer *Setup other than the above is forbidden.	INCK / IOP_PREPLLCK_DIV = 1 to 12 MHz
	0x0306	[2:0]	IVT_PLL_MPY [10:8]	The PLL multiplier for Internal Video Timing System Clock Range : 29 to 290 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.	IVTCK = 338 to 1740 MHz
	0x0307	[7:0]	IVT_PLL_MPY [7:0]	The PLL multiplier for Internal Output Pixel System "Dual PLL mode" (PLL_MULT_DRIV=1). Range : 29 to 1840 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.	IOPCK = 338 to 1840 MHz
	0x030e	[2:0]	IOP_PLL_MPY [10:8]		
	0x030f	[7:0]	IOP_PLL_MPY [7:0]		

**Table 5-3 PLL mode select**

<sup>I<sup>2</sup>C register</sup>	Address	Bit	Name	Description	Notes
	0x0310	[0]	PLL_MULT_DRIV	PLL mode select 0 : Single PLL mode 1 : Dual PLL mode	

### 5.1.1.1. INCK

INCK is the base of all clock system which shall be applied by external camera system.

INCK shall be in the range of 6 to 27 MHz

**Table 5-4 INCK Frequency setting**

<sup>I<sup>2</sup>C register</sup>	Address	Bit	Name	Description	Setting constraint
	0x0136	[7:0]	EXCK_FREQ[15:8]	External clock(INCK) frequency [MHz] Bit[15:8] integer	=INT(INCK[MHz] * 256)
	0x0137	[7:0]	EXCK_FREQ[7:0]	Bit[7:0] decimal	

### 5.1.2. Sensor internal operation clocks

These clocks are the root of all the operation clocks in this sensor and it designates the data rate.

#### 5.1.2.1. IVTCK, IOPCK: PLL output(PLL single mode)

$$IOPCK = INCK \text{ frequency} \times \text{PreDivider setting} \times \text{PLL multiple setting}$$

$$* \text{PreDivider setting} = 1 / \text{IVT\_PREPLLCK\_DIV}$$

$$* \text{PLL multiple setting} = \text{IVT\_PLL\_MPY}$$

$$IVTCK = IOPCK$$

$$CKP, CKN = IOPCK \times \text{CSI2 divide} \times (1 / \text{IOP\_SYCK\_DIV})$$

$$* \text{CSI2 divide} = 1/2$$

#### 5.1.2.2. IVTCK, IOPCK: PLL output (PLL dual mode)

$$IVTCK = INCK \text{ frequency} \times \text{PreDivider setting} \times \text{PLL multiple setting}$$

$$* \text{PreDivider setting} = 1 / \text{IVT\_PREPLLCK\_DIV}$$

$$* \text{PLL multiple setting} = \text{IVT\_PLL\_MPY}$$

$$IOPCK = INCK \text{ frequency} \times \text{PreDivider setting} \times \text{PLL multiple setting}$$

$$* \text{PreDivider setting} = 1 / \text{IOP\_PREPLLCK\_DIV}$$

\* PLL multiple setting = IOP\_PLL\_MPY

**CKP, CKN** = IOPCK × CSI2 divide × (1/ IOP\_SYCK\_DIV)

\* CSI2 divide = 1/2

### 5.1.2.3. Clock frequency configuration examples

**Table 5-5 PLL frequency table IVTCK (include PLL single mode)**

CLK	Input Clock (INCK)	Pre division	PLL Input frequency	Multiple	PLL Oscillation frequency
IVTCK	6 MHz	1	6.0 MHz	57	342.0 MHz
				166	996.0 MHz
				250	1500.0 MHz
				290	1740.0 MHz
	12 MHz	2	6.0 MHz	57	342.0 MHz
				166	996.0 MHz
				250	1500.0 MHz
				290	1740.0 MHz
	13.5 MHz	2	6.75 MHz	51	344.25 MHz
				148	999.00 MHz
				222	1498.50 MHz
				257	1734.75 MHz
	18 MHz	3	6.0 MHz	57	342.0 MHz
				166	996.0 MHz
				250	1500.0 MHz
				290	1740.0 MHz
	24 MHz	4	6.0 MHz	57	342.0 MHz
				166	996.0 MHz
				250	1500.0 MHz
				290	1740.0 MHz
	27 MHz	4	6.75 MHz	51	344.25 MHz
				148	999.00 MHz
				222	1498.50 MHz
				257	1734.75 MHz

**Table 5-6 PLL frequency table IOPCK**

CLK	Input Clock (INCK)	Pre division	PLL Input frequency	Multiple	PLL Oscillation frequency
IOPCK	6 MHz	6	1.0 MHz	338	338.0 MHz
				1000	1000.0 MHz
				1500	1500.0 MHz
				1840	1840.0 MHz
	12 MHz	12	1.0 MHz	338	338.0 MHz
				1000	1000.0 MHz
				1500	1500.0 MHz
				1840	1840.0 MHz
	13.5 MHz	12	1.125 MHz	301	338.625 MHz
				888	999.00 MHz
				1333	1499.625 MHz
				1635	1839.375 MHz
	18 MHz	15	1.2 MHz	282	338.4 MHz
				833	999.6 MHz
				1250	1500.0 MHz
				1533	1839.6 MHz
	24 MHz	12	2.0 MHz	169	338.0 MHz
				500	1000.0 MHz
				750	1500.0 MHz
				920	1840.0 MHz
	27 MHz	15	1.8 MHz	188	338.4 MHz
				555	999.0 MHz
				833	1499.4 MHz
				1022	1839.6 MHz

### 5.1.3. IVTPXCK Clock

The clock for internal image processing is generated by dividing IVTCK into 1/10 or 1/20 frequency.

This clock is used as the base of integration time, frame rate, etc.

$$\text{IVTPXCK clock frequency} = \text{IVTCK} \times \text{IVTPXCK clock division ratio}$$

$$* \text{IVTPXCK clock division ratio} = 1 / (\text{IVT\_SYCK\_DIV} * \text{IVT\_PXCK\_DIV})$$

**Table 5-7 IVTPXCK divider setting**

I <sup>2</sup> C register	Address	Bit	Name	Description	Notes
	0x0303	[2:0]	IVT_SYCK_DIV	The System Clock Divider for Internal Video Timing System Range : 2, 4 Format : 3-bit unsigned integer *Setup other than the above is forbidden.	
	0x0301	[4:0]	IVT_PXCK_DIV	The Pixel Clock Divider for Internal Video Timing System Range : 6 Format : 5-bit unsigned integer *Setup other than the above is forbidden.	

**5.1.4. IOPSYCK Clock**

The clock for internal image processing is generated by dividing IOPCK into 1/1, 1/2 or 1/4 frequency according to the word length of the CSI2 interface. This clock designates the pixel rate etc.

IOPSYCK clock frequency = IOPCK × *IOPSYCK clock division ratio*

\* *IOPSYCK clock division ratio* = 1 / (IOP\_SYCK\_DIV)

**Table 5-8 IOPSYCK divider setting**

I <sup>2</sup> C register	Address	Bit	Name	Description	Notes
	0x030b	[4:0]	IOP_SYCK_DIV	The System Clock Divider for Internal Output Pixel System Range : 1, 2, 4 Format : 2-bit unsigned integer *Setup other than the above is forbidden.	

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**Table 5-9 IOPSYCK frequency table**

CLK	IOPCK frequency	IOP_SYCK_DIV	IOPSYCK frequency
IOPSYCK	338MHz~1840MHz	1	338MHz - 1840MHz
		2	220MHz - 920MHz
		4	220MHz - 460MHz

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## 5.2. Description of mode operation

Main modes of this sensor are Full resolution, 2x2 Adjacent Pixel Binning mode (HV:1/2).

### 5.2.1. Image size related settings

This sensor can output full size and/or re-sized (shrunk) images. Examples are shown in the table below.

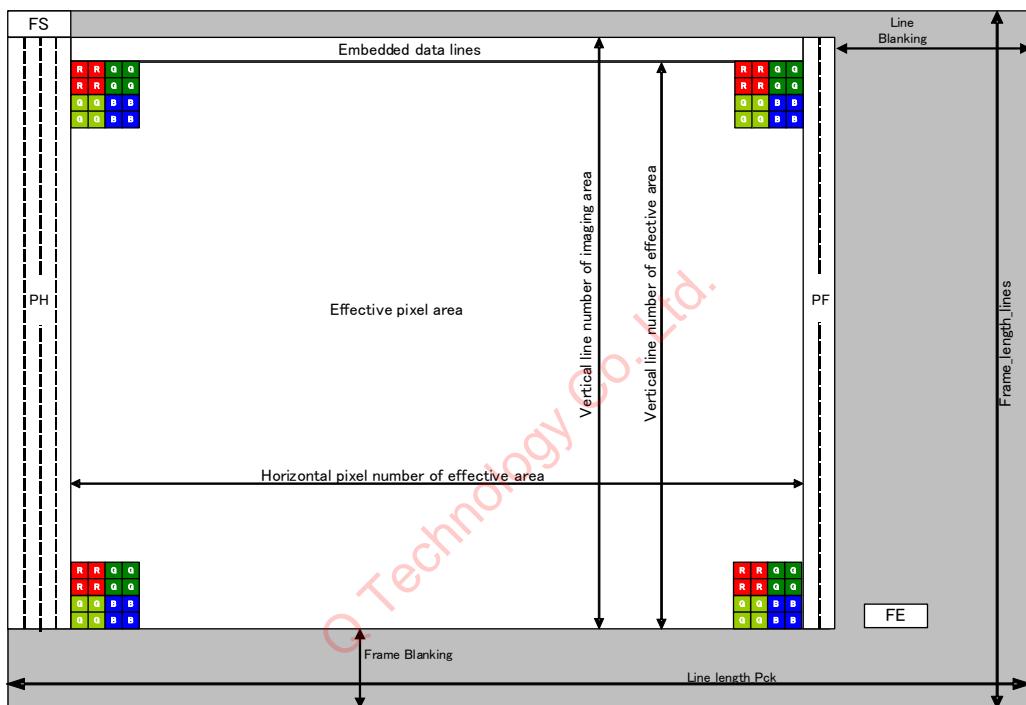


Figure 5-3 Image size parameter definition

**Table 5-10 Typical image output of main capture modes (1)**

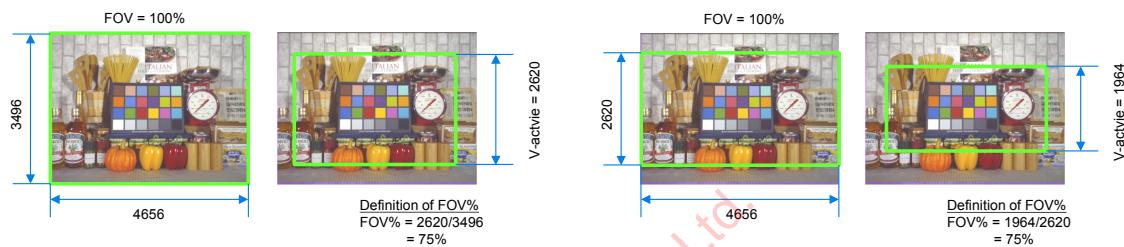
	Modes			
	Full-pixel		2x2 Adjacent Pixel Binning (V:1/2, H:1/2)	
Number of vertical lines in imaging area	3496		1748	
Number of horizontal pixels in effective area	4656		2328	
Number of lines and start position	Start position	Number of lines	Start position	Number of lines
Frame start	1	1	1	1
Embedded data lines	2	2	2	2
Number of vertical pixels in effective area	4	3496	4	1748
Frame end	3500	1	1752	1

**Table 5-11 Typical image output of main capture modes (2)**

	Modes		
	Full-pixel	2x2 Adjacent Pixel Binning	1080p
VT/OP	1.0 :1.0	1.0 :1.0	1.0 :1.0
Cropping	Non(4:3)	Non(4:3)	Vcrop(16:9)
Sub-sampling	Non	Non	Non
Binning	Non	H/V	H/V
Scaling	Non	Non	Non
H Pixels	4656	2328	2328
V Pixels	3496	1748	1304
Frame Rate	30fps	120fps	150fps
Bit Rate	1740Mbps	1740Mbps	1740Mbps
FOV			
Output			

**Table 5-12 FOV% vs FPS(Crop)**

Binning	Aspect ratio	FOV %	Actual RAW size	Scaling (V)	Scaling (H)	Max. FPS
No(Full)	4:3	100	4656 x 3496	No	No	30
		75	3492 x 2620	No	No	40
		50	2328 x 1748	No	No	60
		33	1536 x 1152	No	No	90
		16	744 x 556	No	No	170
	16:9	100	4656 x 2620	No	No	40
		75	3492 x 1964	No	No	50
		50	2328 x 1308	No	No	80
		33	1536 x 864	No	No	110
		16	744 x 416	No	No	210



Note: H-Analog Crop is prohibited.

The following table shows the setting list for the supporting operation modes of capture mode.

Other settings are not supported in this sensor.

**Table 5-13 Support list of operation mode of capture mode**

Operation mode	BINNING setting				Sub-sampling setting			
	0x0900 [0]	0x0901 [7:0]	0x3F4C [7:0]	0x3F4D [7:0]	0x0381 [2:0]	0x0383 [2:0]	0x0385 [3:0]	0x0387 [3:0]
Full Resolution	0x0	x	0x01	0x01	0x1	0x1	0x1	0x1
2x2 Adjacent Pixel Binning	0x1	0x22	0x81	0x81				

Note \*1: X\_EVN\_INC and X\_ODD\_INC are fix value (1) in this sensor

### 5.2.2. Normal capture mode settings (full and binning mode)

Register settings for Binning mode are as follows.

**Table 5-14 Normal capture mode settings (full and binning mode)**

	Address	Bit	Name	Description
<sup>I<sup>2</sup>C register</sup>	0x0900	[0]	BINNING_MODE	Binning enable control 0=None 1=Enable
	0x0901	[7:4]	BINNING_TYPE_H[3:0]	BINNING_TYPE_H : Binning type selection for Horizontal 1 : no binning 2 : 2x2 Adjacent Pixel Binning * Setup other than the above is forbidden.
	0x0901	[3:0]	BINNING_TYPE_V[3:0]	BINNING_TYPE_V : Binning type selection for Vertical 1 : no binning 2 : 2x2 Adjacent Pixel Binning * Setup other than the above is forbidden
	0x0902	[7:0]	BINNING_WEIGHTING[7:0] <sup>*1</sup>	Bit[1:0] Binning type selection 0 : Averaged 1 : Summed * Setup other than the above is forbidden. Bit [7:2] : 6'b000010 Fixed See Table 5-31 Output pixel level according to binning modes
	0x3F4C	[7:0]	BINNING_PRIORITY_V[7:0]	Bit[0] : must be set 1 Bit [6:1]: Reserved Bit[7] : Binning options for Vertical 0 : No binning 1 : Adjacent pixel binning * Setup other than the above is forbidden.
	0x3F4D	[7:0]	BINNING_PRIORITY_H[7:0]	Bit[0] : must be set 1 Bit [6:1]: Reserved Bit[7] : Binning options for Horizontal 0 : No binning 1 : Adjacent pixel binning * Setup other than the above is forbidden.

Note \*1: See 5.5.3 for the description of BINNING\_WEIGHTING [7:0]

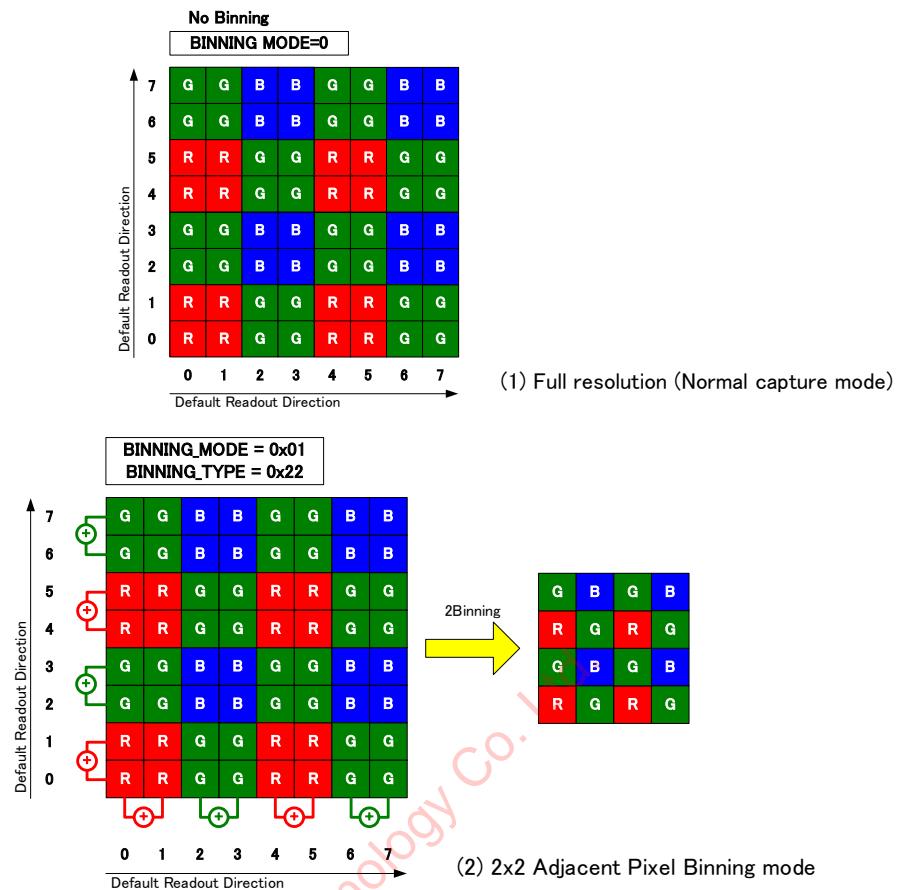


Figure 5-4 Binning mode image

### 5.2.3. Image size related functions

The relationships of image output size and the registers are shown below.

In this sensor, Horizontal analog cropping is prohibited.

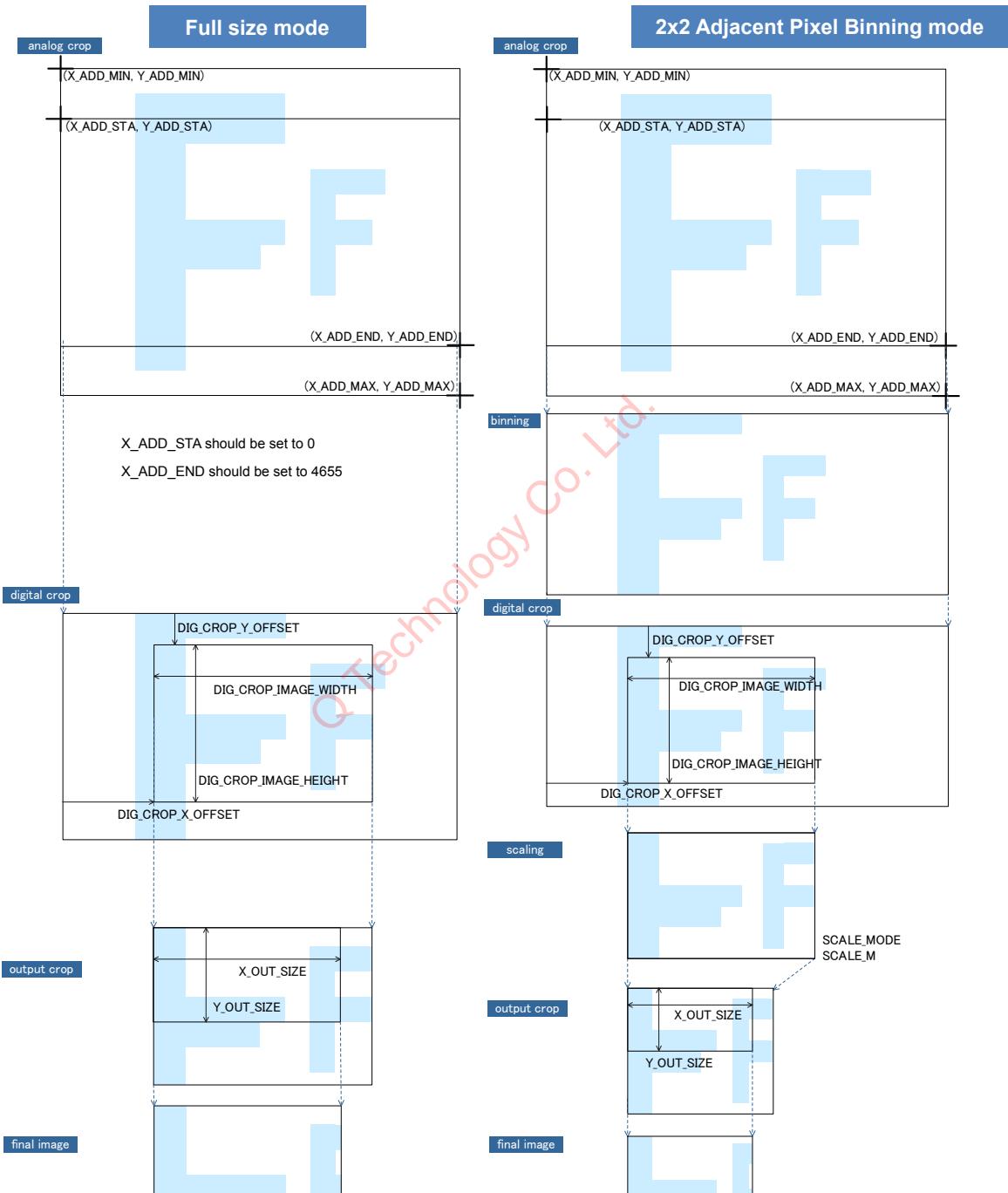


Figure 5-5 Image size related functions

### Analog crop

Please refer to “4.3 Imaging area determination”.

In this sensor, Horizontal analog cropping is prohibited.

### Binning

Settings and see 5.2.2 Normal capture mode settings (full and binning mode) for details.

### Digital crop

Digital crop is processed after image readout operation or in order of [Analog crop → Binning → Digital crop] and is common for Normal capture mode. The crop size (DIG\_CROP\_IMAGE\_WIDTH and DIG\_CROP\_IMAGE\_HEIGHT) must always be set properly even if cropping is not used.

**Table 5-15 Digital crop setting**

I <sup>2</sup> C register	Address	Bit	Name	Description
	0x0408	[4:0]	DIG_CROP_X_OFFSET[12:8]	Offset from X_ADD_STA after binning and Sub-sampling
	0x0409	[7:0]	DIG_CROP_X_OFFSET[7:0]	
	0x040a	[3:0]	DIG_CROP_Y_OFFSET[11:8]	Offset from Y_ADD_STA after binning and Sub-sampling
	0x040b	[7:0]	DIG_CROP_Y_OFFSET[7:0]	
	0x040c	[4:0]	DIG_CROP_IMAGE_WIDTH[12:8] * <sup>1</sup>	Image width after digital cropping
	0x040d	[7:0]	DIG_CROP_IMAGE_WIDTH[7:0] * <sup>1</sup>	Unit : pixels
	0x040e	[3:0]	DIG_CROP_IMAGE_HEIGHT[11:8] * <sup>1</sup>	Image height after digital cropping
	0x040f	[7:0]	DIG_CROP_IMAGE_HEIGHT[7:0] * <sup>1</sup>	Unit : lines

Note \*1: (DIG\_CROP\_IMAGE\_WIDTH and DIG\_CROP\_IMAGE\_HEIGHT) must always be set properly even if cropping is not used.

## Output crop

The width and height of the visible pixel area within the frame of data output from the sensor can be programmed by the “X\_OUT\_SIZE” and “Y\_OUT\_SIZE”.

Note that this function does not have “offset” setting just not like as Digital Crop’s Offset capability. So, the picture will not centered any more if the output size is trimmed with Out Crop function.

**Table 5-16 Output crop setting**

I <sup>2</sup> C register	Address	Bit	Name	Description
	0x034c	[4:0]	X_OUT_SIZE[12:8]	The sensor output size of horizontal Unit : pixels (multiple of 4)
	0x034d	[7:0]	X_OUT_SIZE[7:0]	
	0x034e	[4:0]	Y_OUT_SIZE[11:8]	The sensor output size of vertical Unit : lines (multiple of 4)
	0x034f	[7:0]	Y_OUT_SIZE[7:0]	

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### 5.3. Frame rate calculation formula

The frame rate of the output image of this sensor can be calculated by the formula below.

$$\text{Frame Rate [frame/s]} = \text{Pixel\_rate [pixels/s]} / \text{Total number of pixels [pixels/frame]}$$

$$\text{Pixel rate [pixels/s]} = \text{IVTPXCK [MHz]} * 4 \text{ (Total number of IVTPX channel)}$$

$$\text{Total number of pixels [pixels/frame]}$$

$$= \text{FRM\_LENGTH\_LINES [lines/frame]} * \text{LINE\_LENGTH\_PCK [pixels/line]}$$

See 5.1.3 for the calculation formula for IVTPXCK.

See 5.1.4 for the descriptions of registers used for the calculation formula.

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## 5.4. Electronic shutter and integration time settings

### 5.4.1. Registers related to integration time (electronic shutter setting)

The integration time setting registers are shown below.

**Table 5-17 Electronic shutter setting register**

I <sup>2</sup> C register	Address	Bit	Name	Description	Notes
	0x0202	[7:0]	COARSE_INTEG_TIME[15:8]	Coarse storage time Unit : lines Format : 16-bit unsigned integer	
	0x0203	[7:0]	COARSE_INTEG_TIME[7:0]		

**Table 5-18 Integration time setting register**

I <sup>2</sup> C register	Address	Bit	Name	Description	Notes
	0x0200	[7:0]	FINE_INTEG_TIME[15:8]	Fine storage time Unit : pixels Format : 16-bit unsigned integer	Read only
	0x0201	[7:0]	FINE_INTEG_TIME[7:0]		
	0x0342	[7:0]	LINE_LENGTH_PCK[15:8]	The length of line Unit : pixels Format : 16-bit unsigned integer	*LINE_LENGTH_PCK Has been constrained. * Must be set fixed value as Table4-5.
	0x0343	[7:0]	LINE_LENGTH_PCK[7:0]		
	0x0350	[0]	FRM_LENGTH_CTL	Frame length automatic tracking control Select whether or not the frame length is changed automatically when FRM_LENGTH_LINES < COARSE_INTEG_TIME + $\alpha$ ( $\alpha$ = type-specific adjustment parameter, and is 18(d) for this type) 0 : no automatic tracking control of frame length 1 : automatic tracking control of frame length In this case, "COARSE_INTEG_TIME + $\alpha$ " operates instead of FRM_LENGTH_LINES	1(default)

### 5.4.2. Integration time calculation

The integration time or shutter time( $T_{SH}$ ) can be obtained from the following relational equation.

$T_{line} = \text{LINE\_LENGTH\_PCK} \text{ [pixels/line]} * \text{IVTPXCK\_period} / 4$  (*Total number of image pipe lines*)

$T_{sh} = T_{line} * (\text{COARSE\_INTEG\_TIME} \text{ [lines]} + \text{FINE\_INTEG\_TIME} \text{ [pixels]} / \text{LINE\_LENGTH\_PCK} \text{ [pixels/line]})$

This relationship stands up regardless of the operating mode; full pixel mode, binning modes, Sub-sampling mode or combination of Sub-sampling and binning mode.

Settings and storage times are shown below.

\* FINE\_INTEG\_TIME is a fixed value.

To set exposure time longer than “FRM\_LENGTH\_LINES”, you can either automatically extend it with the setting FRM\_LENGTH\_CTL=1 or perform truncation by frame length with the setting FRM\_LENGTH\_CTL = 0.

**Table 5-19 Integration time setting  
(In case of FRM\_LENGTH\_CTL=0)**

Parameter Setting		Frame time / Integration Time	
FRM_LENGTH_LINES [15:0]	COARSE_INTEG_TIME [15:0]	Frame time	Integration time (Tline stands for the duration of one line)
M	1	prohibited	
	...	prohibited	
	3	prohibited	
	4	M Tline	(4+ $\alpha$ )Tline
	...		
	M-18		((M-18)+ $\alpha$ )Tline
	(M-17) ~	prohibited	

\* $\alpha$ =FINE\_INTEG\_TIME/LINE\_LENGTH\_PCK

\* M: set value for given capture mode <= 65534

**Table 5-20 Integration time setting  
(In case of FRM\_LENGTH\_CTL=1)**

Parameter Setting		Frame time / Integration Time	
FRM_LENGTH_LINES [15:0]	COARSE_INTEG_TIME [15:0]	Frame time	Integration time (H stands for the duration of one line)
M	1	prohibited	
	...	prohibited	
	3	prohibited	
	4	M Tline	(4+ $\alpha$ ) Tline
	...		...
	M-18		((M-18)+ $\alpha$ ) Tline
	M-17	(M+1) Tline	((M-17)+ $\alpha$ ) Tline
	M-16	(M+2) Tline	((M-16)+ $\alpha$ ) Tline
	...	...	...
	N	(N+18) Tline	( N + $\alpha$ ) Tline

\* $\alpha$ =FINE\_INTEG\_TIME/LINE\_LENGTH\_PCK

\* M: set value for given capture mode <= 65534

\* N: can be set with values greater than M <= 65516

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## 5.5. Gain setting

This sensor can apply analog gain on photo-electron signal and digital gain on digital signal after ADC.

Range of settable range is as follows.

**Table 5-21 Range of Gains**

	Max.	Note
Analog Gain	24dB	Normal ADC mode
Digital Gain	24dB	Functionally Settable

### 5.5.1. Analog gain settings

The formula for analog gain is shown below.

Analog gain parameters are set with registers. Analog gain and digital gain are set separately.

$$\text{Analog Gain} = (m0 \times X + c0) / (m1 \times X + c1)$$

The variables of above equation are specified in the table below.

**Table 5-22 Variables of analog gain settings**

<sup>I<sup>2</sup>C</sup> register	Address	Bit	Name	Description	Notes
	0x008c	[7:0]	ANA_GAIN_M0 [15:8]	m0: fixed to 0	Read only static
	0x008d	[7:0]	ANA_GAIN_M0 [7:0]		
	0x0090	[7:0]	ANA_GAIN_M1 [15:8]	m1: fixed to -1	Read only static
	0x0091	[7:0]	ANA_GAIN_M1 [7:0]		
	0x008e	[7:0]	ANA_GAIN_C0 [15:8]	c0: fixed to 1024	Read only static
	0x008f	[7:0]	ANA_GAIN_C0 [7:0]		
	0x0092	[7:0]	ANA_GAIN_C1 [15:8]	c1: fixed to 1024	Read only static
	0x0093	[7:0]	ANA_GAIN_C1 [7:0]		
	0x0204	[1:0]	ANA_GAIN_GLOBAL [9:8]	X: Analog gain setting value	0 to 960
	0x0205	[7:0]	ANA_GAIN_GLOBAL [7:0]		

As a result, analog gain is calculated by the formula below.

$$\text{Analog Gain} = 1024 / (1024 - X)$$

The relationship between the setting values X of ANA\_GAIN\_GLOBAL and the gain is shown in the following table. The ANA\_GAIN\_GLOBAL value is normally set in the range from 0 to 960 [0 dB to 24 dB].

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**Table 5-23 Analog gain setting reference [0 to 159]**

ana_gain_global	Gain(times)	Gain(dB)
0	1.000	0.000
1	1.001	0.008
2	1.002	0.017
3	1.003	0.025
4	1.004	0.034
5	1.005	0.043
6	1.006	0.051
7	1.007	0.060
8	1.008	0.068
9	1.009	0.077
10	1.010	0.085
11	1.011	0.094
12	1.012	0.102
13	1.013	0.111
14	1.014	0.120
15	1.015	0.128
16	1.016	0.137
17	1.017	0.145
18	1.018	0.154
19	1.019	0.163
20	1.020	0.171
21	1.021	0.180
22	1.022	0.189
23	1.023	0.197
24	1.024	0.206
25	1.025	0.215
26	1.026	0.223
27	1.027	0.232
28	1.028	0.241
29	1.029	0.250
30	1.030	0.258
31	1.031	0.267
32	1.032	0.276
33	1.033	0.285
34	1.034	0.293
35	1.035	0.302
36	1.036	0.311
37	1.037	0.320
38	1.039	0.328
39	1.040	0.337
40	1.041	0.346
41	1.042	0.355
42	1.043	0.364
43	1.044	0.373
44	1.045	0.381
45	1.046	0.390
46	1.047	0.399
47	1.048	0.408
48	1.049	0.417
49	1.050	0.426
50	1.051	0.435
51	1.052	0.444
52	1.053	0.453
53	1.055	0.462
54	1.056	0.471
55	1.057	0.480
56	1.058	0.488
57	1.059	0.497
58	1.060	0.506
59	1.061	0.515
60	1.062	0.524
61	1.063	0.533
62	1.064	0.542
63	1.066	0.552
64	1.067	0.561
65	1.068	0.570
66	1.069	0.579
67	1.070	0.588
68	1.071	0.597
69	1.072	0.606
70	1.073	0.615
71	1.075	0.624
72	1.076	0.633
73	1.077	0.642
74	1.078	0.652
75	1.079	0.661
76	1.080	0.670
77	1.081	0.679
78	1.082	0.688
79	1.084	0.697
80	1.085	0.707
81	1.086	0.716
82	1.087	0.725
83	1.088	0.734
84	1.089	0.743
85	1.091	0.753
86	1.092	0.762
87	1.093	0.771
88	1.094	0.780
89	1.095	0.790
90	1.096	0.799
91	1.098	0.808
92	1.099	0.818
93	1.100	0.827
94	1.101	0.836
95	1.102	0.846
96	1.103	0.855
97	1.105	0.864
98	1.106	0.874
99	1.107	0.883
100	1.108	0.893
101	1.109	0.902
102	1.111	0.911
103	1.112	0.921
104	1.113	0.930
105	1.114	0.940
106	1.115	0.949
107	1.117	0.959
108	1.118	0.968
109	1.119	0.978
110	1.120	0.987
111	1.122	0.997
112	1.123	1.006
113	1.124	1.016
114	1.125	1.025
115	1.127	1.035
116	1.128	1.044
117	1.129	1.054
118	1.130	1.063
119	1.131	1.073
120	1.133	1.083
121	1.134	1.092
122	1.135	1.102
123	1.137	1.112
124	1.138	1.121
125	1.139	1.131
126	1.140	1.140
127	1.142	1.150
128	1.143	1.160
129	1.144	1.170
130	1.145	1.179
131	1.147	1.189
132	1.148	1.199
133	1.149	1.208
134	1.151	1.218
135	1.152	1.228
136	1.153	1.238
137	1.154	1.248
138	1.156	1.257
139	1.157	1.267
140	1.158	1.277
141	1.160	1.287
142	1.161	1.297
143	1.162	1.306
144	1.164	1.316
145	1.165	1.326
146	1.166	1.336
147	1.168	1.346
148	1.169	1.356
149	1.170	1.366
150	1.172	1.376
151	1.173	1.386
152	1.174	1.396
153	1.176	1.406
154	1.177	1.416
155	1.178	1.426
156	1.180	1.436
157	1.181	1.446
158	1.182	1.456
159	1.184	1.466

**Table 5-24 Analog gain setting reference [160 to 319]**

ana_gain_global	Gain(times)	Gain(dB)
160	1.185	1.476
161	1.187	1.486
162	1.188	1.496
163	1.189	1.506
164	1.191	1.516
165	1.192	1.526
166	1.193	1.536
167	1.195	1.546
168	1.196	1.557
169	1.198	1.567
170	1.199	1.577
171	1.200	1.587
172	1.202	1.597
173	1.203	1.607
174	1.205	1.618
175	1.206	1.628
176	1.208	1.638
177	1.209	1.648
178	1.210	1.659
179	1.212	1.669
180	1.213	1.679
181	1.215	1.689
182	1.216	1.700
183	1.218	1.710
184	1.219	1.720
185	1.221	1.731
186	1.222	1.741
187	1.223	1.751
188	1.225	1.762
189	1.226	1.772
190	1.228	1.783
191	1.229	1.793
192	1.231	1.804
193	1.232	1.814
194	1.234	1.824
195	1.235	1.835
196	1.237	1.845
197	1.238	1.856
198	1.240	1.866
199	1.241	1.877
200	1.243	1.887
201	1.244	1.898
202	1.246	1.909
203	1.247	1.919
204	1.249	1.930
205	1.250	1.940
206	1.252	1.951
207	1.253	1.962
208	1.255	1.972
209	1.256	1.983
210	1.258	1.994
211	1.260	2.004
212	1.261	2.015
213	1.263	2.026
214	1.264	2.036
215	1.266	2.047
216	1.267	2.058
217	1.269	2.069
218	1.270	2.079
219	1.272	2.090
220	1.274	2.101
221	1.275	2.112
222	1.277	2.123
223	1.278	2.133
224	1.280	2.144
225	1.282	2.155
226	1.283	2.166
227	1.285	2.177
228	1.286	2.188
229	1.288	2.199
230	1.290	2.210
231	1.291	2.221
232	1.293	2.231
233	1.295	2.242
234	1.296	2.253
235	1.298	2.264
236	1.299	2.275
237	1.301	2.287
238	1.303	2.298
239	1.304	2.309
240	1.306	2.320
241	1.308	2.331
242	1.309	2.342
243	1.311	2.353
244	1.313	2.364
245	1.315	2.375
246	1.316	2.386
247	1.318	2.398
248	1.320	2.409
249	1.321	2.420
250	1.323	2.431
251	1.325	2.442
252	1.326	2.454
253	1.328	2.465
254	1.330	2.476
255	1.332	2.487
256	1.333	2.499
257	1.335	2.510
258	1.337	2.521
259	1.339	2.533
260	1.340	2.544
261	1.342	2.556
262	1.344	2.567
263	1.346	2.578
264	1.347	2.590
265	1.349	2.601
266	1.351	2.613
267	1.353	2.624
268	1.354	2.636
269	1.356	2.647
270	1.358	2.659
271	1.360	2.670
272	1.362	2.682
273	1.364	2.693
274	1.365	2.705
275	1.367	2.716
276	1.369	2.728
277	1.371	2.740
278	1.373	2.751
279	1.374	2.763
280	1.376	2.775
281	1.378	2.786
282	1.380	2.798
283	1.382	2.810
284	1.384	2.821
285	1.386	2.833
286	1.388	2.845
287	1.389	2.857
288	1.391	2.868
289	1.393	2.880
290	1.395	2.892
291	1.397	2.904
292	1.399	2.916
293	1.401	2.928
294	1.403	2.940
295	1.405	2.951
296	1.407	2.963
297	1.409	2.975
298	1.410	2.987
299	1.412	2.999
300	1.414	3.011
301	1.416	3.023
302	1.418	3.035
303	1.420	3.047
304	1.422	3.059
305	1.424	3.071
306	1.426	3.084
307	1.428	3.096
308	1.430	3.108
309	1.432	3.120
310	1.434	3.132
311	1.436	3.144
312	1.438	3.156
313	1.440	3.169
314	1.442	3.181
315	1.444	3.193
316	1.446	3.205
317	1.448	3.218
318	1.450	3.230
319	1.452	3.242

**Table 5-25 Analog gain setting reference [320 to 479]**

<b>ana_gain_global</b>	<b>Gain(times)</b>	<b>Gain(dB)</b>									
320	1.455	3.255	360	1.542	3.763	400	1.641	4.302	440	1.753	4.878
321	1.457	3.267	361	1.544	3.776	401	1.644	4.316	441	1.756	4.893
322	1.459	3.279	362	1.547	3.789	402	1.646	4.330	442	1.759	4.908
323	1.461	3.292	363	1.549	3.802	403	1.649	4.344	443	1.762	4.922
324	1.463	3.304	364	1.552	3.815	404	1.652	4.358	444	1.766	4.937
325	1.465	3.316	365	1.554	3.828	405	1.654	4.372	445	1.769	4.952
326	1.467	3.329	366	1.556	3.841	406	1.657	4.386	446	1.772	4.967
327	1.469	3.341	367	1.559	3.855	407	1.660	4.400	447	1.775	4.982
328	1.471	3.354	368	1.561	3.868	408	1.662	4.414	448	1.778	4.998
329	1.473	3.366	369	1.563	3.881	409	1.665	4.428	449	1.781	5.013
330	1.476	3.379	370	1.566	3.894	410	1.668	4.443	450	1.784	5.028
331	1.478	3.391	371	1.568	3.908	411	1.670	4.457	451	1.787	5.043
332	1.480	3.404	372	1.571	3.921	412	1.673	4.471	452	1.790	5.058
333	1.482	3.416	373	1.573	3.934	413	1.676	4.485	453	1.793	5.073
334	1.484	3.429	374	1.575	3.948	414	1.679	4.499	454	1.796	5.089
335	1.486	3.442	375	1.578	3.961	415	1.681	4.514	455	1.800	5.104
336	1.488	3.454	376	1.580	3.974	416	1.684	4.528	456	1.803	5.119
337	1.491	3.467	377	1.583	3.988	417	1.687	4.542	457	1.806	5.134
338	1.493	3.480	378	1.585	4.001	418	1.690	4.557	458	1.809	5.150
339	1.495	3.492	379	1.588	4.015	419	1.693	4.571	459	1.812	5.165
340	1.497	3.505	380	1.590	4.028	420	1.695	4.585	460	1.816	5.180
341	1.499	3.518	381	1.593	4.042	421	1.698	4.600	461	1.819	5.196
342	1.501	3.530	382	1.595	4.055	422	1.701	4.614	462	1.822	5.211
343	1.504	3.543	383	1.598	4.069	423	1.704	4.629	463	1.825	5.227
344	1.506	3.556	384	1.600	4.082	424	1.707	4.643	464	1.829	5.242
345	1.508	3.569	385	1.603	4.096	425	1.710	4.657	465	1.832	5.258
346	1.510	3.581	386	1.605	4.110	426	1.712	4.672	466	1.835	5.273
347	1.513	3.594	387	1.608	4.123	427	1.715	4.687	467	1.838	5.289
348	1.515	3.607	388	1.610	4.137	428	1.718	4.701	468	1.842	5.305
349	1.517	3.620	389	1.613	4.151	429	1.721	4.716	469	1.845	5.320
350	1.519	3.633	390	1.615	4.164	430	1.724	4.730	470	1.848	5.336
351	1.522	3.646	391	1.618	4.178	431	1.727	4.745	471	1.852	5.351
352	1.524	3.659	392	1.620	4.192	432	1.730	4.760	472	1.855	5.367
353	1.526	3.672	393	1.623	4.205	433	1.733	4.774	473	1.858	5.383
354	1.528	3.685	394	1.625	4.219	434	1.736	4.789	474	1.862	5.399
355	1.531	3.697	395	1.628	4.233	435	1.739	4.804	475	1.865	5.415
356	1.533	3.710	396	1.631	4.247	436	1.741	4.818	476	1.869	5.430
357	1.535	3.723	397	1.633	4.261	437	1.744	4.833	477	1.872	5.446
358	1.538	3.737	398	1.636	4.275	438	1.747	4.848	478	1.875	5.462
359	1.540	3.750	399	1.638	4.288	439	1.750	4.863	479	1.879	5.478

**Table 5-26 Analog gain setting reference [480 to 639]**

ana_gain_global	Gain(times)	Gain(dB)
480	1.882	5.494
481	1.886	5.510
482	1.889	5.526
483	1.893	5.542
484	1.896	5.558
485	1.900	5.574
486	1.903	5.590
487	1.907	5.607
488	1.910	5.623
489	1.914	5.639
490	1.918	5.655
491	1.921	5.671
492	1.925	5.688
493	1.928	5.704
494	1.932	5.720
495	1.936	5.737
496	1.939	5.753
497	1.943	5.770
498	1.947	5.786
499	1.950	5.803
500	1.954	5.819
501	1.958	5.836
502	1.962	5.853
503	1.965	5.869
504	1.969	5.886
505	1.973	5.903
506	1.977	5.919
507	1.981	5.936
508	1.984	5.953
509	1.988	5.970
510	1.992	5.987
511	1.996	6.004
512	2.000	6.021
513	2.004	6.038
514	2.008	6.055
515	2.012	6.072
516	2.016	6.089
517	2.020	6.106
518	2.024	6.123
519	2.028	6.140

ana_gain_global	Gain(times)	Gain(dB)
520	2.032	6.157
521	2.036	6.175
522	2.040	6.192
523	2.044	6.209
524	2.048	6.227
525	2.052	6.244
526	2.056	6.261
527	2.060	6.279
528	2.065	6.296
529	2.069	6.314
530	2.073	6.331
531	2.077	6.349
532	2.081	6.367
533	2.086	6.384
534	2.090	6.402
535	2.094	6.420
536	2.098	6.438
537	2.103	6.455
538	2.107	6.473
539	2.111	6.491
540	2.116	6.509
541	2.120	6.527
542	2.124	6.545
543	2.129	6.563
544	2.133	6.581
545	2.138	6.599
546	2.142	6.617
547	2.147	6.636
548	2.151	6.654
549	2.156	6.672
550	2.160	6.690
551	2.165	6.709
552	2.169	6.727
553	2.174	6.746
554	2.179	6.764
555	2.183	6.783
556	2.188	6.801
557	2.193	6.820
558	2.197	6.838
559	2.202	6.857

ana_gain_global	Gain(times)	Gain(dB)
560	2.207	6.876
561	2.212	6.894
562	2.216	6.913
563	2.221	6.932
564	2.226	6.951
565	2.231	6.970
566	2.236	6.989
567	2.241	7.008
568	2.246	7.027
569	2.251	7.046
570	2.256	7.065
571	2.260	7.084
572	2.265	7.103
573	2.271	7.122
574	2.276	7.142
575	2.281	7.161
576	2.286	7.180
577	2.291	7.200
578	2.296	7.219
579	2.301	7.239
580	2.306	7.258
581	2.312	7.278
582	2.317	7.298
583	2.322	7.317
584	2.327	7.337
585	2.333	7.357
586	2.338	7.377
587	2.343	7.396
588	2.349	7.416
589	2.354	7.436
590	2.359	7.456
591	2.365	7.476
592	2.370	7.496
593	2.376	7.516
594	2.381	7.537
595	2.387	7.557
596	2.393	7.577
597	2.398	7.597
598	2.404	7.618
599	2.409	7.638

ana_gain_global	Gain(times)	Gain(dB)
600	2.415	7.659
601	2.421	7.679
602	2.427	7.700
603	2.432	7.720
604	2.438	7.741
605	2.444	7.762
606	2.450	7.782
607	2.456	7.803
608	2.462	7.824
609	2.467	7.845
610	2.473	7.866
611	2.479	7.887
612	2.485	7.908
613	2.491	7.929
614	2.498	7.950
615	2.504	7.972
616	2.510	7.993
617	2.516	8.014
618	2.522	8.035
619	2.528	8.057
620	2.535	8.078
621	2.541	8.100
622	2.547	8.121
623	2.554	8.143
624	2.560	8.165
625	2.566	8.187
626	2.573	8.208
627	2.579	8.230
628	2.586	8.252
629	2.592	8.274
630	2.599	8.296
631	2.606	8.318
632	2.612	8.340
633	2.619	8.362
634	2.626	8.385
635	2.632	8.407
636	2.639	8.429
637	2.646	8.452
638	2.653	8.474
639	2.660	8.497

**Table 5-27 Analog gain setting reference [640 to 799]**

ana_gain_global	Gain(times)	Gain(dB)
640	2.667	8.519
641	2.674	8.542
642	2.681	8.565
643	2.688	8.587
644	2.695	8.610
645	2.702	8.633
646	2.709	8.656
647	2.716	8.679
648	2.723	8.702
649	2.731	8.725
650	2.738	8.749
651	2.745	8.772
652	2.753	8.795
653	2.760	8.819
654	2.768	8.842
655	2.775	8.865
656	2.783	8.889
657	2.790	8.913
658	2.798	8.936
659	2.805	8.960
660	2.813	8.984
661	2.821	9.008
662	2.829	9.032
663	2.837	9.056
664	2.844	9.080
665	2.852	9.104
666	2.860	9.128
667	2.868	9.153
668	2.876	9.177
669	2.885	9.201
670	2.893	9.226
671	2.901	9.251
672	2.909	9.275
673	2.917	9.300
674	2.926	9.325
675	2.934	9.349
676	2.943	9.374
677	2.951	9.399
678	2.960	9.424
679	2.968	9.450

ana_gain_global	Gain(times)	Gain(dB)
680	2.977	9.475
681	2.985	9.500
682	2.994	9.525
683	3.003	9.551
684	3.012	9.576
685	3.021	9.602
686	3.030	9.628
687	3.039	9.653
688	3.048	9.679
689	3.057	9.705
690	3.066	9.731
691	3.075	9.757
692	3.084	9.783
693	3.094	9.809
694	3.103	9.836
695	3.112	9.862
696	3.122	9.889
697	3.131	9.915
698	3.141	9.942
699	3.151	9.968
700	3.160	9.995
701	3.170	10.022
702	3.180	10.049
703	3.190	10.076
704	3.200	10.103
705	3.210	10.130
706	3.220	10.157
707	3.230	10.185
708	3.241	10.212
709	3.251	10.240
710	3.261	10.267
711	3.272	10.295
712	3.282	10.323
713	3.293	10.351
714	3.303	10.379
715	3.314	10.407
716	3.325	10.435
717	3.336	10.463
718	3.346	10.492
719	3.357	10.520

ana_gain_global	Gain(times)	Gain(dB)
720	3.368	10.549
721	3.380	10.577
722	3.391	10.606
723	3.402	10.635
724	3.413	10.664
725	3.425	10.693
726	3.436	10.722
727	3.448	10.751
728	3.459	10.780
729	3.471	10.810
730	3.483	10.839
731	3.495	10.869
732	3.507	10.898
733	3.519	10.928
734	3.531	10.958
735	3.543	10.988
736	3.556	11.018
737	3.568	11.048
738	3.580	11.079
739	3.593	11.109
740	3.606	11.140
741	3.618	11.170
742	3.631	11.201
743	3.644	11.232
744	3.657	11.263
745	3.670	11.294
746	3.683	11.325
747	3.697	11.356
748	3.710	11.388
749	3.724	11.419
750	3.737	11.451
751	3.751	11.483
752	3.765	11.515
753	3.779	11.547
754	3.793	11.579
755	3.807	11.611
756	3.821	11.643
757	3.835	11.676
758	3.850	11.708
759	3.864	11.741

ana_gain_global	Gain(times)	Gain(dB)
760	3.879	11.774
761	3.894	11.807
762	3.908	11.840
763	3.923	11.873
764	3.938	11.907
765	3.954	11.940
766	3.969	11.974
767	3.984	12.007
768	4.000	12.041
769	4.016	12.075
770	4.031	12.109
771	4.047	12.144
772	4.063	12.178
773	4.080	12.213
774	4.096	12.247
775	4.112	12.282
776	4.129	12.317
777	4.146	12.352
778	4.163	12.387
779	4.180	12.423
780	4.197	12.458
781	4.214	12.494
782	4.231	12.530
783	4.249	12.566
784	4.267	12.602
785	4.285	12.638
786	4.303	12.674
787	4.321	12.711
788	4.339	12.748
789	4.357	12.785
790	4.376	12.822
791	4.395	12.859
792	4.414	12.896
793	4.433	12.934
794	4.452	12.971
795	4.472	13.009
796	4.491	13.047
797	4.511	13.085
798	4.531	13.124
799	4.551	13.162

**Table 5-28 Analog gain setting reference [800 to 978]**

ana_gain_global	Gain(times)	Gain(dB)									
800	4.571	13.201	845	5.721	15.149	890	7.642	17.664	935	11.506	21.218
801	4.592	13.240	846	5.753	15.198	891	7.699	17.729	936	11.636	21.316
802	4.613	13.279	847	5.785	15.247	892	7.758	17.795	937	11.770	21.416
803	4.633	13.318	848	5.818	15.296	893	7.817	17.861	938	11.907	21.516
804	4.655	13.358	849	5.851	15.345	894	7.877	17.927	939	12.047	21.618
805	4.676	13.397	850	5.885	15.395	895	7.938	17.994	940	12.190	21.720
806	4.697	13.437	851	5.919	15.445	896	8.000	18.062	941	12.337	21.824
807	4.719	13.477	852	5.953	15.495	897	8.063	18.130	942	12.488	21.930
808	4.741	13.517	853	5.988	15.546	898	8.127	18.199	943	12.642	22.036
809	4.763	13.557	854	6.024	15.597	899	8.192	18.268	944	12.800	22.144
810	4.785	13.598	855	6.059	15.648	900	8.258	18.338	945	12.962	22.253
811	4.808	13.638	856	6.095	15.700	901	8.325	18.408	946	13.128	22.364
812	4.830	13.679	857	6.132	15.752	902	8.393	18.479	947	13.299	22.476
813	4.853	13.720	858	6.169	15.804	903	8.463	18.550	948	13.474	22.590
814	4.876	13.762	859	6.206	15.856	904	8.533	18.622	949	13.653	22.705
815	4.900	13.803	860	6.244	15.909	905	8.605	18.695	950	13.838	22.821
816	4.923	13.845	861	6.282	15.962	906	8.678	18.768	951	14.027	22.940
817	4.947	13.887	862	6.321	16.016	907	8.752	18.842	952	14.222	23.059
818	4.971	13.929	863	6.360	16.069	908	8.828	18.917	953	14.423	23.181
819	4.995	13.971	864	6.400	16.124	909	8.904	18.992	954	14.629	23.304
820	5.020	14.013	865	6.440	16.178	910	8.982	19.068	955	14.841	23.429
821	5.044	14.056	866	6.481	16.233	911	9.062	19.144	956	15.059	23.556
822	5.069	14.099	867	6.522	16.288	912	9.143	19.222	957	15.284	23.685
823	5.095	14.142	868	6.564	16.344	913	9.225	19.300	958	15.515	23.815
824	5.120	14.185	869	6.606	16.399	914	9.309	19.378	959	15.754	23.948
825	5.146	14.229	870	6.649	16.456	915	9.394	19.457	960	16.000	24.082
826	5.172	14.273	871	6.693	16.512	916	9.481	19.538			
827	5.198	14.317	872	6.737	16.569	917	9.570	19.618			
828	5.224	14.361	873	6.781	16.626	918	9.660	19.700			
829	5.251	14.405	874	6.827	16.684	919	9.752	19.782			
830	5.278	14.450	875	6.872	16.742	920	9.846	19.865			
831	5.306	14.495	876	6.919	16.801	921	9.942	19.949			
832	5.333	14.540	877	6.966	16.860	922	10.039	20.034			
833	5.361	14.585	878	7.014	16.919	923	10.139	20.120			
834	5.389	14.631	879	7.062	16.979	924	10.240	20.206			
835	5.418	14.677	880	7.111	17.039	925	10.343	20.293			
836	5.447	14.723	881	7.161	17.099	926	10.449	20.381			
837	5.476	14.769	882	7.211	17.160	927	10.557	20.471			
838	5.505	14.816	883	7.262	17.222	928	10.667	20.561			
839	5.535	14.863	884	7.314	17.283	929	10.779	20.652			
840	5.565	14.910	885	7.367	17.346	930	10.894	20.743			
841	5.596	14.957	886	7.420	17.408	931	11.011	20.836			
842	5.626	15.005	887	7.474	17.472	932	11.130	20.930			
843	5.657	15.052	888	7.529	17.535	933	11.253	21.025			
844	5.689	15.101	889	7.585	17.599	934	11.378	21.121			

### 5.5.2. Digital gain settings

Digital gain of this sensor can be set by color. The registers for digital gain settings are shown in the table below.

**Table 5-29 Digital gain setting**

<sup>I<sup>2</sup>C register</sup>	Address	Bit	Name	Description	Notes
	0x3ff9	[0]	DPGA_USE_GLOBAL_GAIN	Digital gain control mode select 0 : by color 1 : all color(DIG_GAIN_GR setting is used for all color)	
	0x020e	[7:0]	DIG_GAIN_GR [15:8]	Digital gain control code for GR in case of individual control. When global control is selected, treated with a code for all colors. Format : 16-bit unsigned real Range : 0x0100 to 0xFFFF *Setup other than the above is forbidden.	range: 1 to 15
	0x020f	[7:0]	DIG_GAIN_GR [7:0]		range: 0 to 255
	0x0210	[7:0]	DIG_GAIN_R [15:8]	Digital gain control code for R	range: 1 to 15
	0x0211	[7:0]	DIG_GAIN_R [7:0]	Format : 16-bit unsigned real	range: 0 to 255
	0x0212	[7:0]	DIG_GAIN_B [15:8]	Digital gain control code for B	range: 1 to 15
	0x0213	[7:0]	DIG_GAIN_B [7:0]	Format : 16-bit unsigned real	range: 0 to 255
	0x0214	[7:0]	DIG_GAIN_GB [15:8]	Digital gain control code for GB	range: 1 to 15
	0x0215	[7:0]	DIG_GAIN_GB [7:0]	Format : 16-bit unsigned real	range: 0 to 255

#### 5.5.2.1. Global Digital Gain Control

Global Digital Gain Control can be used. When using in Bayer type sensor, can set global digital gain setting.

#### 5.5.2.2. Individual Digital Gain Control

Each register is comprised of 2 bytes with the *upper\_byte* [15:8] setting the integer portion and the *lower\_byte* [7:0] setting the decimal portion of the gain. The gain for each color is obtained by the following formula.

$$\text{Digital gain} = \text{upper\_byte} + \text{lower\_byte} / 256 \text{ [times]}$$

The unit of Digital gain is times. The upper byte can be set to a value ranging from 1 to 15 and the

lower byte to a value ranging from 0 to 255. Therefore, the range of digital gain is shown as follows.

$$1 + 0/256 \text{ [times]} (0 \text{ dB}) \leq \text{Digital gain} \leq 15 + 255/256 \text{ [times]} (\doteq 24 \text{ dB})$$

When representing the gain by log-linear scale [dB], lower gain takes coarse steps and high gain takes fine steps for the incrimination of the register value. The table below indicates the register values in 0.1 dB steps for reference.

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**Table 5-30 Digital gain setting reference (0 to 23.9[dB])**

Upper		Lower		Gain [times]	Gain [dB]
dec	hex	dec	hex		
1	1	0	0	1	0
1	1	3	3	1.01	0.1
1	1	6	6	1.02	0.2
1	1	9	9	1.04	0.3
1	1	12	C	1.05	0.4
1	1	15	F	1.06	0.49
1	1	18	12	1.07	0.59
1	1	21	15	1.08	0.68
1	1	25	19	1.1	0.81
1	1	28	1C	1.11	0.9
1	1	31	1F	1.12	0.99
1	1	35	23	1.14	1.11
1	1	38	26	1.15	1.2
1	1	41	29	1.16	1.29
1	1	45	2D	1.18	1.41
1	1	48	30	1.19	1.49
1	1	52	34	1.2	1.61
1	1	55	37	1.21	1.69
1	1	59	3B	1.23	1.8
1	1	63	3F	1.25	1.91
1	1	66	42	1.26	1.99
1	1	70	46	1.27	2.1
1	1	74	4A	1.29	2.21
1	1	78	4E	1.3	2.31
1	1	81	51	1.32	2.39
1	1	85	55	1.33	2.49
1	1	89	59	1.35	2.59
1	1	93	5D	1.36	2.69
1	1	97	61	1.38	2.79
1	1	101	65	1.39	2.89
1	1	106	6A	1.41	3.01
1	1	110	6E	1.43	3.1
1	1	114	72	1.45	3.2
1	1	118	76	1.46	3.29
1	1	123	7B	1.48	3.41
1	1	127	7F	1.5	3.5
1	1	131	83	1.51	3.59
1	1	136	88	1.53	3.7
1	1	140	8C	1.55	3.79
1	1	145	91	1.57	3.90
1	1	150	96	1.59	4.01
1	1	154	9A	1.6	4.09
1	1	159	9F	1.62	4.2
1	1	164	A4	1.64	4.3
1	1	169	A9	1.66	4.4
1	1	174	AE	1.68	4.5
1	1	179	B3	1.7	4.6
1	1	184	B8	1.72	4.7
1	1	189	BD	1.74	4.8
1	1	194	C2	1.76	4.9
1	1	199	C7	1.78	5
1	1	205	CD	1.8	5.11
1	1	210	D2	1.82	5.2
1	1	215	D7	1.84	5.3
1	1	221	DD	1.86	5.41
1	1	226	E2	1.88	5.5
1	1	232	E8	1.91	5.6
1	1	237	ED	1.93	5.69
1	1	243	F3	1.95	5.8
1	1	249	F9	1.97	5.9

Upper		Lower		Gain [times]	Gain [dB]
dec	hex	dec	hex		
1	1	255	FF	2	6
2	2	5	5	2.02	6.11
2	2	11	B	2.04	6.21
2	2	17	11	2.07	6.3
2	2	23	17	2.09	6.4
2	2	29	1D	2.11	6.5
2	2	35	23	2.14	6.59
2	2	42	2A	2.16	6.71
2	2	48	30	2.19	6.8
2	2	55	37	2.21	6.91
2	2	61	3D	2.24	7
2	2	68	44	2.27	7.1
2	2	74	52	2.29	7.19
2	2	81	51	2.32	7.3
2	2	88	58	2.34	7.4
2	2	95	5F	2.37	7.5
2	2	102	66	2.4	7.6
2	2	109	6D	2.43	7.7
2	2	116	74	2.45	7.79
2	2	124	7C	2.48	7.9
2	2	131	83	2.51	8
2	2	138	8A	2.54	8.09
2	2	146	92	2.57	8.2
2	2	154	9A	2.6	8.3
2	2	161	A1	2.63	8.4
2	2	169	A9	2.66	8.5
2	2	177	B1	2.69	8.6
2	2	185	B9	2.72	8.7
2	2	193	C1	2.75	8.8
2	2	201	C9	2.79	8.9
2	2	210	D2	2.82	9.01
2	2	218	DA	2.85	9.10
2	2	226	E2	2.88	9.2
2	2	235	EB	2.92	9.3
2	2	244	F4	2.95	9.41
2	2	252	FC	2.98	9.5
3	3	5	5	3.02	9.6
3	3	14	E	3.05	9.7
3	3	23	17	3.09	9.8
3	3	32	20	3.13	9.9
3	3	42	2A	3.16	10
3	3	51	33	3	10.1
3	3	60	3C	3.23	10.2
3	3	70	46	3.27	10.3
3	3	80	50	3.31	10.4
3	3	90	5A	3.35	10.5
3	3	99	63	3.39	10.6
3	3	109	6D	3.43	10.7
3	3	120	78	3.47	10.8
3	3	130	82	3.51	10.9
3	3	140	8C	3.55	11
3	3	151	97	3.59	11.1
3	3	161	A1	3.63	11.2
3	3	172	AC	3.67	11.3
3	3	183	B7	3.71	11.4
3	3	194	C2	3.76	11.5
3	3	205	CD	3.8	11.6
3	3	217	D9	3.85	11.7
3	3	228	E4	3.89	11.8
3	3	239	EF	3.93	11.9

Upper		Lower		Gain [times]	Gain [dB]
dec	hex	dec	hex		
3	3	251	FB	3.98	12
4	4	7	7	4.03	12.1
4	4	19	13	4.07	12.2
4	4	31	1F	4.12	12.3
4	4	43	2B	4.17	12.4
4	4	56	38	4.22	12.5
4	4	68	44	4.27	12.6
4	4	81	51	4.32	12.7
4	4	93	5D	4.36	12.8
4	4	106	6A	4.41	12.9
4	4	120	78	4.47	13
4	4	133	85	4.52	13.1
4	4	146	92	4.57	13.2
4	4	160	A0	4.63	13.3
4	4	173	AD	4.68	13.4
4	4	187	BB	4.73	13.5
4	4	201	C9	4.79	13.6
4	4	215	D7	4.84	13.7
4	4	230	E6	4.9	13.8
4	4	244	F4	4.95	13.9
5	5	3	3	5.01	14
5	5	33	21	5.13	14.2
5	5	48	30	5.19	14.3
5	5	64	40	5.25	14.4
5	5	79	4F	5.31	14.5
5	5	160	A0	5.63	15
5	5	176	B0	5.69	15.1
5	5	193	C1	5.75	15.2
5	5	210	D2	5.82	15.3
5	5	227	E3	5.89	15.4
5	5	245	F5	5.96	15.5
6	6	7	7	6.03	15.6
6	6	24	18	6.09	15.7
6	6	42	2A	6.16	15.8
6	6	61	3D	6.24	15.9
6	6	79	4F	6.31	16
6	6	98	62	6.38	16.1
6	6	117	75	6.46	16.2
6	6	136	88	6.53	16.3
6	6	155	9B	6.61	16.4
6	6	175	AF	6.68	16.5
6	6	195	C3	6.76	16.6
6	6	215	D7	6.84	16.7
6	6	235	EB	6.92	16.8
7	7	0	00	7.00	16.9
7	7	20	14	7.08	17
7	7	41	29	7.16	17.1
7	7	63	3F	7.25	17.2
7	7	84	54	7.33	17.3
7	7	106	6A	7.41	17.4
7	7	128	80	7.50	17.5
7	7	150	96	7.59	17.6
7	7	172	AC	7.67	17.7
7	7	195	C3	7.76	17.8
7	7	218	DA	7.85	17.9
15	F	217	D9	15.85	24

### 5.5.3. Change in output pixel level depending on binning mode

The output pixel level in Binning mode changes as shown in the table.

**Table 5-31 Output pixel level according to binning modes**

	0x0900 [0]	0x0901 [7:0]	0x3F4C [7:0]	0x3F4D [7:0]	0x0902 [1:0]	Output Pixel Level Ratio	Max Analog Gain[dB]
	BINNING_MODE [0]	BINNING_TYPE_H [7:4] BINNING_TYPE_V [3:0]	BINNING_PRIORITY _V [7:0]	BINNING_PRIORITY _H [7:0]	BINNING_WEIGHTING [1:0]		
Full-pixel	0x0	x	x	x	x	1	24
2x2 Adjacent Pixel Binning	0x1	0x22	0x81	0x81	0x0	2	24
					0x1	4	24

\* Values in parentheses for pixel level are output pixel level to which pedestal level (0x40) is added.

**Table 5-32 Binning mode determining registers**

I <sup>2</sup> C register	Address	Bit	Name	Description
	0x0902	[7:0]	BINNING_WEIGHTING	Bit[1:0] Binning type selection 0 : Averaged 1 : Summed *Setup other than the above is forbidden. Bit [7:2] : 6'b000010 Fixed

\*For BINNING\_MODE and BINNING\_TYPE see 5.2.2

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## 5.6. Optical black level clamp

### 5.6.1. Default setting (normal usage)

This sensor has the optical black level clamping function to make the black level stable against changes in operating conditions. The average value of the black level is adjusted to the pedestal level (0x40).

### 5.6.2. Test mode setting

Set the registers shown in the table below to control output black level for test purpose.

**Table 5-33 Optical black level clamp related registers and descriptions**

<sup>I<sup>2</sup>C register</sup>	Address	Bit	Name	Description
	0x3032	[1:0]	MANUAL_DATA_PEDESTAL_VALUE[9:8]	Manual setting value for Data Pedestal Default setting value : 0x40 (pedestal value = 0x40 for 10bit system)
	0x3033	[7:0]	MANUAL_DATA_PEDESTAL_VALUE[7:0]	
	0x3030	[0]	MANUAL_DATA_PEDESTAL_EN	Output black level is controlled with MANUAL_DATA_PEDESTAL_VALUE register value 0x0 : pedestal = 0x40 (fixed value) 0x1 : pedestal = MANUAL_DATA_PEDESTAL_VALUE else : inhibited value

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## 5.7. Image compensation function setting

There are some other functions in the sensor image pipeline. Use-case may be chosen in terms of trade-off for power consumption and image quality, for example.

### 5.7.1. Defect Pixel Correction (DPC)

Defect Pixel Correction can be used in Binning mode only with this sensor.

#### 5.7.1.1. Static Defect Correction

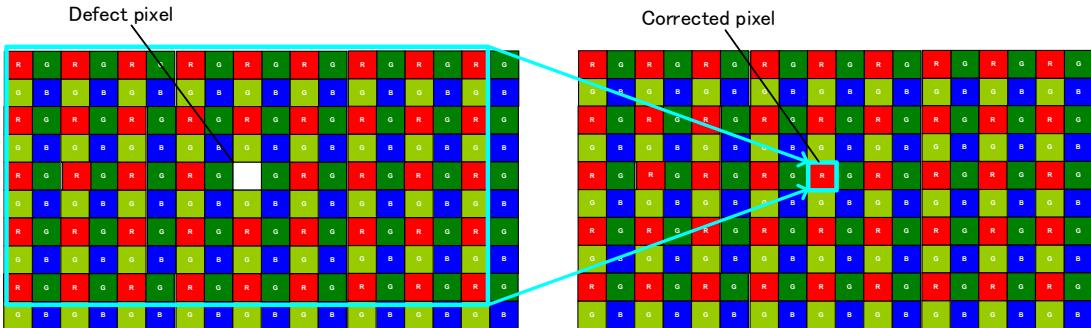
This function correct the pixel defects up to 299 defects by matching the physical address information of defect pixels stored in the OTP in advance and the read address to access when you actually read. It does defect correction processing of the pixel data corresponding to the address that matches. The address matching between the physical address and the read address is automatically done within the sensor.

"Single Defect pixel" and "Continuous Defect Pixels" (including Same Color Continuous Defect Pixels) can be corrected.

#### 5.7.1.2. Dynamic Defect Correction

This is a function to detect and correct single pixel defects. It performs defect compensation with using pixels surrounding a defect pixel.

\* If an adjacent pixel of the same color is defective, this function cannot correct the defect.

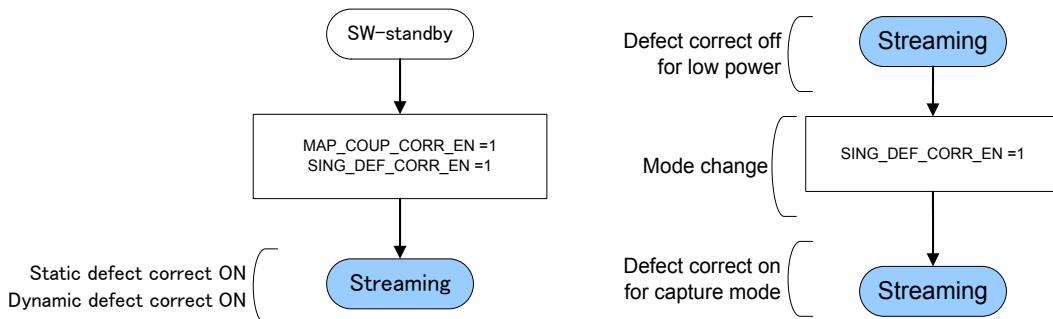


**Figure 5-6 Dynamic Defect Correction model figure (after adjacent pixel binning)**

Whether to turn each Defect Correction ON or OFF can be set with the following registers.

**Table 5-34 Defect correction register**

$\text{I}^2\text{C}$ register	Address	Bit	Name	Description
	0x0b05	[0]	MAP_COUP_CORR_EN	Mapped couplet correction control 0 : disable 1 : enable
	0x0b06	[0]	SING_DEF_CORR_EN	dynamic singlet correction control 0 : disable 1 : enable



**Figure 5-7 Defect correction flow chart**

## 6. Power ON/OFF Sequence

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### 6.1. Power ON sequence

#### 6.1.1. Power ON reset

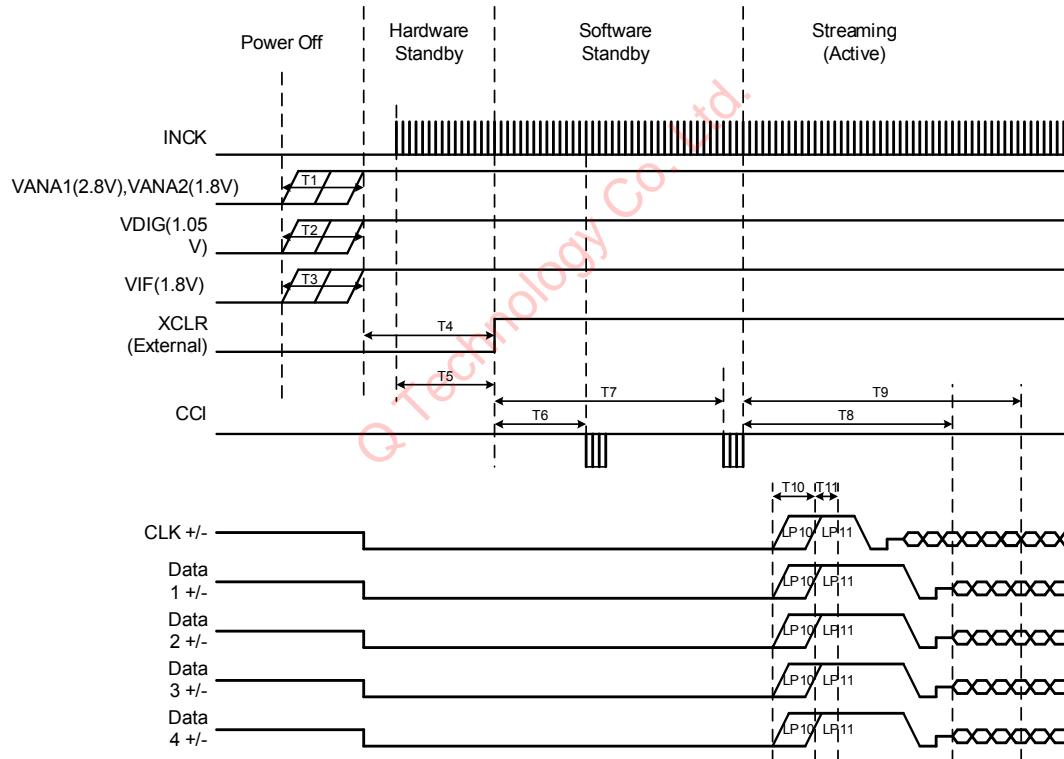
This sensor doesn't have a built-in "Power ON Reset" function.

The XCLR pin is set to "LOW" and the power supplies are brought up. Then the XCLR pin should be set to "High" after INCK supplied.

#### 6.1.2. Power ON sequence

##### 6.1.2.1. Start up sequence with 2-wire serial communication (external reset)

Follow the power supply start up sequence below.



**Figure 6-1 Start up sequence with 2-wire serial communication (external reset)**

\*Presence of INCK during Power Off is acceptable despite of above chart.

**Table 6-1 Startup sequence timing constraints (2-wire serial communication mode with external reset)**

Item	Label	Min.	Max.	Unit	Comment
VANA rising – VANA ON	T1	VANA, VDIG and VIF may rise in any order.		μs	Slew rate of VANA, VDIG and VIF(0%-100%) : refer to Datasheet, 7-2-1 Power on slew rate
VDIG rising – VDIG ON	T2			μs	
VIF rising – VIF ON	T3			μs	
VANA, VDIG and VIF rising – XCLR rising	T4	0		μs	Later of T1, T2 and T3
INCK start - XCLR rising	T5	0		ms	
INCK start and XCLR rising till CCI Read version ID register wait time	T6	0.6		ms	
INCK start and XCLR rising till Send Streaming Command wait time (To complete reading all parameters from OTP)	T7	8		ms	
Start of first streaming from Sending Streaming Command.	T8		4.0 ms + The delay of the coarse integration time value + 13H		
Start of first streaming with valid frame after power-on sequence.	T9		T8 + 1Frame	ms	
DPHY power up	T10	1		ms	
DPHY init	T11	100		μs	

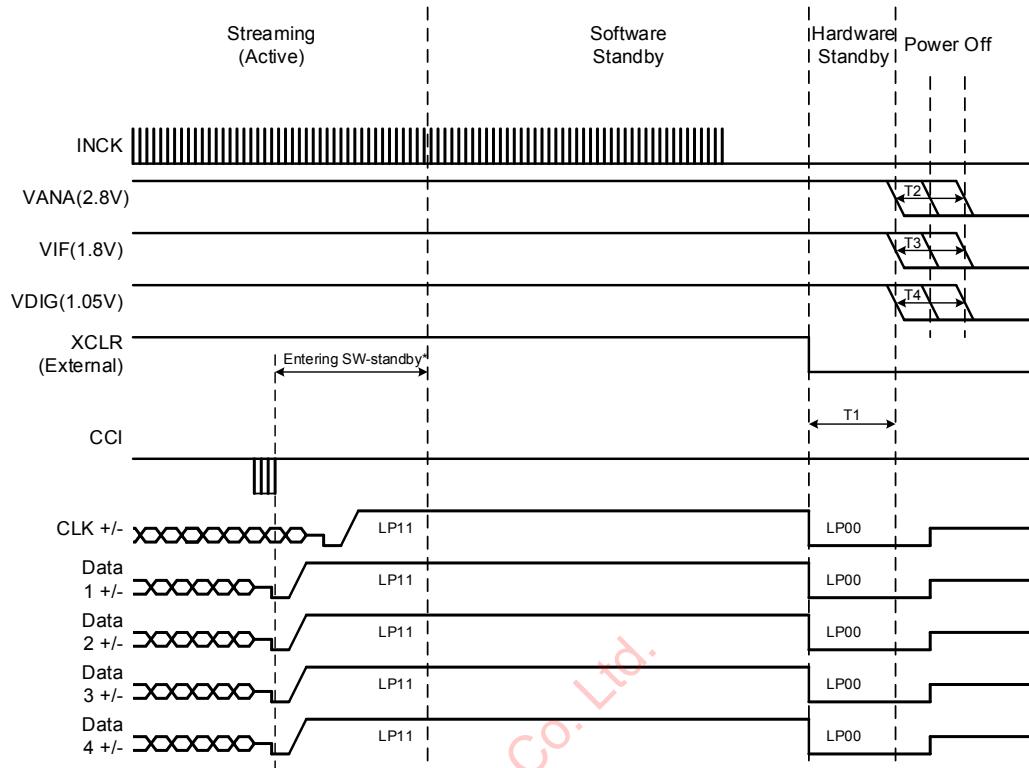
\* XCLR needs to be Low level until all power supplies complete power-ON.

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## 6.2. Power down sequence

### 6.2.1. Power down sequence with 2-wire serial communication

Follow the power down sequence below.



**Figure 6-2 Power down sequence with 2-wire serial communication (external reset)**

**Table 6-2 Power down sequence timing constraints (2-wire serial communication mode with external reset)**

Item	Label	Min.	Max.	Unit	Comment
XCLR Neg-edge – VANA (VDIG or VIF) fall	T1	0		ns	Presence of INCK during Power Off is acceptable.
Sequence free of VANA falling and VDIG falling and VIF falling	T2,T3,T4	VANA, VDIG and VIF may fall in any order.		ns	

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## 7. Mode Transition Sequence and Register Update Timing

SRM-230-00088-01

### 7.1. Transition between SW-standby and Streaming

Sensor can make transition between SW-standby and streaming without using power ON/OFF.

#### 7.1.1. SW-standby to Streaming

The following figure shows how to start streaming at first time after power on sequence and register setting timing restriction

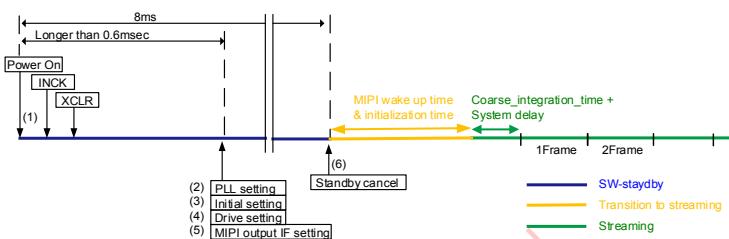
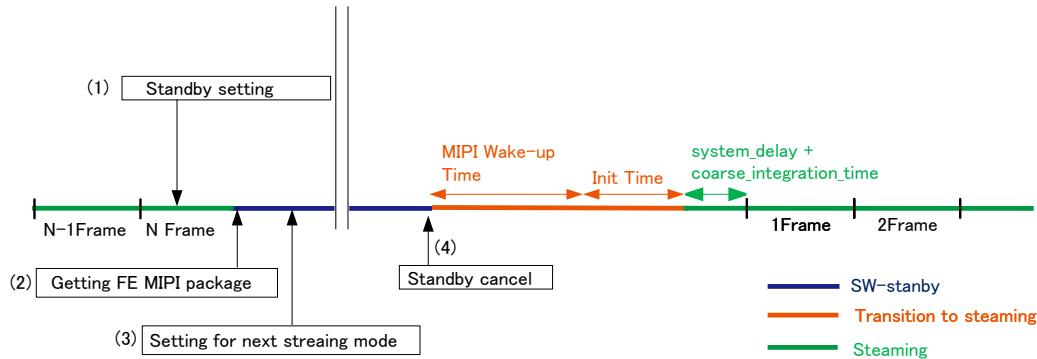


Figure 7-1 Start streaming sequence after power ON

Table 7-1 Start streaming sequence after power ON

(1)	Refer to power up sequence timing diagram	Note: Refer to Power Related sequence of 6.1.2 for procedure of (2) - (6).
(2)	Set PLL parameters	
(3)	Basic settings (operation-critical setting)	
(4)	Set readout mode (start/end position, size, mode, integration time, and gain)	
(5)	Set MIPI interface parameters	
(6)	Start streaming with 0x0100 (MODE_SEL = 1)	
	After "MIPI Wake Up Time" + "Initialize Time", 1st frame starts and images come out	

The following figure shows how to start a streaming after first streaming.



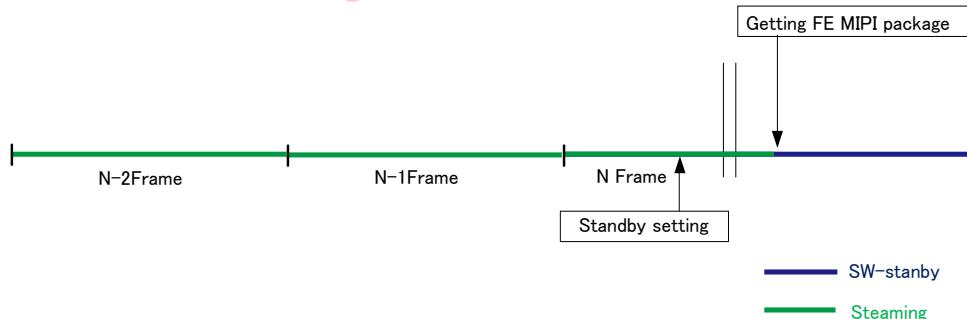
**Figure 7-2 Start streaming after first streaming**

**Table 7-2 Start streaming after first streaming**

(1)	Standby setting in streaming with 0x0100 (MODE_SEL = 0)	Note: Refer to 6.1.2 for procedure of (1) to (4).
(2)	Waiting for MIPI FE package	
(3)	Set register for next streaming mode	
(4)	Start streaming with 0x0100 (MODE_SEL = 1)	
	After "MIPI Wake Up Time" + "Initialize Time", 1st frame starts and images come out	

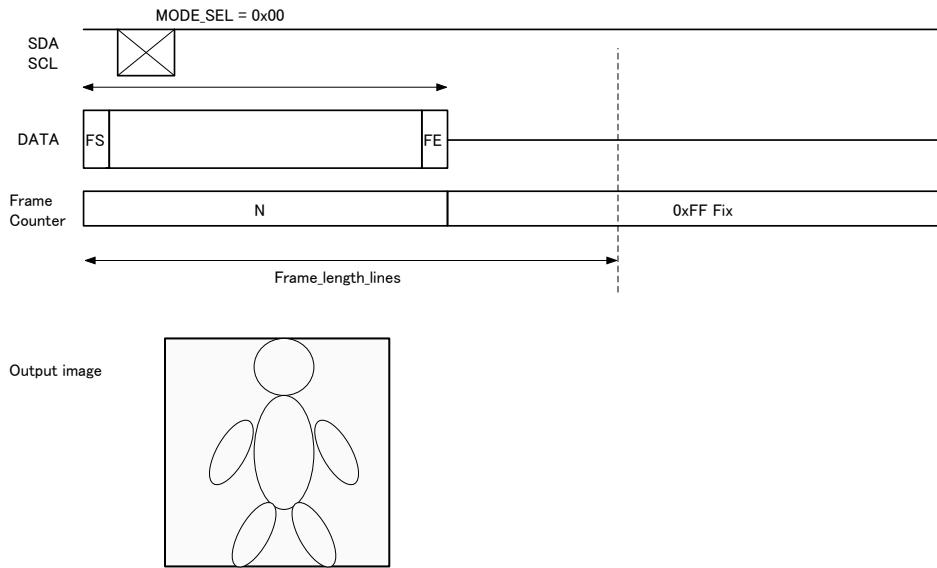
### 7.1.2. Streaming to SW-standby

This section will introduce how to end streaming and exit to SW-standby.



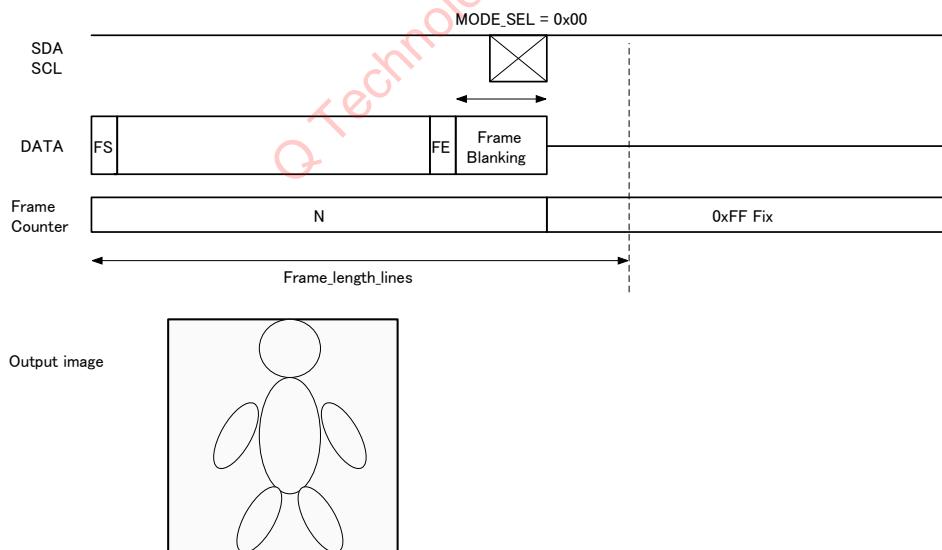
**Figure 7-3 transition to SW-standby from streaming**

- (1) In case a SW-standby command is issued in between "FS" and "FE", this sensor completes outputting the image data and transits to a standby state.



**Figure 7-4 SW-standby transition pattern 1**

- (2) In case a SW-standby command is issued within a “Frame Blanking” period, this sensor immediately transits to a software standby state.



**Figure 7-5 SW-standby standby transition pattern 2**

- (3) In case a SW-standby command is issued in between “FS” and “FE” while the sensor is working in fast SW-standby mode, this sensor completes outputting the line’s image data to where the command belongs and transit to the standby.

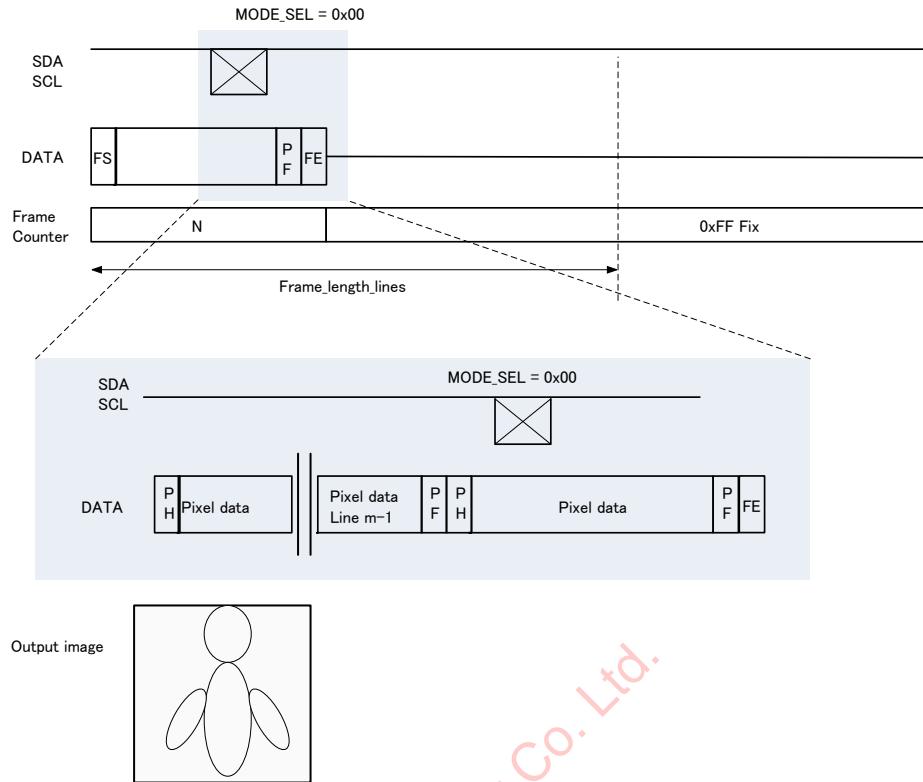


Figure 7-6 Software standby transition pattern 3 (Fast SW standby)

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## 7.2. Streaming mode transition

In this section, various knowledge on streaming mode change is explained. Basically, mode transition is grouped into two general categories: 1) via software standby transition and 2) on-the-fly transition.

Basic knowledge to know first is about registers which can be updated only in software standby and ones which cause a corrupted frame. Then, based on the knowledge, basic four streaming mode changes are explained.

### 7.2.1. registers to be set only in SW-standby as mode transition

In case the following register are updated between the streaming mode, the streaming mode change must be made via software standby mode.

**Table 7-3 List of registers to be set only in SW-standby as mode transition.**

I <sup>2</sup> C register	Address	Bit	Name	Description
	0x0106	[0]	FAST_STANDBY_CTL	0 : after outputting all current frames, switch to software standby. Effective in Via SW-standby transition 1 : immediately after stopping outputting all current frames, switch to software standby
	0x0350	[0]	FRM_LENGTH_CTL	Frame length automatic tracking control as shutter time exceeding a current operation vertical period Select whether or not the frame length is changed automatically when FRM_LENGTH_LINES < COARSE_INTEG_TIME + α (α = type-specific adjustment parameter, and is 18(d) for this type) 0 : no automatic tracking control of frame length 1 : automatic tracking control of frame length In this case, "COARSE_INTEG_TIME + α" operates instead of FRM_LENGTH_LINES
	0x3020	[0]	SHORT_FRAME_RS	Fast mode transition. Effective in On-the-fly transition. 0: normal mode change 1: Fast mode change
	0x3f44	[0]	COMPLETE_FRAME_TRGS	The type of fast mode transition. 0: truncated frame 1: complete frame
	0x0114	[1:0]	CSI_LANE_MODE	Number of lanes for CSI 0 : 1-lane *not supported 1 : 2-lane 2 : 3-lane *not supported 3 : 4-lane
	0x0112	[7:0]	CSI_DT_FMT_H [7:0]	The output data format for CSI CSI_DT_FMT_H : Uncompressed Data Bit Width CSI_DT_FMT_L : Compressed Data Bit Width
	0x0113	[7:0]	CSI_DT_FMT_L [7:0]	0x0808 : RAW8 (top 8bit of internal data) 0x0A08 : COMP8 (10bit to 8bit compression) 0x0A0A : RAW10 (top 10bit of internal data)

			Setup other than the above is forbidden.
0x0301	[4:0]	IVT_PXCK_DIV	The Pixel Clock Divider for Internal Video Timing System Range : 6 Format : 5-bit unsigned integer *Setup other than the above is forbidden.
0x0303	[2:0]	IVT_SYCK_DIV	The System Clock Divider for Internal Video Timing System Range : 2, 4 Format : 16-bit unsigned integer *Setup other than the above is forbidden.
0x0305	[3:0]	IVT_PREPLLCK_DIV	The pre-PLL Clock Divider for Internal Video Timing System Clock, when PLL_MULT_DRIV=1. The pre-PLL Clock Divider for Internal Video Timing System and Internal Output Pixel System, when PLL_MULT_DRIV=0. Range : 1 to 4 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.
0x0306	[2:0]	IVT_PLL_MPY[10:8]	The PLL multiplier for Internal Video Timing Range : 29 to 290 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.
0x0307	[7:0]	IVT_PLL_MPY[7:0]	
0x030b	[4:0]	IOP_SYCK_DIV	The System Clock Divider for Internal Output Pixel System Range : 1, 2, 4 Format : 16-bit unsigned integer *Setup other than the above is forbidden.
0x030d	[3:0]	IOP_PREPLLCK_DIV	The pre-PLL Clock Divider for Internal Output Pixel System during "Dual PLL mode" (PLL_MULT_DRIV=1). Range : 1 to 15 Step : 1 Format : 16-bit unsigned integer *Setup other than the above is forbidden.
0x030e	[2:0]	IOP_PLL_MPY[10:8]	The PLL multiplier for Internal Output Pixel System "Dual PLL mode" (PLL_MULT_DRIV=1). Range : 29 to 1840 Step : 1

	0x030f	[7:0]	IOP_PLL_MPY[7:0]	Format : 16-bit unsigned integer *Setup other than the above is forbidden.
	0x0310	[0]	PLL_MULT_DRIV	PLL mode select 0 : Single PLL mode 1 : Dual PLL mode
	0x0820	[7:0]	REQ_LINK_BIT_RATE_MBPS[31:24]	Output Data Rate [Mbps] Bit[32:16] integer Bit[15:0] decimal
	0x0821	[7:0]	REQ_LINK_BIT_RATE_MBPS[23:16]	
	0x0822	[7:0]	REQ_LINK_BIT_RATE_MBPS[15:8]	
	0x0823	[7:0]	REQ_LINK_BIT_RATE_MBPS[7:0]	

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### 7.2.2. Change sequence of corrupted frame related registers

When changing the mode with Corrupted-frame-related registers (vertical direction parameters and some other registers listed in Table 7-3 photo-electron charge integration operation becomes irregular for one frame after updating of the register. This frame shall be treated as invalid frame. Invalid frame should not be output.

**Table 7-4 List of corrupted frame causing registers**

	Address	Bit	Name	Description
<i>I<sup>2</sup>C register</i>	0x0101	[1]	IMG_ORIENTATION_V	Image orientation for Vertical direction 0 : normal 1 : reverse
	0x0342	[7:0]	LINE_LENGTH_PCK[15:8]	The length of line Unit : pixels Format : 16-bit unsigned integer
	0x0343	[7:0]	LINE_LENGTH_PCK[7:0]	* LINE_LENGTH_PCK has been constrained. * Must be set fixed value as Table4-5.
	0x0346	[3:0]	Y_ADD_STA[11:8]	Vertical direction analog cropping start position within the active pixels area Unit : pixels Format : 16-bit unsigned integer
	0x0347	[7:0]	Y_ADD_STA[7:0]	* Note that this is the cropping end position when flipping (IMG_ORIENTATION_V=1)
	0x034a	[3:0]	Y_ADD_END[11:8]	Vertical direction analog cropping end position within the active pixels area Unit : pixels Format : 16-bit unsigned integer
	0x034b	[7:0]	Y_ADD_END[7:0]	* Note that this is the cropping start position when flipping (IMG_ORIENTATION_V=1)
	0x0385	[3:0]	Y_EVN_INC[3:0]	No. of lines skipped from even number line to odd number line in Sub-sampling mode Format : 16-bit unsigned integer
	0x0387	[3:0]	Y_ODD_INC[3:0]	No. of lines skipped from odd number line to even number line in Sub-sampling mode Format : 16-bit unsigned integer
	0x0900	[0]	BINNING_MODE	Binning mode enable 0=None 1=Enable
	0x0901	[7:4]	BINNING_TYPE_H[3:0]	Binning type selection for Horizontal 1 : no binning 2 : 2x2 Adjacent Pixel Binning *Setup other than the above is forbidden.
	0x0901	[3:0]	BINNING_TYPE_V[3:0]	Binning type selection for Vertical 1 : no binning

			2 : 2x2 Adjacent Pixel Binning *Setup other than the above is forbidden.
0x3F4C	[7:0]	BINNING_PRIORITY_V[7:0]	Bit[0] : must be set 1 Bit [6:1]: Reserved Bit[7] : Binning options for Vertical 0 : No binning 1 : Adjacent pixel binning *Setup other than the above is forbidden.
0x3F4D	[7:0]	BINNING_PRIORITY_H[7:0]	Bit[0] : must be set 1 Bit [6:1]: Reserved Bit[7] : Binning options for Horizontal 0 : No binning 1 : Adjacent pixel binning *Setup other than the above is forbidden.

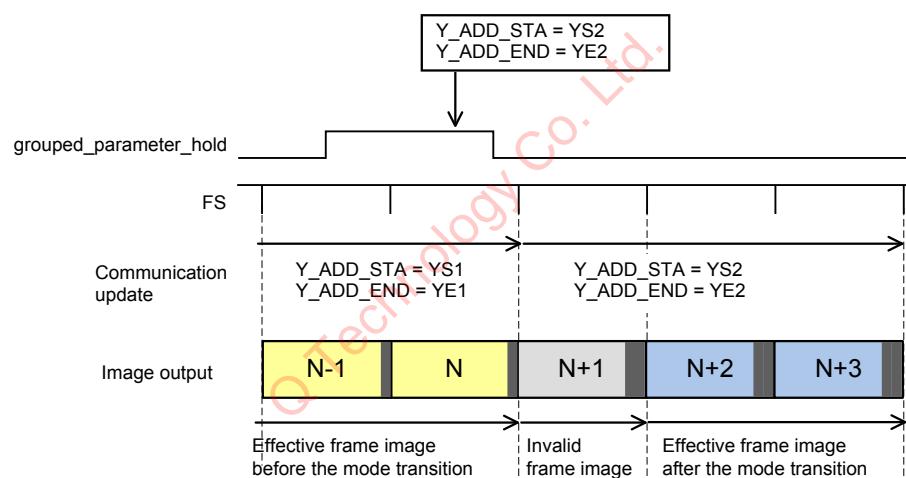


Figure 7-7 Corrupted-frame-related registers change sequence

### 7.2.3. Summary of Streaming Mode Change

In this paragraph, summary of four available mode transition in this sensor are explained together with their use case. You can find conditions of using each mode transition method and causing an invalid frame on which details are already explained in previous sections.

**Table 7-5 List of available mode transitions (possibility of occurrence of corrupt frames, and other precautions)**

Mode transition		Availability of each transition mode		
Mode name	Features and notes/conditions for use	With changes of PLL/MIPI related settings (see Table 7-3)	Without change of PLL/MIPI related settings.	
Via SW standby	SW-standby mode transition (default)	- Standard method for any kind of mode transition. - No corrupted frame.	Available	Available
	Fast SW-standby mode transition	- Versatile and fast transition method. - When MODE_SEL[0] falls, picture output stops and mode transition occurs.	Available	Available
On-the-fly	Complete mode transition (default)	- Usable only the case without clock change.	Not available	Available
	Truncate mode transition	- Usable only the case without clock change but fast mode change. - When GRP_PARAM_HOLD falls, picture output stops and mode transition occurs.	Not available	Available.

### 7.2.4. SW-standby mode transition

A diagram below illustrates mode transition sequence when clock setting change is required (see Table 7-3). Let the sensor go into SW-standby mode by setting MODE\_SEL = 0 before mode change. After setting parameters for the next streaming, set MODE\_SEL=1. This mode transition method can also be used for cases which do not require clock change. This mode does not cause any invalid frame both before and after the transition.

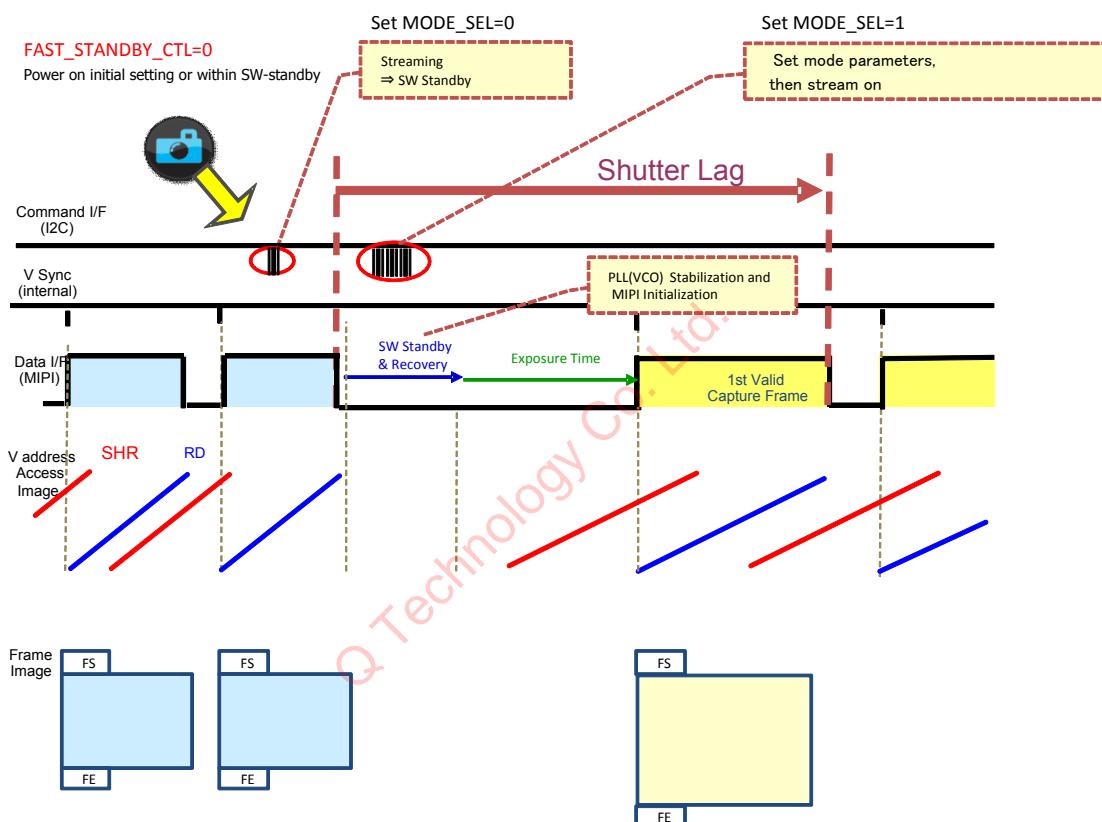


Figure 7-8 SW-standby mode transition (available for with/without clock change)

Table 7-6 SW-standby related register

I <sup>2</sup> C register	Address	Bit	Name	Description
	0x0100	[4:0]	MODE_SEL[4:0]	Mode Select 0 : Software Standby 1 : Streaming <small>*Setup other than the above is forbidden.</small>

### 7.2.5. Fast SW-standby mode transition

A diagram below illustrates mode transition sequence when clock setting change is required. This method of mode transition is shortest shutter lag and is versatile. This mode also go into the SW-standby (MODE\_SEL=0) mode once for setting mode parameters for next streaming, then get out by MODE\_SEL=1. However differently from the SW-standby mode transition, the last frame before mode transition is stopped during streaming (corrupted frame) by setting MODE\_SEL=1 under the condition FAST\_STANDBY\_CTL = 1 is set once before the mode transition, e.g. in power on sequence or during SW-standby. This mode transition method can be also used for the mode transition without clock change.

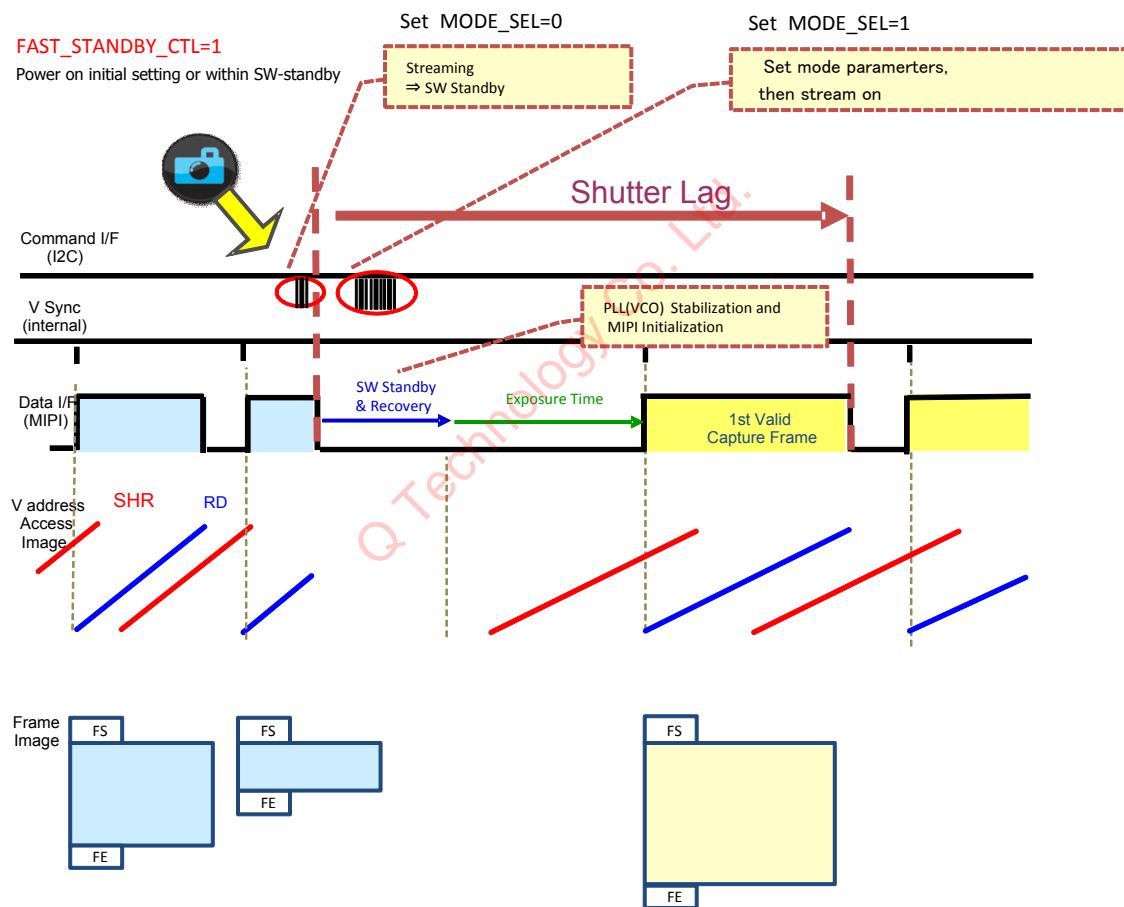


Figure 7-9 Fast SW-standby mode transition

Table 7-7 Fast SW-standby related registers

I <sup>2</sup> C regis <sup>ter</sup>	Address	Bit	Name	Description
---------------------------------------	---------	-----	------	-------------

	0x0100	[4:0]	MODE_SEL[4:0]	Mode Select 0 : Software Standby 1 : Streaming *Setup other than the above is forbidden.
	0x0106	[0]	FAST_STANDBY_CTL	0 : after outputting all current frames, switch to software standby 1 : immediately after stopping outputting all current frames, switch to software standby

### 7.2.6. Complete mode transition

A diagram below illustrates mode transition sequence when clock setting remain the same.

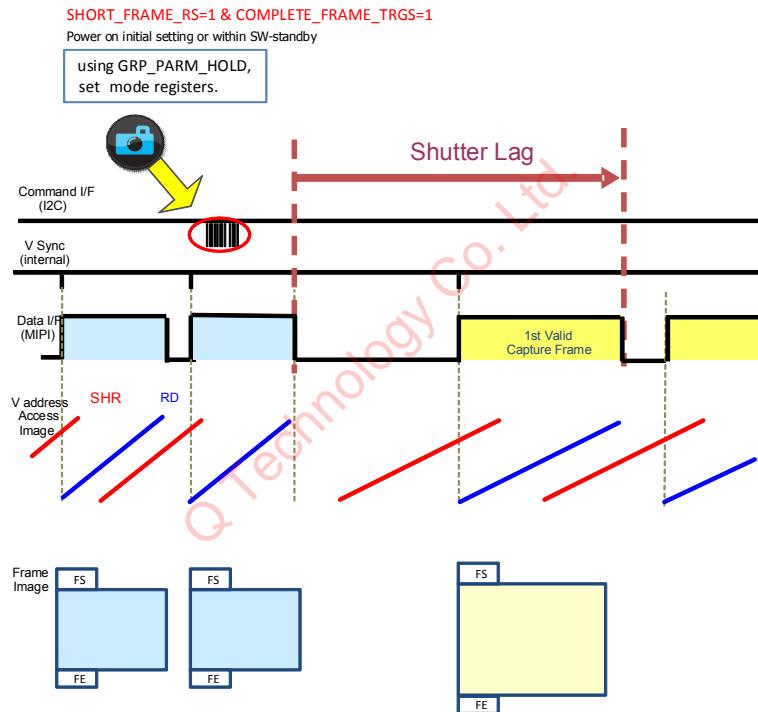


Figure 7-10 Complete mode transition (without clock change)

### 7.2.7. Truncate mode transition

A diagram below illustrates mode transition sequence for the sensor when clock setting remain the same (when corrupted frame related registers (see Table 7-4 List of corrupted frame causing registers) and CIT target register are changed at the same time).

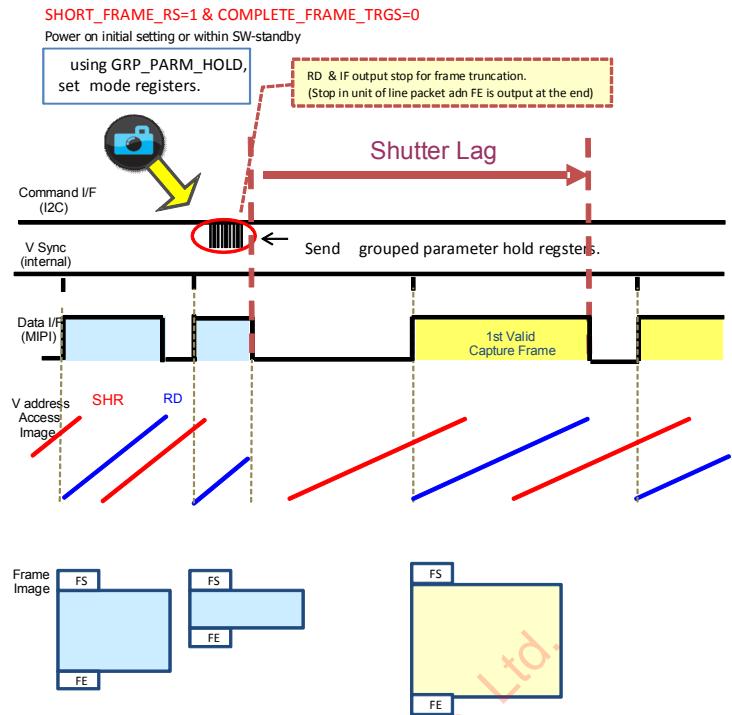


Figure 7-11 Truncate mode transition

Table 7-8 Truncate mode transition related register

	Address	Bit	Name	Description
$I^2C$ register	0x3020	[0]	SHORT_FRAME_RS	Mode transition 0: normal mode change 1: Fast mode change
	0x3F44	[0]	COMPLETE_FRAME_TRGS	Fast Mode transition (SHORT_FRAME_RS=1) 0: Truncate mode 1: Complete mode
	0x0104	[0]	GRP_PARAM_HOLD	This register is a hold register for updating multiple parameters in the same frame. 0 : consume as normal 1 : hold

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### 7.3. Exposure and gain change sequence and AE bracketing

This section describes about the timing to update changes in integration time related registers, and changes in gain system registers. In addition, it describes the method to update registers at every

vertical period using AE bracketing feature.

### 7.3.1. Integration time change sequence

Basically, GPH must be used in changing exposure time or shutter time. Set the value “1” to GRP\_PARAM\_HOLD register and set the integration duration value to COARSE\_INTEG\_TIME (CIT) register. Then set GRP\_PARAM\_HOLD back to “0”. The integration time is changed from the next frame and the image shot with the new integration time is output from the second frame after resetting GRP\_PARAM\_HOLD register.

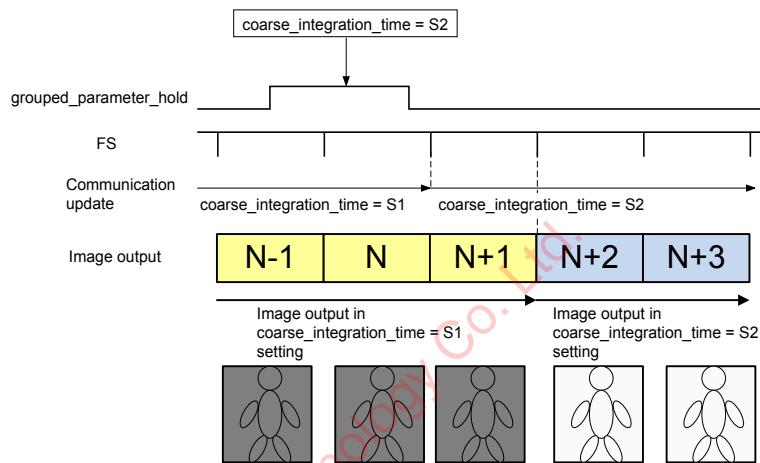


Figure 7-12 Integration time change sequence

Table 7-9 Integration time setting register

<sup>I<sup>2</sup>C register</sup>	Address	Bit	Name	Description
	0x0202	[7:0]	COARSE_INTEG_TIME[15:8]	Coarse storage time Unit : lines Format : 16-bit unsigned integer
	0x0203	[7:0]	COARSE_INTEG_TIME[7:0]	
	0x0104	[0]	GRP_PARAM_HOLD	This register is a hold register for updating multiple parameters in the same frame. 0 : consume as normal 1 : hold

### 7.3.2. Gain change sequence

With this sensor, register settings for Gain are updated 2 frames after those set with GPH. In the case of IMX214, this update timing is different because it depends on the settings of summing, however there are always 2 frames delays for the update timing with this sensor. Gain change

sequence also requires a usage of GPH together with integration time settings.

### Basic gain change sequence

Set the values to ANA\_GAIN\_GLOBAL / DIG\_GAIN\_R / DIG\_GAIN\_B/DIG\_GAIN\_GR/ DIG\_GAIN\_B/DIG\_GAIN\_GB registers. Then set GRP\_PARAM\_HOLD back to “0”. The gain values are changed from the 2nd next frame and the image shot with the new gains is output from the 2nd frame after resetting “GRP\_PARAM\_HOLD” register. Hence, if the new gain and integration time is changed within the same GPH slot, a capture with both setting in synchronous is output.

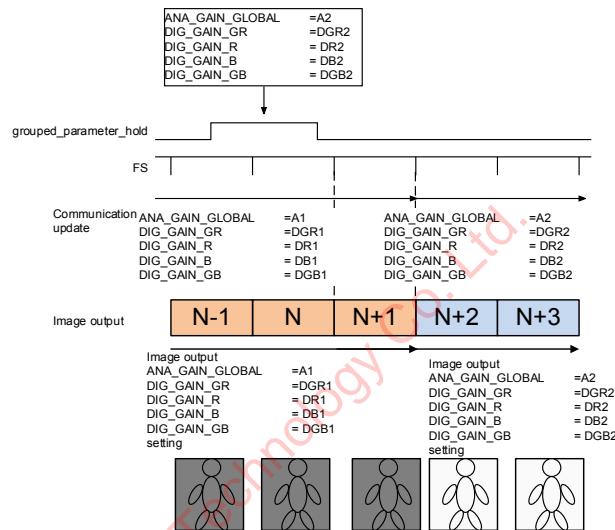


Figure 7-13 Gain change sequence

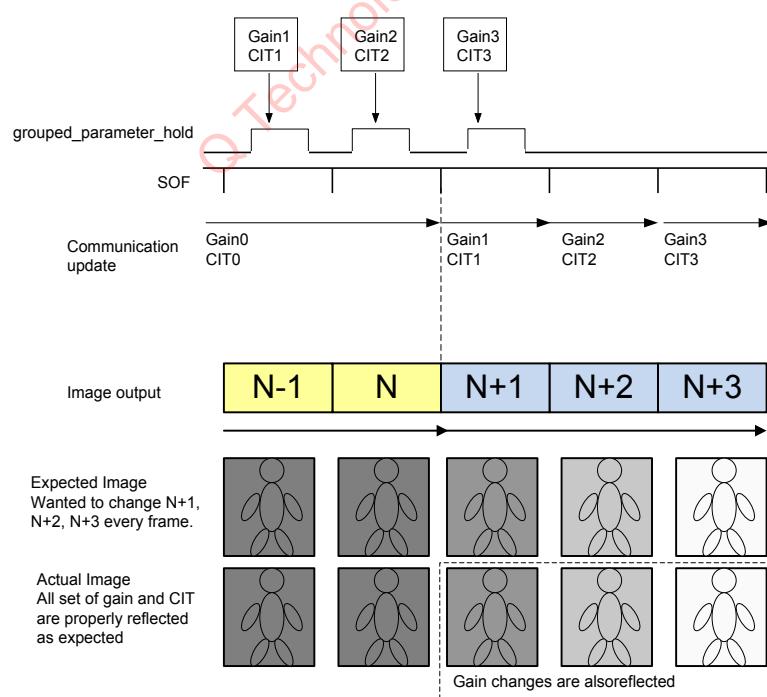
Table 7-10 Gain setting register

I <sup>2</sup> C register	Address	Bit	Name	Description
	0x0204	[1:0]	ANA_GAIN_GLOBAL[9:8]	Analog gain control code for ALL color Format : 16-bit unsigned integer Range : 0 to 960 *Setup other than the above is forbidden. Gain[times] = 1024 / ( 1024 - ANA_GAIN_GLOBAL)
	0x0205	[7:0]	ANA_GAIN_GLOBAL[7:0]	Digital gain control code for ALL color when DPGA_USE_GLOBAL_GAIN = 1 Digital gain control code for GR when DPGA_USE_GLOBAL_GAIN = 0 Format : 16-bit unsigned iReal Range : 0x0100 to 0xFFFF *Setup other than the above is forbidden.
	0x020e	[7:0]	DIG_GAIN_GR[15:8]	
	0x020f	[7:0]	DIG_GAIN_GR[7:0]	

			Gain[times] = DIG_GAIN_GR[15:8] + (DIG_GAIN_GR[7:0] / 256)
0x0210	[7:0]	DIG_GAIN_R[15:8]	Digital gain control code for R. Valid only DPGA_USE_GLOBAL_GAIN = 0. Format : 16-bit unsigned real
0x0211	[7:0]	DIG_GAIN_R[7:0]	
0x0212	[7:0]	DIG_GAIN_B[15:8]	Digital gain control code for B. Valid only DPGA_USE_GLOBAL_GAIN = 0. Format : 16-bit unsigned real
0x0213	[7:0]	DIG_GAIN_B[7:0]	
0x0214	[7:0]	DIG_GAIN_GB[15:8]	Digital gain control code for GB. Valid only DPGA_USE_GLOBAL_GAIN = 0. Format : 16-bit unsigned real
0x0215	[7:0]	DIG_GAIN_GB[7:0]	
0x3FF9	[0]	DPGA_USE_GLOBAL_GAIN	Digital Gain select 0: by color 1: all color
0x0104	[0]	GRP_PARAM_HOLD	This register is a hold register for updating multiple parameters in the same frame. 0 : consume as normal 1 : hold

With this sensor, Changing gain and CIT can be updated in every frame from HOST by using GPH.

Note that the Gain update timing differs to the IMX214. It is recommended that GPH is used for this setting.



**Figure 7-14 Gain change sequence (With CIT change)**

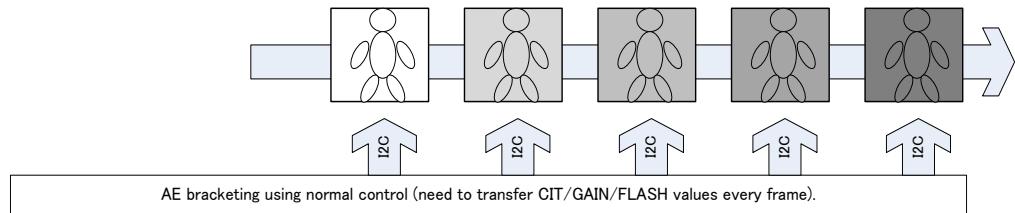
#### Constraints:

- 1) Register change shall be only CIT, analog gain and digital gain.
- 2) Host should complete settings by I2C within 1 frame (see "communication period" shown in Figure 2-15)

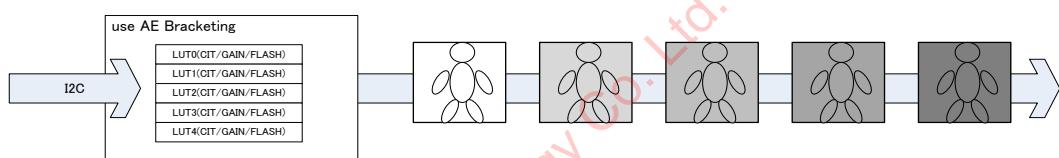
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### 7.3.3. AE bracketing

This function could be used to output the picture for up to five frames continuously, without transmitting coarse integration time, analog/digital gain, and flash settings every frame and setting by setting LUT in advance. This sensor is designed to repeat pre assigned LUT for multiple times.



**Figure 7-15 AE bracketing - without use of LUT**



**Figure 7-16 AE bracketing - with use of LUT**

**Table 7-11 AE bracketing related registers**

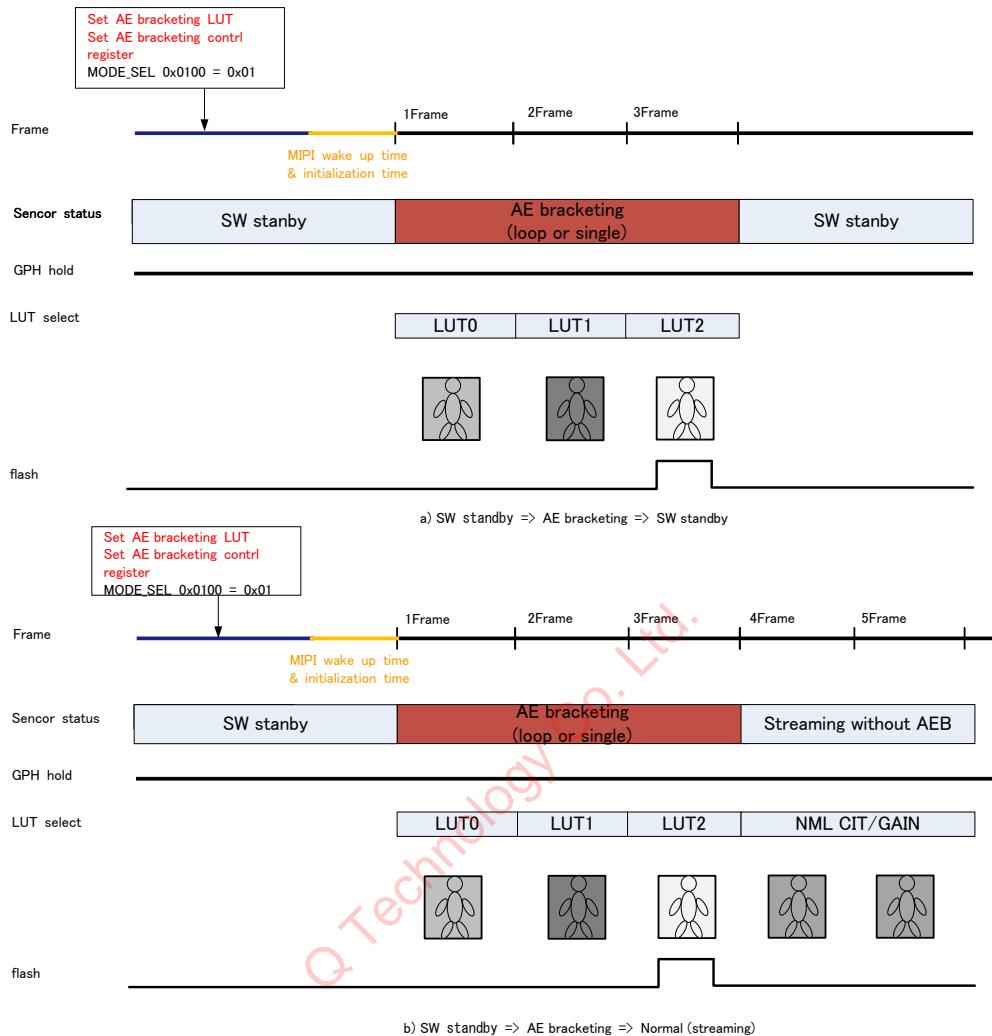
	Address	Bit	Name	Description
$I^2C$ register	0x0e00	[7:0]	BRACKETING_LUT_CTL	Bracketing Look Up Table control 0 : disabled 1 to n : bracketing over n frame. (n = type-specific parameter, and is 5(d) for this type)
	0x0e01	[7:0]	BRACKETING_LUT_MODE	Bit[0] Bracketing sequence control 0 : return to SW standby after bracketing 1 : continue in streaming after bracketing Bit[1] Loop control 0 : single bracketing 1 : loop mode Bit[2] Output mask control 0 : no output mask 1 : output mask

			Bit[7:3] Reserved
0x0104	[0]	GRP_PARAM_HOLD	This register is a hold register for updating multiple parameters in the same frame. 0 : consume as normal 1 : hold
0x0e10	[7:0]	LUT_A_COARSE_INTEG_TIME[15:8]	Coarse integration time for bracketing_LUT_frame_A
0x0e11	[7:0]	LUT_A_COARSE_INTEG_TIME[7:0]	
0x0e12	[1:0]	LUT_A_ANA_GAIN_GLOBAL[9:8]	Global analogue gain code for bracketing_LUT_frame_A
0x0e13	[7:0]	LUT_A_ANA_GAIN_GLOBAL[7:0]	
0x0e14	[7:0]	LUT_A_DIG_GAIN_GLOBAL[15:8]	Global digital gain value for bracketing_LUT_frame_A
0x0e15	[7:0]	LUT_A_DIG_GAIN_GLOBAL[7:0]	
0x0e1d	[4]	LUT_A_FLASH_TRIG_RS	Bit[3:0] Reserved Bit[4] Flash strobe trigger for bracketing_LUT_frame_A 0 : disable 1 : flash strobe is retimed to this frame Bit[7:5] Reserved
:	:	:	:
0x0e48	[7:0]	LUT_E_COARSE_INTEG_TIME[15:8]	Coarse integration time for bracketing_LUT_frame_E
0x0e49	[7:0]	LUT_E_COARSE_INTEG_TIME[7:0]	
:	:	:	:
0x0e55	[4]	LUT_E_FLASH_TRIG_RS	Bit[3:0] Reserved Bit[4] Flash strobe trigger for bracketing_LUT_frame_E 0 : disable 1 : flash strobe is retimed to this frame Bit[7:5] Reserved

See this sensor Register Map for complete set of registers for five look-up tables.

### How to control AE bracketing features

AE bracketing sequence always starts during SW-standby, but there are two possible ways to exit; 1) back to SW-standby and 2) move to streaming mode. Additionally, single mode bracketing and loop mode bracketing is available. AE bracketing function continues to repeat until setting BRACKETING\_LUT\_CTL = 0, See below for details.



**Figure 7-17 AE bracketing sequence timing chart (example of single mode)**

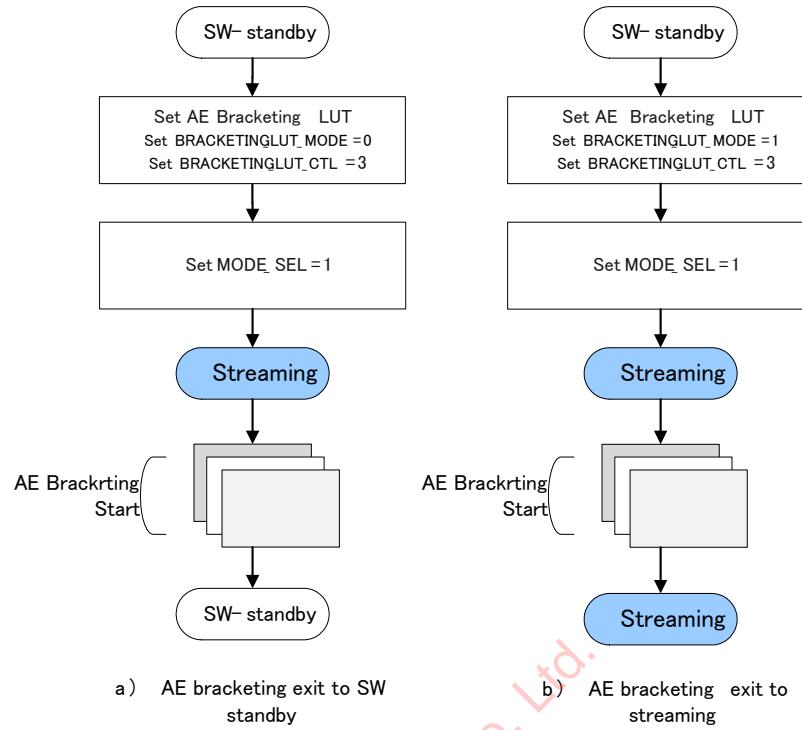


Figure 7-18 Auto bracketing sequence flow chart

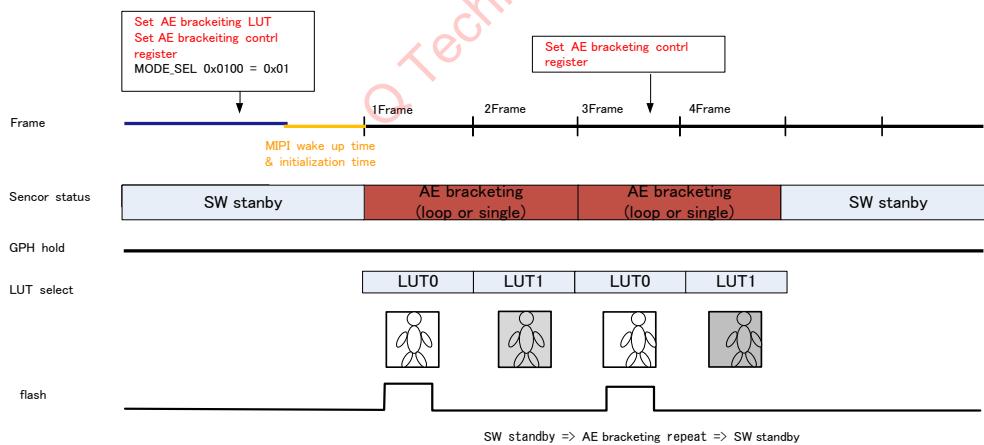
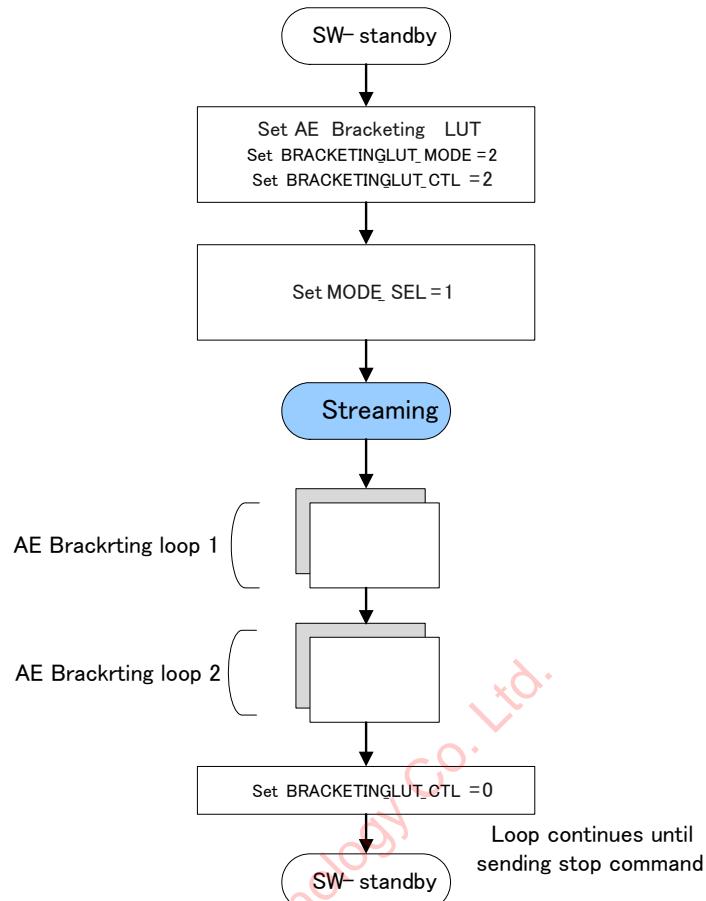


Figure 7-19 AE bracketing sequence (example of 2-repeat mode)



**Figure 7-20 AE bracketing sequence (example of 2-repeat mode)**

Above example show the limited combination of possible function for AE bracketing. Other combinations of repeat or single mode and either of exit modes are possible with those registers introduced in this paragraph.

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## 8. Miscellaneous Function

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### 8.1. Thermal meter

This function reads the thermal data from an internal sensor and averages it, it can be read as I2C or EBD data (See A-2 Embedded data lines)

Thermal meter function only works under the condition with calibration data. The calibration data is optimized by individual sensor and is measured / stored in factory area of OTP.

Also, due to moving average principle, the temperature data is only valid after completion of 8 frame moving average every time after mode transition and power on sequence.

#### 8.1.1. Thermal meter related registers

The following table shows thermal meter related control registers.

**Table 8-1 Thermal meter register setting**

Name	Address	Bit	Description
TEMP_SEN_CTL	0x0138	[0]	Temperature control enable 0 : disable 1 : enable
TEMP_SEN_OUT	0x013a	[7:0]	Temperature sensor output 0x81~0xEC -20 deg 0xED -19 deg ... 0x00 0 deg ... 0x4F 79 deg 0x50~0x7F 80 deg

### 8.1.2. Thermal meter operation sequence

Thermal meter works both during Standby and streaming. While the thermal meter is ON, transition from Standby to Streaming or Streaming to Standby is possible.

#### Temperature measurement during SW-standby

The sequence for operating the thermal gauge while in Standby is shown as follows.

Valid thermal data is output from the longer than 5.0mSec.

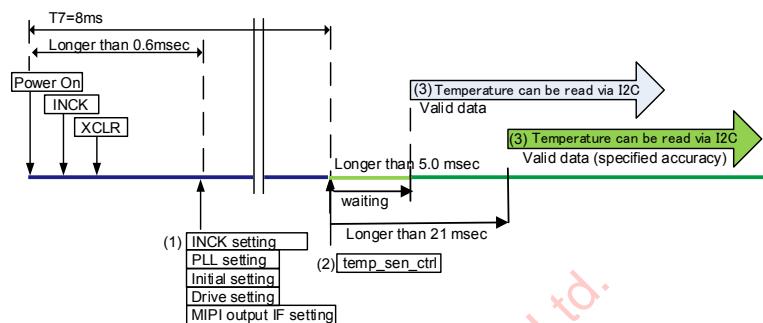


Figure 8-1 Thermal meter working in standby

Table 8-2 Thermal meter working in standby

(1)	Set the INCK frequency (0x0136,0x0137)
(2)	Set the TEMP_SEN_CTL (0x0138)
(3)	Read TEMP_SEN_OUT to get the temperature (0x013a)

#### Temperature measurement in streaming mode (1)

The following diagram and table shows about a thermal meter operation sequence working in streaming with TEMP\_SEN\_CTL being set before MODE\_SEL=1 (streaming-1)

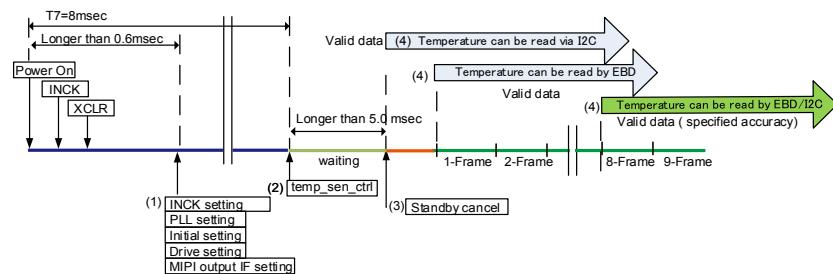


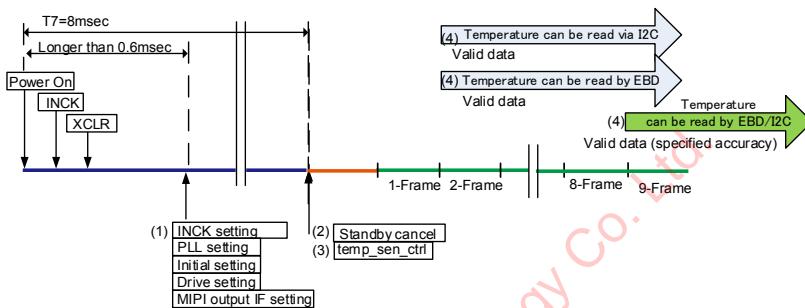
Figure 8-2 Thermal meter working in streaming (1)

**Table 8-3 Thermal meter working in streaming (1)**

(1)	Set the INCK frequency (0x0136,0x0137)
(2)	Set the TEMP_SEN_CTL (0x0138)
(3)	Set the MODE_SEL (0x0100)
(4)	Read TEMP_SEN_OUT to get the temperature (0x013a)

Temperature measurement in streaming mode (2)

The following diagram and table shows about a thermal meter operation sequence working in streaming with TEMP\_SEN\_CTL being set after MODE\_SEL=1. (streaming-2)

**Figure 8-3 Thermal meter working in streaming (2)****Table 8-4 Thermal meter working in streaming (2)**

(1)	Set the INCK frequency (0x0136,0x0137)
(2)	Set the MODE_SEL (0x0100)
(3)	Set the TEMP_SEN_CTL (0x0138)
(4)	Read TEMP_SEN_OUT to get the temperature (0x013a)

**8.1.3. Accuracy of temperature measurements**

This sensor internally performs 8 frames moving average to output higher accuracy temperature. When it operates in thermal mode during Standby and when it measures temperature during Streaming more than 8 frames after TEMP\_SEN\_CTL =1, 8 frames averaged temperature data can be obtained after 9 frames.

\* **Sensor output is guaranteed for -20-60deg ±3deg (60-80deg ±5deg).**

This specification may be changed without prior notice. And in that case, we will announce the

change to customers each time.

- \* **Thermal mode offers extremely low power consumption.**
- \* **Sensor shipped with no calibration data in OTP does not operate normally.**
- \* **If calibration data is not written in OTP, TEMP\_SEN\_OUT is 0x6c (or other fixed values) regardless of temperature.**

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## 8.2. Test pattern output (types of test patterns)

This sensor can output test patterns by using a built-in pattern generator.

### 8.2.1. Types of test patterns

This sensor has a function to output fixed video signals from a built-in test pattern generator by setting related registers.

While related register must be set to output a test pattern, there is no restriction on the sequence for setting the registers. The required test pattern can be output by setting the related registers during image capturing.

**Table 8-5 Test pattern related registers and description**

<sup>I<sup>2</sup>C register</sup>	Address	Bit	Name	Description
	0x0600			Test Pattern selection 0 : No pattern 1 : Solid color 2 : 100% color bars 3 : Fade to grey color bars 4 : PN9 *Setup other than the above is forbidden.
	0x0601	[0] [7:0]	TP_MODE [8] TP_MODE [7:0]	
	0x0602	[1:0]	TD_R [9:8]	Test data for replacing R pixels when using test patterns
	0x0603	[7:0]	TD_R [7:0]	
	0x0604	[1:0]	TD_GR [9:8]	Test data for replacing GR pixels when using test patterns
	0x0605	[7:0]	TD_GR[7:0]	
	0x0606	[1:0]	TD_B [9:8]	Test data for replacing B pixels when using test patterns
	0x0607	[7:0]	TD_B[7:0]	
	0x0608	[1:0]	TD_GB [9:8]	Test data for replacing GB pixels when using test patterns
	0x0609	[7:0]	TD_GB[7:0]	

Black level is automatically set as 0.

Registers other than those listed above are setup as the hardware initial value.

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### 8.3. Long exposure

Long exposure<sup>\*1</sup> feature is expected to be an improvement method of sensitivity in dark in some product's use case. In this section, register setting method and some important precautions on image quality impact are explained.

Note \*1: Long exposure is defined as shutter time of beyond 1/30 [sec] in this document for the convenience of explanation.

#### 8.3.1. Register setting for the long exposure

Basic idea of integration time setting is explained in "5.4.2 Integration time calculation" including shutter time setting beyond the given frame period under constraints of maximum settable range of FRM\_LENGTH\_LINES and/or LINE\_LENGTH\_PCK. In this section, Long exposure mode, elongated shutter time setting beyond the aforementioned constraints in much simpler method, is discussed.

Long exposure mode is a function to extend exposure up to approx. 128 times longer than FRM\_LENGTH\_LINES (0x0340, 0x0341) which is allowed in normal setting. This function enables long exposure by extending only V-bank without changing any other setting such as FRM\_LENGTH\_LINES and the setting of LINE\_LENGTH\_PCK (0x0342, 0x0343), while offering low power consumption.

**Table 8-6 Long exposure mode related registers**

Address	Name	Bit	Description
0x3100	CIT_LSHIFT	[2:0]	<p>Long exposure mode setting.            0 : Long exposure mode OFF            Exposure time = COARSE_INTEG_TIME            Other : Long exposure mode ON            Exposure time = COARSE_INTEG_TIME &lt;&lt; LSHIFT            ex.            1=2times            2=4times            3=8times            ...            7=128times (max setting)</p>

0x0202			Coarse storage time Unit : lines Format : 16-bit unsigned integer
0x0203	COARSE_INTEG_TIME	[15:0]	
0x0340			The length of frame Unit : lines Format : 16-bit unsigned integer
0x0341	FRM_LENGTH_LINES	[15:0]	
0x0342			The length of line Unit : pixels Format : 16-bit unsigned integer
0x0343	LINE_LENGTH_PCK	[15:0]	* LINE_LENGTH_PCK has been constrained. * Must be set fixed value as Table4-5.

### Long exposure mode setting

**Table 8-7 Setting for long exposure**

(1)	Set CIT_LSHIFT as you want
	Set COARSE_INTEG_TIME as you want
	Set FRM_LENGTH_LINES as you want
	Select LINE_LENGTH_PCK from Table4-5

The frame rate during long exposure mode is as follows:

$$\text{Frame Rate [frame/s]} = \text{Pixel_rate [pixels/s]} / (\text{Total number of pixels [pixels/frame]} \times 2^{\text{CIT\_LSHIFT}})$$

$$\text{Pixel rate [pixels/s]} = \text{IVTPXCK [MHz]} * 4 \text{ (Total number of VTPX channel)}$$

$$\text{Total number of pixels [pixels/frame]}$$

$$= \text{FRM_LENGTH_LINES [lines/frame]} * \text{LINE_LENGTH_PCK [pixels/line]}$$

The setting range of exposure time during long exposure mode is as follows:

$$1 \leq \text{COARSE_INTEG_TIME} \leq \text{FRM_LENGTH_LINES} - 18$$

### Setting example

**Table 8-8 Long exposure time related registers (example)**

4:3 full resolution output mode IVTPXCK=145MHz	CIT_LSHIFT	3d (x8)
	COARSE_INTEG_TIME	65516d
	LINE_LENGTH_PCK	5120d (initial value)
	FRM_LENGTH_LINES	65534d

### Exposure time

$$\text{Exposure time} = (65516 * 8 * 5120) / (145[\text{MHz}] * 4) = 4.63 \text{ [sec]}$$

\* When this long exposure mode is used, mode transition of SW-standby mode transition or Fast SW-standby mode transition (see 7.2.4 or 7.2.5) is recommended.

#### 8.3.2. Precautions for long exposure application

As mentioned beginning, long exposure is an effective mean to improve sensitivity in dark. However, due to and nature of elongated exposure time, there are some known image quality phenomenon of which needed to thought. It is highly recommended to make careful study for the below listed image quality items before making a decision.

- 1) Growth in level and count of white spots in the dark. (See Table 8-9)
- 2) Increments of black level attributable to dark signal may happen. (See Table 8-9)
- 3) Quantization noises of 10bit system become discernable in exchange of improvement in random noise performance. Basically, the phenomenon is more perceptible with a frame addition of multiple frames shot under condition of long exposure and low analog gain.

**Table 8-9 Example capture of dark image over different exposure time**

Exposure Time	1/30s	1/10s	1/3s	1s	3s
Dark Image					
Black level (dec)	63.42	63.41	63.46	63.53	63.76

Note) As setting exposure time longer, white spot count becomes more and its level and the black level goes higher. Note that above captures are obtained with dynamic DPC OFF using typical sensor type only for an

explanatory purpose. Turning on the dynamic DPC makes single defect corrected but couplet or cluster defects left uncorrected. Practically, couplet or cluster defects are subjects for evaluation.

**Table 8-10 Quantization error example over an addition of multiple long exposure frames**

Gain (dB)	Frame Addition: 0 Exposure time/frame = 2sec	Frame Addition: 32 Exposure time/frame = 2sec
0		
6		
12		Vertical banding FPN is slightly discernable
18		
24		

Note) As setting exposure time longer and frame addition more in addition to a small analog gain setting, quantization error and/or fixed pattern noise become more perceptible. Note that the above captures are obtained using typical sensor type is enhanced with higher gamma for explanation purpose only.

It is essential that these characteristics that would be attributable to long exposure time shall be evaluated and judged by yourself referring to your product application. Following information may help in understanding the distinctive performances relating to elongated exposure time and then making evaluation plans.

- White spot: Allowable white spots are specified with the signal level and numbers under exposure time of 1/30 [s]. The signal level of white spots is proportional to the exposure time. see "Spot Pixel Specification" in the data sheet for actual level and allowable spot count at the time of shipment.
- Dark signal: Dark signal is specified with the unit of LSB under exposure time of 1/15 [s] in darkness.

The dark signal increases as exposure time become longer and somehow affect the gradation characteristics.

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#### 8.4. Flash light control sequence

This sensor can internally generate the control pulse assuming to trigger the flash light emission and output from the external pins. The flash light trigger pulse width and output timing can be controlled by registers shown in Table9-9. Flash control pulse is output from FSTROBE pins. The setting of strobe pulse is determined by reference point, delay and trigger mode. Details of setting are explained by following sections.

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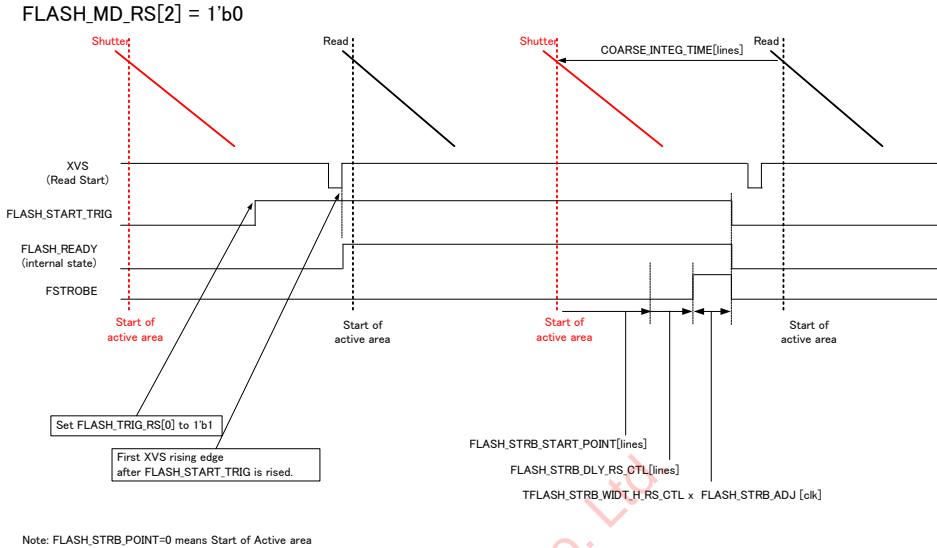
**Table 8-11 Flash light control setting registers**

I <sup>2</sup> C register	Address	Bit	Name	Description	Notes
	0x0c12	[7:0]	FLASH_STRB_ADJ [7:0]	Register to control counter for flash pulse width in rolling shutter mode. Flash pulse width (high) = $(TFLASH_STRB_WIDT_H_RS_CTL / INCK frequency) * FLASH_STRB_ADJ$ Flash pulse width (low) = $(TFLASH_STRB_WIDT_L_RS_CTL / INCK frequency) * FLASH_STRB_ADJ$ Range : 1 to 255	
	0x0c14	[7:0]	FLASH_STRB_START_POINT [15:8]	Register to select reference point for flash pulse in rolling shutter mode.	
	0x0c15	[7:0]	FLASH_STRB_START_POINT [7:0]	Adjustable in one line steps. Range : 0 to last line	
	0x0c16	[7:0]	TFLASH_STRB_DLY_RS_CTL [15:8]	Register to control the rising edge point of Flash pulse from FLASH_STRB_START_POINT in rolling shutter mode. Step : 1H Range : 0 to 65535	
	0x0c18	[7:0]	TFLASH_STRB_WIDTH_H_RS_CTL [15:8]	Register to control the high level width of flash pulse in rolling shutter mode. Flash pulse width (high) = $(TFLASH_STRB_WIDT_H_RS_CTL / INCK frequency) * FLASH_STRB_ADJ$	
	0x0c19	[7:0]	TFLASH_STRB_WIDTH_H_RS_CTL [7:0]	Bit[0] flash pulse mode control 0 : single trigger mode. 1 : continuous mode. Bit[1] flash pulse complete or truncated select 0 : complete pulse mode in rolling shutter mode 1 : truncated pulse mode in rolling shutter mode Bit[2] reference start point select 0 : exposure 1 : readout (in rolling shutter mode) Bit[3] flash pulse sync or async select 0 : synchronous 1 : asynchronous Bit[4] Reserved	
	0x0c1a	[7:0]	FLASH_MD_RS [7:0]		

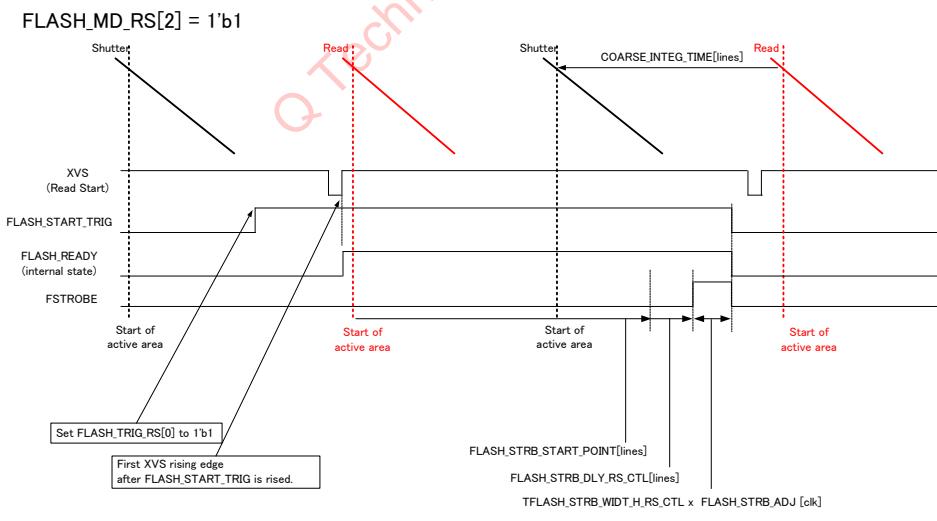
			Bit[5] flash pulse single or multi select 0 : single 1 : multiple Bit[7:6] Reserved	
0x0c1b	[7:0]	FLASH_TRIG_RS [7:0]	Flash trigger 0 : disable 1 : enable *Return to 0 in single mode, automatically *Setup other than the above is forbidden.	
0x0c1c	[7:0]	FLASH_STAT [7:0]	Bit[0] flash pulse status 0 : Not retimed to this frame 1 : Retimed to this frame When using a flash light control sequence in the AEB mode, this register is tied to 0. Bit[1] flash status for global reset mode *not supported 0 : Not active in global reset mode 1 : Active in global reset mode Bit[7:2] Reserved	read only
0x0c26	[7:0]	TFLASH_STRB_WIDTH2_H_RS_CTL [15:8]	Register to control the high level width of 2nd flash pulse in rolling shutter mode when TFLASH_STRB_CNT_RS_CTL=2. Range : 1 to 65535	
0x0c27	[7:0]	TFLASH_STRB_WIDTH2_H_RS_CTL [7:0]	2nd Flash pulse width (high) = (TFLASH_STRB_WIDT2_H_RS_CTL / INCK frequency ) * FLASH_STRB_ADJ	
0x0c28	[7:0]	TFLASH_STRB_WIDTH_L_RS_CTL [15:8]	Register to control the low level width of flash pulse in rolling shutter mode. Range : 1 to 65535	
0x0c29	[7:0]	TFLASH_STRB_WIDTH_L_RS_CTL [7:0]	Flash pulse width (low) = (TFLASH_STRB_WIDT_L_RS_CTL / INCK frequency ) * FLASH_STRB_ADJ	
0x0c2a	[7:0]	TFLASH_STRB_CNT_RS_CTL [7:0]	Register to control flash pulse count in rolling shutter mode. Range : 1 to 255	

### 8.4.1. Reference point

Reference point is the base point of delay settings for flash control pulse and can be determined by FLASH\_MD\_RS[2]. As example, following charts shows single trigger mode. It is also same for other trigger modes.



**Figure 8-4 Reference point (Start of exposure)**



**Figure 8-5 Reference point (Start of readout)**

### 8.4.2. Single trigger mode / Continuous mode

This sensor supports both single trigger strobe mode and continuous mode.

Single trigger mode is enabled by setting FLASH\_MD\_RS[0] to 1'b0.

FLASH\_MD\_RS[0] = 1'b0

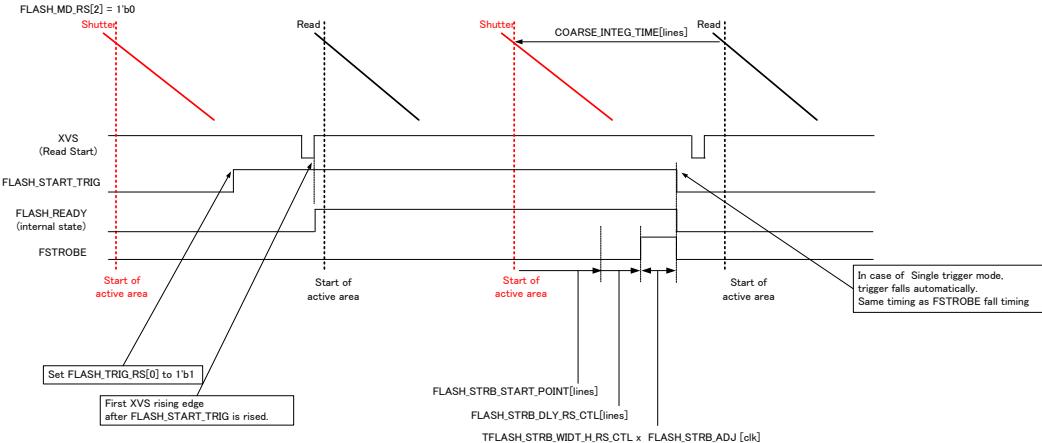


Figure 8-6 Single Trigger mode

Continuous mode is enabled by setting FLASH\_MD\_RS[0] to 1'b1. In this mode, flash control pulse can be output both continuously and periodically.

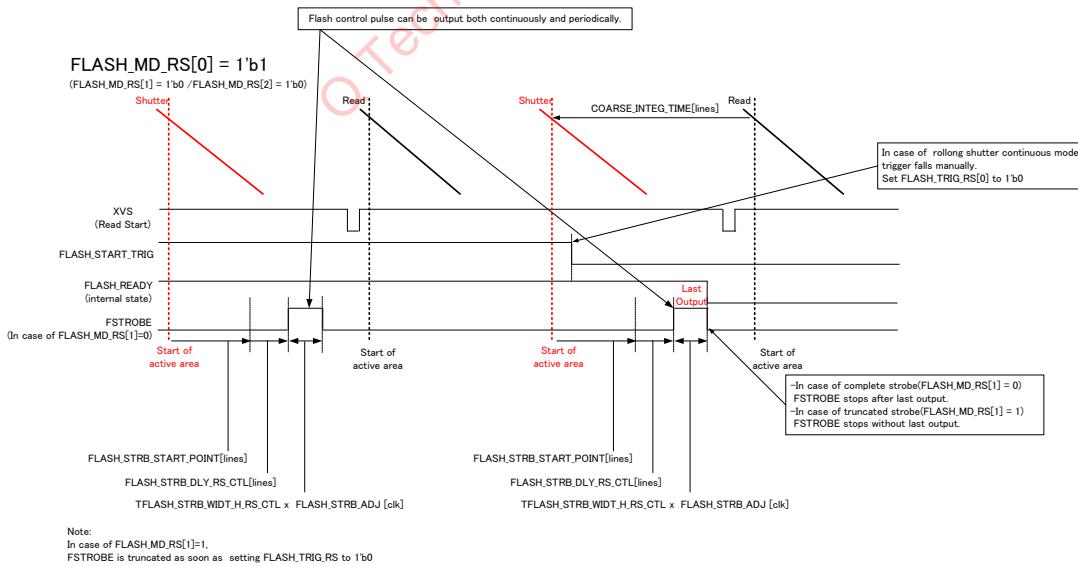


Figure 8-7 Continuous mode

### 8.4.3. Multiple strobe

This sensor supports both single flash strobe mode and multiple flash modes. Multiple flash strobe mode is enabled by setting FLASH\_MD\_RS[5] to 1'b1. In this mode, more than one output of flash control pulse can be controlled. Multiple strobes can set not only in single trigger mode but also in continuous mode. Following chart shows single trigger mode and reference point of shutter as an example. Number of flash control pulse is determined by TFLASH\_STRB\_CNT\_RS\_CTL. In case more than 3 strobes are output in 1 frame, width of strobe pulse can't be set separately. On the other hand, dual flash strobe can control the pulse width separately. Following Table shows duty and width period that you can set.

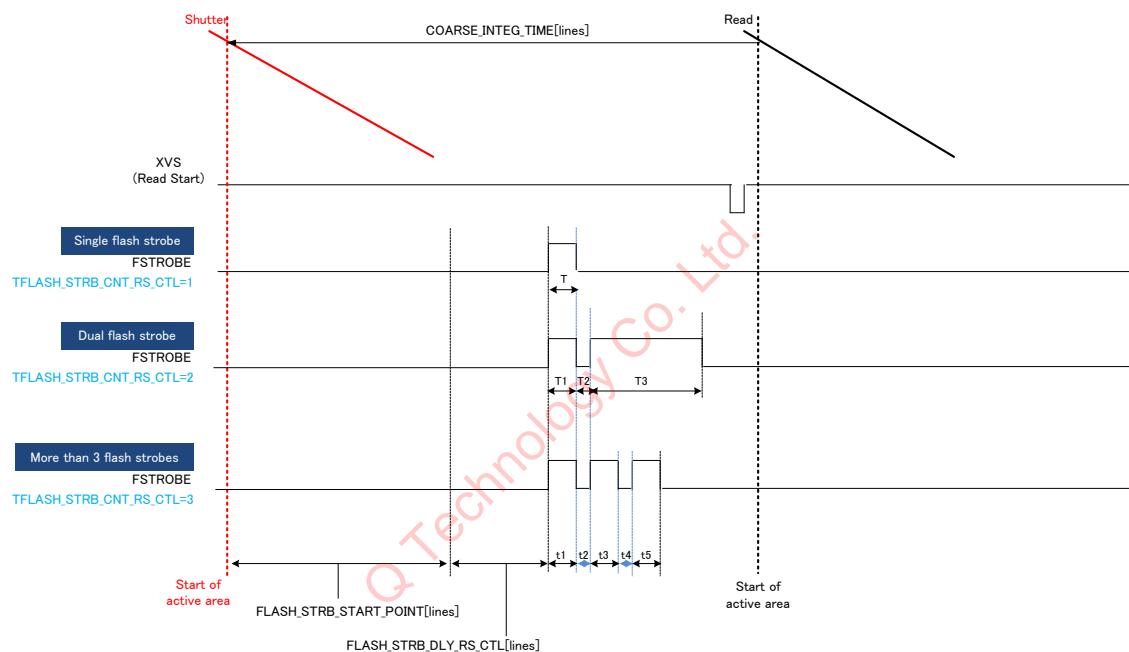


Figure 8-8 Single flash strobe / Multiple flash strobe

**Table 8-12 Single Flash strobe duty control register**

Time	Register
T	TFLASH_STRB_WIDTH_H_RS_CTL × FLASH_STRB_ADJ[clk]

**Table 8-13 Dual Flash strobe duty control register**

Time	Register
T1	TFLASH_STRB_WIDTH_H_RS_CTL × FLASH_STRB_ADJ[clk]
T2	TFLASH_STRB_WIDTH_L_RS_CTL × FLASH_STRB_ADJ[clk]
T3	TFLASH_STRB_WIDTH2_H_RS_CTL × FLASH_STRB_ADJ[clk]

**Table 8-14 More than 3 Flash strobe duty control register**

Time	Register
t1	TFLASH_STRB_WIDTH_H_RS_CTL × FLASH_STRB_ADJ[clk]
t2	TFLASH_STRB_WIDTH_L_RS_CTL × FLASH_STRB_ADJ[clk]
t3	TFLASH_STRB_WIDTH_H_RS_CTL × FLASH_STRB_ADJ[clk]
t4	TFLASH_STRB_WIDTH_L_RS_CTL × FLASH_STRB_ADJ[clk]
t5	TFLASH_STRB_WIDTH_H_RS_CTL × FLASH_STRB_ADJ[clk]

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## 8.5. One time programmable (OTP) memory

See OTP Manual of this sensor

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## 8.6. Pulse for OIS driver

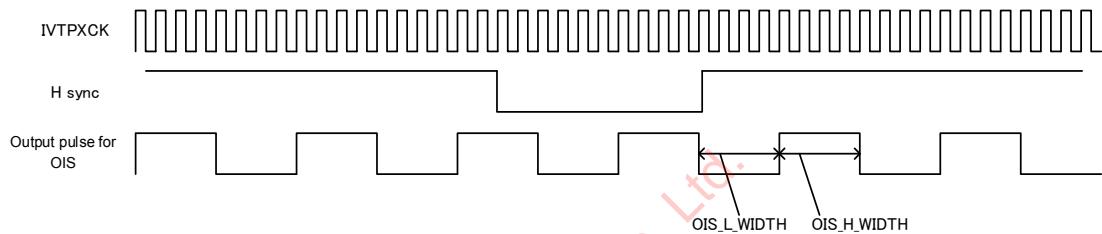
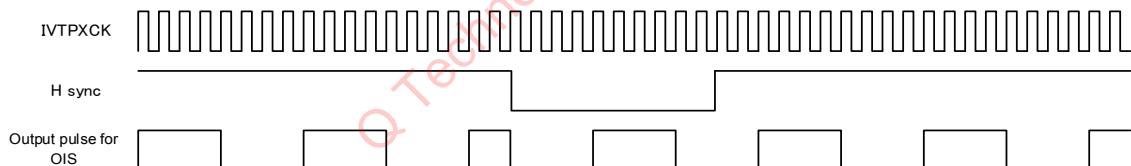
This sensor can output the pulse for OIS driver. This pulse is generated from IVTPXCK.

High period and Low period can be set by registers. The pulse can be reset by H sync.

Refer to 8.7 “Monitor terminal settings” for outputting OIS Pulse from the monitor terminal.

**Table 8-15 Pulse output setting registers for OIS driver**

I2C register	Address	Bit	Name	Description
	0x3FE0 0x3FE1	[15:0]	OIS_H_WIDTH	High frequency pulse output for OIS driver is set with IVTPXCK cycle number [1-65535] (def:8)
	0x3FE2 0x3FE3	[15:0]	OIS_L_WIDTH	Low frequency pulse output for OIS driver is set with IVTPXCK cycle number [1-65535] (def:8)
	0x4bc6	[0]	OIS_HRESET_EN	Enable H sync reset for pulse output for OIS driver. (def:0) 0: Do not reset 1: Reset with H sync

**Figure 8-9 OIS\_HRESET\_EN=0 operation****Figure 8-10 OIS\_HRESET\_EN=1 operation**

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### 8.6.1. CDS Frequency

$$\text{CDS Frequency[KHz]} = (\text{IVTPXCK[MHz]} \times 1000) / (\text{CDS Clock})$$

This sensor's CDS clock cycle are shown below.

**Table 8-16 CDS clock cycle**

Operation mode	CDS Clock [cycle] @IVTPXCK
Full resolution	276
2 Binning	276

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### 8.7. Monitor terminal settings

This sensor can output 3 internal signals (H Sync/V Sync/OIS pulse) via monitor terminals.

The monitor terminals mean the following two(2) terminals, such as XVS(39 pin) and GPO(53 pin) See the following table for register settings.

**Table 8-17 Monitor terminal setting**

I2C register	Address	Bit	Name	Setting value
	0x4289	[1:0]	OUTIF1	XVS IO Control 0d : Output
	0x428A	[1:0]	OUTIF2	GPO IO Control 0d : Output
	0x42B0	[4:0]	CKTESTSEL[4:0]	Monitor select 0d : Output
	0x4270	[4:0]	GPIOSEL	00h
	0x4BD5	[7:0]	MNTTEST3_SEL[7:0]	19d: H sync is selected. 20d: V sync is selected. 22d: OIS Pulse is selected.
	0x4BD6	[7:0]	MNTTEST2_SEL[7:0]	
	0x4BD7	[7:0]	MNTTEST1_SEL[7:0]	
	0x42A9	[7:0]	TESTMNT1	FFh: XVS's signal is selected by MNTTEST1_SEL[7:0] FEh: XVS's signal is selected by MNTTEST2_SEL[7:0] FDh: XVS's signal is selected by MNTTEST3_SEL[7:0]
	0x42AA	[7:0]	TESTMNT2	FFh: GPO's signal is selected by MNTTEST1_SEL[7:0] FEh: GPO's signal is selected by MNTTEST2_SEL[7:0] FDh: GPO's signal is selected by MNTTEST3_SEL[7:0]

#### GPO (53 pin)

V sync / H sync / OIS Pulse can be selected and output via GPO pin.

Signal is selected by MNTTEST1\_SEL[8:0] (TESTMNT2 [7:0] = FFh ) or MNTTEST2\_SEL [8:0]

( TESTMNT2 [7:0] = FEh ) or MNTTEST3\_SEL [8:0] ( TESTMNT2 [7:0] = FDh )

#### XVS (39 pin)

V sync / H sync / OIS Pulse can be selected and output via XVS pin.

Signal is selected by MNTTEST1\_SEL[8:0] (TESTMNT1 [7:0] = FFh ) or MNTTEST2\_SEL [8:0] ( TESTMNT1 [7:0] = FEh ) or MNTTEST3\_SEL [8:0] ( TESTMNT1 [7:0] = FDh )

#### **Setting examples:**

Case1: simultaneous output of H sync and OIS Pulse.

**Table 8-18 Monitor Setting example case 1**

Pin name	Selected Signal	Setting value
GPO	H sync	MNTTEST2_SEL :19d, MNTTEST3_SEL :22d, TESTMNT2:FEh, TESTMNT1: FDh GPIOSEL:00h
XVS	OIS Pulse	

Case2: simultaneous output of OIS Pulse and V sync.

**Table 8-19 Monitor Setting example case 2**

Pin name	Selected Signal	Setting value
GPO	OIS Pulse	MNTTEST2_SEL :22d, MNTTEST3_SEL :20d, TESTMNT2:FEh, TESTMNT1: FDh GPIOSEL:00h
XVS	V sync	

Case3: simultaneous output of V sync and H sync.

**Table 8-20 Monitor Setting example case 3**

Pin name	Selected Signal	Setting value
GPO	V sync	MNTTEST2_SEL :20d, MNTTEST3_SEL :19d, TESTMNT2:FEh, TESTMNT1: FDh GPIOSEL:00h
XVS	H sync	

### 8.7.1. V sync / H sync

V sync and H sync are the internal timing of image sensor.

V sync is the timing of the frame unit, and H sync is the line unit ones. Polarity and Pulse width of V sync / H sync can be set.

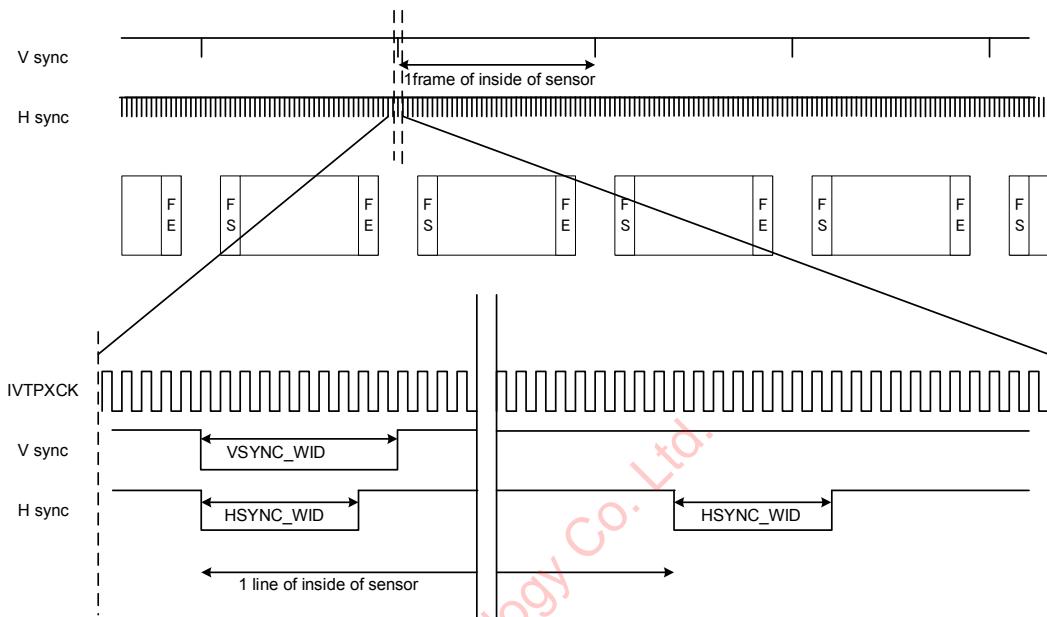


Figure 8-11 Image of V sync / H sync

Table 8-21 V sync / H sync settings

I2C register	Address	Bit	Name	comment
	0x510C	[0]	VSYNC_POL	Polarity of V sync Pulse (def:0) 0:Lo-Active, 1:Hi-Active
	0x510D	[2:0]	VSYNC_WID	Pulse width of V sync Pulse (Unit: IVTPXCK cycle) (def:0) 0d: x10 1d: x20 2d: x50 3d: x100 4d: x200 5d: x500 6d: x1000 7d: x2000
	0x510E	[0]	HSYNC_POL	Polarity of H sync Pulse (def:0) 0:Lo-Active, 1:Hi-Active
	0x510F	[2:0]	HSYNC_WID	Pulse width of H sync Pulse (Unit: IVTPXCK cycle) (def:0) 0d: x10 1d: x20 2d: x50 3d: x100 4d: x200 5d: x500 6d: x1000 7d: x2000

### 8.7.2. Setting value output

This sensor can output the setting value(low or high) via monitor terminals. The monitor terminals mean the following three(3) terminals, such as FSTROBE, XVS, and GPO.

**Table 8-22 Setting value output from FSTROBE pin**

I2C register	Address	Bit	Name	comment
I2C register	0x3e50	[0]	GPO_CTRL0[8:0]	FSTROBE pin [8] : Output CTRL 0 Disable : Controlled by sensor (default) 1 Enable : Controlled by user [7:1]: Reserved [0] : Output Value 0: low output (default) 1: high output
	0x3e51	[7:0]		

**Table 8-23 Setting value output from XVS pin**

I2C register	Address	Bit	Name	comment
I2C register	0x3e52	[0]	GPO_CTRL1[8:0]	XVS pin [8] : Output CTRL 0 Disable : Controlled by sensor (default) 1 Enable : Controlled by user [7:1]: Reserved [0] : Output Value 0: low output (default) 1: high output
	0x3e53	[7:0]		

**Table 8-24 Setting value output from GPO pin**

I2C register	Address	Bit	Name	comment
I2C register	0x3e54	[0]	GPO_CTRL2[8:0]	GPO pin [8] : Output CTRL 0 Disable : Controlled by sensor (default) 1 Enable : Controlled by user [7:1]: Reserved [0] : Output Value 0: low output (default) 1: high output
	0x3e55	[7:0]		

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### 8.8. Dual camera operation

This section describes a method of dual camera operation, which outputs pair of synchronous images from two sensors controlled by one host device. This sensor can be either of a master or a slave device by register configurations. When a sensor operates as a master device, it controls vertical synchronous timings and outputs synchronous signal called V-sync signal or XVS signal for a slave device. When a sensor operates as a slave device, it outputs images synchronizing with V-sync

or XVS signal.

In Sony CIS, there are two dual camera control methods. One is Full-synchronous system and the other is Quasi-synchronous system.

In Full-synchronous system, the master device controls shutter and read timings of the slave device and in Quasi-synchronous system, the master device can only control shutter timings of the slave device and read timings are controlled by slave register settings.

This sensor has Quasi-synchronous system.

The main feature of Quasi-synchronous system is that Coarse integral time of the slave device is absolutely guaranteed by the register setting whereas in Full synchronous system, Coarse integral time of slave sensor has a possibility of shortened by synchronous signal from master device because the read timing of slave sensor synchronized with master synchronous signal.

This sensor has following functions:

- CCI 1<sup>st</sup> and 2<sup>nd</sup> address configuration.
- XVS signal multiplied , thinned-out and delay function in master/slave mode.
- XVS pin connectivity check for debugging.

In dual camera system, master/slave sensor can be operated with a different operation mode. Host shall be taken care in real time domain[in [sec]], not in COARSE\_INTEG\_TIME setting because 1H timing may be different in master/slave sensor.

Each sensor is possible to change gain settings individually while keeping synchronous relation between sensors.

### 8.8.1. CCI 1<sup>st</sup> and 2<sup>nd</sup> slave address for dual camera

The CCI slave 1<sup>st</sup> and 2<sup>nd</sup> address is shown in the following Table 8-25, Table 8-26.

See chapter 2.3.1 and 2.3.2 for detail..

**Table 8-25 1<sup>st</sup> slave address**

Slave address (Write or Read)											SLASEL
Bit [7:0]	7	6	5	4	3	2	1	0*	Type	Value	SLASEL
Bit value	0	0	1	1	0	1	0	0	Write	0x34	L or NC
	0	0	1	1	0	1	0	1	Read	0x35	
Bit [7:0]	7	6	5	4	3	2	1	0*	Type	Value	SLASEL
Bit value	0	0	1	0	0	0	0	0	Write	0x20	H
	0	0	1	0	0	0	0	1	Read	0x21	

Note \* : Bit[0] is R/W setting bit.

**Table 8-26 2<sup>nd</sup> slave address**

Bit [7:0]	7	6	5	4	3	2	1	0*	Type	Value
Bit value	0	1	1	0	1	1	0	0	Write	0x6C
	0	1	1	0	1	1	0	1	Read	0x6D

Note \* : Bit[0] is R/W setting bit.

### 8.8.2. Block diagram

Figure 8-12 shows an example block diagram of the dual camera system using synchronous signal. In this example, accessing two sensors is achieved with shared CCI bus by having two different 1<sup>st</sup> CCI addresses and two common 2<sup>nd</sup> CCI addresses between two sensors. Dual camera synchronization is realized by connecting synchronous signal: XVS signal, V-sync signal. Refer to the Figure 8-16 for the definition of XVS signal and V-sync signal.

1<sup>st</sup> sensor: master mode function

- Outputs the XVS signal from the XVS pin.
- The XVS signal can be replaced with V-sync signal using XVS pin and GPO pin with some constraints, refer to 8.8.4 for more details.
- If a slave device is not a Sony product, select the XVS signal or V-sync signal according to slave device requirements.

2<sup>nd</sup> sensor: slave mode function

- Receive the XVS signal if a master device is a Sony product.
- Receive the V-sync signal if a master device is not a Sony product.

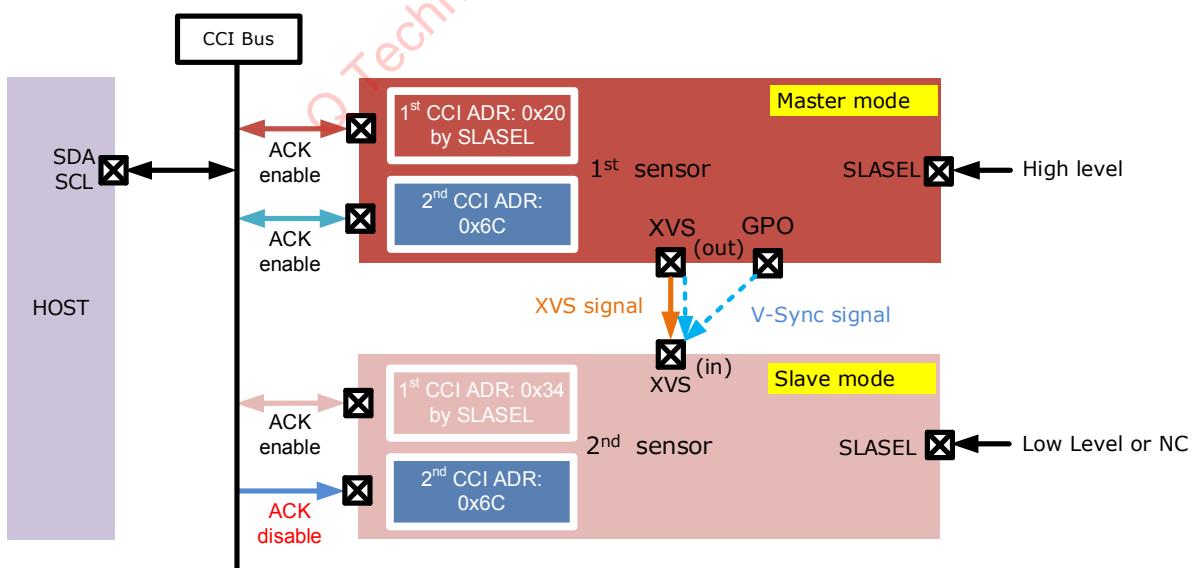


Figure 8-12 Dual camera system block diagram with synchronous signal

### 8.8.3. Control sequence

Figure 8-13 shows a control sequence of the dual camera operation with the shared CCI bus.

In Figure 8-13, it is important that a register “MODE\_SEL” setting for the slave device shall be set first.

In shared CCI bus connection, CCI address setting should be set as follows,

- Any settings using 1<sup>st</sup> CCI addresses are independently applied for each sensor.
- Settings with 2<sup>nd</sup> CCI address are commonly applied for both sensors.

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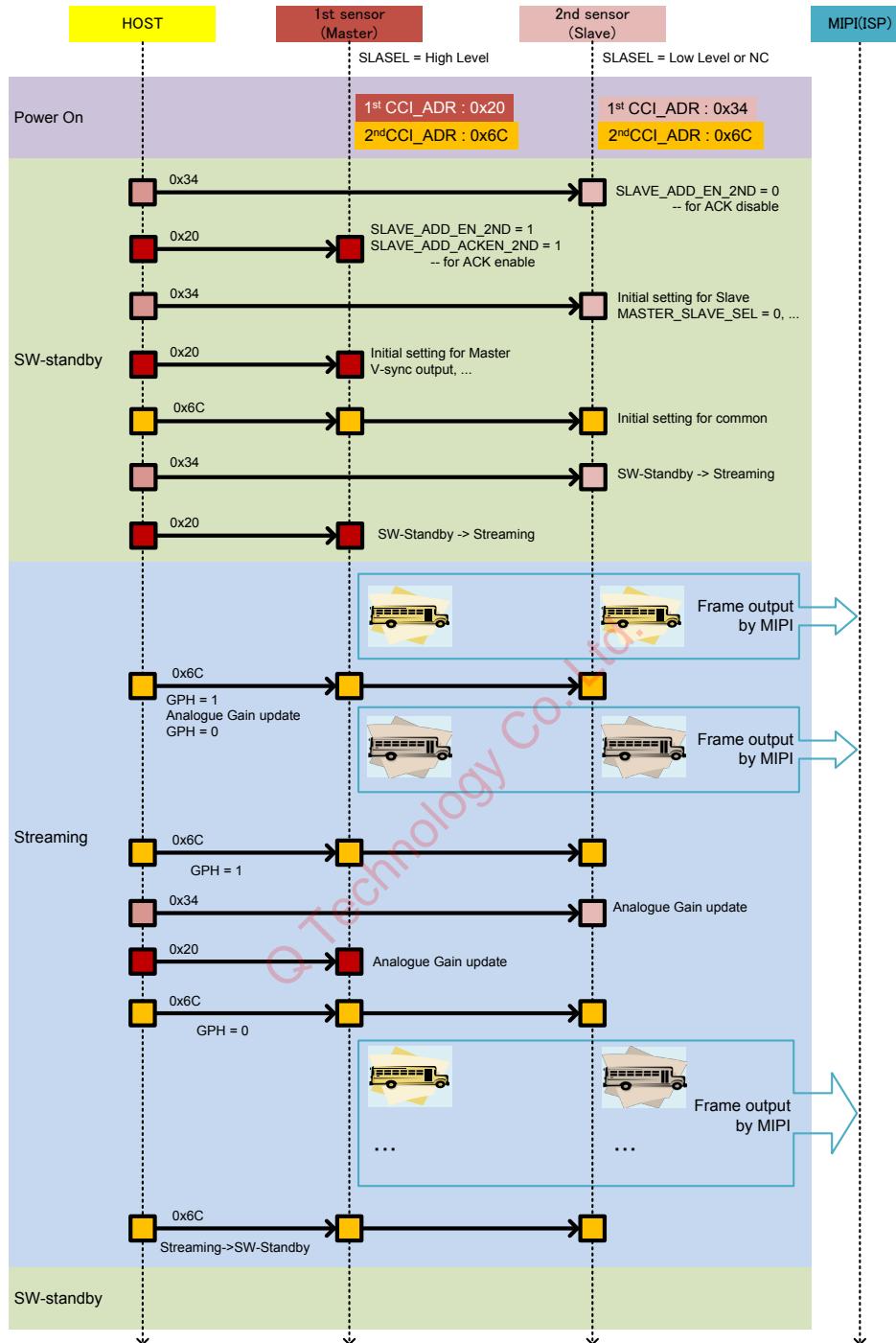


Figure 8-13 Control sequence of the dual camera operation with the shared CCI bus

#### 8.8.4. Usage in master mode

This chapter describes master mode settings. When the sensor is used in master mode, XVS and GPO pins are available for a synchronous output signal to a slave device.

The relationship between Pin and Signal name is shown in Table 8-27.

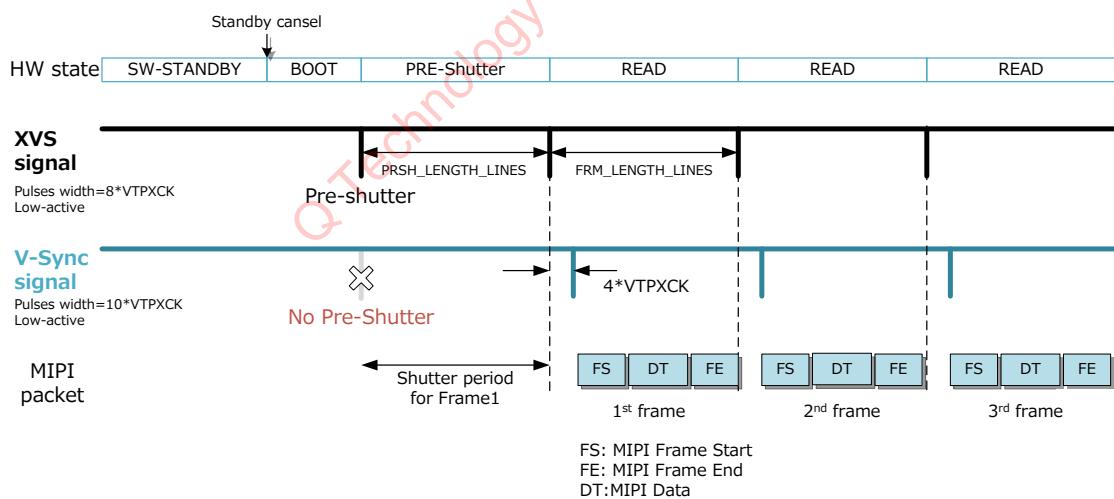
**Table 8-27 XVS and GPO specification**

Pin name	Signal name	Pre-shutter pulse	Delay,Thin-out, Multiple output
XVS(39pin)	XVS signal	Available	Available
	V-Sync signal	Not Available	Not Available
GPO(53pin)	V-Sync signal	Not Available	Not Available

Figure 8-14 shows the difference between the XVS signal and the V-Sync signal. Regarding the XVS signal, a first pulse, which called a Pre-shutter pulse is outputted. The Pre-shutter pulse can be used as triggering the pre-shutter timing at a slave sensor. Regarding the V-Sync signal, Pre-shutter pulse is not outputted.

XVS pin is pulled up.

### Master mode



**Figure 8-14 Difference between XVS signal and V-Sync signal**

V-Sync signal delays four cycles of VTPXCK with respect to XVS signal because of H/W internal delay. If Sony product is chosen as a slave device, use the XVS signal to output 1<sup>st</sup> frame simultaneously as master sensor. If a Sony product is not chosen as a slave device, choose XVS signal or V-sync signal according to a slave device requirement.

Table 8-28 shows the register setting for master.

**Table 8-28 Master mode related registers without output signal setting.**

Address	Bit	Name	Description	Master Mode Setting (HEX)
0x3F0B	[0]	MC_MODE	Multi Camera mode setting 0 : Minimum time mode (default) Pre-shutter period is defined by COARSE_INTEG_TIME 1 : Fixed time mode Pre-shutter period is defined by PRSH_LENGTH_LINES	1'h1
0x3041	[0]	MASTER_SLAVE_SEL	Master or Slave mode setting 0 : Slave mode 1 : Master mode (default)	1'h1 (default)
0x3F39 ~ 0x3F3B	[23:0]	PRSH_LENGTH_LINES	Pre-Shutter period [line] 0: Prohibited Effective if PRESHR_MODE=1 Set COARSE_INTEG_TIME+20 Where 20 is hardware dependent fixed value:	See description
0x0350	[0]	FRM_LENGTH_CTL	Frame length automatic tracking control Select whether or not the frame length is changed automatically when FRM_LENGTH_LINES < COARSE_INTEG_TIME + $\alpha$ ( $\alpha$ = type-specific adjustment parameter, and is CIT_MARGIN for this type) 0 : no automatic tracking control of frame length In this case, [FRM_LENGTH_LINES - $\alpha$ ] operates instead of COARSE_INTEG_TIME 1 : automatic tracking control of frame length In this case, [COARSE_INTEG_TIME + $\alpha$ ] operates instead of FRM_LENGTH_LINES	0

The period of XVS signal and V-Sync signal can be calculated by following equations.

$$T_{period}[s] = \text{Total number of pixel clocks [pixel clocks/frame]} / \text{Pixel_rate [pixels/s]}$$

where

*Total number of pixel clocks [pixel clocks/frame]*

$$= \text{FRM\_LENGTH\_LINES} [\text{lines/frame}] \times 2^{\text{CIT\_LSHIFT}} \times \text{LINE\_LENGTH\_PCK} [\text{pixel clocks/line}]$$

*Pixel\_rate*[pixels/s]

$$= \text{VTPXCK\_clock\_frequency} [\text{Hz}] \times \text{Number of internal pipeline} (= 4)$$

Table 8-29 show XVS signal output control registers, set this register if XVS signal is used as synchronous signal to slave sensor.

**Table 8-29 XVS signal output control registers**

Address	Bit	Name	Description	Master Mode Setting (HEX)
0x3040	[0]	XVS_IO_CTRL	XVS IO control 0 : Input (Slave mode) (default) 1 : Output (Master mode)	1'h1
0x3F5D	[0]	EXTOUT_EN	XVS output setting 0 : output disable 1 : output enable	1'h1
0x4B83	[0]	EXTOUT_XVS_POL	XVS output polarity 0 : high active 1: low active	1'h1*
0x4B82	[2:0]	EXTOUT_XVS_WID	Pulse width 0: 1 cycles of VTPXCK 1: 2 cycles of VTPXCK 2: 4 cycles of VTPXCK 3: 8 cycles of VTPXCK	3'h3

Note \*: When Master-Slave is connected by Sony's sensor

If V-Sync signal is chosen as a synchronous signal, refer to Table 8-30.

**Table 8-30 GPO/XVS pins register setting**

Pin name	Setting value
GPO	CKTESTSEL(0x42B0)=0h TESTMNT2(0x42AA)=FFh, MNTTEST1_SEL(0x4BD7) = 14h OUTIF2(0x428A)=0h(output)
XVS	CKTESTSEL(0x42B0)=0h TESTMNT1(0x42A9)=FFh MNTTEST1_SEL(0x4BD7) = 14h OUTIF1(0x4289)=0h(output)

Polarity and pulse width of the V-Sync signal is adjustable, refer to Table8-20 VSYNC\_POL and VSYNC\_WID registers.

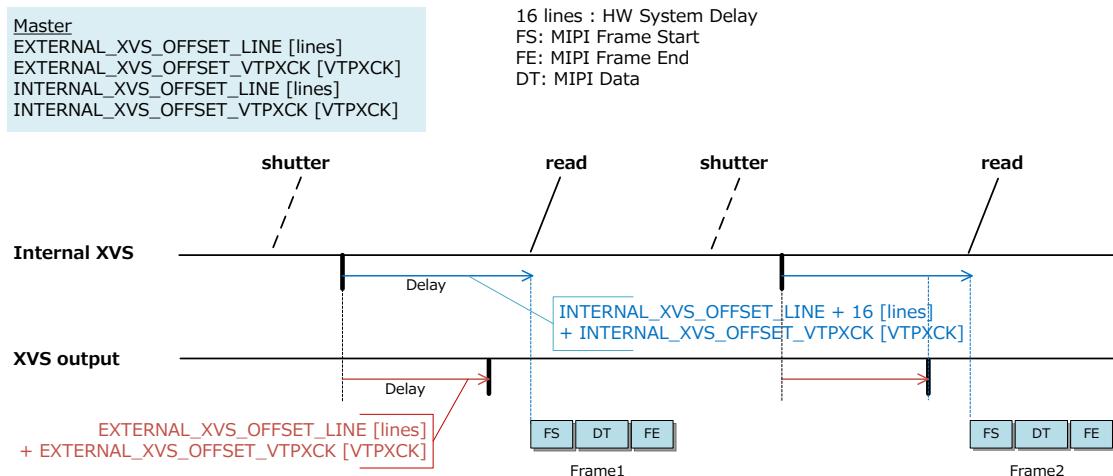
This sensor can delay the XVS signal output or internal XVS signal by setting registers. The register setting shall be made during SW standby.

**Table 8-31 Master Control registers to delay XVS signal output**

Address	Bit	Name	Description
0x3F64 ~0x3F65	[15:0]	EXTERNAL_XVS_OFFSET_LINE	Delay setting for XVS output. (set the number of lines) (default : 0)
0x3F66 ~0x3F67	[15:0]	EXTERNAL_XVS_OFFSET_VTPXCK	Delay setting for XVS output. (set the number of clocks) (default : 0)

**Table 8-32 Master Control registers to delay internal XVS signal**

Address	Bit	Name	Description
0x3F68 ~0x3F69	[15:0]	INTERNAL_XVS_OFFSET_LINE	Delay setting for internal XVS. (set the number of lines) (default : 0)
0x3F6A ~0x3F6B	[15:0]	INTERNAL_XVS_OFFSET_VTPXCK	Delay setting for internal XVS (set the number of clocks) (default : 0)



**Figure 8-15 Master delay XVS signal output and internal XVS signal**

This sensor can also thin out or multiply XVS signal output by setting the registers below. The register setting shall be made during SW standby..

**Table 8-33 Master control registers to thin out or multiply XVS signal output**

Address	Bit	Name	Description
0x3F6C	[0]	EXTOUT_XVS_MULT_SEL	0 : Thin out XVS output (default) 1: Multiply XVS output
0x3F6D	[6:0]	EXTOUT_XVS_MULT	Thin out setting for XVS output if EXTOUT_XVS_MULT_SEL=0. 0: not thin out. (output XVS period = Internal XVS period)(default) 1: 1/2 thin out. (output XVS period = Internal XVS period x 2) 2: 1/3 thin out. (output XVS period = Internal XVS period x 3) ... 127: 1/128 thin out. (output XVS period = Internal XVS period x 128) Multiple setting for XVS output if EXTOUT_XVS_MULT_SEL=1 0: not multiply. (output XVS period = Internal XVS period) 1: 2 multiply. (output XVS period x 2 = Internal XVS period) ... 127: 128 multiply. (output XVS period x 128 = Internal XVS period)

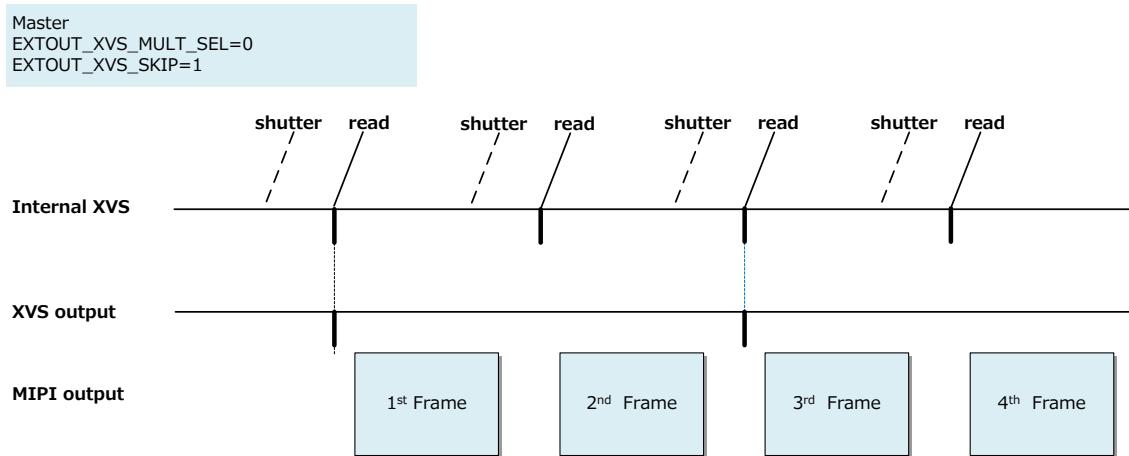


Figure 8-16 Master thin out XVS signal

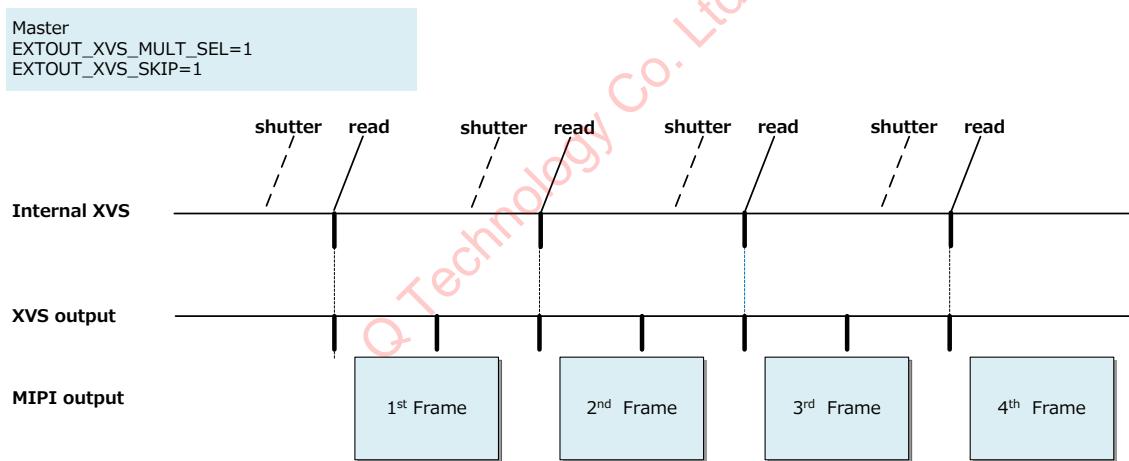
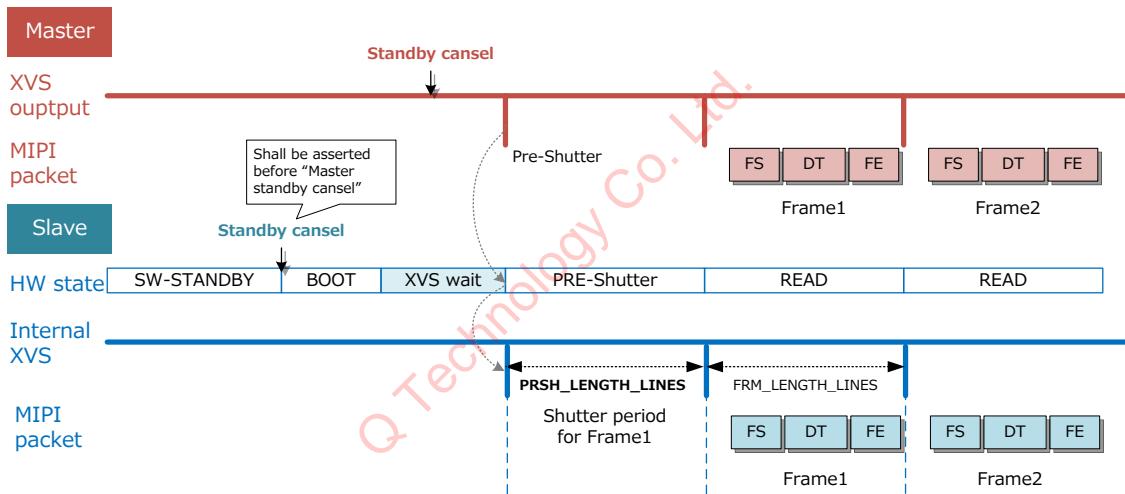


Figure 8-17 Master multiple XVS signal

### 8.8.5. Usage in slave mode

This chapter describes the slave mode setting. When the sensor is used in the slave mode, only XVS pin is available for a synchronous signal. In the slave mode, the 1<sup>st</sup> image outputs at the 2<sup>nd</sup> XVS signal input because 1<sup>st</sup> XVS signal input is used them as the pre-shutter pulse: start timing of shutter for a 1<sup>st</sup> image. In the slave mode, after receiving standby cancel, HW state changes from "SW-Standby" to "XVS wait" and keep waiting XVS signal from a master sensor. When XVS signal comes from the master, HW state changes to "PRE-Shutter" state.

Figure 8-18 shows how the Pre-Shutter pulse is used in a slave sensor and internal state. The standby cancel shall be set to the slave sensor prior to the master sensor.



**Figure 8-18 Frame output timing and HW state in the slave mode**

Table 8-34 shows the register setting for slave.

**Table 8-34 Slave mode related registers**

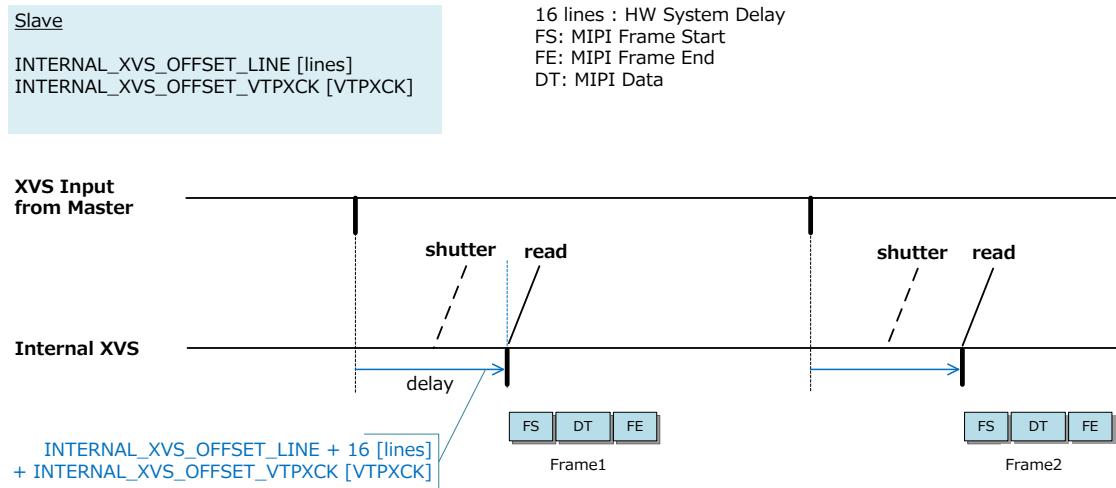
Address	Bit	Name	Description	Slave Mode Setting (HEX)
0x3F0B	[0]	MC_MODE	Multi Camera mode setting 0 : Minimum time mode (default) Pre-shutter period is defined by	1'h1

			COARSE_INTEG_TIME 1 : Fixed time mode Pre-shutter period is defined by PRSH_LENGTH_LINES	
0x3041	[0]	MASTER_SLAVE_SEL	Master or Slave mode setting 0 : Slave mode 1 : Master mode (default)	1'h0
0x3040	[0]	XVS_IO_CTRL	XVS IO control 0 : Input (Slave mode) (default) 1 : Output (Master mode)	1'h0 (default)
0x3F39 ~ 0x3F3B	[23:0]	PRSH_LENGTH_LINES	Pre-Shutter period [line] 0: Prohibited Effective if PRESHR_MODE=1 Set FRAME_LENGTH_LINE of master and slave. If CIT_LSHIFT ≠ 0 , set FRAME_LENGTH_LINE*2 <sup>CIT_LSHIFT</sup>	See description
0x3F5D	[0]	EXTOUT_EN	XVS output setting 0 : output disable 1 : output enable	1'h0 (default)
0x3F50	[0]	FRM_LENGTH_CTL	Frame length automatic tracking control Select whether or not the frame length is changed automatically when FRM_LENGTH_LINES < COARSE_INTEG_TIME + α (α = type-specific adjustment parameter, and is CIT_MARGIN for this type)  0 : no automatic tracking control of frame length In this case, [FRM_LENGTH_LINES - α] operates instead of COARSE_INTEG_TIME  1 : automatic tracking control of frame length In this case, [COARSE_INTEG_TIME + α] operates instead of FRM_LENGTH_LINES	0

Internal XVS signal can be delayed by register. Register setting shall be issued during SW standby.

**Table 8-35 Slave Control registers to delay XVS signal input**

Address	Bit	Name	Description
0x3F68 ~0x3F69	[15:0]	INTERNAL_XVS_OFFSET_LINE	Delay setting for XVS input from Master. (set the number of lines) (default : 0)
0x3F6A ~0x3F6B	[15:0]	INTERNAL_XVS_OFFSET_VTPXCK	Delay setting for XVS input from Master. (set the number of clocks) (default : 0)

**Figure 8-19 Slave delay XVS input****Table 8-36 Slave control registers to thin out XVS signal input**

Address	Bit	Name	Description
0x3F6E	[0]	EXTIN_XVS_MULT_SEL	0 : thin out internal XVS (default) 1 : multiply internal XVS
0x3F6F	[6:0]	EXTIN_XVS_MULT	Thin out setting for internal XVS if EXTIN_XVS_MULT_SEL=0 0: not thin out. (incoming XVS period = Internal XVS period) (default) 1: 1/2 thin out. (incoming XVS period = Internal XVS period x 2) ... 127: 128 thin out. (incoming XVS period = Internal XVS period x 128) Multiply setting for internal XVS if EXTIN_XVS_MULT_SEL=1 0: Prohibited 1: 2 multiply. (incoming XVS period = Internal XVS period) ... 127: 128 multiply. (incoming XVS period = Internal XVS period)

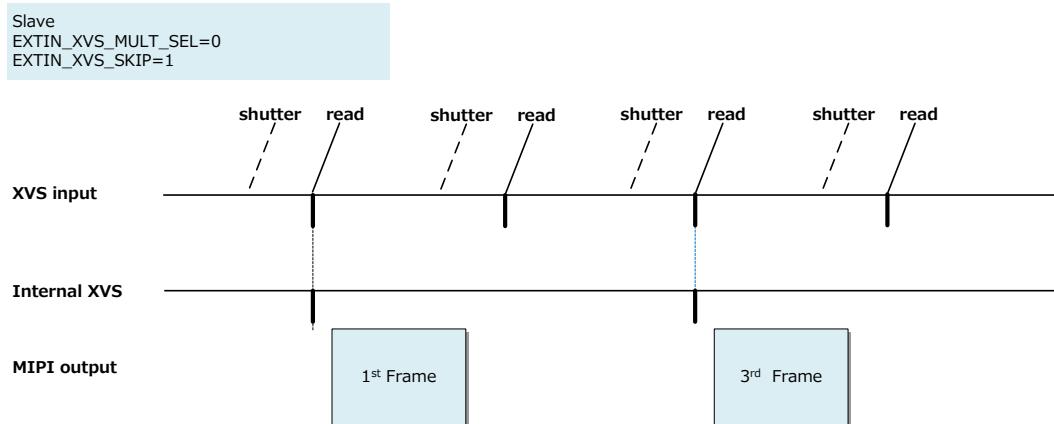


Figure 8-20 Slave thin out XVS signal input

Table 8-37 Slave control registers to thin out or multiply XVS signal input

	Address	Bit	Name	Description
	0x3F6E	[0]	EXTIN_XVS_MULT_SEL	0 : thin out internal XVS (default) 1 : multiply internal XVS
I2C register	0x3F6F	[6:0]	EXTIN_XVS_MULT	Thin out setting for internal XVS if EXTIN_XVS_MULT_SEL=0 0: not thin out. (incoming XVS period = Internal XVS period) (default) 1: 1/2 thin out. (incoming XVS period = Internal XVS period x 2) ... 127: 128 thin out. (incoming XVS period = Internal XVS period x 128) Multiply setting for internal XVS if EXTIN_XVS_MULT_SEL=1 0: Prohibited 1: 2 multiply. (incoming XVS period = Internal XVS period) ... 127: 128 multiply. (incoming XVS period = Internal XVS period)

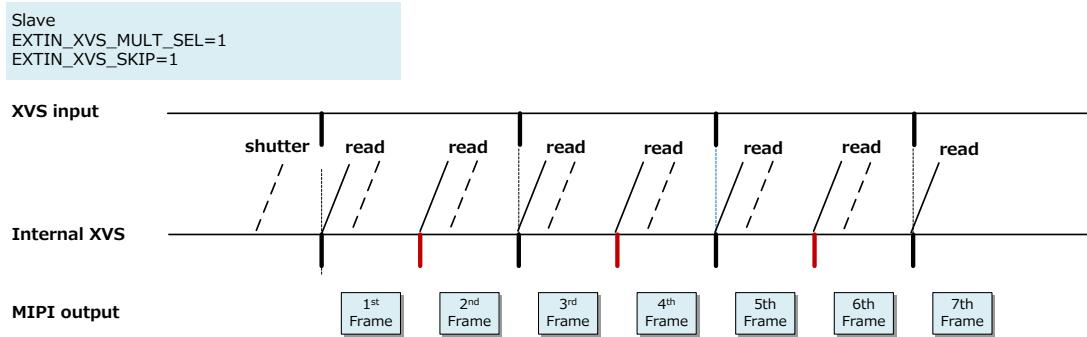
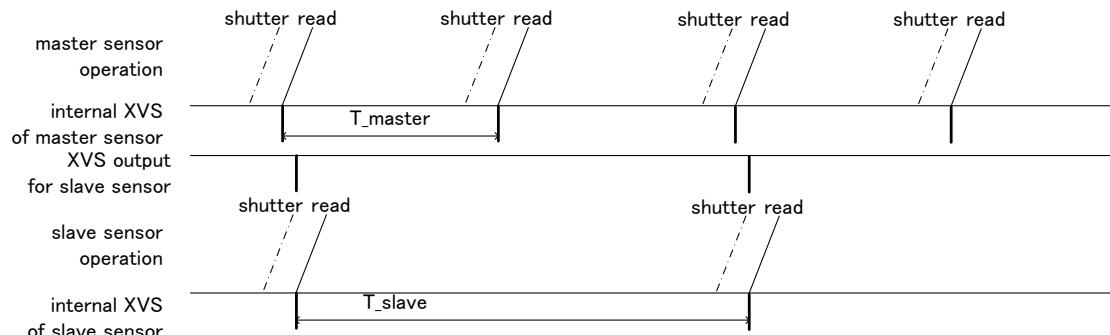


Figure 8-21 Slave multiple XVS signal input

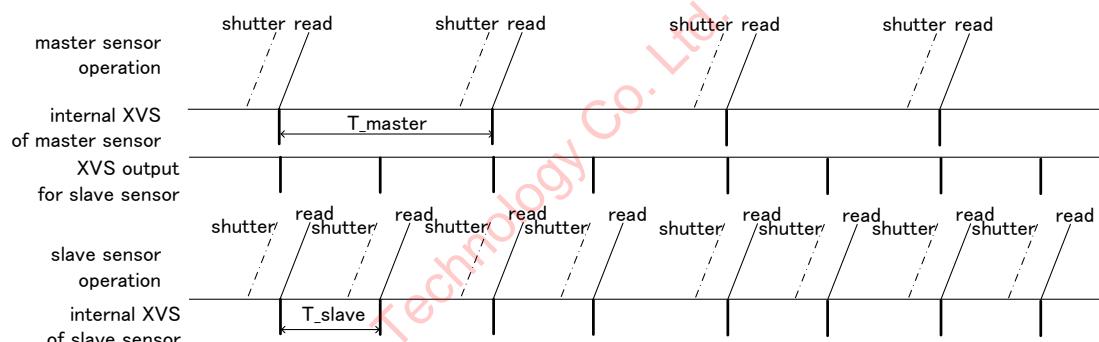
#### 8.8.5.1. Restriction in the slave mode operation

1. Keep  $T_{frame\_master}[s] > T_{frame\_slave}[s] + 2T_{line\_slave}[s]$  relationship.
2. If FRM\_LENGTH\_CTL = 1, slave "COARSE\_INTEG\_TIME + CIT\_MARGIN + 2" shall be less than master FRAME\_LENGTH\_LINES. Where default value of CIT\_MARGIN is 18.
3. Set  $T_{frame\_master}$  and  $T_{frame\_slave}$  as frame length (  $FRM\_LENGTH\_LINES \times LINE\_LENGTH\_PCK / pixel\_clock\_frequency$  ) for master and slave sensor. Set n as multiple or thin out number (n = 1,2,4,...,128).  
If XVS signal is thinned out,  $n \times T_{frame\_master}$  must be greater than  $T_{frame\_slave} + 2T_{line\_slave}$  (see Figure 8-22 ).  
If XVS signal is multiplied,  $T_{frame\_master}$  must be greater than  $n \times T_{frame\_slave} + 2T_{line\_slave}$  (see Figure 8-23 ).
4. In slave mode, the XVS terminal of this sensor inhibits high input signal from a master sensor during power off.
5. The embedded thermal meter of slave sensor in standby mode is not supported. If you want to use embedded thermal meter at standby mode, it is only available in master sensor.
6. Thinned out or multiple function and internal or output XVS signal delay function must be changed during SW-standby.
6. AEB (AE bracketing) mode is not supported.
8. GPH (grouped parameter hold) must be used for updating gain during streaming.
9. Fast mode transition is not supported
10. Power save streaming is not supported
11. Between two sensors, there exists a worst case time difference in MIPI outputs calculated with the following equation.  $\Delta t_{max} = 145 * t_{INCK} = 145 / f_{INCK}$  (Worst case). Where  $t_{INCK}$  is external clock period and  $f_{INCK}$  is external clock frequency to the sensor.



Restriction :  $n \times T_{master} > T_{slave} + 2T_{line\_slave}$

**Figure 8-22 Frame length restriction when XVS signal is thinned out**



Restriction :  $T_{master} > n \times T_{slave} + 2T_{frame\_slave}$

**Figure 8-23 Frame length restriction when XVS signal is multiplied**

### 8.8.6. XVS pin connectivity debug function

This function offers users to check XVS pin connectivity. Overall XVS pin connectivity check diagram is shown in Figure 8-24. Master sensor can output fixed high/low signal from XVS pin by register control .Slave sensor can monitor XVS signal input by reading register.

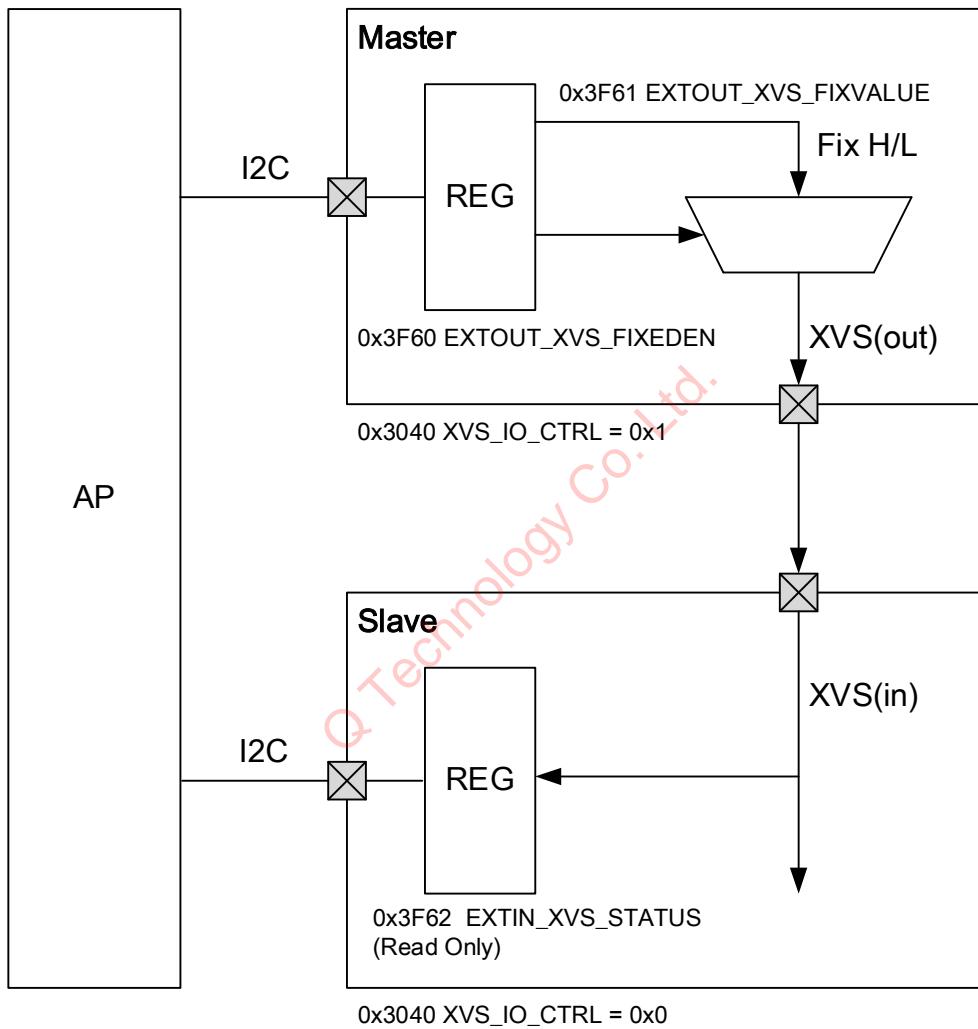


Figure 8-24 XVS pin connectivity check diagram

**Table 8-38 XVS pin connectivity check related registers**

I2C register	Address	Bit	Name	Description
	0x3F61	[0]	EXTOUT_XVS_FIXED_VALUE	0 : Fixed Low output (default) 1: Fixed High output
	0x3F60	[0]	EXTOUT_XVS_FIXED_EN	0: disable (default) 1: enable
	0x3F62	[0]	EXTIN_XVS_STATUS	Show XVS input level from Master 0: Low level 1 : High level (default)
	0x3040	[0]	XVS_IO_CTRL	XVS IO control 0 : Input (Slave mode) (default) 1 : Output (Master mode)

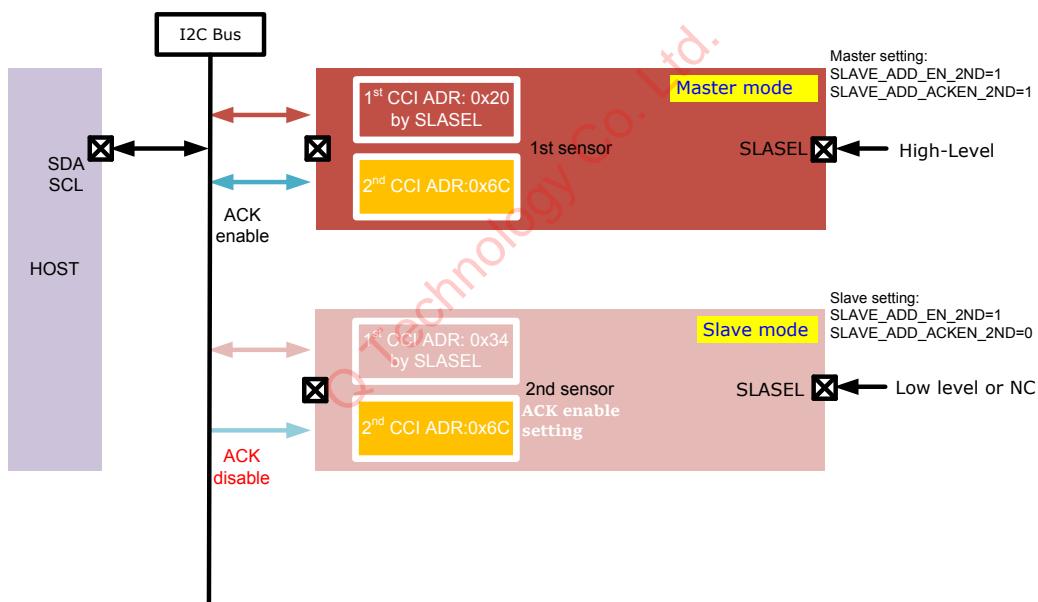
### 8.8.7. Dual camera using shared CCI bus

#### 8.8.7.1. Block diagram

The 2<sup>nd</sup> slave address shall be activated and the master sensor should be set as ACK responder based on .

**Table 8-39 Control register of 2<sup>nd</sup> slave address**

I2C Address	Bit	Name	Description	Initial value (HEX)	Master setting	Slave setting
0x3010	[0]	SLAVE_ADD_EN_2ND	2nd Slave Address Enable 0: disable 1: enable	1'h0	1'h1	1'h1
0x3011	[0]	SLAVE_ADD_ACKEN_2ND	2nd Slave Address Ack Enable 0: disable 1: enable	1'h0	1'h1	1'h0



**Figure 8-25 Dual camera system block diagram with shared CCI**

Figure 8-25 shows the block diagram of the dual camera application using shared CCI bus.

In this sensor, synchronization of two sensors is achieved with shared CCI bus by having different slave address between two sensors and by issuing MODE\_SEL=1 at the same time onto the shared bus. With this approach, this sensor can be either of a master device or a slave device.

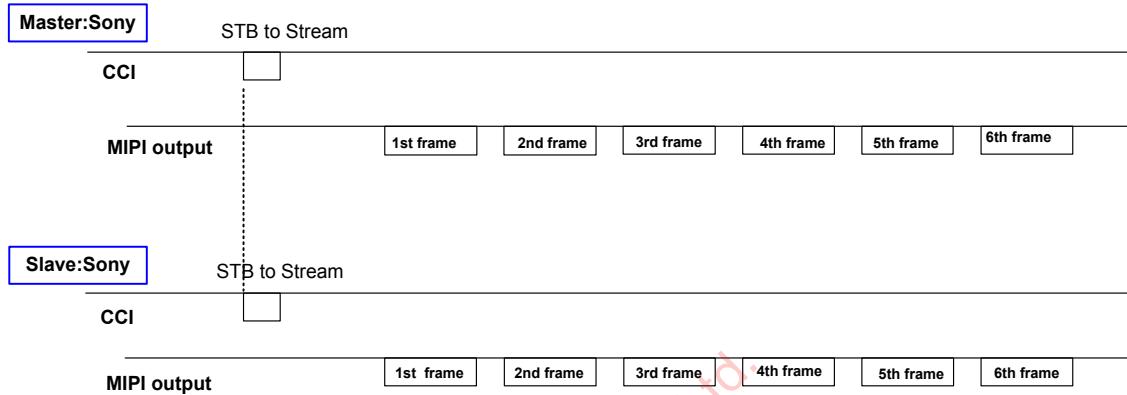
Besides the above mentioned CCI address, this sensor has a built-in 2<sup>nd</sup> slave address of 0x6C which is common for all sensors. See 2.3.2 about the details of activation of the 2<sup>nd</sup> slave address.

As the second CCI address is activated and with different SLASEL setting, each sensor have each CCI addresses; first sensor with 0x20 and 0x6c, second sensor with 0x34 and 0x6c. ACK responder for the

2nd slave address (0x6c) shall be set either one.

The above configuration enables to set different settings on each sensor and talk "start streaming" both together. Consequently each sensor can synchronously capture a same scene with individual exposure time and individual gain setting.

See following paragraph for hardware configuration and control sequence of the dual camera operation.



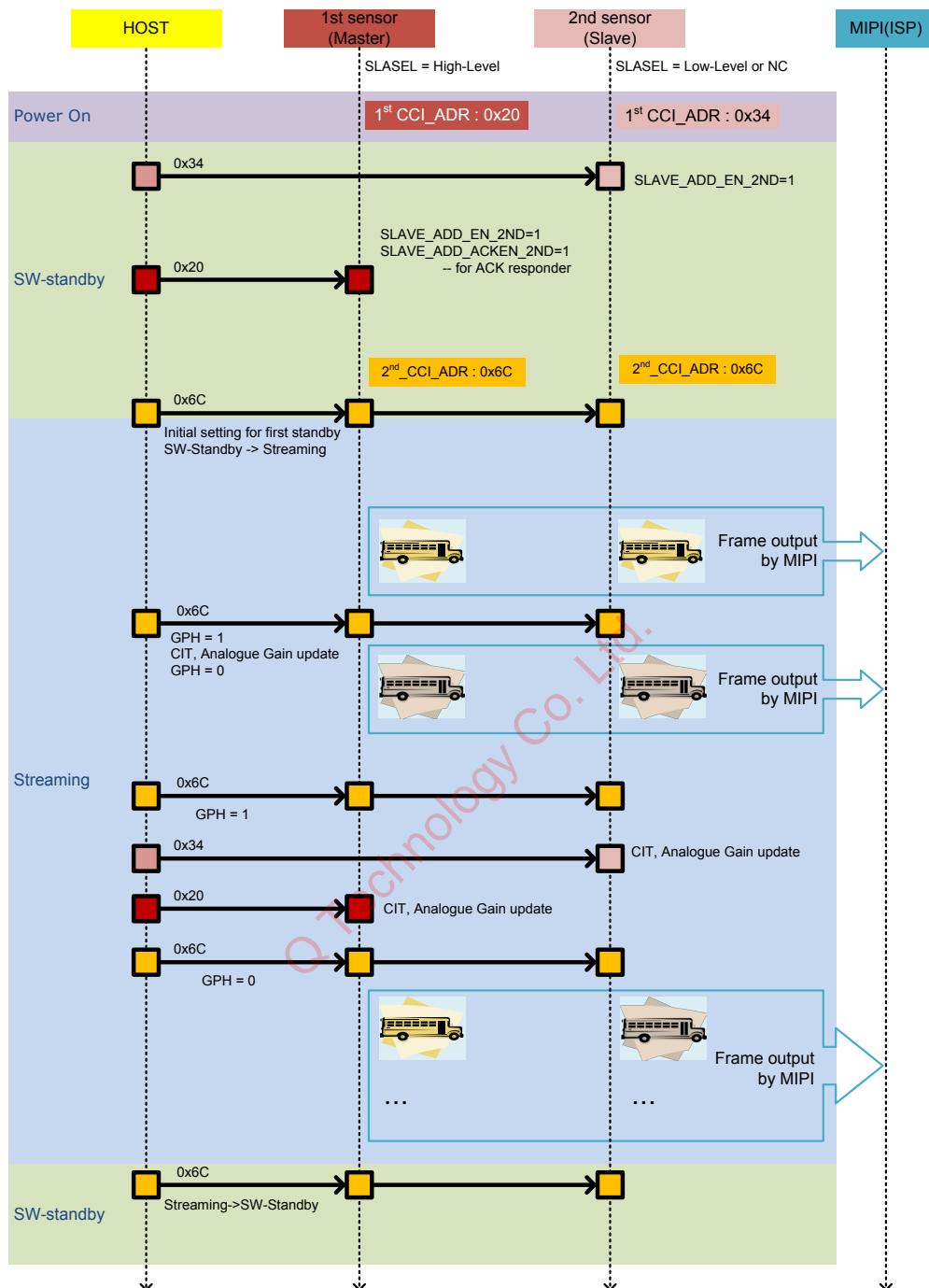
**Figure 8-26 Dual camera approach using shared CCI bus**

#### 8.8.7.2. Control sequence

Any settings using 1st CCI addresses are separately applied for each sensor.

Settings with 2<sup>nd</sup> CCI address are commonly applied for both sensors.

The following figure shows temporal and spatial sequence of dual camera control.

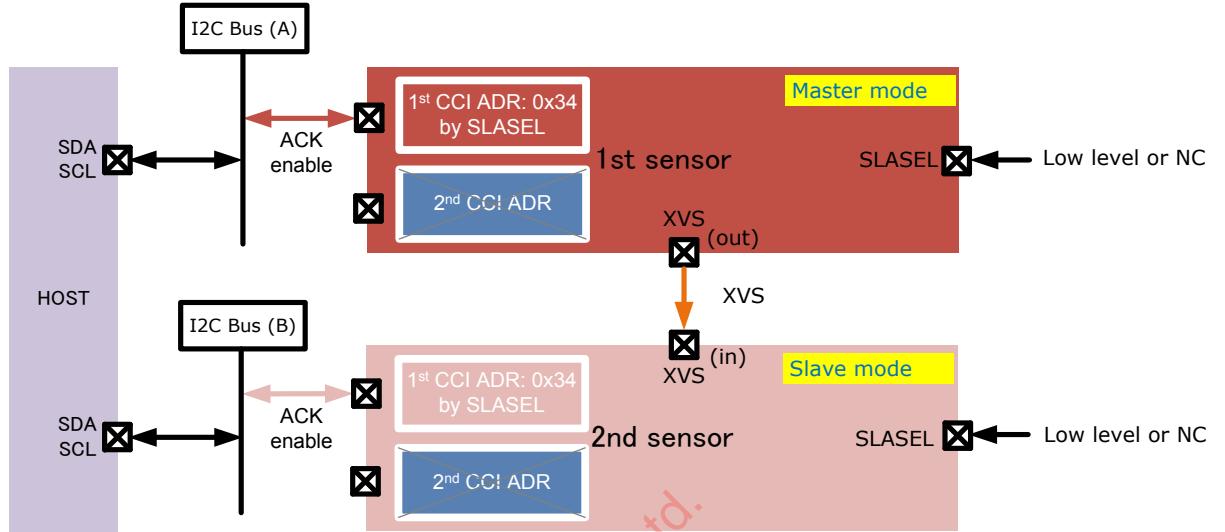


**Figure 8-27 Communication control and timing**

#### **8.8.8. Dual camera system with Separated CCI bus (optional)**

The following figure shows the block diagram of the Dual camera system using with separated CCI bus. In this use case, one sensor is connected to I2C Bus (A) and the other is connected to I2C Bus (B). When the Dual camera system with Separated CCI Bus is operated, both of 1<sup>st</sup> CCI addresses

do not require the different CCI address. It means that the same 1<sup>st</sup> CCI address is acceptable in this connection. On the other hand, there is no need to setting for 2<sup>nd</sup> Slave address.



**Figure 8-28 Dual camera system block diagram with separated CCI bus**

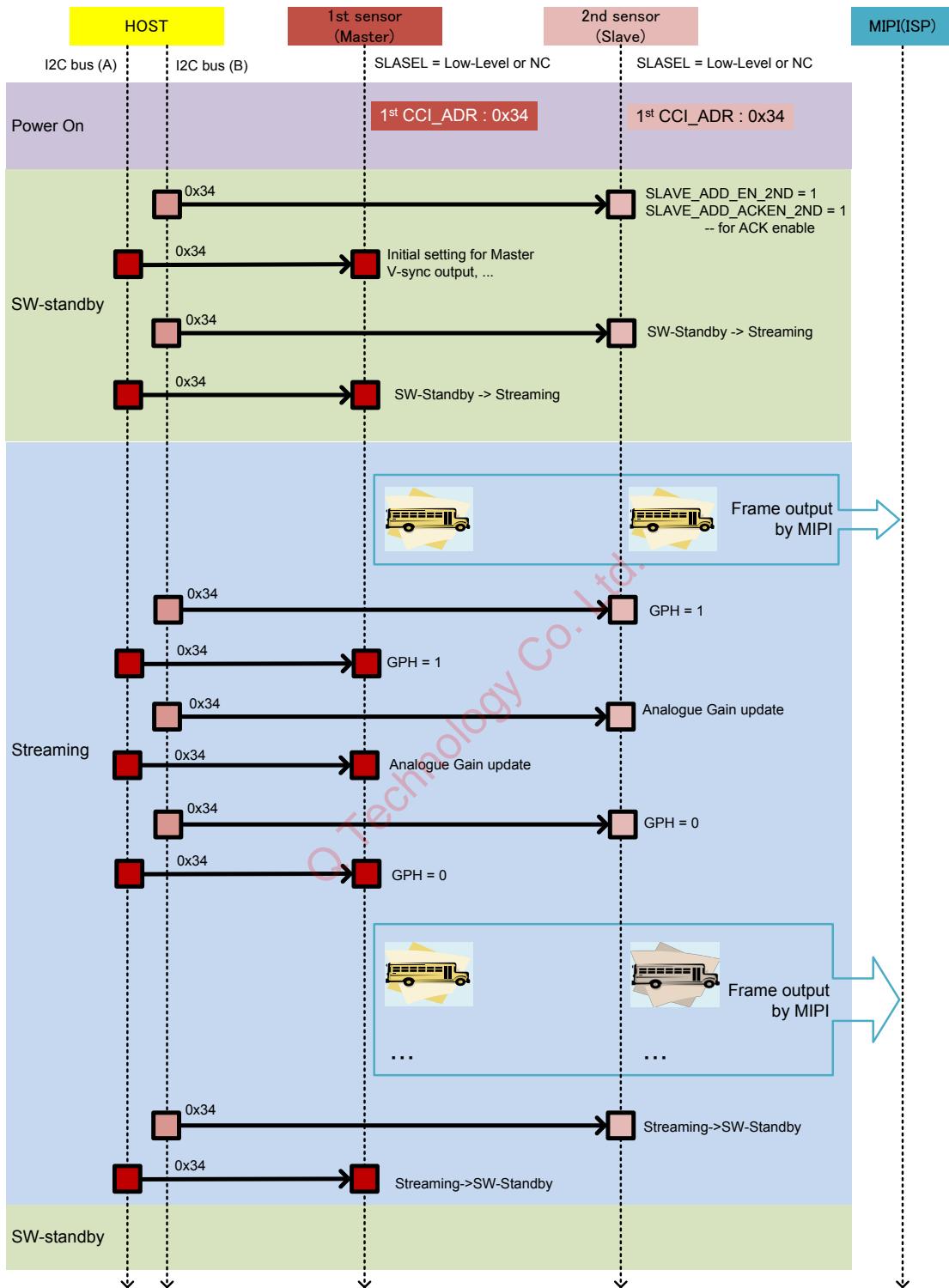
The following figure shows the system control sequence of the Dual camera system using with separated CCI Bus.

First of all, it is necessary to set "MODE\_SEL" to the Slave mode sensor before streaming starts.

Then, "MODE\_SEL" for Master mode sensor should be set.

If you need to change the both sensors setting at same time, it is necessary to pay attention about setting delay time between separated CCI Bus. If there is a large delay time, it will be happen that there is not a synchronized case between master and slave sensors.

The other restrictions are same as Dual camera system with shared CCI Bus.



**Figure 8-29 Communication control and timing with separated CCI Bus**

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## 8.9. Charge pump setting

This sensor has two charge pump block to generate voltage (VRL, VRLRD) for the pixels array.

The charge pumping clock is common. Internal capacitor value should be set the same value for both charge pump out.

Setting for CP control mode.

**Table 8-40 Register setting for CP control mode**

I2C register	Block	Address	Bit	Name	Description
	VRL VRLRD	0x521F	[1:0]	CPCSEL_AUTOEN	Clock auto select 0 : Disable (Manual mode) 2 : Enable (Auto mode, default setting) 1, 3 Reserve

Setting for pumping clock setting (manual mode only).

The charge pumping clock is driven by inck during SW standby. So this setting is invalid during SW standby.

The pumping frequency shall be in the range of 6MHz~27MHz.

**Table 8-41 Register setting for pumping clock**

I2C register	Block	Address	Bit	Name	Description
	VRL VRLRD	0x521E	[4:0]	CPCSEL	Pumping clock setting 0: prohibited                    1: prohibited 2: 1/2 of IVTPXCK            3: 1/4 of IVTPXCK 4: 1/4 of IVTPXCK            5: 1/5 of IVTPXCK 6: 1/6 of IVTPXCK            7: 1/7 of IVTPXCK 8: 1/8 of IVTPXCK            9: 1/9 of IVTPXCK 10: 1/10 of IVTPXCK          11: 1/11 of IVTPXCK 12: 1/12 of IVTPXCK          13: 1/13 of IVTPXCK 14: 1/14 of IVTPXCK          15: 1/15 of IVTPXCK 16: 1/16 of IVTPXCK          17: 1/17 of IVTPXCK 18: 1/18 of IVTPXCK          19: 1/19 of IVTPXCK 20: 1/20 of IVTPXCK          21: 1/22 of IVTPXCK 22: 1/24 of IVTPXCK          23: 1/26 of IVTPXCK 24: 1/28 of IVTPXCK          25: 1/30 of IVTPXCK 26: 1/32 of IVTPXCK          27: 1/34 of IVTPXCK 28: 1/36 of IVTPXCK          29: 1/38 of IVTPXCK 30: 1/40 of IVTPXCK          31: 1/42 of IVTPXCK

Setting for CP drive internal capacitor (\*CP manual mode only)

**Table 8-42 Register setting for CP drive internal capacitor**

I2C register	Block	Address	Bit	Name	Description
	VRL VRLRD	0x5B54	[1:0]	CPCSEL	CP drive internal capacity 0: 60pF 1: 80pF 2: 100pF 3: 120pF (default)

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## 9. Lens Shading Correction (LSC)

This sensor has a built-in lens shading correction (LSC) function for each color (R/Gr/Gb/B) separately.

A purpose of the LSC function in this sensor is primarily for module level shading calibration of four colors. However, it can be also usable as a substitute function of LSC function as usually done in ISP.

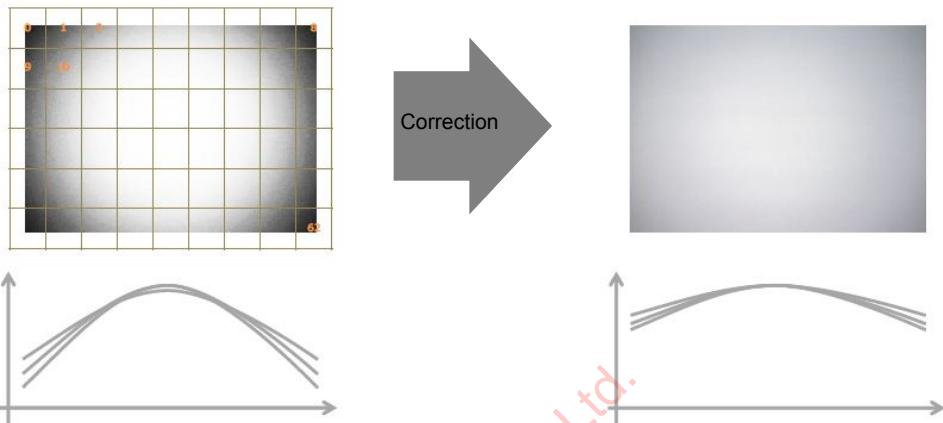


Figure 9-1 Lens Shading Correction

**Table 9-1 LSC configuration registers**

I2C Address	Bit	Name	default	Description
0x0b00	[0]	SHD_CORR_EN	1'b0	LSC Enable 0:disable, 1:enable
0x3804	[1:0]	LSC_CALC_MODE	2'b10	Table select mode 2'b00: Sensor adjust (auto) mode 2'b10: Table select (manual) mode others: reserved
0x3805	[1:0]	LSC_MANUAL_TABLE_SEL	2'b00	select table - When LSC_CALC_MODE = 2'b10 2'b00: table1 2'b01: table2 2'b10: table3 2'b11:reserved
0x8246	[1:0]	KNOT_FMT_R	2'b00	define Knot point (R pixel) * <sup>1</sup> 2'b00: u2.8, 2'b01:u3.7, 2'b10:u1.9, 2'b11:u4.6
0x8247	[1:0]	KNOT_FMT_GR	2'b00	define Knot point (Gr pixel) * <sup>1</sup> 2'b00: u2.8, 2'b01:u3.7, 2'b10:u1.9, 2'b11:u4.6
0x8248	[1:0]	KNOT_FMT_Gb	2'b00	define Knot point (Gb pixel) * <sup>1</sup> 2'b00: u2.8, 2'b01:u3.7, 2'b10:u1.9, 2'b11:u4.6
0x8249	[1:0]	KNOT_FMT_B	2'b00	define Knot point (B pixel) * <sup>1</sup> 2'b00: u2.8, 2'b01:u3.7, 2'b10:u1.9, 2'b11:u4.6

Note \*1: copied from OTP and it should be set as common value.

**Table 9-2 LSC Knot point RAM tables**

I2C Address	Bit	Name	default	Description
0x9B00 - 0x9D2F	-	KNOT_POINT_TABLE1	-	Knot point parameter for Table1 * <sup>2</sup> 10(H) * 7(V) * 4(R/Gr/Gb/B) * 10(resolution)
0x9D30-0x9F5F	-	KNOT_POINT_TABLE2	-	Knot point parameter for Table2 10(H) * 7(V) * 4(R/Gr/Gb/B) * 10(resolution)
0x9F60-0xA18F	-	KNOT_POINT_TABLE3	-	Knot point parameter for Table3 10(H) * 7(V) * 4(R/Gr/Gb/B) * 10(resolution)

Note \*2: copied from OTP table

**Table 9-3 Sensor adjust (auto) mode configuration registers**

I2C Address	Bit	Name	default	Description
0x9742	[15:8]	LSC_TH_COLOR_B		threshold level of color temperature boundary 1
0x9743	[7:0]	LEND_1	16'h0000	>= WBG_R_GR : select table3
0x9744	[15:8]	LSC_TH_COLOR_B		threshold level of color temperature boundary 2
0x9745	[7:0]	LEND_2	16'h0000	> WBG_R_GR: select blend table(2&3)
0x9746	[15:8]	LSC_TH_COLOR_B		threshold level of color temperature boundary 3
0x9747	[7:0]	LEND_3	16'h0000	>= WBG_R_GR : select table2
0x9748	[15:8]	LSC_TH_COLOR_B		threshold level of color temperature boundary 4
0x9749	[7:0]	LEND_4	16'h0000	> WBG_R_GR : select blend table(1&2) <= WBG_R_GR : select table1
0xBA06	[15:8]			white balance ratio (ABS_GAIN_R / ABS_GAIN_GR) (u8.8)
0xBA07	[7:0]	WBG_R_GR	16'h0000	- When LSC_CALC_MODE = 2'b00 (auto mode) is valid *This value vs. color temperature relation shall be defined according to the relation between RAM table and color temperature.
0x974C	[15:0]	LSC_OUTDOOR_TH_IN	16'h03E3	exposure tuning mode - When LSC_CALC_MODE = 2b'00 (auto mode) 16'h0000 : disable exposure tuning Others : reserved
0x974E	[15:0]	LSC_OUTDOOR_TH_OUT	16'h01F0	exposure tuning mode - When LSC_CALC_MODE = 2b'00 (auto mode) 16'h0000 : disable exposure tuning Others : reserved

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### 9.1. Abstract of LSC system

In this sensor, LSC function supports two modes (manual and auto) and consists of an OTP table, three RAM tables and a blend block. Each table consists of 10(H) x 7(V) Knot point tables for each color.

**Table 9-4 LSC function**

LSC function		Note
Correction algorithm		B-spline correction
Color correction mode		4 color mode (R / Gr / Gb / B )
Knot point	Horizontal	10
	Vertical	7

	Resolution	10bit
Color temperature correction SRAM table		3 Knot point tables (Update by ISP via CCI bus. Only Table1 could be read from OTP .See Figure 9-2)
Correction mode	Calibration (manual) mode	Available
	Sensor adjust (auto) mode	Available
OTP memory size		283Byte (280Byte x 1 table + 3Byte for LSC control)

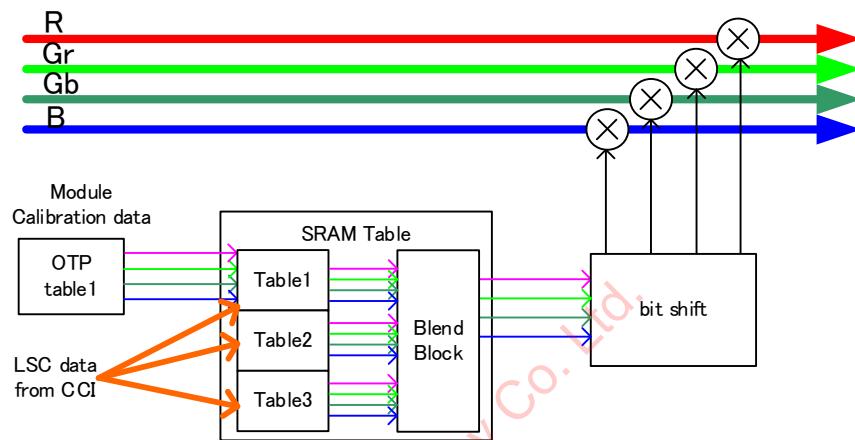
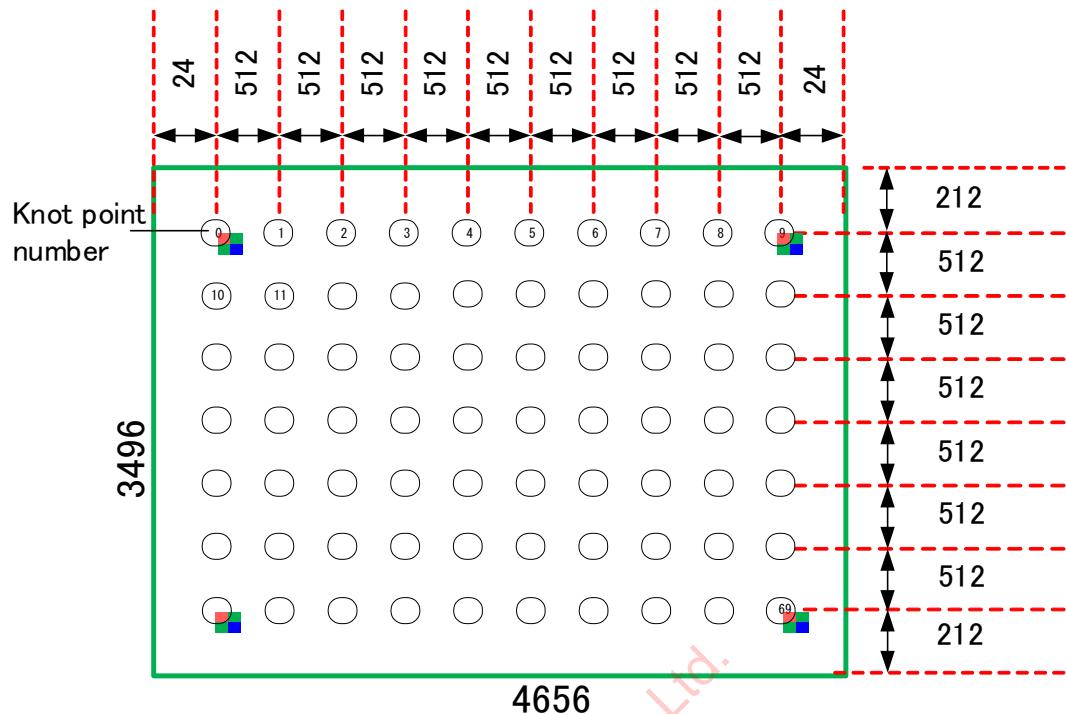


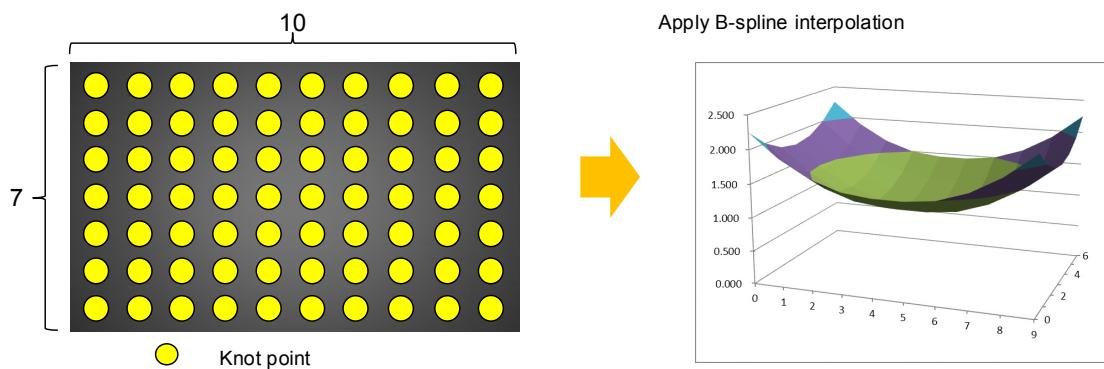
Figure 9-2 Block diagram for LSC knot point table setting



**Figure 9-3 Knot point tables (10(H) x 7(V))**

#### Calibration mode (manual mode)

Each data of Knot point tables can be stored in OTP and the data is automatically loaded into SRAM Table 1 during initialization (See Figure 9-2). LSC function performs the Lens shading correction by adapting the B-spline interpolation with Knot point data.

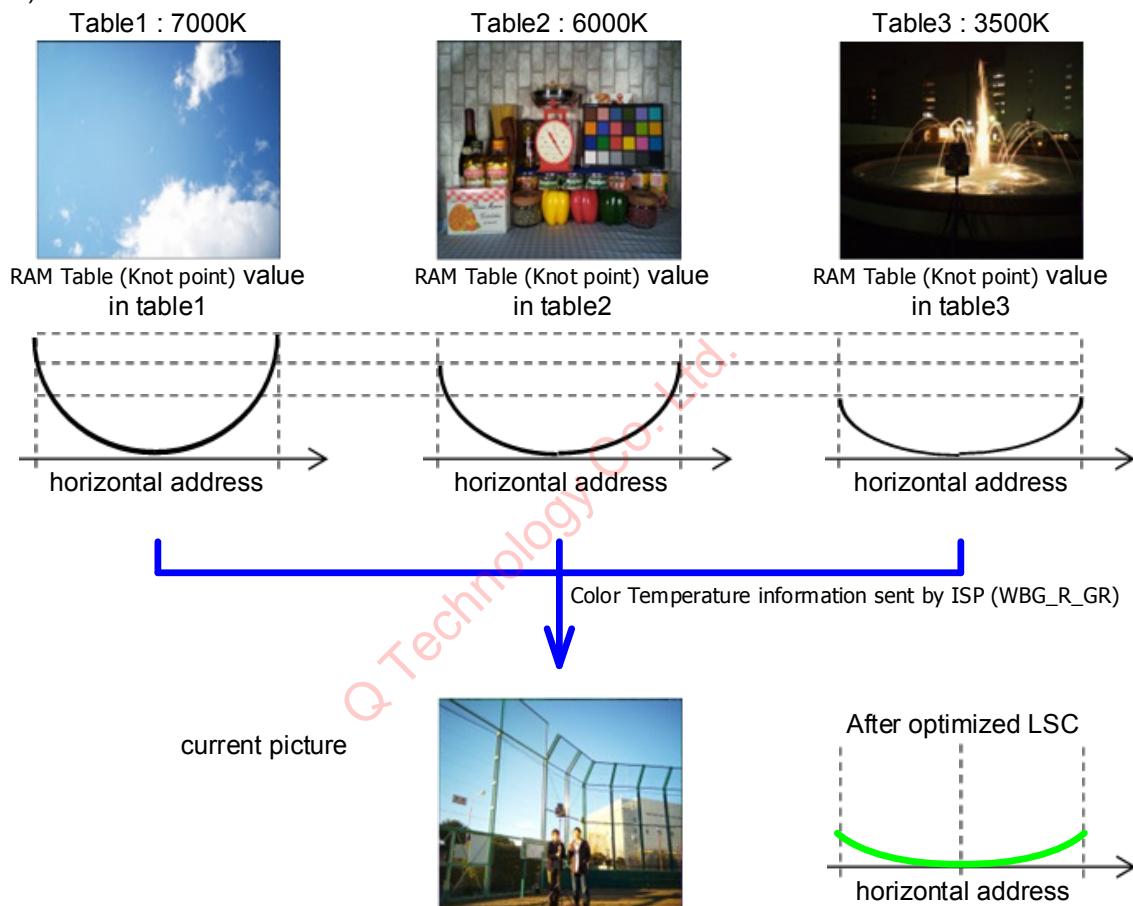


**Figure 9-4 B-spline interpolation**

### Sensor adjust mode (auto mode)

This mode supports generally called LSC function that is usually done in back-end ISP. Three color shading tables (RAM Tables 1-3) updated via CCI bus can be selected/blended according to color temperature information sent by ISP/AP.

ex)

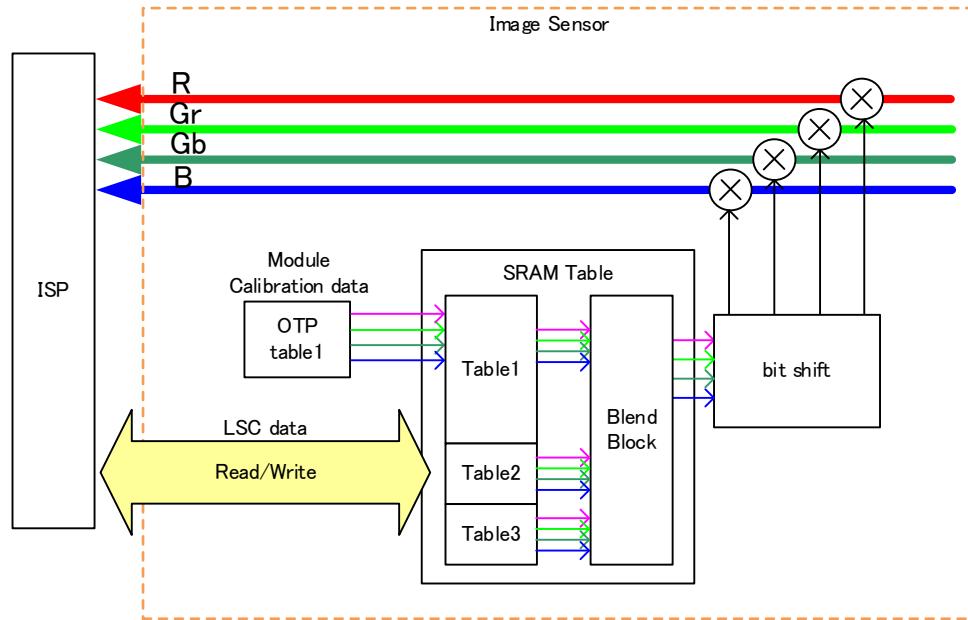


\* Sensor calculates optimized LSC parameters by white balance ratio

**Figure 9-5 RAM(Knot) table selection(auto mode)**

ISP can get module calibration data which is stored in sensor's OTP area by reading SRAM Table1 to activate Sensor adjust mode.

Then LSC data calculated and tuned over color temperature change in ISP should be transferred back to sensor SRAM Table1-3.



**Figure 9-6 Sensor adjust mode (auto mode)**

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## 9.2. Control scheme -- overall setting scheme

This sensor supports two Lens Shading Correction mode, “Calibration (manual) mode” and “Sensor adjust (auto) mode”.

In Calibration (manual) mode, select RAM Table 1 to reflect calibration values to main RAW data path (see Figure 9-2, Figure 9-7). In Sensor adjust (auto) mode, the optimized lens shading correction setting which is calculated from the SRAM table 1, 2, 3 by this sensor can be used in each scheme.

### Calibration (manual) Mode

- 1: LSC function enable (SHD\_CORR\_EN=1)
- 2: Select LSC calculation mode (LSC\_CALC\_MODE=2'b10)
- 3: Select the LSC table from table1 (LSC\_MANUAL\_TABLE\_SEL=2'b00)

### Sensor adjust (auto) mode

- 1: Set three color temperature table (Table1, 2, and 3) by ISP during initialization. (See Figure 9-10 for data address for each table)
- 2: LSC function enable (SHD\_CORR\_EN=1)
- 3: Select LSC calculation mode (LSC\_CALC\_MODE=2'b00)
- 4: Set the threshold level of each color temperature boundary (LSC\_TH\_COLOR\_BLEND\_1/2/3/4 )

Note: There are following constraints to use auto mode function.

0x971C、0x971D : LSC\_OUTDOOR\_TH\_IN = 0x0000

0x971E、0x971F : LSC\_OUTDOOR\_TH\_OUT = 0x0000

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The following two charts show overview of LSC control flow

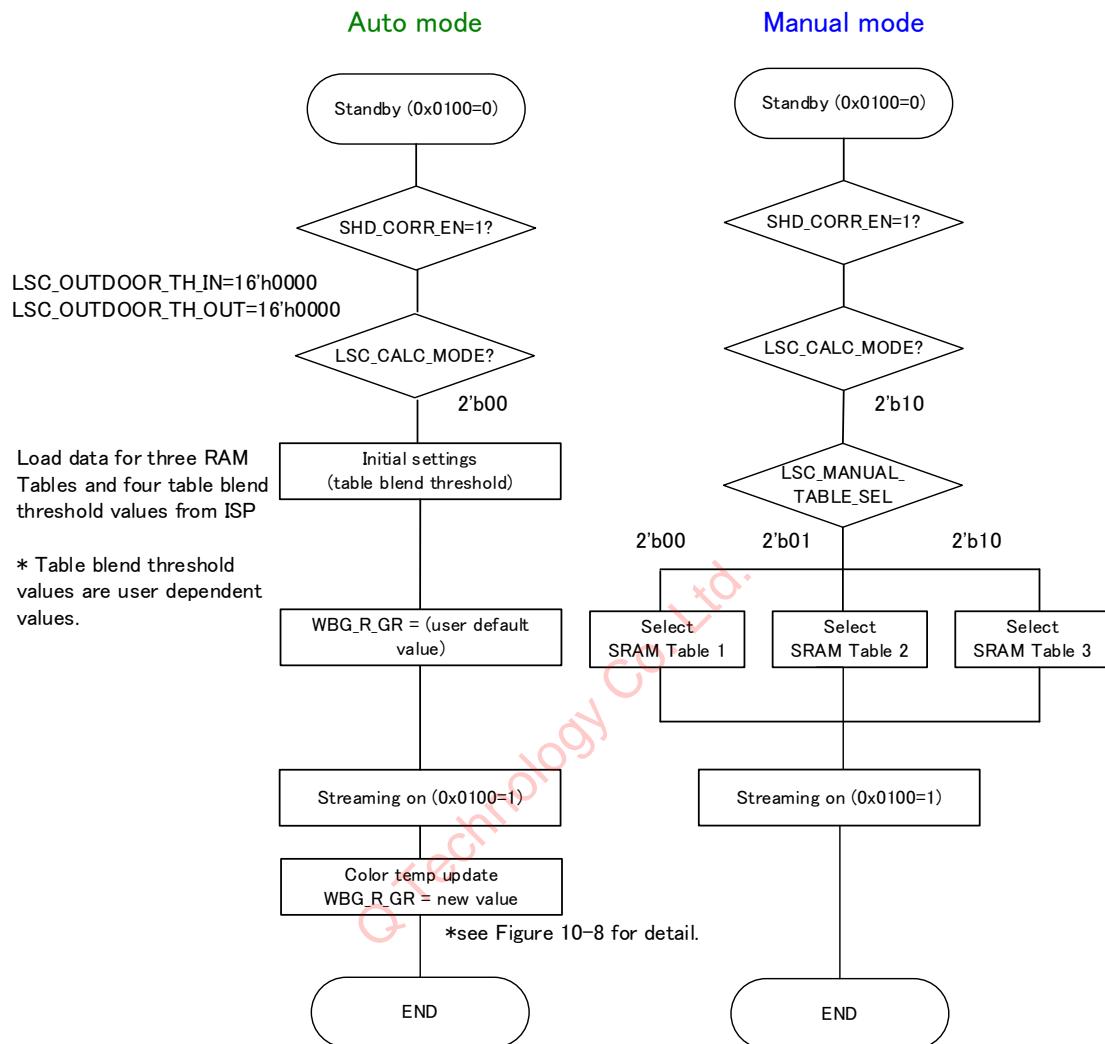


Figure 9-7 LSC control flow chart

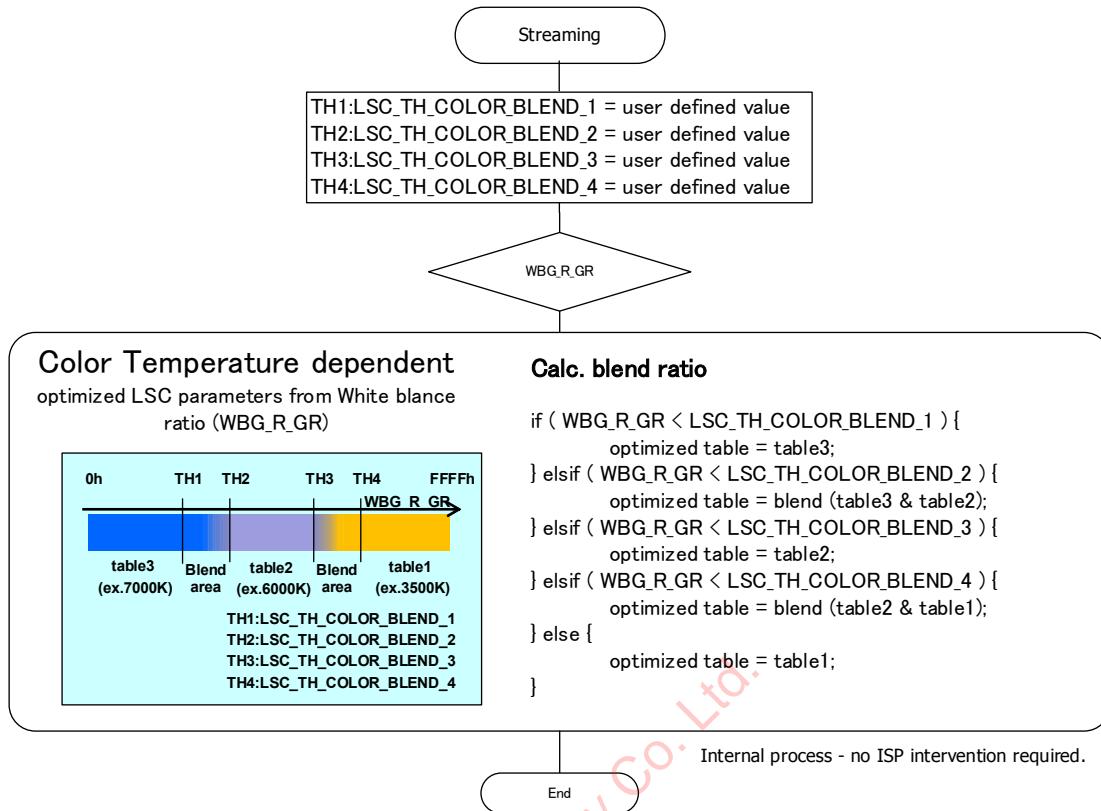


Figure 9-8 LSC table calculation according to color temperature

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### 9.3. LSC data information in OTP

There are two areas to store the LSC related data in OTP. One is for LSC compressed data storage area which consists of three tables and the other is LSC control parameters storage area. These LSC data and control parameters are automatically loaded to the sensor after power on.

#### Relation between copied SRAM data and OTP data

Each LSC Knot Point data stored in OTP is transformed as follows and common setting value of Global\_OFFSET is used in each color(R/Gr/Gb/B) and each table.

SRAM table data (Knot\_xx[9:0]) is copied from OTP table with the following relation.

$$\text{Knot\_xx}[9:0] = \text{GLOBAL\_OFFSET}[9:0] + \text{LSC\_TABLEEx\_y\_zz}[7:0]$$

Note: GLOBAL\_OFFSET[9:0] (address 472d to 473d),

LSC\_TABLEEx\_y\_zz[7:0] (address 192d to 471d)

(x=1, 2, 3; y=R, Gr, Gb, B; zz=00, 01,..., 69)

Knot point is an u2.8 number. E.g. 1101111111b means  $3+127/256$  in decimal.

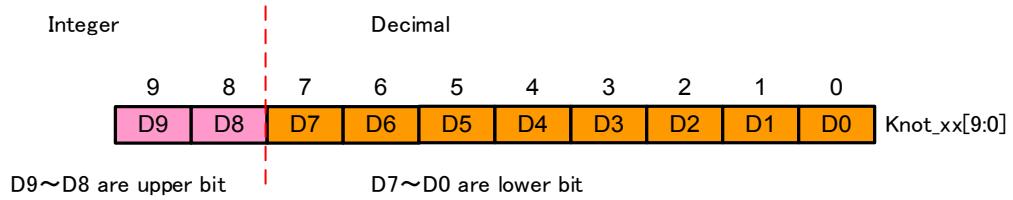


Figure 9-9 Knot point DATA structure (u2.8)

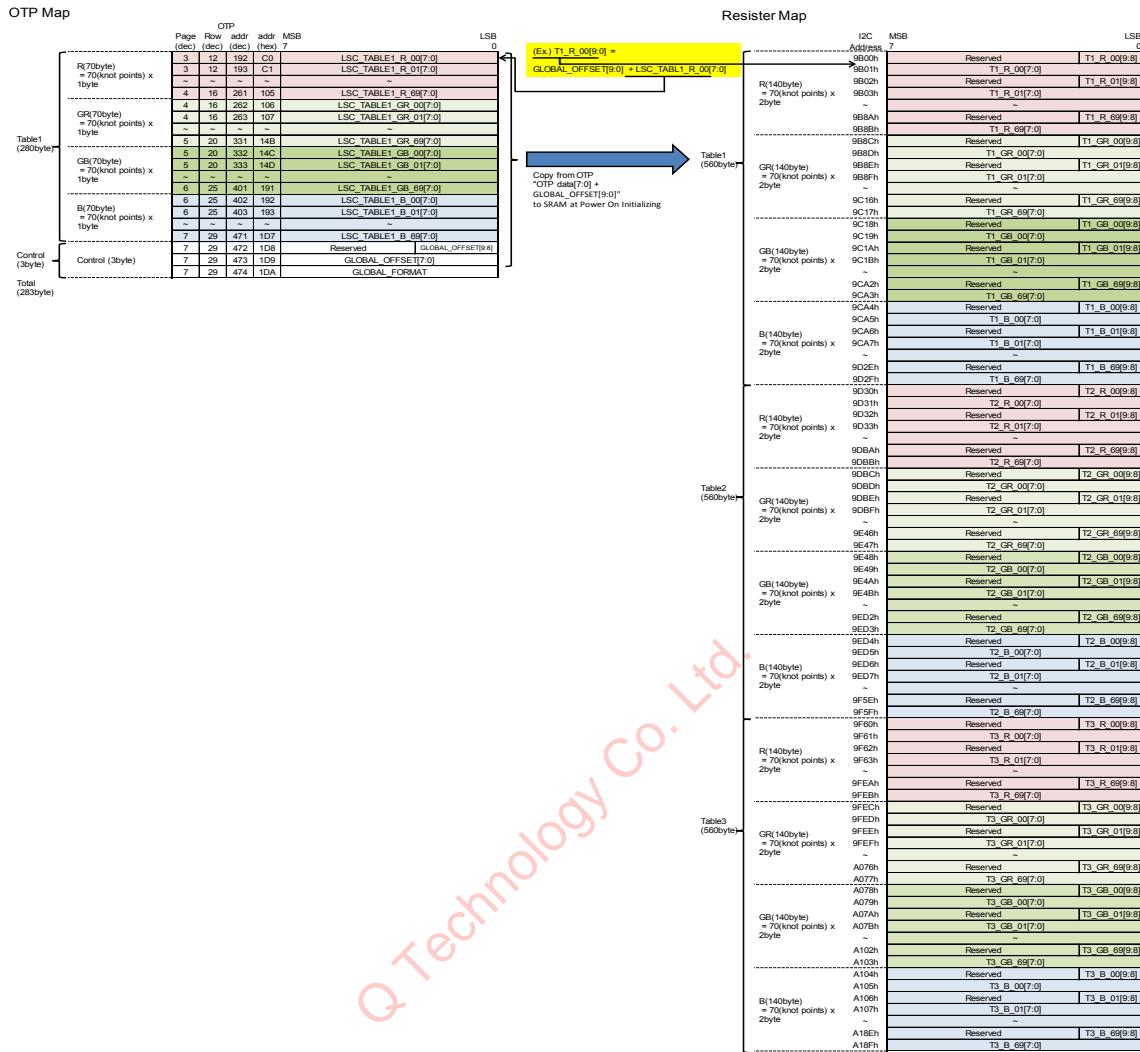


Figure 9-10 Knot table data loaded to sensor SRAM

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## 10. Register Map

See Register Map of this sensor.

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## Appendix

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### A-1. Register update grouping

In 7.1 and 7.2, operation and setting method of each register is mainly discussed. In this Appendix chapter, on the other hand, registers are discussed as groups classified by update timing, setting reason, behavior of each register depending on various mode transition, Practical method of combining and updating various types of registers are main theme of this section.

#### A-1.1 Procedure for mode transition setting

In this sensor, most of registers are grouped as follows from register update aspect.

##### Group A (Global setting only in Power On)

A-1: INCK and PLL setting

A-2: Global settings (basic configuration, Analog parameters and IQ parameters)

##### Group B (Operation mode settings for every mode change)

B-1: must be set in SW-standby (see Table 7-3)

B-2: corrupted frame related registers (see Table 7-4)

B-3: other most registers in address # of 0x0xx and 0x3xx (except Group A/B-1/B-2/C)

##### Group C (special purpose registers)

C-2: must be set every time before change in streaming as work around (defined as needed).

C-3: Temperature sensor related registers (for detail see 8.1 )

#### A-1.2 Things to be considered for mode transitions

The following table shows various issues around mode transitions that have to be kept in mind.

As you can see in the following table, there are two methods in the capture mode transitions as follows:

##### Via SW-standby transition

In this method, all mode change related registers are set during software standby state and is universal method of mode transition. The SW-standby is controlled by MODE\_SEL.

### On-the-fly transition

This mode transition is to instantly change the streaming without using SW-standby. This mode does not insert black out of image during mode transition if the condition of usage is matched. On-the-fly transition method usually has some constraints for usage, and so the usable case is limited. On-the-fly transition is controlled by GPH (Grouped parameter hold).

**Table A-1 Summary of mode transition related issues**

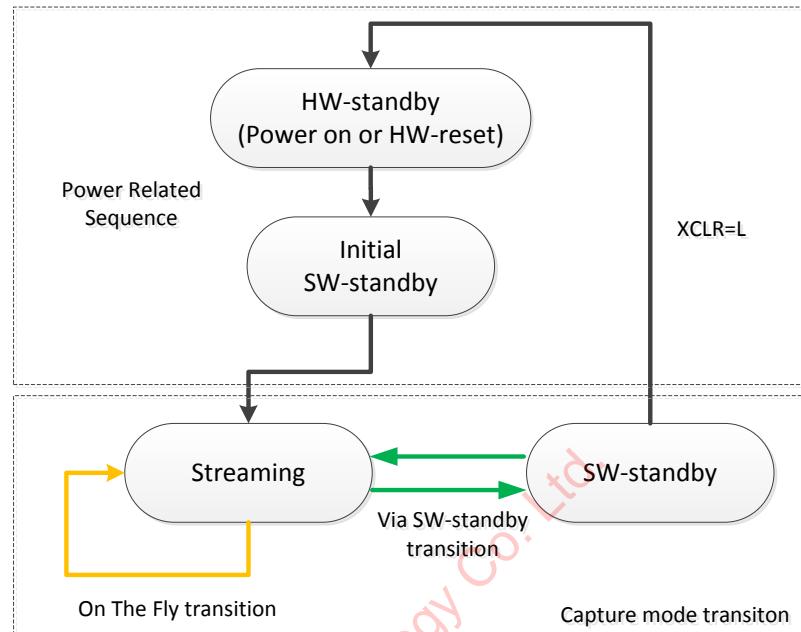
Capture mode transition method		Use of GPH	Shutter lag	Corrupted frame output	Applicable register update Group	Register example *1
Via SW-standby	SW-standby mode transition	No	Long	No	All of A, B, C	IOP_SYS_DIV REQ_LINK_BIT_RATE_MBPS
	Fast SW-standby mode transition	No	Short	Yes	All of A, B, C	
On the fly	Complete mode transition	Yes	Long	No	B-2, B-3	Y_ADD_STA BINNING_TYPE
	Truncate mode transition	Yes	Short	Yes	B-2, B-3	

Note \*1: To know more about group classification of each register, see Register Map of this sensor or Register Setting Table of this sensor.

### A-1.3 Mode transition procedure

In this paragraph, practical method of mode transition sequence and register settings are explained.

From mode transition view point, sensor's states are divided into the following four stats; (1) Power ON, (2) Initial SW-standby, (3) Streaming and (4) SW-standby.



**Figure A-1 Mode transitions**

Purpose of the above figure is to simply describe the mode transitions from power on to streaming (Power related sequence) and between streaming (Capture mode transitions).

**Table A-2 Mode transition procedures**

Mode transition	Transition procedures
← Power related sequence	Group A-1 → Group A-2, Group B(all) → MODE_SEL=1 Minimum setting <sup>1</sup> : Difference from registers' default value of Group B
← On The Fly transition	GPH=1 → Group B-2, B-3, Group C-1 → GPH=0 Example: From Normal capture mode of full 2 Binning to Normal capture mode of full resolution. Minimum setting <sup>1</sup> : Difference of register value between the transition modes.
← Via SW-standby	MODE_SEL=0 → Group B-1, B-2, B-3, Group C-1 → MODE_SEL=1 Example: From Normal capture mode of full resolution to Normal capture mode of 2-binning with MIPI low data rate Minimum setting <sup>1</sup> : Difference of register value between the transition modes.

Note \*1 : Minimum setting can reduce CCI transfer time.

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## A-2. Embedded data lines

Contents and output sequence of Embedded Data Lines are shown as below.

**Table A-3 EBD LINE 0**

Pixel#	Index	Register Name	EBD Byte	Meaning of EBD Byte
1			0x0A	EBD Format Code (0x0a = Simplified 2byte Tagged Data Format)
2			0xAA	Tag
3			0x00	Register Address MSB[15:8]
4			0xA5	Tag
5			0x05	Register Address LSB[7:0]
6			0x5A	Tag
7	0x0005	FRM_CNT	value	Valid data
8			0x5A	Tag
9	0x0006	PIX_ORDER	value	Valid data
10			0x55	Tag
11			0x07	Dummy data
12			0x5A	Tag
13	0x0008	DT_PEDESTAL[9:8]	value	Valid data
14			0x5A	Tag
15	0x0009	DT_PEDESTAL[7:0]	value	Valid data
16			0xAA	Tag
17			0x01	Register Address MSB[15:8]
18			0xA5	Tag
19			0x01	Register Address LSB[7:0]
20			0x5A	Tag
21	0x0101	IMG_ORIENTATION_V/IMG_ORIENTATION_H	value	Valid data
22			0xA5	Tag
23			0x10	Register Address LSB[7:0]
24			0x5A	Tag
25	0x0110	CSI_CH_ID	value	Valid data
26			0xA5	Tag
27			0x36	Register Address LSB[7:0]

Pixel#	Index	Register Name	EBD Byte	Meaning of EBD Byte
28			0x5A	Tag
29	0x0136	EXCK_FREQ[15:8]	value	Valid data
30			0x5A	Tag
31	0x0137	EXCK_FREQ[7:0]	value	Valid data
32			0x5A	Tag
33	0x0138	TEMP_SEN_CTL	value	Valid data
34			0x55	Tag
35			0x07	Dummy data
36			0x5A	Tag
37	0x013A	TEMP_SEN_OUT	value	Valid data
38			0xAA	Tag
39			0x02	Register Address MSB[15:8]
40			0xA5	Tag
41			0x00	Register Address LSB[7:0]
42			0x5A	Tag
43	0x0200	FINE_INTEG_TIME[15:8]	value	Valid data
44			0x5A	Tag
45	0x0201	FINE_INTEG_TIME[7:0]	value	Valid data
46			0x5A	Tag
47	0x0202	COARSE_INTEG_TIME[15:8]	value	Valid data
48			0x5A	Tag
49	0x0203	COARSE_INTEG_TIME[7:0]	value	Valid data
50			0x5A	Tag
51	0x0204	ANA_GAIN_GLOBAL[9:8]	value	Valid data
52			0x5A	Tag
53	0x0205	ANA_GAIN_GLOBAL[7:0]	value	Valid data
54			0xA5	Tag
55			0x0E	Register Address LSB[7:0]
56			0x5A	Tag
57	0x020E	DIG_GAIN_GR[15:8]	value	Valid data
58			0x5A	Tag
59	0x020F	DIG_GAIN_GR[7:0]	value	Valid data
60			0x5A	Tag
61	0x0210	DIG_GAIN_R[15:8]	value	Valid data

Pixel#	Index	Register Name	EBD Byte	Meaning of EBD Byte
62			0x5A	Tag
63	0x0211	DIG_GAIN_R[7:0]	value	Valid data
64			0x5A	Tag
65	0x0212	DIG_GAIN_B[15:8]	value	Valid data
66			0x5A	Tag
67	0x0213	DIG_GAIN_B[7:0]	value	Valid data
68			0x5A	Tag
69	0x0214	DIG_GAIN_GB[15:8]	value	Valid data
70			0x5A	Tag
71	0x0215	DIG_GAIN_GB[7:0]	value	Valid data
72			0xAA	Tag
73			0x03	Register Address MSB[15:8]
74			0xA5	Tag
75			0x01	Register Address LSB[7:0]
76			0x5A	Tag
77	0x0301	IVT_PXCK_DIV	value	Valid data
78			0x55	Tag
79			0x07	Dummy data
80			0x5A	Tag
81	0x0303	IVT_SYCK_DIV	value	Valid data
82			0x55	Tag
83			0x07	Dummy data
84			0x5A	Tag
85	0x0305	IVT_PREPLLCK_DIV	value	Valid data
86			0x5A	Tag
87	0x0306	IVT_PLL_MPY[10:8]	value	Valid data
88			0x5A	Tag
89	0x0307	IVT_PLL_MPY[7:0]	value	Valid data
90			0x55	Tag
91			0x07	Dummy data
92			0x5A	Tag
93	0x0309	IOP_PXCK_DIV	value	Valid data
94			0x55	Tag
95			0x07	Dummy data

Pixel#	Index	Register Name	EBD Byte	Meaning of EBD Byte
96			0x5A	Tag
97	0x030B	IOP_SYCK_DIV	value	Valid data
98			0x55	Tag
99			0x07	Dummy data
100			0x5A	Tag
101	0x030D	IOP_PREPLLCK_DIV	value	Valid data
102			0x5A	Tag
103	0x030E	IOP_PLL_MPY[10:8]	value	Valid data
104			0x5A	Tag
105	0x030F	IOP_PLL_MPY[7:0]	value	Valid data
106			0x5A	Tag
107	0x0310	PLL_MULT_DRIV	value	Valid data
108			0xA5	Tag
109			0x40	Register Address LSB[7:0]
110			0x5A	Tag
111	0x0340	FRM_LENGTH_LINES[15:8]	value	Valid data
112			0x5A	Tag
113	0x0341	FRM_LENGTH_LINES[7:0]	value	Valid data
114			0x5A	Tag
115	0x0342	LINE_LENGTH_PCK[15:8]	value	Valid data
116			0x5A	Tag
117	0x0343	LINE_LENGTH_PCK[7:0]	value	Valid data
118			0x5A	Tag
119	0x0344	X_ADD_STA[12:8]	value	Valid data
120			0x5A	Tag
121	0x0345	X_ADD_STA[7:0]	value	Valid data
122			0x5A	Tag
123	0x0346	Y_ADD_STA[11:8]	value	Valid data
124			0x5A	Tag
125	0x0347	Y_ADD_STA[7:0]	value	Valid data
126			0x5A	Tag
127	0x0348	X_ADD_END[12:8]	value	Valid data
128			0x5A	Tag
129	0x0349	X_ADD_END[7:0]	value	Valid data

Pixel#	Index	Register Name	EBD Byte	Meaning of EBD Byte
130			0x5A	Tag
131	0x034A	Y_ADD_END[11:8]	value	Valid data
132			0x5A	Tag
133	0x034B	Y_ADD_END[7:0]	value	Valid data
134			0x5A	Tag
135	0x034C	X_OUT_SIZE[12:8]	value	Valid data
136			0x5A	Tag
137	0x034D	X_OUT_SIZE[7:0]	value	Valid data
138			0x5A	Tag
139	0x034E	Y_OUT_SIZE[11:8]	value	Valid data
130			0x5A	Tag
141	0x034F	Y_OUT_SIZE[7:0]	value	Valid data
142			0xA5	Tag
143			0x80	Register Address LSB[7:0]
144			0x5A	Tag
145			0x00	Reserved data
146			0x5A	Tag
147	0x0381	X_EVN_INC	value	Valid data
148			0x5A	Tag
149			0x00	Reserved data
150			0x5A	Tag
151	0x0383	X_ODD_INC	value	Valid data
152			0x5A	Tag
153			0x00	Reserved data
154			0x5A	Tag
155	0x0385	Y_EVN_INC	value	Valid data
156			0x5A	Tag
157			0x00	Reserved data
158			0x5A	Tag
159	0x0387	Y_ODD_INC	value	Valid data
160			0x07	End of Data
161			0x07	End of Data

**Table A-4 EBD LINE 1**

Pixel#	Index	Register Name	EBD Byte	Meaning of EDB Byte
1			0x0A	EBD Format Code (0x0a = Simplified 2byte Tagged Data Format)
2			0xAA	Tag
3			0x09	Register Address MSB[15:8]
4			0xA5	Tag
5			0x00	Register Address LSB[7:0]
6			0x5A	Tag
7	0x0900	BINNING_MODE	value	Valid data
8			0x5A	Tag
9	0x0901	BINNING_TYPE_H/BINNING_TYPE_V	value	Valid data
10			0x5A	Tag
11	0x0902	BINNING_WEIGHTING	value	Valid data
12			0xAA	Tag
13			0x0B	Register Address MSB[15:8]
14			0xA5	Tag
15			0x00	Register Address LSB[7:0]
16			0x5A	Tag
17	0xB00	SHD_CORR_EN	value	Valid data
18			0xA5	Tag
19			0x04	Register Address LSB[7:0]
20			0x5A	Tag
21	0xB04	BLK_LEV_CORR_EN	value	Valid data
22			0x5A	Tag
23	0xB05	MAP_COUP_CORR_EN	value	Valid data
24			0x5A	Tag
25	0xB06	SING_DEF_CORR_EN	value	Valid data
26			0xA5	Tag
27			0x8E	Register Address LSB[7:0]
28			0x5A	Tag
29	0xB8E	ABS_GAIN_GR[15:8]	value	Valid data
30			0x5A	Tag
31	0xB8F	ABS_GAIN_GR[7:0]	value	Valid data
32			0x5A	Tag

Pixel#	Index	Register Name	EBD Byte	Meaning of EDB Byte
33	0x0B90	ABS_GAIN_R[15:8]	value	Valid data
34			0x5A	Tag
35	0x0B91	ABS_GAIN_R[7:0]	value	Valid data
36			0x5A	Tag
37	0x0B92	ABS_GAIN_B[15:8]	value	Valid data
38			0x5A	Tag
39	0x0B93	ABS_GAIN_B[7:0]	value	Valid data
40			0x5A	Tag
41	0x0B94	ABS_GAIN_GB[15:8]	value	Valid data
42			0x5A	Tag
43	0x0B95	ABS_GAIN_GB[7:0]	value	Valid data
44			0xAA	Tag
45			0x0C	Register Address MSB[15:8]
46			0xA5	Tag
47			0x12	Register Address LSB[7:0]
48			0x5A	Tag
49	0x0C12	FLASH_STRB_ADJ	value	Valid data
50			0x55	Tag
51			0x07	Dummy data
52			0x5A	Tag
53	0x0C14	FLASH_STRB_START_POINT[15:8]	value	Valid data
54			0x5A	Tag
55	0x0C15	FLASH_STRB_START_POINT[7:0]	value	Valid data
56			0x5A	Tag
57	0x0C16	TFLASH_STRB_DLY_RS_CTL[15:8]	value	Valid data
58			0x5A	Tag
59	0x0C17	TFLASH_STRB_DLY_RS_CTL[7:0]	value	Valid data
60			0x5A	Tag
61	0x0C18	TFLASH_STRB_WIDTH_H_RS_CTL[15:8]	value	Valid data
62			0x5A	Tag
63	0x0C19	TFLASH_STRB_WIDTH_H_RS_CTL[7:0]	value	Valid data
64			0x5A	Tag
65	0x0C1A	FLASH_MD_RS	value	Valid data
66			0x5A	Tag

Pixel#	Index	Register Name	EBD Byte	Meaning of EDB Byte
67			value	Reserved data
68			0x5A	Tag
69	0x0C1C	FLASH_STAT	value	Valid data
70			0xA5	Tag
71			0x26	Register Address LSB[7:0]
72			0x5A	Tag
73	0x0C26	TFLASH_STRB_WIDTH2_H_RS_CTL[15:8]	value	Valid data
74			0x5A	Tag
75	0x0C27	TFLASH_STRB_WIDTH2_H_RS_CTL[7:0]	value	Valid data
76			0x5A	Tag
77	0x0C28	TFLASH_STRB_WIDTH_L_RS_CTL[15:8]	value	Valid data
78			0x5A	Tag
79	0x0C29	TFLASH_STRB_WIDTH_L_RS_CTL[7:0]	value	Valid data
80			0x5A	Tag
81	0x0C2A	TFLASH_STRB_CNT_RS_CTL	value	Valid data
82			0xAA	Tag
83			0x30	Register Address MSB[15:8]
84			0xA5	Tag
85			0x03	Register Address LSB[7:0]
86			0x5A	Tag
87	0x3003		value	Reserved data
88			0xAA	Tag
89			0x31	Register Address MSB[15:8]
90			0xA5	Tag
91			0x00	Register Address LSB[7:0]
92			0x5A	Tag
93	0x3100	CIT_LSHIFT	value	Valid data
94			0xAA	Tag
95			0x37	Register Address MSB[15:8]
96			0xA5	Tag
97			0xC8	Register Address LSB[7:0]
98			0x5A	Tag
99			value	Dummy data
100			0x5A	Tag

Pixel#	Index	Register Name	EBD Byte	Meaning of EDB Byte
101			value	Dummy data
102			0x5A	Tag
103			value	Dummy data
104			0x5A	Tag
105			value	Dummy data
106			0xAA	Tag
107			0x3D	Register Address MSB[15:8]
108			0xA5	Tag
109			0x90	Register Address LSB[7:0]
110			0x5A	Tag
111	0x3D90		value	Invalid data
112			0x5A	Tag
113	0x3D91		value	Invalid data
114			0xAA	Tag
115			0x3F	Register Address MSB[15:8]
116			0xA5	Tag
117			0x4C	Register Address LSB[7:0]
118			0x5A	Tag
119	0x3F4C	BINNING_PRIORITY_V	value	Valid data
120			0x5A	Tag
121	0x3F4D	BINNING_PRIORITY_H	value	Valid data
122			0xA5	Tag
123			0x6C	Register Address LSB[7:0]
124			0x5A	Tag
125	0x3F6C	EXTOUT_XVS_MULT_SEL	value	Valid data
126			0x5A	Tag
127	0x3F6D	EXTOUT_XVS_MULT	value	Valid data
128			0x5A	Tag
129	0x3F6E	EXTIN_XVS_MULT_SEL	value	Valid data
130			0x5A	Tag
131	0x3F6F	EXTIN_XVS_MULT	value	Valid data
132			0xA5	Tag
133			0xF9	Register Address LSB[7:0]
134			0x5A	Tag

Pixel#	Index	Register Name	EBD Byte	Meaning of EDB Byte
135	0x3FF9	DPGA_USE_GLOBAL_GAIN	value	Valid data
136			0x07	End of Data
137			0x07	

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