# Single Supply Dual Operational Amplifiers

LM258, LM358, LM358A, LM358E, LM2904, LM2904A, LM2904E, LM2904V, NCV2904

Utilizing the circuit designs perfected for Quad Operational Amplifiers, these dual operational amplifiers feature low power drain, a common mode input voltage range extending to ground/V_{EE}, and single supply or split supply operation. The LM358 series is equivalent to one−half of an LM324.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 V or as high as 32 V, with quiescent currents about one−fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

Features

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- ESD Clamps on the Inputs Increase Ruggedness of the Device without Affecting Operation
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant
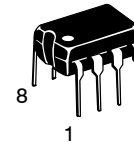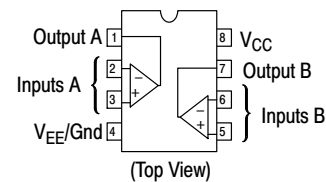
PDIP−8
N, AN, VN SUFFIX
CASE 626

SOIC−8
D, VD SUFFIX
CASE 751
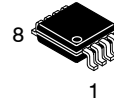
Micro8™
DMR2 SUFFIX
CASE 846A

PIN CONNECTIONS

Output A [1] [8] V_{CC}
Inputs A { [2] [3] [7] Output B
[6] } Inputs B
V_{EE}/Gnd [4] [5]

(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

DEVICE MARKING INFORMATION

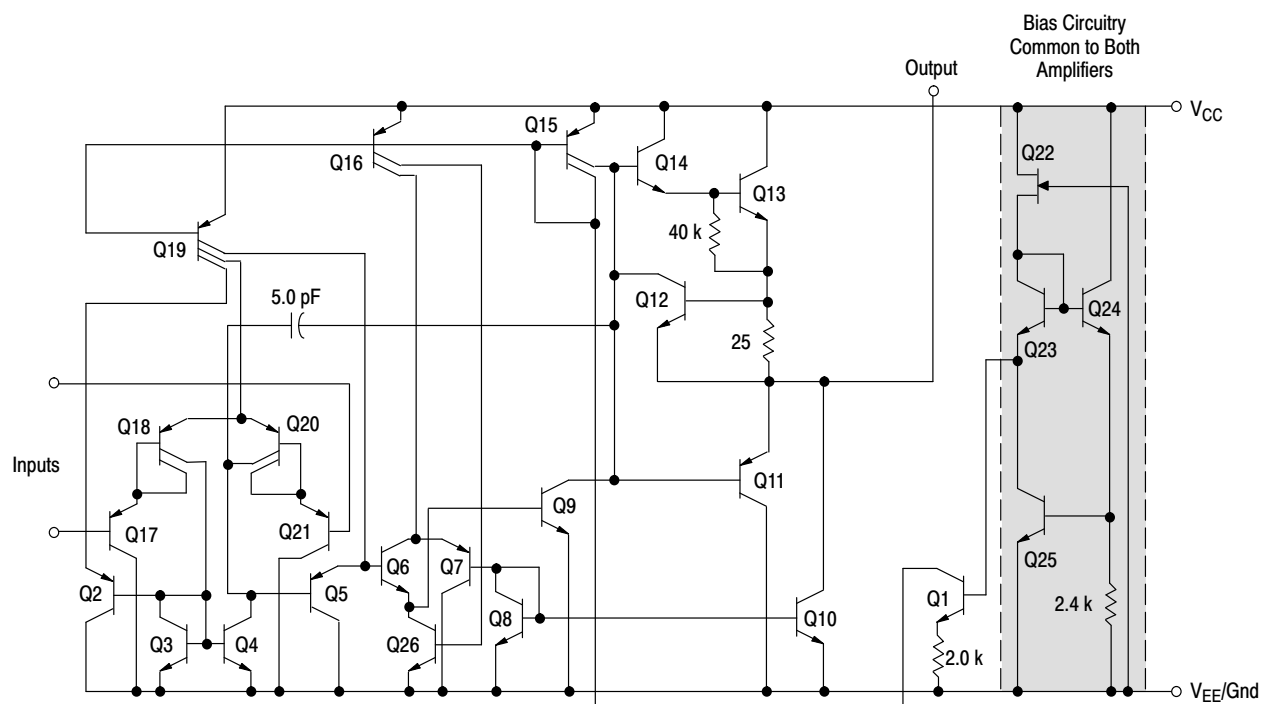See general marking information in the device marking section on page 11 of this data sheet.

LM258, LM358, LM358A, LM358E, LM2904, LM2904A, LM2904E, LM2904V, NCV2904

Single Supply

Split Supplies

Figure 1.

Figure 2. Representative Schematic Diagram
(One−Half of Circuit Shown)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	32 ±16	Vdc
Input Differential Voltage Range (Note 1)	V_{IDR}	±32	Vdc
Input Common Mode Voltage Range	V_{ICR}	−0.3 to 32	Vdc
Output Short Circuit Duration	t_{SC}	Continuous	
Junction Temperature	T_J	150	°C
Thermal Resistance, Junction−to−Air (Note 2) Case 846A Case 751 Case 626	$R_{\theta JA}$	238 212 161	°C/W
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Ambient Temperature Range LM258 LM358, LM358A, LM358E LM2904, LM2904A, LM2904E LM2904V, NCV2904 (Note 3)	T_A	 −25 to +85 0 to +70 −40 to +105 −40 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Split Power Supplies.
2. All $R_{\theta JA}$ measurements made on evaluation board with 1 oz. copper traces of minimum pad size. All device outputs were active.
3. *NCV2904 is qualified for automotive use.*

ESD RATINGS

Rating	HBM	MM	Unit
ESD Protection at any Pin (Human Body Model – HBM, Machine Model – MM) NCV2904 (Note 3) LM358E, LM2904E LM358DG/DR2G, LM2904DG/DR2G All Other Devices	 2000 2000 250 2000	 200 200 100 200	 V V V V

LM258, LM358, LM358A, LM358E, LM2904, LM2904A, LM2904E, LM2904V, NCV2904

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = GND, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	LM258 Min	LM258 Typ	LM258 Max	LM358, LM358E Min	LM358, LM358E Typ	LM358, LM358E Max	LM358A Min	LM358A Typ	LM358A Max	Unit
Input Offset Voltage V_{CC} = 5.0 V to 30 V, V_{IC} = 0 V to V_{CC} −1.7 V, $V_O \simeq$ 1.4 V, R_S = 0 Ω 　T_A = 25°C 　T_A = T_{high} (Note 4) 　T_A = T_{low} (Note 4)	V_{IO}	– – –	2.0 – –	5.0 7.0 7.0	– – –	2.0 – –	7.0 9.0 9.0	– – –	2.0 – –	3.0 5.0 5.0	mV
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low} (Note 4)	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	–	–	7.0	–	µV/°C
Input Offset Current 　T_A = T_{high} to T_{low} (Note 4) Input Bias Current 　T_A = T_{high} to T_{low} (Note 4)	I_{IO} I_{IB}	– – – –	3.0 – −45 −50	30 100 −150 −300	– – – –	5.0 – −45 −50	50 150 −250 −500	– – – –	5.0 – −45 −50	30 75 −100 −200	nA
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low} (Note 4)	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	pA/°C
Input Common Mode Voltage Range (Note 5), V_{CC} = 30 V V_{CC} = 30 V, T_A = T_{high} to T_{low}	V_{ICR}	0 0	– –	28.3 28	0 0	– –	28.3 28	0 0	– –	28.5 28	V
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
Large Signal Open Loop Voltage Gain R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing, T_A = T_{high} to T_{low} (Note 4)	A_{VOL}	50 25	100 –	– –	25 15	100 –	– –	25 15	100 –	– –	V/mV
Channel Separation 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	CS	–	−120	–	–	−120	–	–	−120	–	dB
Common Mode Rejection R_S ≤ 10 kΩ	CMR	70	85	–	65	70	–	65	70	–	dB
Power Supply Rejection	PSR	65	100	–	65	100	–	65	100	–	dB
Output Voltage–High Limit T_A = T_{high} to T_{low} (Note 4) V_{CC} = 5.0 V, R_L = 2.0 kΩ, T_A = 25°C V_{CC} = 30 V, R_L = 2.0 kΩ V_{CC} = 30 V, R_L = 10 kΩ	V_{OH}	 3.3 26 27	 3.5 – 28	 – – –	 3.3 26 27	 3.5 – 28	 – – –	 3.3 26 27	 3.5 – 28	 – – –	V
Output Voltage–Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, 　T_A = T_{high} to T_{low} (Note 4)	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	20	mV
Output Source Current V_{ID} = +1.0 V, V_{CC} = 15 V T_A = T_{high} to T_{low} (LM358A Only)	I_{O+}	20	40	–	20	40	–	20 10	40 –	– –	mA
Output Sink Current V_{ID} = −1.0 V, V_{CC} = 15 V T_A = T_{high} to T_{low} (LM358A Only) V_{ID} = −1.0 V, V_O = 200 mV	$I_{O−}$	10 12	20 50	– –	10 12	20 50	– –	10 5.0 12	20 – 50	– – –	mA mA µA
Output Short Circuit to Ground (Note 6)	I_{SC}	–	40	60	–	40	60	–	40	60	mA
Power Supply Current (Total Device) T_A = T_{high} to T_{low} (Note 4) V_{CC} = 30 V, V_O = 0 V, R_L = ∞ V_{CC} = 5 V, V_O = 0 V, R_L = ∞	I_{CC}	 – –	 1.5 0.7	 3.0 1.2	 – –	 1.5 0.7	 3.0 1.2	 – –	 1.5 0.7	 2.0 1.2	mA

4. LM258: T_{low} = −25°C, T_{high} = +85°C   LM358, LM358A, LM358E: T_{low} = 0°C, T_{high} = +70°C
　 LM2904/A/E: T_{low} = −40°C, T_{high} = +105°C   LM2904V & NCV2904: T_{low} = −40°C, T_{high} = +125°C
　 NCV2904 is qualified for automotive use.
5. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} − 1.7 V.
6. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

LM258, LM358, LM358A, LM358E, LM2904, LM2904A, LM2904E, LM2904V, NCV2904

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	LM2904/LM2904E Min	Typ	Max	LM2904A Min	Typ	Max	LM2904V, NCV2904 Min	Typ	Max	Unit

Input Offset Voltage
V_{CC} = 5.0 V to 30 V, V_{IC} = 0 V to V_{CC} −1.7 V,
$V_O \simeq$ 1.4 V, R_S = 0 Ω
    T_A = 25°C
    T_A = T_{high} (Note 7)
    T_A = T_{low} (Note 7)
	V_{IO}	
		
		−
		−
		−
			
			2.0
			−
			−
				
				7.0
				10
				10
					
					−
					−
					−
						
						2.0
						−
						−
							
							7.0
							10
							10
								
								−
								−
								−
									
									−
									−
									−
										
										7.0
										13
										10
											mV

Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low} (Note 7)	$\Delta V_{IO}/\Delta T$	−	7.0	−	−	7.0	−	−	7.0	−	µV/°C

Input Offset Current
    T_A = T_{high} to T_{low} (Note 7)
Input Bias Current
    T_A = T_{high} to T_{low} (Note 7)
	I_{IO}
	
	I_{IB}
		−
		−
		−
		−
			5.0
			45
			−45
			−50
				50
				200
				−250
				−500
					−
					−
					−
					−
						5.0
						45
						−45
						−50
							50
							200
							−100
							−250
								−
								−
								−
								−
									5.0
									45
									−45
									−50
										50
										200
										−250
										−500
											nA

Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low} (Note 7)	$\Delta I_{IO}/\Delta T$	−	10	−	−	10	−	−	10	−	pA/°C
Input Common Mode Voltage Range (Note 8), V_{CC} = 30 V V_{CC} = 30 V, T_A = T_{high} to T_{low}	V_{ICR}	0 0	− −	28.3 28	0 0	− −	28.3 28	0 0	− −	28.3 28	V
Differential Input Voltage Range	V_{IDR}	−	−	V_{CC}	−	−	V_{CC}	−	−	V_{CC}	V

Large Signal Open Loop Voltage Gain
    R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing,
    T_A = T_{high} to T_{low} (Note 7)
	A_{VOL}	25
		15
			100
			−
				−
				−
					25
					15
						100
						−
							−
							−
								25
								15
									100
									−
										−
										−
											V/mV

Channel Separation 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	CS	−	−120	−	−	−120	−	−	−120	−	dB
Common Mode Rejection R_S ≤ 10 kΩ	CMR	50	70	−	50	70	−	50	70	−	dB
Power Supply Rejection	PSR	50	100	−	50	100	−	50	100	−	dB

Output Voltage−High Limit
    T_A = T_{high} to T_{low} (Note 7)
    V_{CC} = 5.0 V, R_L = 2.0 kΩ, T_A = 25°C
    V_{CC} = 30 V, R_L = 2.0 kΩ
    V_{CC} = 30 V, R_L = 10 kΩ
	V_{OH}	
		
		3.3
		26
		27
			
			3.5
			−
			28
				
				−
				−
				−
					
					3.3
					26
					27
						
						3.5
						−
						28
							
							−
							−
							−
								
								3.3
								26
								27
									
									3.5
									−
									28
										
										−
										−
										−
											V

Output Voltage−Low Limit
    V_{CC} = 5.0 V, R_L = 10 kΩ,
    T_A = T_{high} to T_{low} (Note 7)
	V_{OL}	−	5.0	20	−	5.0	20	−	5.0	20	mV

Output Source Current V_{ID} = +1.0 V, V_{CC} = 15 V	I_{O+}	20	40	−	20	40	−	20	40	−	mA

Output Sink Current
    V_{ID} = −1.0 V, V_{CC} = 15 V
    V_{ID} = −1.0 V, V_O = 200 mV
	I_{O-}	10
		−
			20
			−
				−
				−
					10
					−
						20
						−
							−
							−
								10
								−
									20
									−
										−
										−
											mA
											µA

Output Short Circuit to Ground (Note 9)	I_{SC}	−	40	60	−	40	60	−	40	60	mA

Power Supply Current (Total Device)
    T_A = T_{high} to T_{low} (Note 7)
    V_{CC} = 30 V, V_O = 0 V, R_L = ∞
    V_{CC} = 5 V, V_O = 0 V, R_L = ∞
	I_{CC}	
		
		−
		−
			
			1.5
			0.7
				
				3.0
				1.2
					
					−
					−
						
						1.5
						0.7
							
							3.0
							1.2
								
								−
								−
									
									1.5
									0.7
										
										3.0
										1.2
											mA

7. LM258: T_{low} = −25°C, T_{high} = +85°C   LM358, LM358A, LM358E: T_{low} = 0°C, T_{high} = +70°C
   LM2904/A/E: T_{low} = −40°C, T_{high} = +105°C   LM2904V & NCV2904: T_{low} = −40°C, T_{high} = +125°C
   NCV2904 is qualified for automotive use.
8. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} − 1.7 V.
9. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

CIRCUIT DESCRIPTION

The LM358 series is made using two internally compensated, two−stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single−ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal−voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.
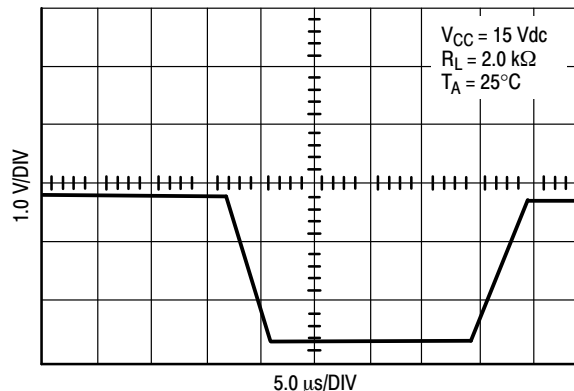
Figure 3. Large Signal Voltage Follower Response
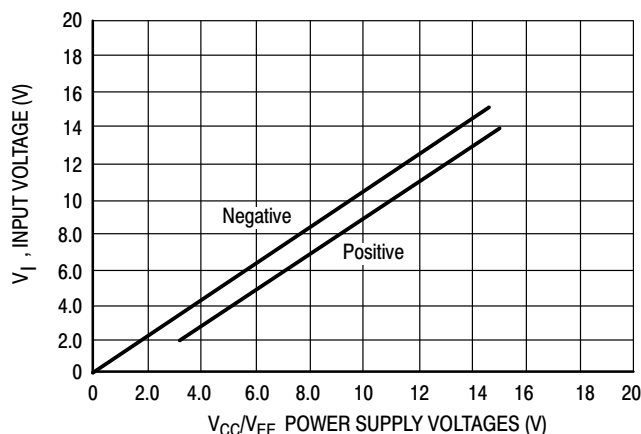
Figure 4. Input Voltage Range
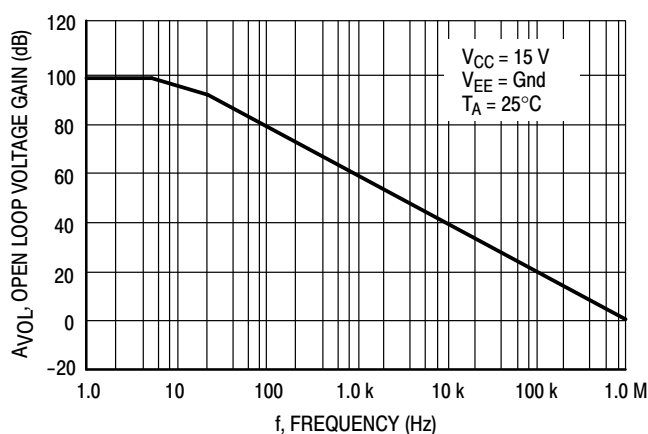
Figure 5. Large−Signal Open Loop Voltage Gain
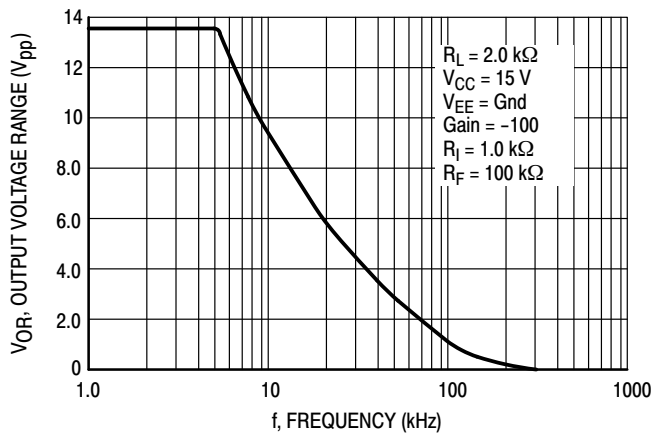
Figure 6. Large−Signal Frequency Response
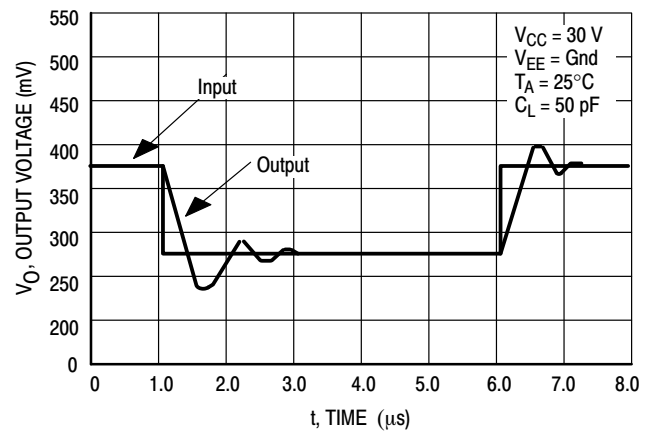
Figure 7. Small Signal Voltage Follower
Pulse Response (Noninverting)
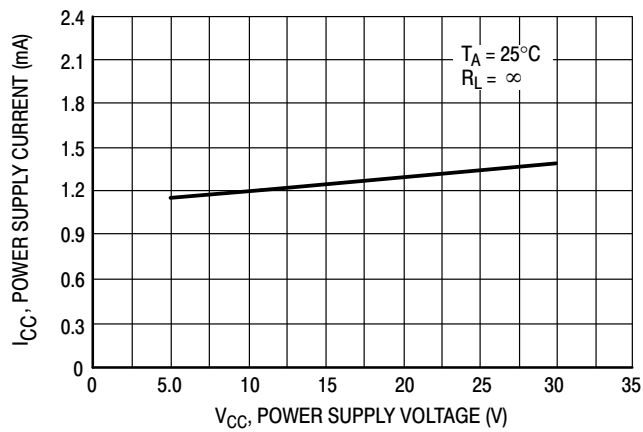
Figure 8. Power Supply Current versus
Power Supply Voltage
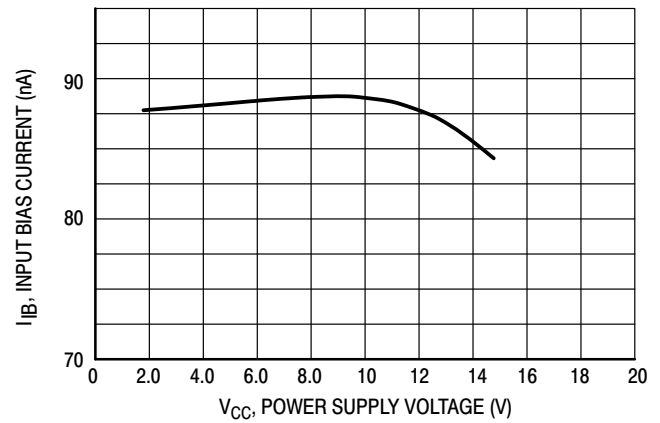
Figure 9. Input Bias Current versus
Supply Voltage
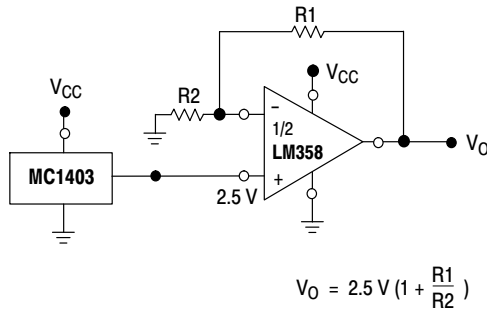
Figure 10. Voltage Reference

$$V_O = 2.5 \text{ V} \left(1 + \frac{R1}{R2}\right)$$
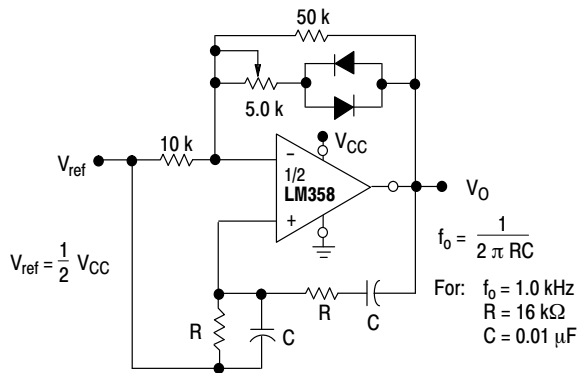
Figure 11. Wien Bridge Oscillator

$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_0 = \frac{1}{2 \pi RC}$$

For: $f_0 = 1.0$ kHz
$R = 16$ kΩ
$C = 0.01$ μF
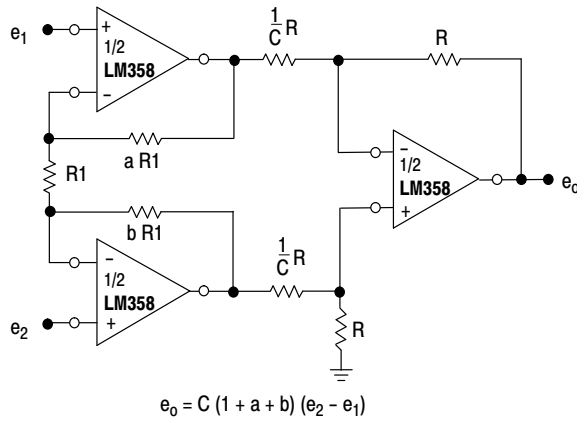
Figure 12. High Impedance Differential Amplifier

$$e_0 = C (1 + a + b)(e_2 - e_1)$$
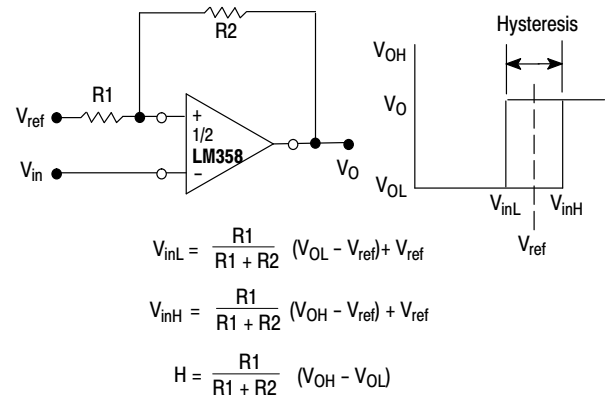
Figure 13. Comparator with Hysteresis

$$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

$$f_0 = \frac{1}{2 \pi RC}$$

$R1 = QR$

$R2 = \dfrac{R1}{T_{BP}}$

$R3 = T_N R2$

$C1 = 10 C$

$$V_{ref} = \frac{1}{2} V_{CC}$$

For: $f_0 = 1.0$ kHz
Q $= 10$
$T_{BP} = 1$
$T_N = 1$

R $= 160$ kΩ
C $= 0.001$ μF
R1 $= 1.6$ MΩ
R2 $= 1.6$ MΩ
R3 $= 1.6$ MΩ

Where: T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain
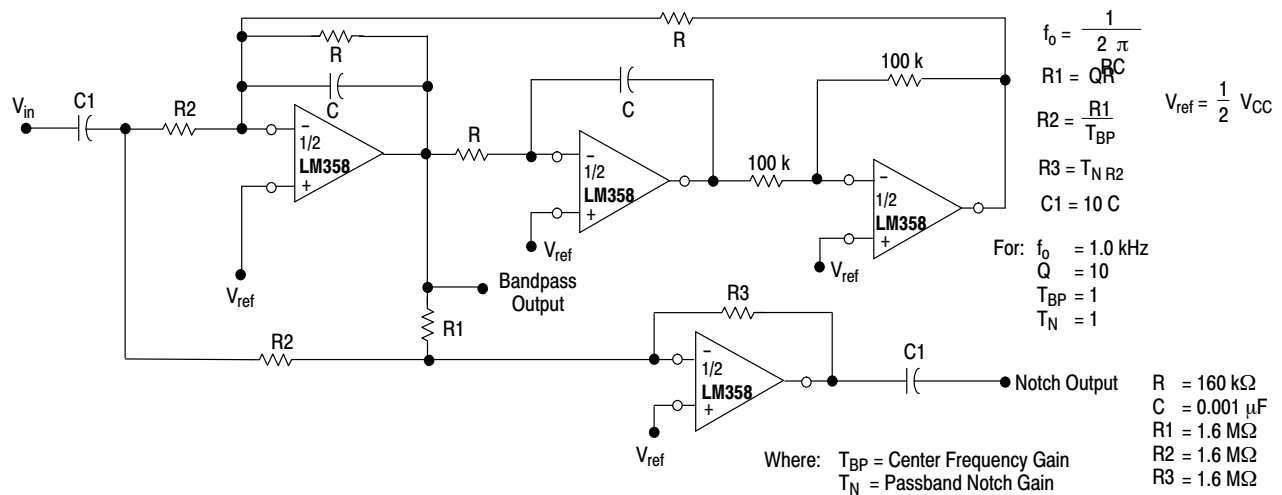
Figure 14. Bi-Quad Filter

$$V_{ref} = \frac{1}{2} V_{CC}$$

Given: f_o = center frequency

$A(f_o)$ = gain at center frequency

Choose value f_o, C

Then: $R3 = \dfrac{Q}{\pi f_o C}$

$R1 = \dfrac{R3}{2 A(f_o)}$

$R2 = \dfrac{R1\ R3}{4Q^2\ R1 - R3}$

For less than 10% error from operational amplifier. $\dfrac{Q_o\ f_o}{BW} < 0.1$

Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

$$f = \frac{R1 + R_C}{4\ CR_f\ R1} \quad \text{if, } R3 = \frac{R2\ R1}{R2 + R1}$$

Figure 15. Function Generator

Figure 16. Multiple Feedback Bandpass Filter

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping[†]
LM358ADR2G	0°C to +70°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM358DG			98 Units / Rail
LM358DR2G			2500 / Tape & Reel
LM358EDR2G		SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM358DMR2G		Micro8 (Pb−Free)	4000 / Tape & Reel
LM358NG		PDIP−8 (Pb−Free)	50 Units / Rail
LM258DG	−25°C to +85°C	SOIC−8 (Pb−Free)	98 Units / Rail
LM258DR2G			2500 / Tape & Reel
LM258DMR2G		Micro8 (Pb−Free)	4000 / Tape & Reel
LM258NG		PDIP−8 (Pb−Free)	50 Units / Rail
LM2904DG	−40°C to +105°C	SOIC−8 (Pb−Free)	98 Units / Rail
LM2904DR2G			2500 / Tape & Reel
LM2904EDR2G		SOIC−8 (Pb−Free)	2500 / Tape & Reel
LM2904DMR2G		Micro8 (Pb−Free)	2500 / Tape & Reel
LM2904NG		PDIP−8 (Pb−Free)	50 Units / Rail
LM2904ADMG		Micro8 (Pb−Free)	4000 / Tape & Reel
LM2904ADMR2G			4000 / Tape & Reel
LM2904ANG		PDIP−8 (Pb−Free)	50 Units / Rail
LM2904VDG	−40°C to +125°C	SOIC−8 (Pb−Free)	98 Units / Rail
LM2904VDR2G			2500 / Tape & Reel
LM2904VDMR2G		Micro8 (Pb−Free)	4000 / Tape & Reel
LM2904VNG		PDIP−8 (Pb−Free)	50 Units / Rail
NCV2904DR2G*		SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV2904DMR2G*		Micro8 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

LM258, LM358, LM358A, LM358E, LM2904, LM2904A, LM2904E, LM2904V, NCV2904

MARKING DIAGRAMS

PDIP−8
N SUFFIX
CASE 626

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8 ┌─────────┐
  │ LMx58N  │
  │ AWL     │
  │ YYWWG   │
1 └─────────┘
```

```
8 ┌─────────┐
  │ LM2904N │
  │ AWL     │
  │ YYWWG   │
1 └─────────┘
```
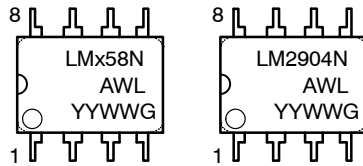
PDIP−8
AN SUFFIX
CASE 626

```
8 ┌──────────┐
  │ LM2904AN │
  │ AWL      │
  │ YYWWG    │
1 └──────────┘
```
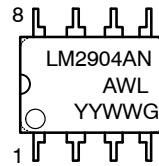
PDIP−8
VN SUFFIX
CASE 626

```
8 ┌──────────┐
  │ LM2904VN │
  │ AWL      │
  │ YYWWG    │
1 └──────────┘
```

SOIC−8
D SUFFIX
CASE 751

```
8 ┌────────┐
  │ LMx58  │
  │ ALYW   │
1 └────────┘
```

```
8 ┌────────┐
  │ LM358  │
  │ ALYWA  │
1 └────────┘
```
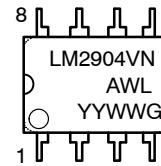
```
8 ┌────────┐
  │ 2904   │
  │ ALYW   │
1 └────────┘
```

SOIC−8
VD SUFFIX
CASE 751

```
8 ┌────────┐
  │ 2904V  │  *
  │ ALYW   │
1 └────────┘
```

```
8 ┌────────┐
  │ 358E   │
  │ ALYWA  │
1 └────────┘
```

```
8 ┌────────┐
  │ 2904E  │
  │ ALYW   │
1 └────────┘
```

Micro8
DMR2 SUFFIX
CASE 846A

```
8 ┌────────┐
  │ x58    │
  │ AYW■   │
1 └────────┘
```

```
8 ┌────────┐
  │ 2904   │
  │ AYW■   │
1 └────────┘
```

```
8 ┌────────┐
  │ 904A   │
  │ AYW■   │
1 └────────┘
```

```
8 ┌────────┐
  │ 904V   │  *
  │ AYW■   │
1 └────────┘
```
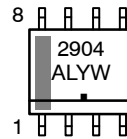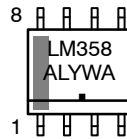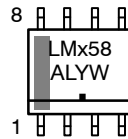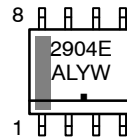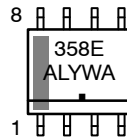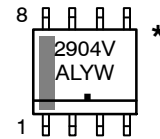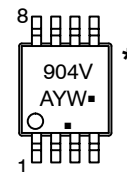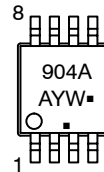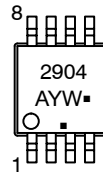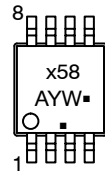
x	= 2 or 3
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Package
■	= Pb−Free Package − (Note: Microdot may be in either location)

*This diagram also applies to NCV2904

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

PDIP-8
CASE 626-05
ISSUE P

DATE 22 APR 2015

SCALE 1:1

TOP VIEW

NOTE 8

END VIEW
WITH LEADS CONSTRAINED
NOTE 5

SIDE VIEW

8X b

⊕ | 0.010 Ⓜ | C | A Ⓜ | B Ⓜ |

END VIEW
NOTE 6
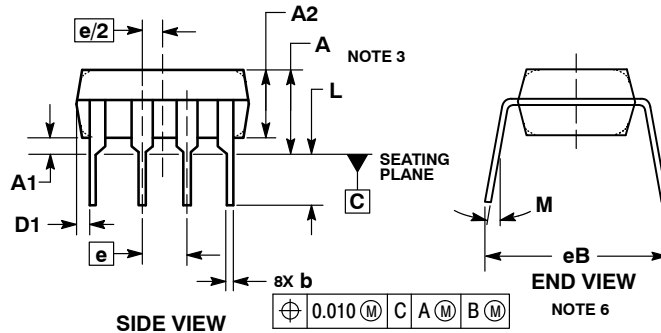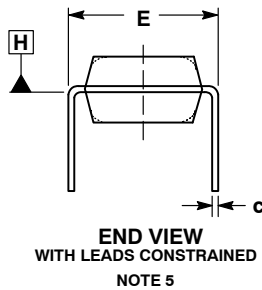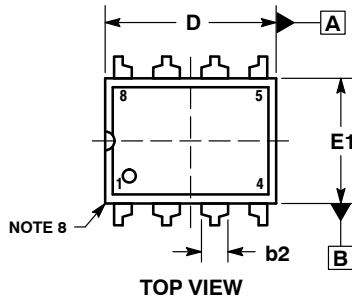
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	**MAX**	**MIN**	**MAX**
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V$_{CC}$

GENERIC
MARKING DIAGRAM*

XXXXXXXXX
AWL
YYWWG
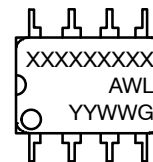
XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪", may or may not be present.

DOCUMENT NUMBER:	98ASB42420B		
DESCRIPTION:	PDIP-8		**PAGE 1 OF 1**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

8

1

SCALE 1:1
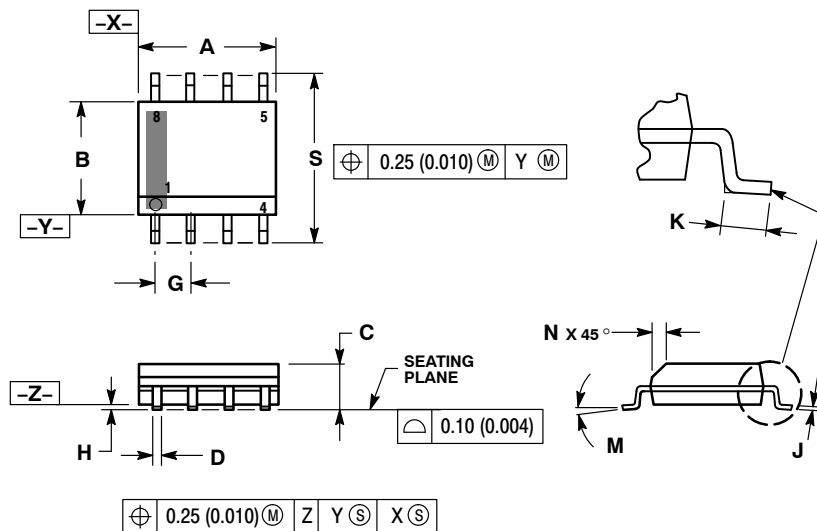
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

⊕ | 0.25 (0.010) Ⓜ | Y Ⓜ

SEATING PLANE

⬜ 0.10 (0.004)

N X 45°

⊕ | 0.25 (0.010) Ⓜ | Z | Y Ⓢ | X Ⓢ

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

$\frac{1.52}{0.060}$

$\frac{7.0}{0.275}$

$\frac{4.0}{0.155}$

$\frac{0.6}{0.024}$

$\frac{1.270}{0.050}$

SCALE 6:1 $\left(\frac{mm}{inches}\right)$

GENERIC MARKING DIAGRAM*

8 XXXXX ALYWX 1 — **IC**

8 XXXXX ALYWX 1 — **IC (Pb−Free)**

8 XXXXXX AYWW 1 — **Discrete**

8 XXXXXX AYWW 1 — **Discrete (Pb−Free)**
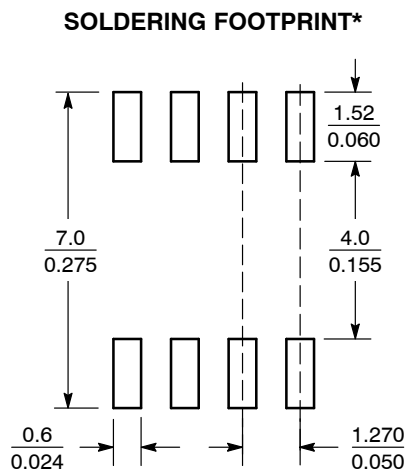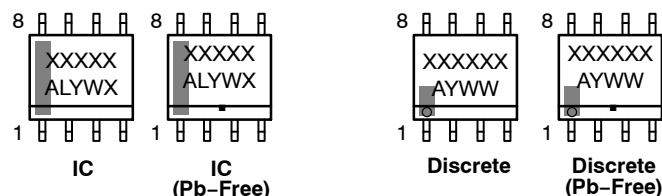
XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B		
DESCRIPTION:	SOIC−8 NB		PAGE 1 OF 2

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

Micro8
CASE 846A–02
ISSUE K

DATE 16 JUL 2020

SCALE 2:1

TOP VIEW

NOTE 3

DETAIL A

SIDE VIEW

END VIEW

DETAIL A

RECOMMENDED
MOUNTING FOOTPRINT

8X 0.48

8X 0.80

5.25

0.65
PITCH

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.

2. CONTROLLING DIMENSION: MILLIMETERS

3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.

4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.

5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.

6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

※ For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***

XXXX
AYW▪

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N–SOURCE
2. N–GATE
3. P–SOURCE
4. P–GATE
5. P–DRAIN
6. P–DRAIN
7. N–DRAIN
8. N–DRAIN

DOCUMENT NUMBER:	98ASB14087C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	MICRO8		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

◊