Circuit Theory and Electronics Fundamentals

Department of Electrical and Computer Engineering, Técnico, University of Lisbon

Third Laboratory Report

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1 Introduction

The objective of this laboratory assignment was to create an AC/DC converter, so a circuit that would transform an input AC voltage of amplitude 230V and frequency of 50Hz to an output DC voltage of 12V using a transformer, an Envelope Detector and a Voltage Regulator circuits according to Figure 1.

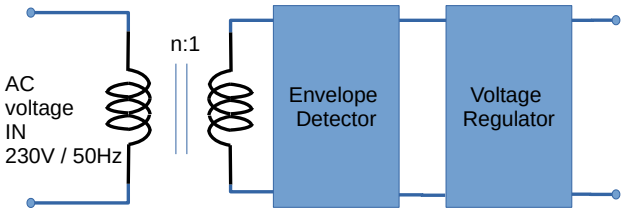

Figure 1: Basic circuit achitecture of an AC/DC converter.

To determine the quality of the circuit and architecture built and to compare it with others, a Merit figure will be calculated based on the following equation:

$$MERIT = \frac{1}{cost * (ripple(v_O) + average(v_O - 12) + 10^{-6})} \tag{1}$$

where the $cost$ value states for sum of the tabulated cost of the components used and the $ripple(v_O)$ and $average(v_O - 12)$ values will be determined throught the output at the Voltage Regulator.

The AC/DC converter circuit built to be theoretically analysed and simulated is shown in Figure 2. The nodes and components are designated with numbers. R1 and C1 states for the resistence and capacitor of the Envelope Detector circuir, respectively. R2 states for the resistence of the Voltage Regulator circuit. A Full-Wave Rectifier circuit with 4 diodes was used. The Voltage Regulator circuit was built using 18 diodes.

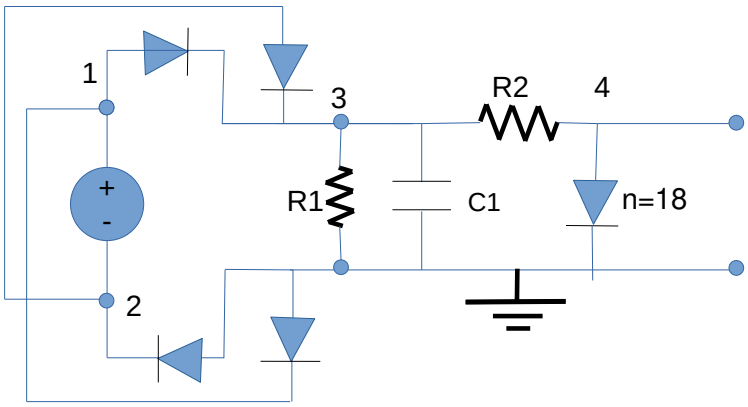

Figure 2: Circuit drawn to build the AC/DC Converter.

The Table 1 shows the values for the resistences and the capacitor used. The n value states for the transformer n:1 ratio used. These values were chosen after running some theoretical and simulation test analysis and are introduced here because they are the values that ended up being used in the last theorethical and simulation analysis, which is the one shown in this report.

Name [unit]	**Value**
n	10.778589
$R_{envelope}$ [kOhm]	150.000000
$C_{envelope}$ [uF]	100.000000
$R_{regulator}$ [kOhm]	5.000000

Table 1: Values considered to build the AC/DC converter circuit.

In Section 2, a theoretical analysis of the circuit built is presented using the values of Table 1. In Section 3, the circuit is analysed by simulation also using the values of Table 1. In Section 4 the results from theoretical and simulation analysis are compared. The conclusions of this study are outlined in Section 5.

2 Theoretical Analysis

In this section we will analyse the circuit shown in Figure 2 theoretically using Octave tools.

The circuit chosen is the most suitable theoretical model we found that was able to most accurately and ideally predict the output of the Envelope Detector as well as the output of the Voltage Regulator.

The tranformer with n:1 ration is represented in our circuit by a voltage source of 230/n [V], where n is the value considered in Table 1. The output of the transformer will be the input of our Envelope detector circuit, which is made of a Full-Wave Rectifier with 4 diodes, a resistence ($R_{envelope}$) and a capacitor ($C_{envelope}$), which values are also in Table 1. The Full-Wave Rectifier was used because it helps to reduce the ripple by reducing the period corresponding to the wave ripple. The output of the Envelope Detector will be the input of the Voltage Regulator. The voltage regulator is made up of 18 diodes and one resistance ($R_{regulator}$) shown in Table 1. The resistance is in series with the 18 diodes

The diodes used are the ideal+V_{ON} diode model with $V_{ON} = 0.67$.

The theoretical results of the avarage output voltage at the the Voltage Regulator circuit, i.e, the avarage output voltage of the AC/DC converter circuit, as well as the output voltage ripple, calculated cost, and merit figure are shown in Table 2:

Name [unit]	**Value**
$Avarage(v_O)$ [V]	12.000000
$Ripple(v_O)$ [V]	0.000900
$Cost$ [MU]	257.200000
$Merit$	4.313424

Table 2: Results from theoretical analysis.

The graphic of the Figure 3 shows the output voltage at the Envelope Detector circuit.

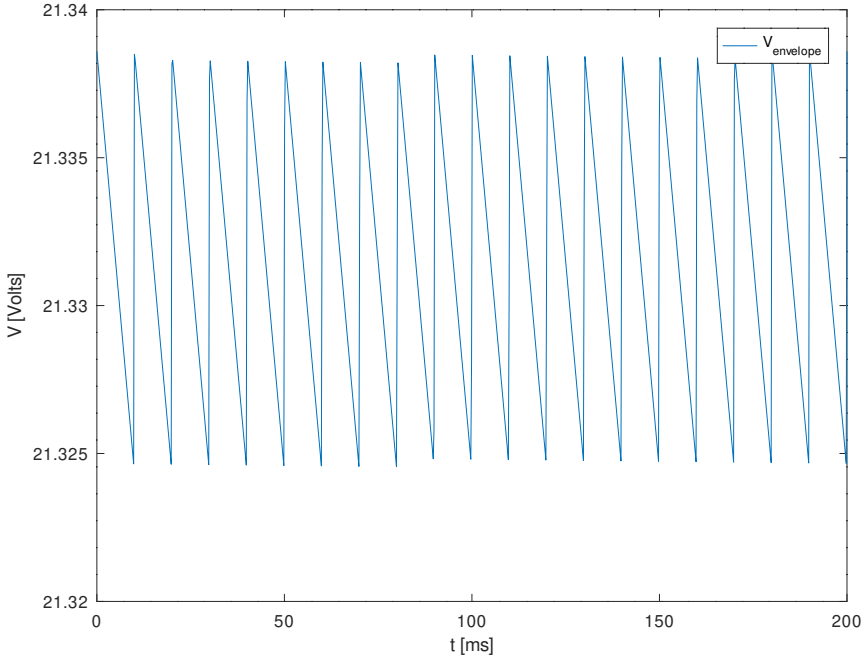

Figure 3: Output voltage at the Envelope Detector.

The graphic of the Figure 4 shows the output voltage at the Voltage Regulator circuit.

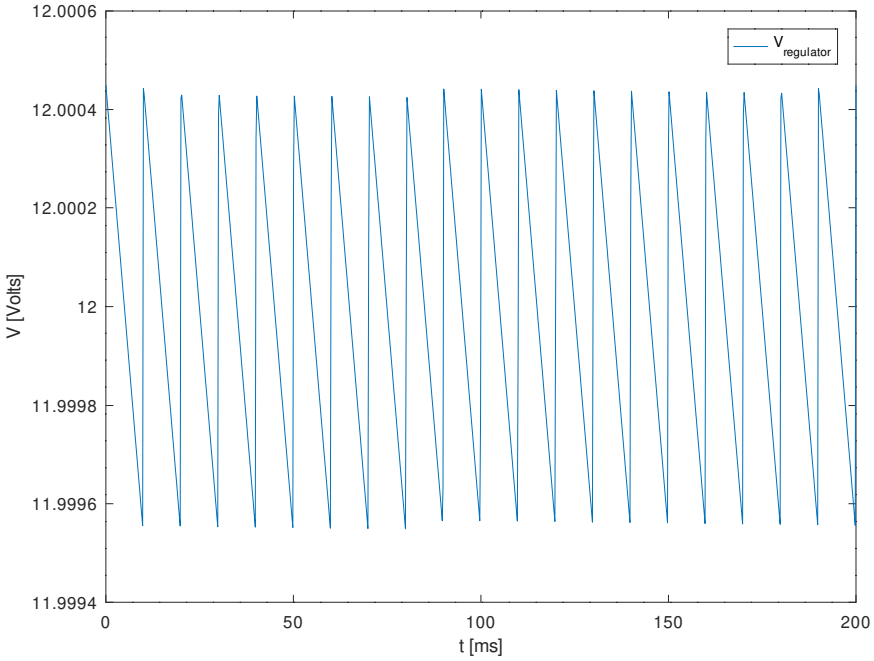

Figure 4: Output voltage at the Voltage Regulator circuit.

The graphic of the Figure 5 shows the deviation of output voltage at the Voltage Regulator from 12V.

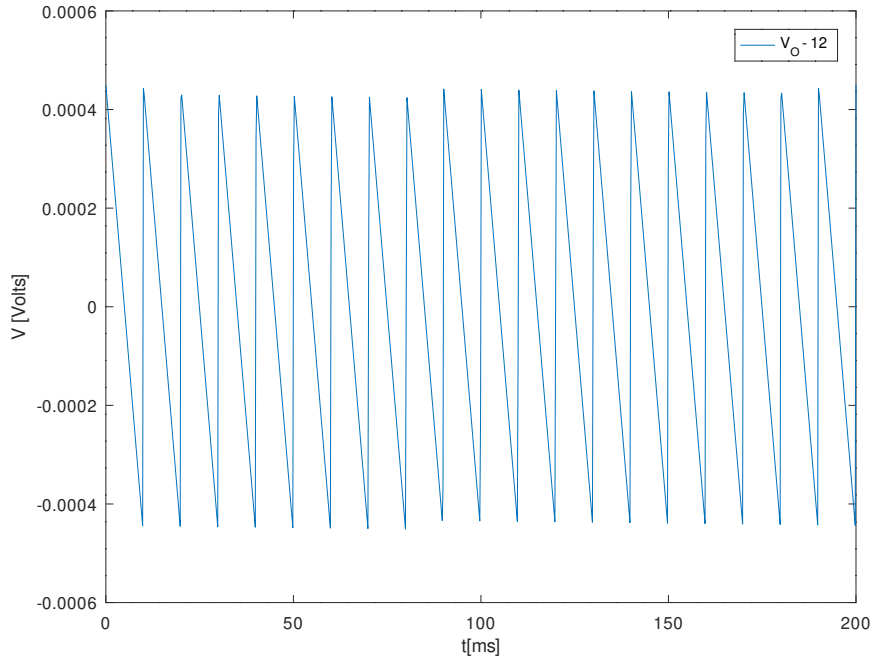

Figure 5: Deviation of output voltage at the Voltage Regulator from 12V.

3 Simulation Analysis

In this section, the circuit built (Figure 2) will be analyzed and simulated using NGSPICE.

Before simulate the circuit shown before, we used NGSPICE tools to simulate different circuit configurations and combinations of values for n of the transformer, for the resistances and for the capacitor in order too obtain a decent merit value, while trying to get a good average and ripple values and a relatively low cost. That is how we ended up using a Full-Wave Rectifier instead of an Half-Wave Rectifier, a Voltage Regulator with 18 diodes and the values shown in Table 1.

Performing transient analysis for 10 periods (200ms) on NGSPICE to simulate the circuit, and using some functions, the results obtained for the avarage output voltage, ripple of the output voltage ($ripple(v_O) = max(v_O) - min(v_O)$), cost and merit figure, are shown in Table 4

Name	**Values**
Vaverage	1.200000e+01 V
Vmax	1.200427e+01 V
Vmin	1.199563e+01 V
Ripple	8.640000e-03 V
Cost	257.20000000 MU
Merit	0.4499508024

Table 3: Results from simulation analysis.

The graphic of the Figure 6 shows the simulated output voltage at the Envelope Detector circuit.

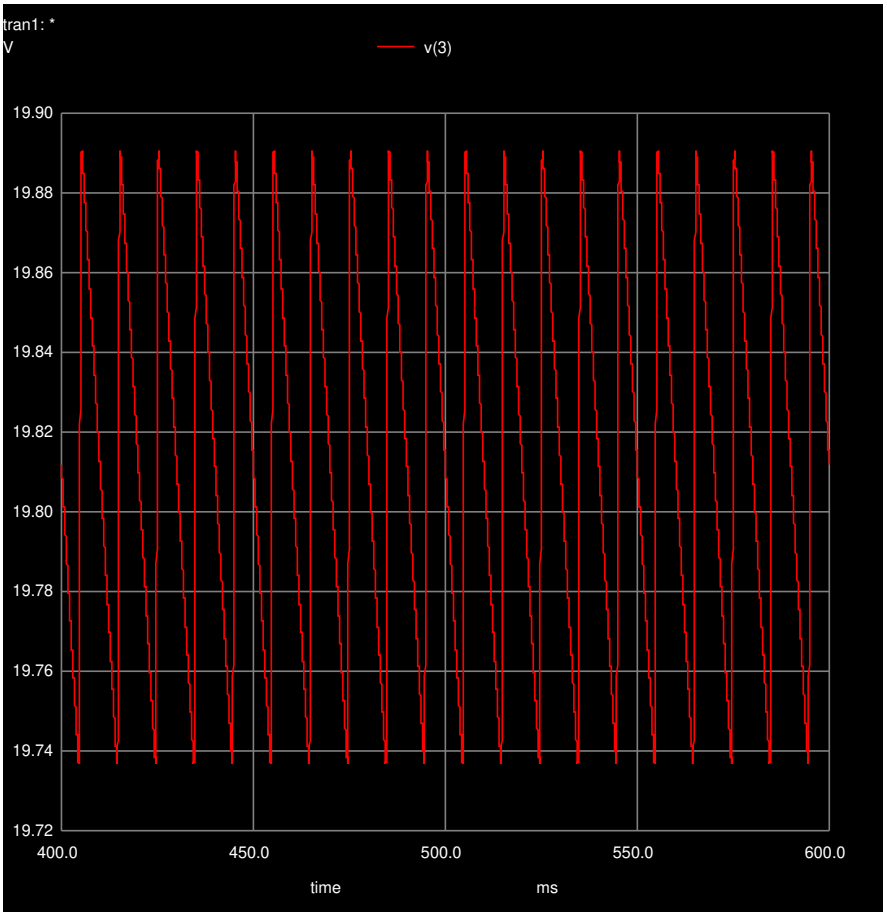

Figure 6: Output voltage at the Envelope Detector. The *x axis* represents the time in miliseconds and the *y axis* the voltage in Volts.

The graphic of the Figure 7 shows the simulated output voltage at the Voltage Regulator circuit.

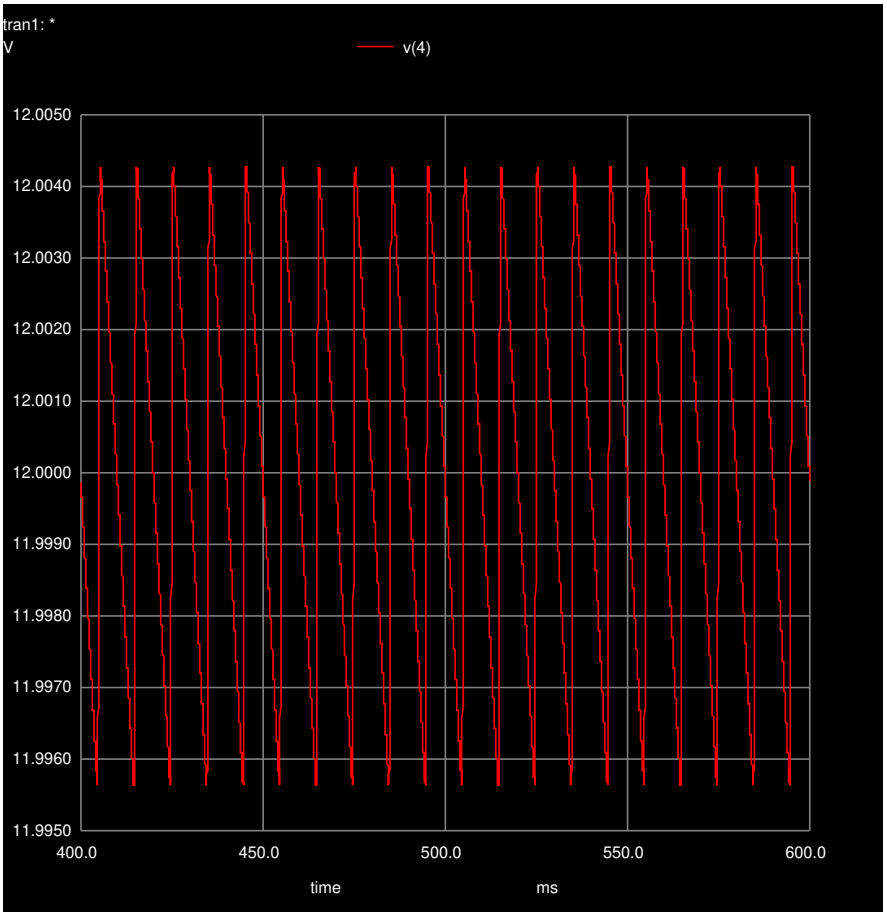

Figure 7: Output voltage at the Voltage Regulator circuit. The *x axis* represents the time in miliseconds and the *y axis* the voltage in Volts.

The graphic of the Figure 8 shows the deviation of the simulated output voltage at the Voltage Regulator from 12V.

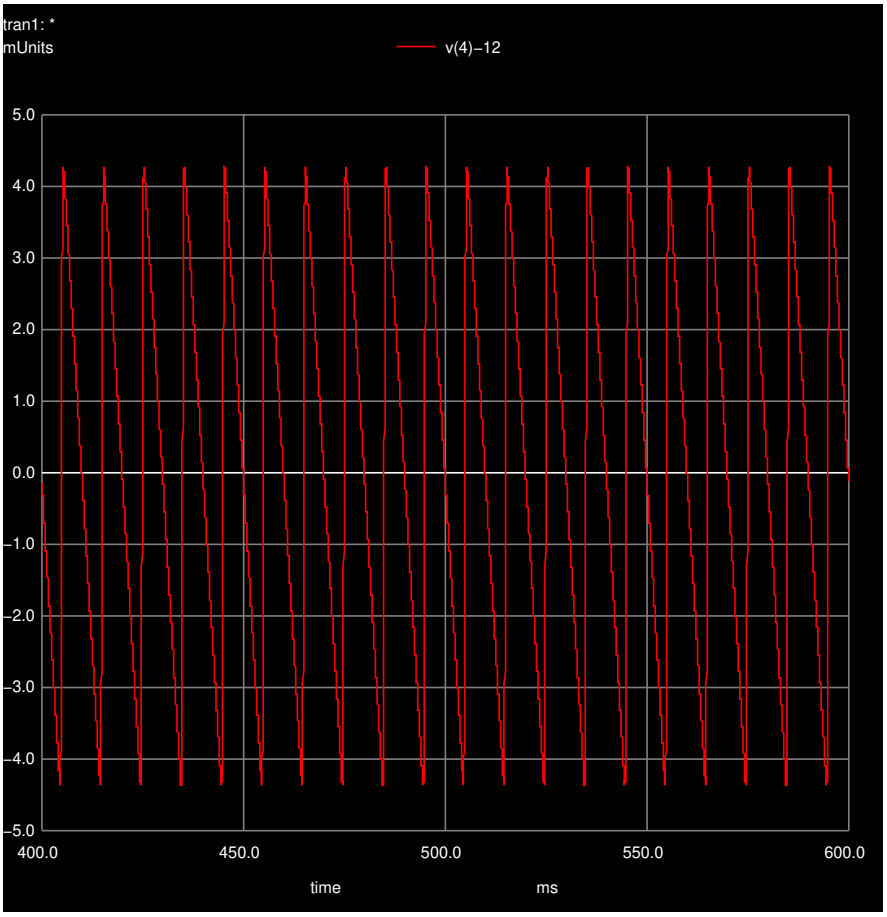

Figure 8: Deviation of the output voltage at the Voltage Regulator from 12V. The *x axis* represents the time in miliseconds and the *y axis* the voltage in Volts.

4 Comparison

We will now compare the results obtained in the theoretical analysis and the simulation analysis.

Name	**Theoretical**	**Simulated**
Average	12.0000 V	12.0000 V
Ripple	0.000900 V	0.008640 V
Cost	257.2 MU	257.2 MU
Merit	4.313424	0.4499508

Table 4: Results from simulation analysis.

The differences in the results are mainly seen in the value of the output voltage ripple, this difference is mainly due to the difference of the models of diodes and the complexity of the various components used both in Octave and Ngspice.

The not very great merit obtained in simulation analysis is due to a bigger than ideal output voltage ripple.

Despite the differences and low merit value on the Ngspice simulation the results achieved were the best found for the architecture chosen, after many iterations, these values for the various components were the best and the ones that gave us the best results, and most importantly the output voltage of 12 V.

5 Conclusion

Given the comparison made previously and the results obtained along the work, we can say that the objectives for this laboratory assignment were achieved. In this lab assignment we were able to analyse, create and study a circuit that represents a AC/DC Converter.

Given all this the objectives for this laboratory assignment were all achieved.